



# 제25회 한국반도체학술대회

The 25<sup>th</sup> Korean Conference on Semiconductors

2018년 2월 5일(월)-7일(수), 강원도 하이원리조트 컨벤션 호텔

2018년 2월 7일(수), 13:15-14:45

Room F (봉래, 6층)

## F. Silicon and Group-IV Devices and Integration Technology 분과

### [WF3-F] Photonics and Nanowire Technology

좌장: 김상완 교수(아주대학교), 안동환 교수(국민대학교)

<p><b>WF3-F-1</b> 13:15-13:30</p>	<p><b>Ge-on-Insulator Structureusing <math>Y_2O_3</math> for Mid-Infrared Photonics Platform</b> SangHyeon Kim<sup>1,2,4</sup>, Jae-Hoon Han<sup>1,4</sup>, Jae-Phil Shim<sup>3</sup>, Hyung-Jun Kim<sup>2,3</sup>, and Won Jun Choi<sup>1</sup> <i><sup>1</sup>Center for Opto-Electronics Materials and Devices, KIST, <sup>2</sup>Nanomaterials Science and Engineering, UST, <sup>3</sup>Center for Spintronics, KIST</i></p>
<p><b>WF3-F-2</b> 13:30-13:45</p>	<p><b>High Concentration Phosphorous Doping in Ge for CMOS-Integrated Laser Applications</b> Heedong Park<sup>1</sup>, Motoki Yako<sup>2</sup>, Yasuhiko Ishikawa<sup>2</sup>, Kazumi Wada<sup>2,3</sup>, and Donghwan Ahn<sup>1</sup> <i><sup>1</sup>School of Materials Science and Engineering, Kookmin University, <sup>2</sup>Department of Materials Engineering, University of Tokyo, <sup>3</sup>Department of Materials Science and Engineering, MIT</i></p>
<p><b>WF3-F-3</b> 13:45-14:00</p>	<p><b>Si Fin/Si<sub>1-x</sub>Ge<sub>x</sub> Shell Channel p-Type FinFET for Sub-10-nm Technology Nodes and Its High-Speed Operation</b> Eunseon Yu<sup>1</sup>, Won-Jun Lee<sup>2</sup>, Jongwan Jung<sup>2</sup>, and Seongjae Cho<sup>1,3</sup> <i><sup>1</sup>Graduate School of IT Convergence Engineering, Gachon University, <sup>2</sup>Department of Nanotechnology and Advanced Materials Engineering, Sejong University, <sup>3</sup>Department of Electronics Engineering, Gachon University</i></p>
<p><b>WF3-F-4</b> 14:00-14:15</p>	<p><b>Statistical Process-Induced Random Variation: Work-Function Variation in Stacked Nanowire FET</b> Jinyoung Park and Changhwan Shin <i>Department of Electrical and Computer Engineering, University of Seoul</i></p>
<p><b>WF3-F-5</b> 14:15-14:30</p>	<p><b>A Characteristic of Stacked Gate-All-Around Nanowire MOSFET based on Source Drain Doping Profile</b> Suhyeon Kim, Junil Lee, Myung-Hyun Baek, Sihyun Kim, Ryoongbin Lee, Hyun-Min Kim, Kitae Lee, and Byung-Gook Park <i>Department of Electrical Engineering, Seoul National University</i></p>
<p><b>WF3-F-6</b> 14:30-14:45</p>	<p><b>Simulation Study on the Effect of Unconformal Work-Function Metal Deposition on the Electrical Characteristic of Stacked-GAA MOSFET</b> Sihyun Kim<sup>1</sup>, Suhyeon Kim<sup>1</sup>, Sangwan Kim<sup>2</sup>, Euyhwan Park<sup>1</sup>, Junil Lee<sup>1</sup>, Ryoongbin Lee<sup>1</sup>, Soyeon Kim<sup>1</sup>, Hyun-Min Kim<sup>1</sup>, Kitae Lee<sup>1</sup>, Jong-Ho Lee<sup>1</sup>, and Byung-Gook<sup>1</sup> <i><sup>1</sup>ISRC and Department of Electrical and Computer Engineering, Seoul National University, <sup>2</sup>Department of Electrical and Computer Engineering, Ajou University</i></p>