2018년 2월 6일(화), 14:10-15:55
Room G (봉래II+III, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[TG2-G] Modeling and Simulation I - Nano Devices
좌장: 김대환 교수(국민대학교), 유현용 교수(고려대학교)

TG2-G-1 14:10-14:40	**[초청]** **Atomistic Simulations of Nanoscale Field Effect Transistors** Mincheol Shin *School of Electrical Engineering, KAIST*
TG2-G-2 14:40-14:55	**Modeling and Analysis of Work Function Variation in Nanowire FET** Kyul Ko[1], Myounggon Kang[2], and Hyungcheol Shin[1] *[1]ISRC and School of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation*
TG2-G-3 14:55-15:10	**Atomic Structure and Electronic Properties of Ge Nanowires along [100], [110] [111] Directions: Density Functional Study** Kai Liu[1,2], Eunjung Ko[1], Cheol Seong Hwang[2], and Jung-Hae Choi[1] *[1]Center for Electronic Materials, Korea Institute of Science and Technology, [2]Department of Materials Science and Engineering and ISRC, Seoul National University*
TG2-G-4 15:10-15:25	**An Efficient Method for Subband Calculation of Nanowire Transistors Using a Coordinate Transformation** Geon-Tae Jang and Sung-Min Hong *School of Electrical Engineering and Computer Science, GIST*
TG2-G-5 15:25-15:40	**Optimization of Nanowire Design according to Trap Quality of Spacer Dielectric for Performance of GAA Nanowires FET** Dong Geun Park, Kwan Hyun Cho, Dong Hyun Kim, Soo Hyun Kim, and Jae Woo Lee *ICT Convergence Technology for Health & Safety and Department of Electronics and Information Engineering, Korea University*
TG2-G-6 15:40-15:55	**Device Optimization of Nanosheet Transistors for 3.5 nm Technology Node** Ju-Hyun Kim[1], Myounggon Kang[2], and Hyungcheol Shin[1] *[1]ISRC and School of Electrical Engineering, Seoul National University, [2]Computer Science, Seoul National University*