



# 제25회 한국반도체학술대회

The 25<sup>th</sup> Korean Conference on Semiconductors

2018년 2월 5일(월)-7일(수), 강원도 하이원리조트 컨벤션 호텔

2018년 2월 6일(화), 09:00-10:45

Room G (봉래III+III, 6층)

## G. Device & Process Modeling, Simulation and Reliability 분과

### [TG1-G] Advanced Devices I - Technology and Simulation

좌장: 김대환 교수(국민대학교), 조인욱 상무(SK 하이닉스)

<p>TG1-G-1 09:00-09:15</p>	<p><b>Analysis of Carrier Lifetime Dependence of Dual Gate Positive Feedback Field-Effect Transistor with Polysilicon Body</b> Kyunchul Park, Min-Woo Kwon, and Byung-Gook Park <i>Department of Electrical Engineering, Seoul National University</i></p>
<p>TG1-G-2 09:15-09:30</p>	<p><b>A Study of Radiation Immunity and Damage Recovery in SiGe pMOSF</b> Ik Kyeong Jin<sup>1</sup>, Hagyoul Bae<sup>1</sup>, Jun-Young Park<sup>1</sup>, Choong-Ki Kim<sup>1</sup>, Il-Woong Tcho<sup>1</sup>, Seong-Yeon Kim<sup>2</sup>, Do-Hyun Kim<sup>2</sup>, Yun-Ik Son<sup>2</sup>, Jae-Hoon Lee<sup>2</sup>, Yong-Taik Kim<sup>2</sup>, Seong-Wan Ryu<sup>2</sup>, and Yang-Kyu Choi<sup>1</sup> <i><sup>1</sup>School of Electrical Engineering, KAIST, <sup>2</sup>SK Hynix Semiconductor Inc</i></p>
<p>TG1-G-3 09:30-09:45</p>	<p><b>Capacitance Matching to Obtain Sub-60mV/Decade Non-hysteretic Operation Regime of Negative Capacitance (NC) FET</b> Pavlo Bidenko<sup>1</sup>, Subin Lee<sup>1</sup>, Jin Dong Song<sup>1,2</sup>, and Sanghyeon Kim<sup>1,2</sup> <i><sup>1</sup>KIST, <sup>2</sup>University of Science and Technology</i></p>
<p>TG1-G-4 09:45-10:00</p>	<p><b>Effects of Shell Thickness on Performance of GaSb/InAs Core-Shell Nanowire pMOSFETs</b> Hyeongu Lee and Mincheol Shin <i>Department of Electronic Engineering, KAIST</i></p>
<p>TG1-G-5 10:00-10:15</p>	<p><b>Analysis of Performance in Nanosheet FET with Negative Capacitance</b> Changbeom Woo<sup>1</sup>, Jang Kyu Lee<sup>1</sup>, Jongsu Kim<sup>1</sup>, Myounggon Kang<sup>2</sup>, and Hyungcheol Shin<sup>1</sup> <i><sup>1</sup>ISRC and School of Electrical Engineering and Computer Science, Seoul National University, <sup>2</sup>Department of Electronics Engineering, Korea National University of Transportation</i></p>
<p>TG1-G-6 10:15-10:30</p>	<p><b>Statistical Analysis of NBTI Considering Trap Position in Nanosheet FET</b> Shinkeun Kim<sup>1</sup>, Dokyun Son<sup>1</sup>, Kyul Ko<sup>1</sup>, Myounggon Kang<sup>2</sup>, and Hyungcheol Shin<sup>1</sup> <i><sup>1</sup>ISRC and School of Electrical Engineering and Computer Science, Seoul National University, <sup>2</sup>Department of Electronics Engineering, Korea National University of Transportation</i></p>
<p>TG1-G-7 10:30-10:45</p>	<p><b>Si-Ge Hetero PN TFET with Junctionless Nanowire FET</b> Ju-Chan Lee, Tae Jun Ahn, and Yun Seop Yu <i>Department of Electrical, Electronic and Control Engineering and IITC, Hankyong National University</i></p>