2018년 2월 6일(화), 14:10-15:55
Room F (봉래I, 6층)

F. Silicon and Group-IV Devices and Integration Technology 분과
[TF2-F] Intergration Technology

좌장: 김춘환 상무(SK 하이닉스), 정성웅 연구위원(SK 하이닉스)

TF2-F-1 **14:10-14:40**	**[초청]** **Highly CMOS Compatible Strategies for Extending Moore's Law** Sangwan Kim, Seong-Su Shin, Hwa Young Gu, and Shinhee Kim *Department of Electrical and Computer Engineering, Ajou University*
TF2-F-2 **14:40-15:10**	**[초청]** **Hafnia Ferroelectric Device for Logic and Memory Applications** Sanghun Jeon *Department of Applied Physics, Korea University*
TF2-F-3 **15:10-15:25**	**Monolithic 3D CMOS-Nanoelectromechanical (NEM) Hybrid Circuits** Hyug Su Kwon, Seung Kyu Kim, and Woo Young Choi *Department of Electronic Engineering, Sogang University*
TF2-F-4 **15:25-15:40**	**Operating Voltage Analysis of CMOS-Nano-Electromechanical (NEM) Hybrid Circuits** Ho Moon Lee and Woo Young Choi *Department of Electronic Engineering, Sogang University*
TF2-F-5 **15:40-15:55**	**Novel Packaging Method of CMOS-Nano-Electromechanical (NEM) Hybrid Circuits** Hyun Chan Jo and Woo Young Choi *Department of Electronic Engineering, Sogang University*