2018년 2월 7일(수), 09:00-10:30
Room I (청옥II+III, 6층)

K. Memory (Design & Process Technology) 분과
[WI1-K] Topics Related to Memory Design

WI1-K-1 **09:00-09:30**	**[초청]** **Physics-based SPICE Modeling for Phase-Change Memory Cell** 전종욱 *건국대학교*
WI1-K-2 **09:30-09:45**	**SPICE-Based Simulation Study of Cu/AlOX/Pt Conductive-Bridge Resistive Access Memory-CMOS Integrated Circuit for Reconfigurable Logic** Jun Tae Jang[1], Geumho Ahn[1], Daehyun Ko[1], Hye Ri Yu[1], Haesun Jung[1], Chansoo Yoon[2], Sangik Lee[2], Bae Ho Park[2], Hyun-Sun Mo[1], Sung-Jin Choi[1], Dong Myong Kim[1], and Dae Hwan Kim[1] *[1]School of Electrical Engineering, Kookmin University, [2]Department of Physics, Konkuk University*
WI1-K-3 **09:45-10:00**	**메모리 예비자원 사용 효율을 고려한 3차원 메모리 수리 기법** 이하영, 한동현, 이승택, 강성호 *Department of Electrical and Electronic Engineering, Yonsei University*
WI1-K-4 **10:00-10:15**	**Low Power Contents Addressable Memory with NMOS Gated Selective Precharge Matchline** Kwanghyo Jeong, Kyeongho Lee, Woong Choi, and Jongsun Park *School of Electrical Engineering, Korea University*