2018년 2월 7일(수), 13:15-14:45
Room G (봉래II+III, 6층)

G. Device & Process Modeling, Simulation and Reliability 분과
[WG3-G] Modeling and Simulation II - Device and Process

WG3-G-1 13:15-13:30	**Physics-Based Capacitance Model of Drift Region in LDMOS and Its Implementation with BSIM4** Jun Hyeok Kim[1], Chan Ho Park[1], Sung Moo Kim[1], Ji-Woon Yang[2], and Geun Tae Kwon[1] *[1]Technology Enabling Team, DB Hitek Co., Ltd., Department of Electronics & Information Engineering, Korea University*
WG3-G-2 13:30-13:45	**A Frequency Domain Solver for Maxwell's Equations and Drift-Diffusion Model** Jaehyeong Jang and Sung-Min Hong *School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology*
WG3-G-3 13:45-14:00	**공정 산포 마진 예측을 위한 Process Emulation Tool과 통계적 분석법을 활용한 Process Integration 모델링** Mi-Na Kim, Hyoung-Gyu Choi, Eun-Young Cheon, Seong-Dong Kim, Seokkiu Lee, and Sungjoo Hong *Device modeling & Reliability Group, R&D Division, SK Hynix Inc*
WG3-G-4 14:00-14:15	**First Principles Approach to Analyze Defect-induced Multiphonon Transition at the Si-SiO$_2$ Interface** Junsung Park and Sung-Min Hong *School of Electrical Engineering and Computer Science, GIST*
WG3-G-5 14:15-14:30	**Characteristics for Self Heating Effects on Stacked Nanosheet FET** Hyunsuk Kim, Dokyun Son, Ilho Myeong, Myounggon Kang, and Hyungcheol Shin *ISRC and School of Electrical Engineering and Computer Science, Seoul National University*
WG3-G-6 14:30-14:45	**Series Resistance Characterization of Junctionless Transistors** D.-Y. Jeon[1], S. J. Park[2], M. Mouis[3], S. Barraud[4], G.-T. Kim[2], and G. Ghibaudo[3] *[1]Institute of Advanced Composite Materials, Korea Institute of Science and Technology, [2]School of Electrical Engineering, Korea University, [3]IMEP-LAHC, Grenoble INP, Minatec, [4]CEA-LETI Minatec*