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G. Device & Process Modeling, Simulation and Reliability 분과 [TG2-G] Modeling and Simulation I - Nano Devices

TG2-G-1 14:10-14:40	[초청] Atomistic Simulations of Nanoscale Field Effect Transistors Mincheol Shin School of Electrical Engineering, KAIST
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TG2-G-2 14:40-14:55	Modeling and Analysis of Work Function Variation in Nanowire FET Kyul Ko ¹ , Myounggon Kang ² , and Hyungcheol Shin ¹ ¹ ISRC and School of Electrical Engineering and Computer Science, Seoul National University, ² Department of Electronics Engineering, Korea National University of Transportation
TG2-G-3 14:55-15:10	Atomic Structure and Electronic Properties of Ge Nanowires along [100], [110] [111] Directions: Density Functional Study Kai Liu ^{1,2} , Eunjung Ko ¹ , Cheol Seong Hwang ² , and Jung-Hae Choi ¹ ¹ Center for Electronic Materials, Korea Institute of Science and Technology, ² Department of Materials Science and Engineering and ISRC, Seoul National University
TG2-G-4 15:10-15:25	An Efficient Method for Subband Calculation of Nanowire Transistors Using a Coordinate Transformation Geon-Tae Jang and Sung-Min Hong School of Electrical Engineering and Computer Science, GIST
TG2-G-5 15:25-15:40	Optimization of Nanowire Design according to Trap Quality of Spacer Dielectric for Performance of GAA Nanowires FET Dong Geun Park, Kwan Hyun Cho, Dong Hyun Kim, Soo Hyun Kim, and Jae Woo Lee ICT Convergence Technology for Health & Safety and Department of Electronics and Information Engineering, Korea University
TG2-G-6 15:40-15:55	Device Optimization of Nanosheet Transistors for 3.5 nm Technology Node Ju-Hyun Kim ¹ , Myounggon Kang ² , and Hyungcheol Shin ¹ ¹ ISRC and School of Electrical Engineering, Seoul National University, ² Computer Science, Seoul National University