



# 제25회 한국반도체학술대회

The 25<sup>th</sup> Korean Conference on Semiconductors

2018년 2월 5일(월)-7일(수), 강원도 하이원리조트 컨벤션 호텔

2018년 2월 6일(화), 14:10-15:55

Room F (봉래, 6층)

## F. Silicon and Group-IV Devices and Integration Technology **분과** [TF2-F] Intergration Technology

TF2-F-1 14:10-14:40	<b>[초청]</b> <b>Highly CMOS Compatible Strategies for Extending Moore's Law</b> Sangwan Kim, Seong-Su Shin, Hwa Young Gu, and Shinhee Kim <i>Department of Electrical and Computer Engineering, Ajou University</i>
TF2-F-2 14:40-15:10	<b>[초청]</b> <b>Hafnia Ferroelectric Device for Logic and Memory Applications</b> Sanghun Jeon <i>Department of Applied Physics, Korea University</i>
TF2-F-3 15:10-15:25	<b>Monolithic 3D CMOS-Nanoelectromechanical (NEM) Hybrid Circuits</b> Hyug Su Kwon, Seung Kyu Kim, and Woo Young Choi <i>Department of Electronic Engineering, Sogang University</i>
TF2-F-4 15:25-15:40	<b>Operating Voltage Analysis of CMOS-Nano-Electromechanical (NEM) Hybrid Circuits</b> Ho Moon Lee and Woo Young Choi <i>Department of Electronic Engineering, Sogang University</i>
TF2-F-5 15:40-15:55	<b>Novel Packaging Method of CMOS-Nano-Electromechanical (NEM) Hybrid Circuits</b> Hyun Chan Jo and Woo Young Choi <i>Department of Electronic Engineering, Sogang University</i>