2018년 2월 6일(화), 08:15-09:00
Room D (함백II+III, 5층)

S. Chip Design Contest 분과
[TD0-S] Chip Design Contest

TD0-S-1 08:15-08:30	**65nm RF CMOS Gilbert-Cell Mixer for Wireless Power Transfer System** Ju-Hwan Lim, Nhut-Tan Doan, Wan-Su Kim, Ngoc-Duy-Hien Lai, and Sang-Woong Yoon *Department of Electronics Engineering, Kyung Hee University*
TD0-S-2 08:30-08:45	**A Low Jitter Clock and Data Recovery Circuit with Pulse-Width-Adjusting Binary Phase Detector Using 180-nm CMOS** Jaeok Yun, Sanghun Baek, Jaepil Park, and Jin-Ku Kang *Department of Electronics Engineering, Inha University*
TD0-S-2 08:30-08:45	**A Low Jitter Clock and Data Recovery Circuit with Pulse-Width-Adjusting Binary Phase Detector Using 180-nm CMOS** Jaeok Yun, Sanghun Baek, Jaepil Park, and Jin-Ku Kang *Department of Electronics Engineering, Inha University*
TD0-S-3 08:45-09:00	**A 1 MHz 1 MΩ Output Impedance CMOS Current Driver and Active Electrode for ECG/ETI Measurement** Xuan Tien Nguyen, Woo-Jin Cho, Jun-Hyeong Kwon, Pham Thanh Son, and Jong-Wook Lee *Department of Electronics Engineering, Kyung Hee University*