2018년 2월 6일(화), 14:10-15:55
Room A (태백I, 5층)

A. Interconnect & Package 분과
[TA2-A] FOWLP & Reliability

TA2-A-1 **14:10-14:40**	**[초청]** **High-Density Fan-out Technology for Advanced 3D SiP and Heterogeneous Integration** KangWook Lee *Global RnD, Amkor Technology Korea Inc.*
TA2-A-2 **14:40-14:55**	**Performance Comparisons between Thermocompression and Laser-Assisted Boning for 3D Stacking Process** Kwang-Seong Choi, Wagno Alves Braganca Junior, leeseul Jeong, Keon-Soo Jang, Seok Hwan Moon, Hyun-Cheol Bae, and Yong-Sung Eom *ICT Materials and Components Laboratory, ETRI*
TA2-A-3 **14:55-15:10**	**Analysis for Burnout Failure on Interconnect Metal Under High Current Stress** Chang Hwi Lee, Jae Young You, Sung Bae Kim, Hur Min Jae, Sangho Won, Si Woo Lee, and Man Ho Seung *SK Hynix*
TA2-A-4 **15:10-15:25**	**3차원 반도체에서 테스트 발열을 고려한 테스트 스케줄링 기법** 이예원, 이인걸, 정민호, 강성호 *Department of Electrical and Electronic Engineering, Yonsei University*
TA2-A-5 **15:25-15:40**	**Electrochemical Polishing of Cu Redistribution Layers for Fan Out Wafer Level Packaging** Ki Moon Park[1], Jin Hyun Lee[2], and Bong Young Yoo[1,2] *[1]Department of Advanced Material Science & Engineering, Hanyang University, [2]Department of Material Science & Engineering, Hanyang University*
TA2-A-6 **15:40-15:55**	**PCW 온도 제어를 통한 Cu CMP Removal Rate 변화 특성 연구** Jinhyung Lee, Yohan Jeon, Seong Sik Kim, Kyung-ho Hwang, and Sang Deok Kim *DRAM C&C, Process Center, SK Hynix*