Electronics in Flatland

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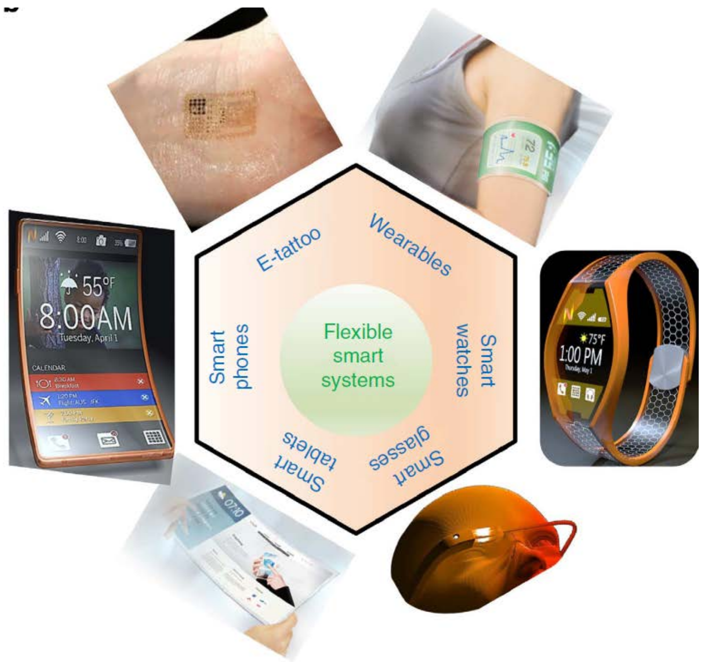
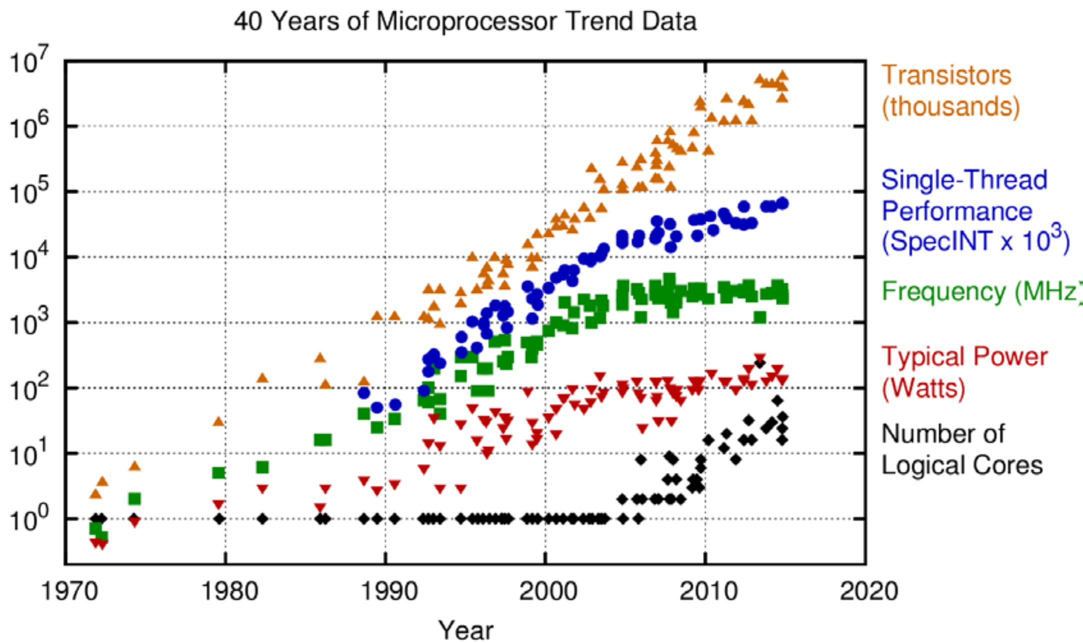
and S.K. Banerjee
University of Texas at Austin

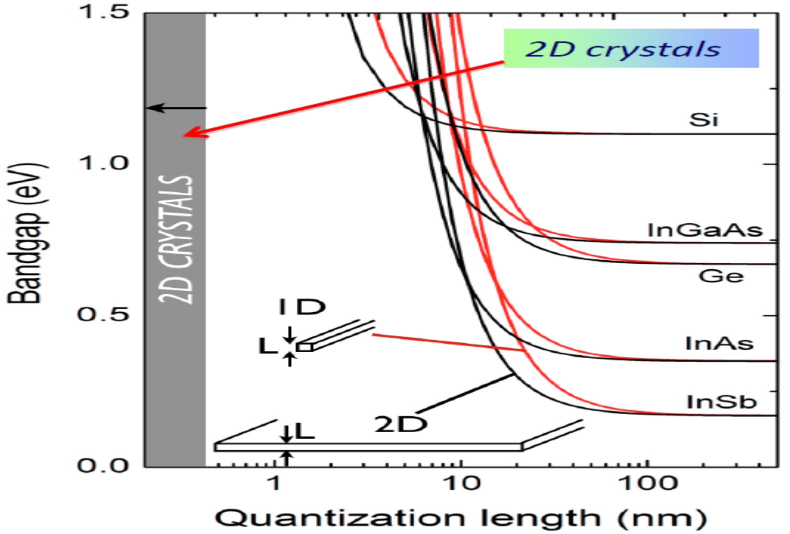


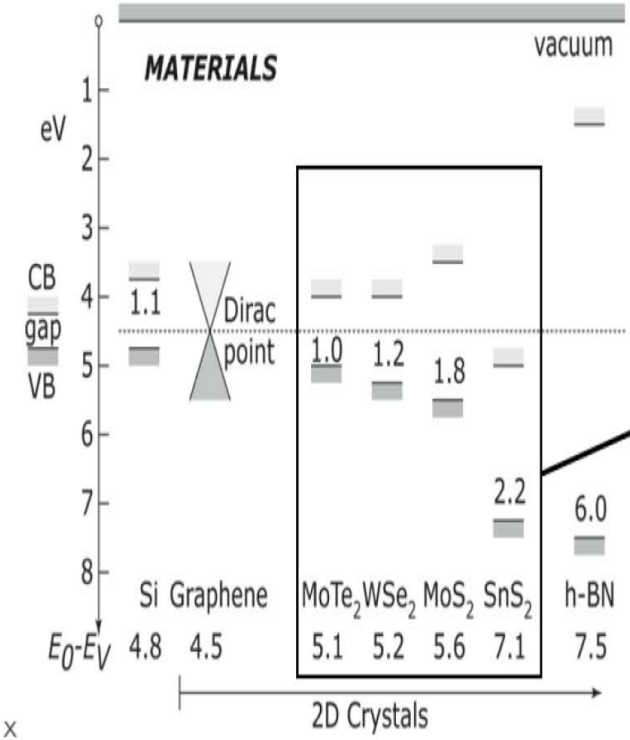


Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

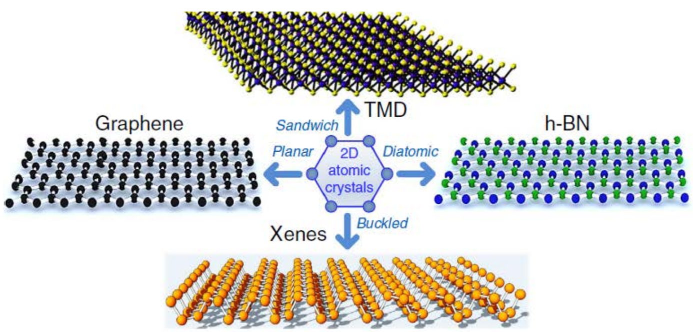
- **Medium Frequency, Low Power IoT Devices**
- **Beyond-CMOS Low Power Transistors**

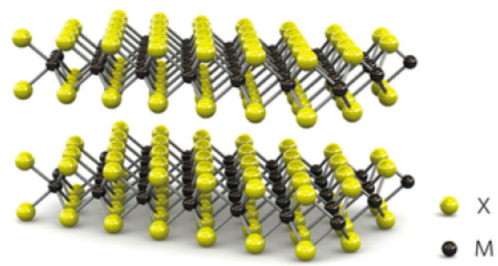
Acknowledgments: NRI SWAN, NSF NASCENT ERC, NNCI, DOE BAPVC, Army STTR

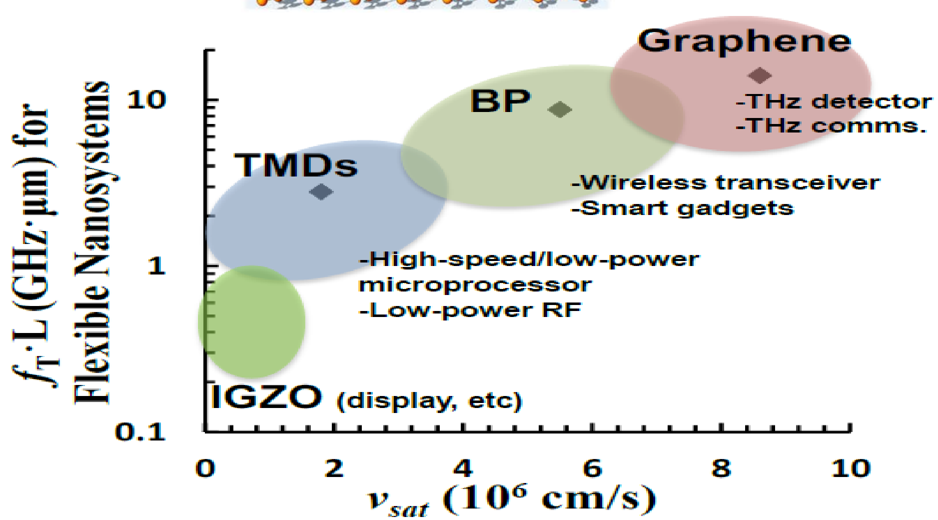


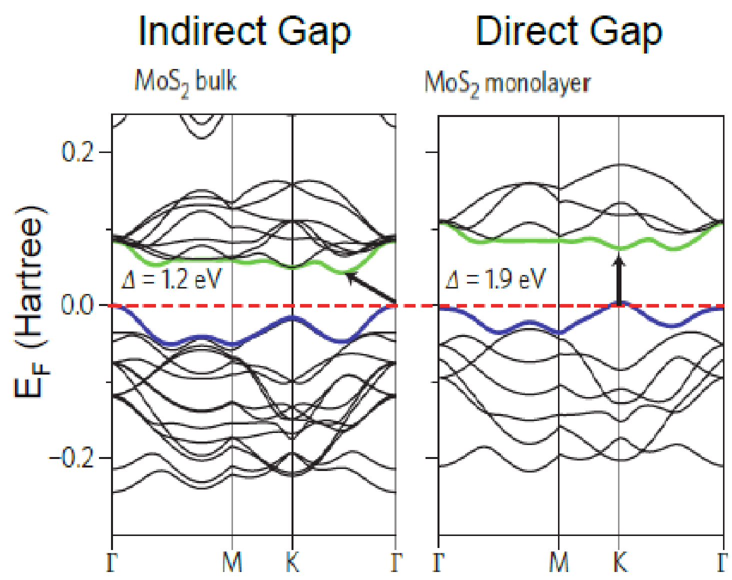


Mo [Kr]$4d^5 5s$
S [Ne]$3s^2 3p^4$

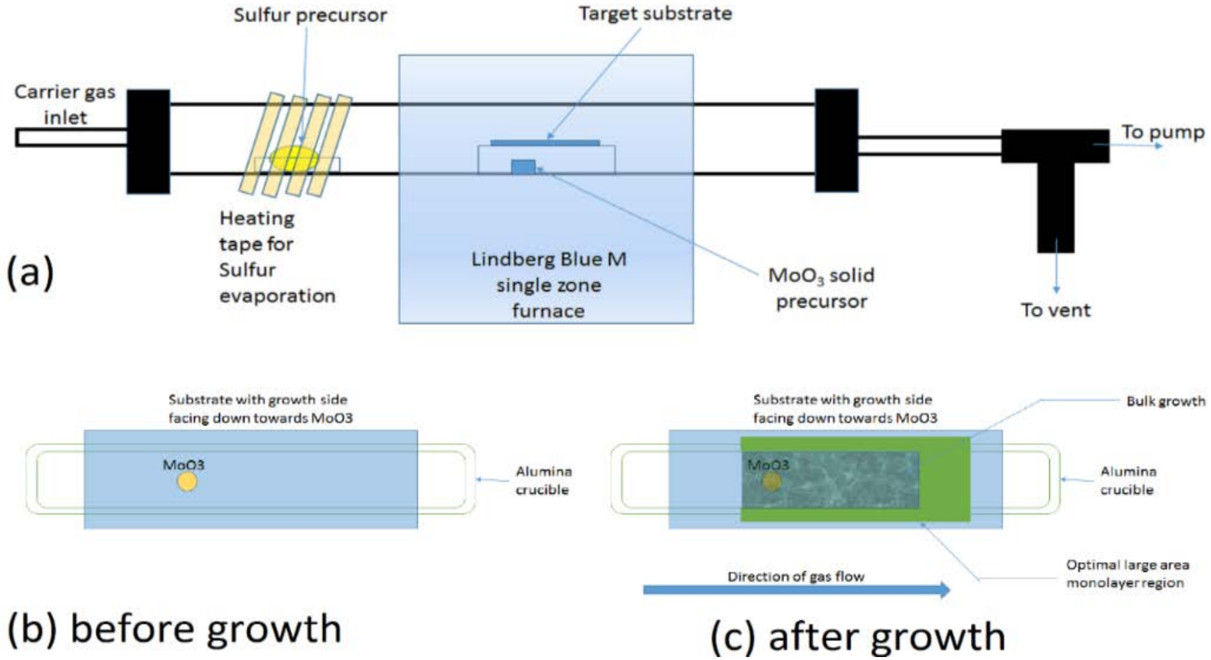


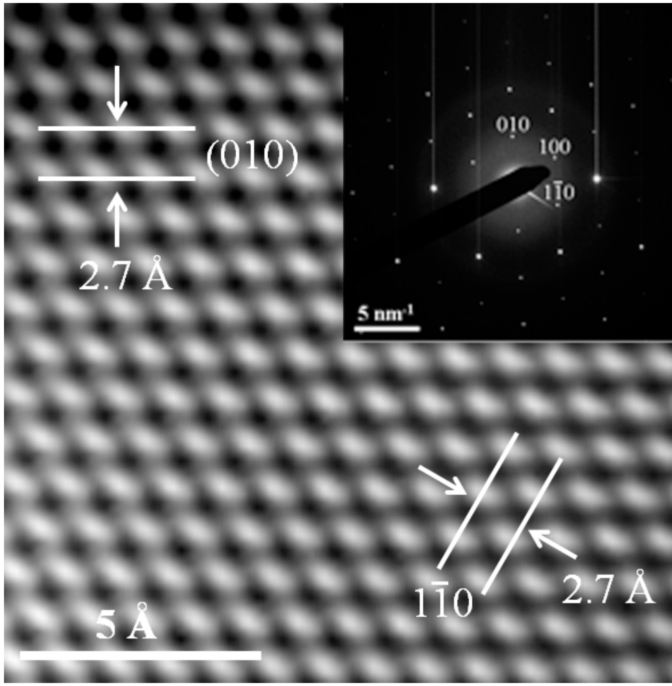


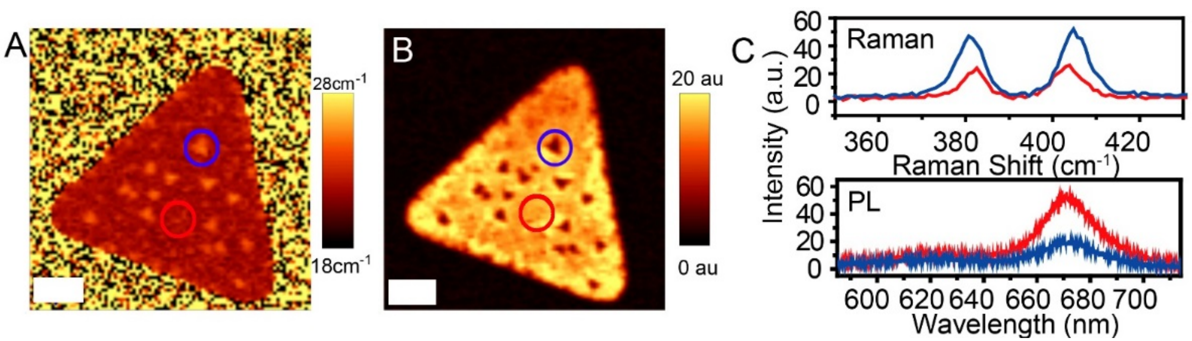


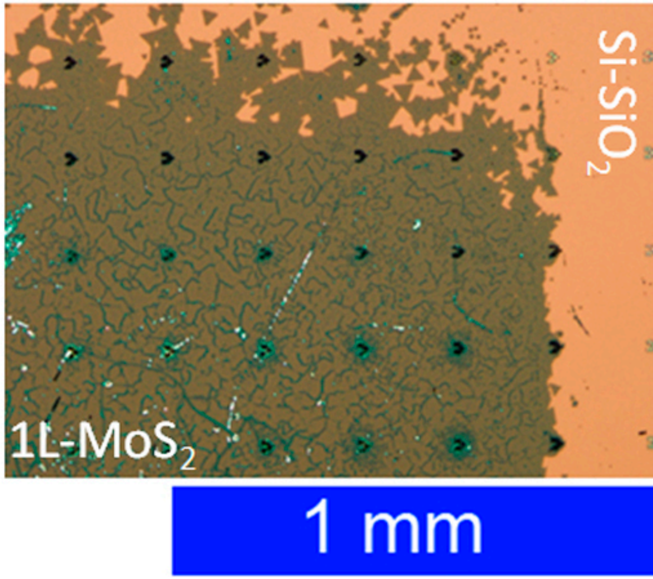


MoS_2 CVD growth chamber with solid precursors

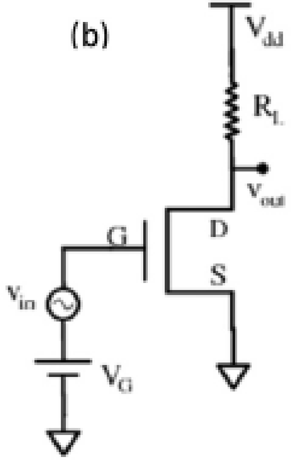


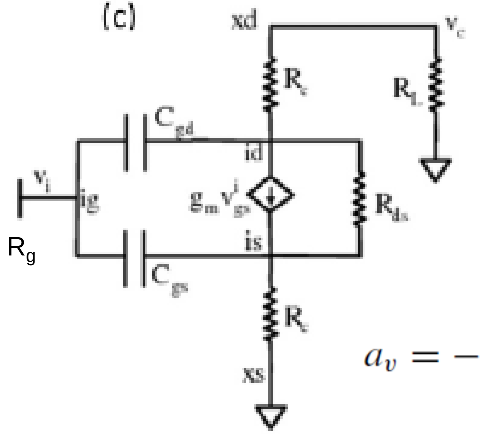




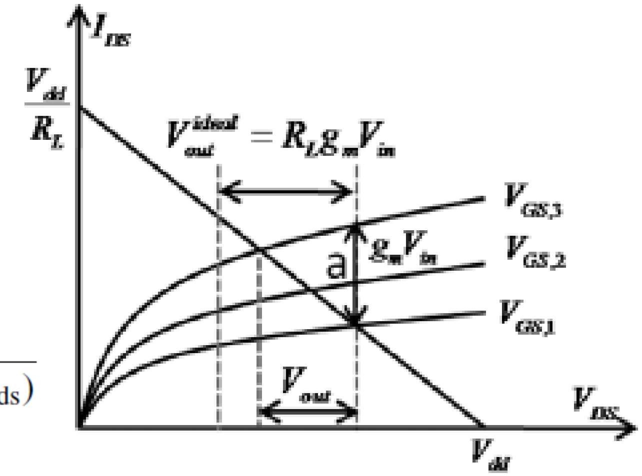


Sanne, Ghosh,… Banerjee, APL 2014



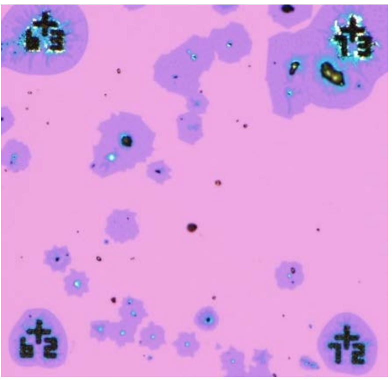


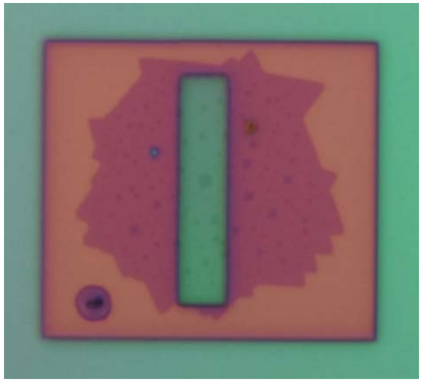
$$a_v = -\frac{R_L g_m R_{ds}}{R_L + R_{ds} + R_c(2 + g_m R_{ds})}$$

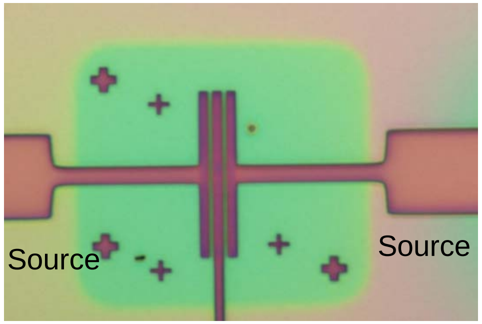


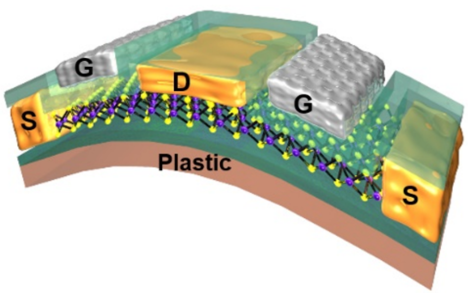
$$\textit{Unity current gain at } f_T = \frac{g_m}{2\pi(C_{gs}+C_{p,gs}+C_{p,gd})\left((R_{c,s}+R_{c,d})g_{ds}+1\right)+C_{p,gd}g_m(R_{c,s}+R_{c,d})} = g_m/\ 2\pi C_{gs} = 1/\ 2\pi\tau$$

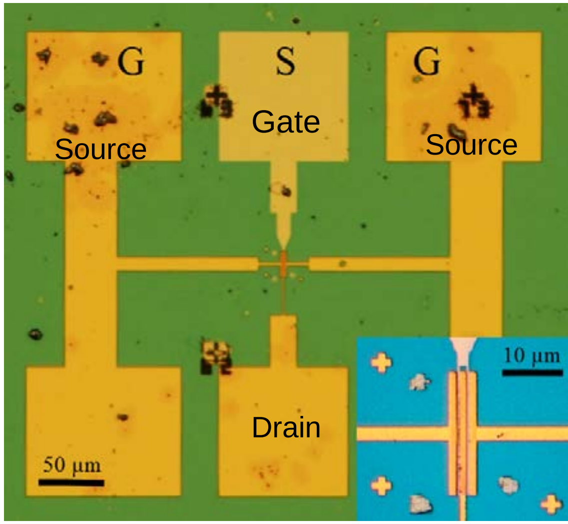
$$\textit{Unity Power gain at } f_{max} = \frac{f_T}{\sqrt{2g_{ds}(R_{c,s} + R_{gate}) + 2\pi f_T C_{p,gd} R_g}}$$





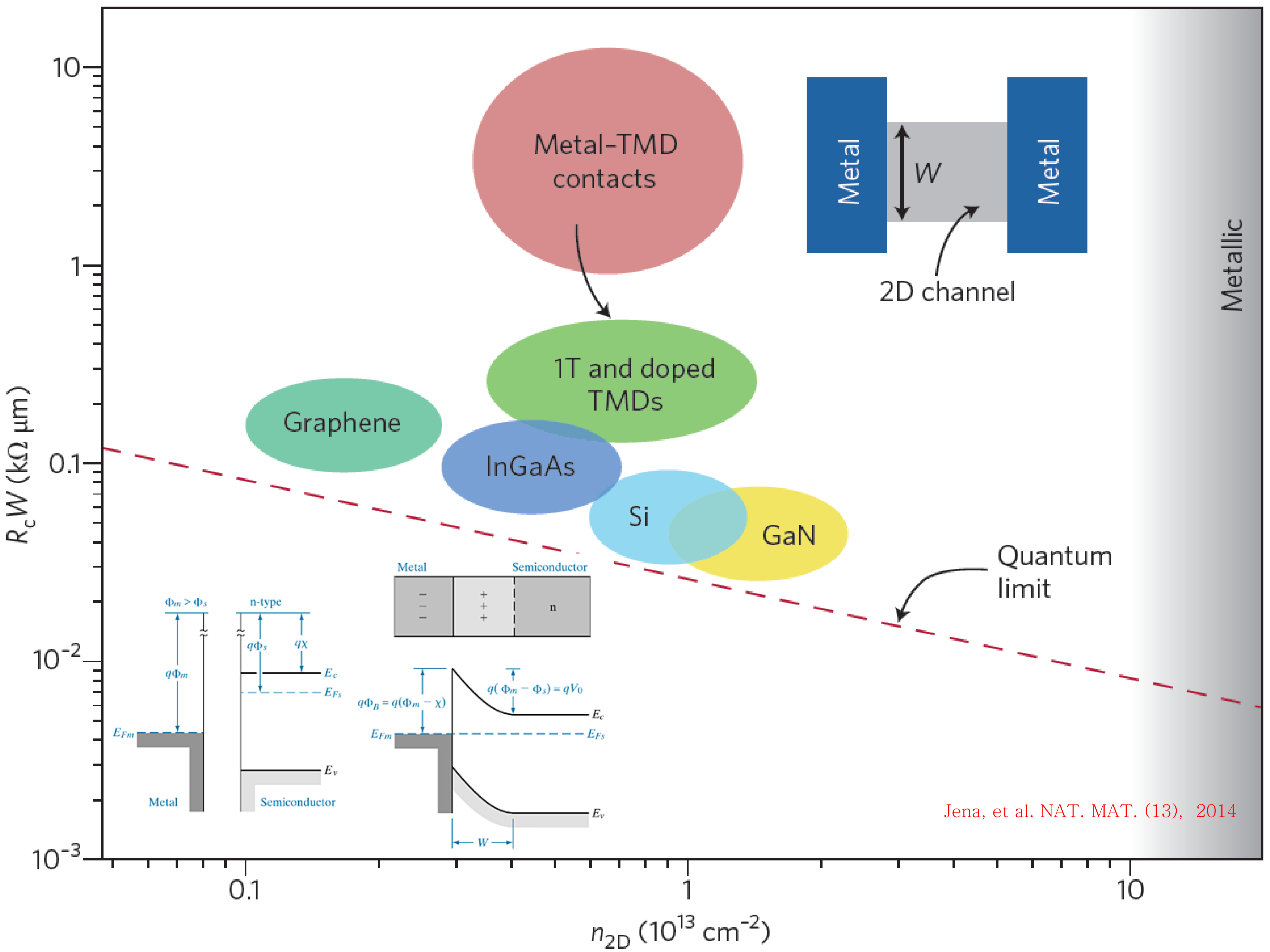






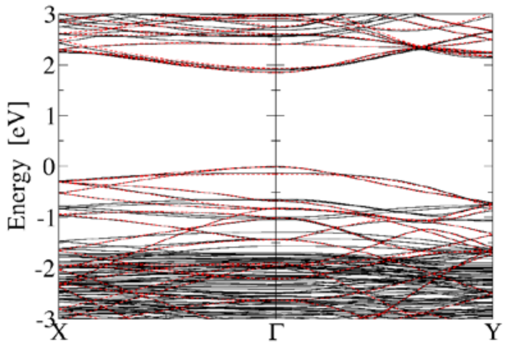
1) Active area
2) S/D contacts
3) Top gate

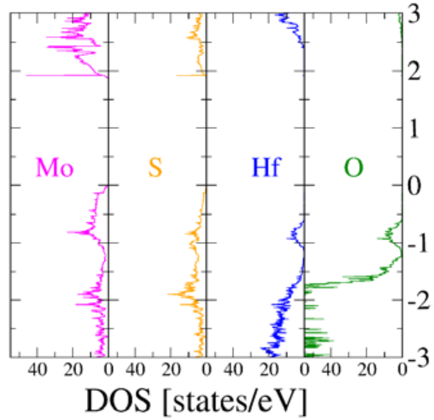
Sanne, Banerjee, Nano.Lett (2015)

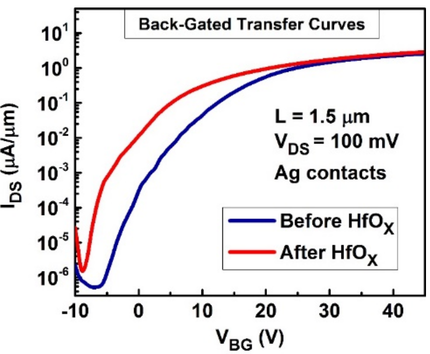

Metal-TMD contacts
1T and doped TMDs
Graphene
InGaAs
Si
GaN
Metal
W
Metal
2D channel
Metallic
Quantum limit
Metal
Semiconductor
n
Φm > Φs
n-type
qΦm
qΦs
qχ
Ec
EFs
EFm
Ev
Metal
Semiconductor
qΦB = q(Φm − χ)
q(Φm − Φs) = qV0
Ec
EFs
EFm
Ev
W
Jena, et al. NAT. MAT. (13), 2014
10
1
0.1
10^-2
10^-3
0.1
1
10
RcW (kΩ μm)
n2D (10^13 cm^-2)

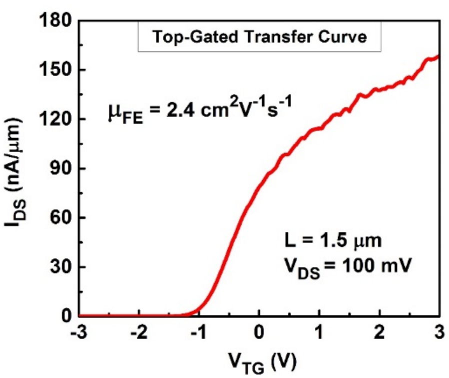
MoS_2 on ALD HfO_2

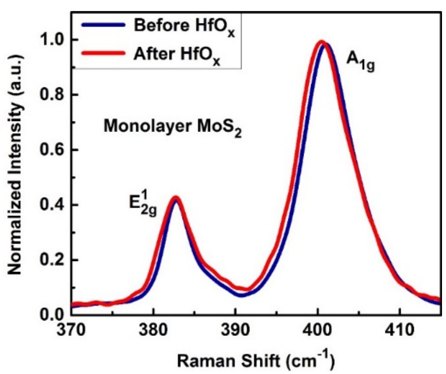
Without O-vacancy: HfO_2



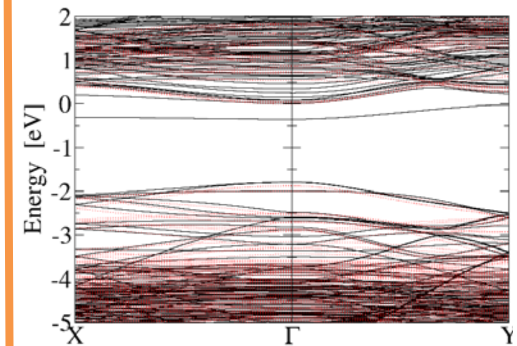


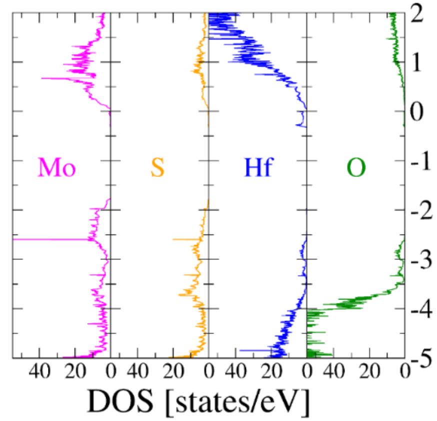


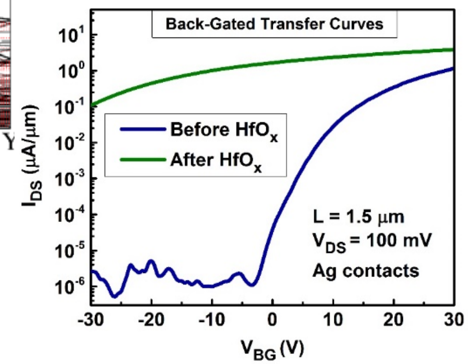


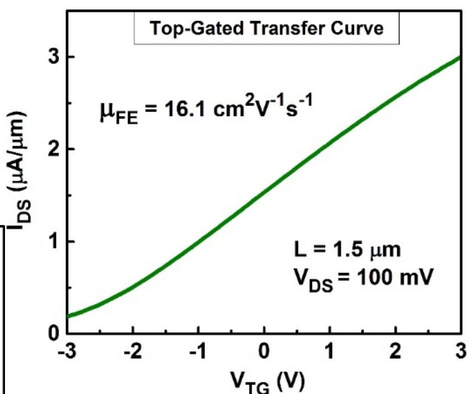


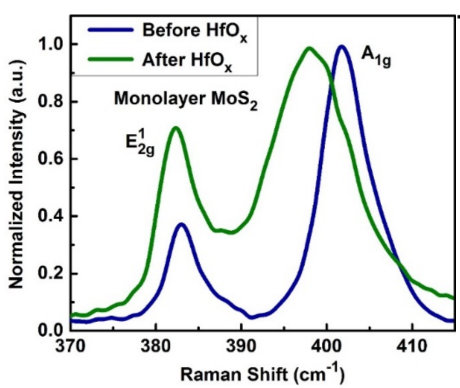
With O-vacancy: $HfO_{1.6}$







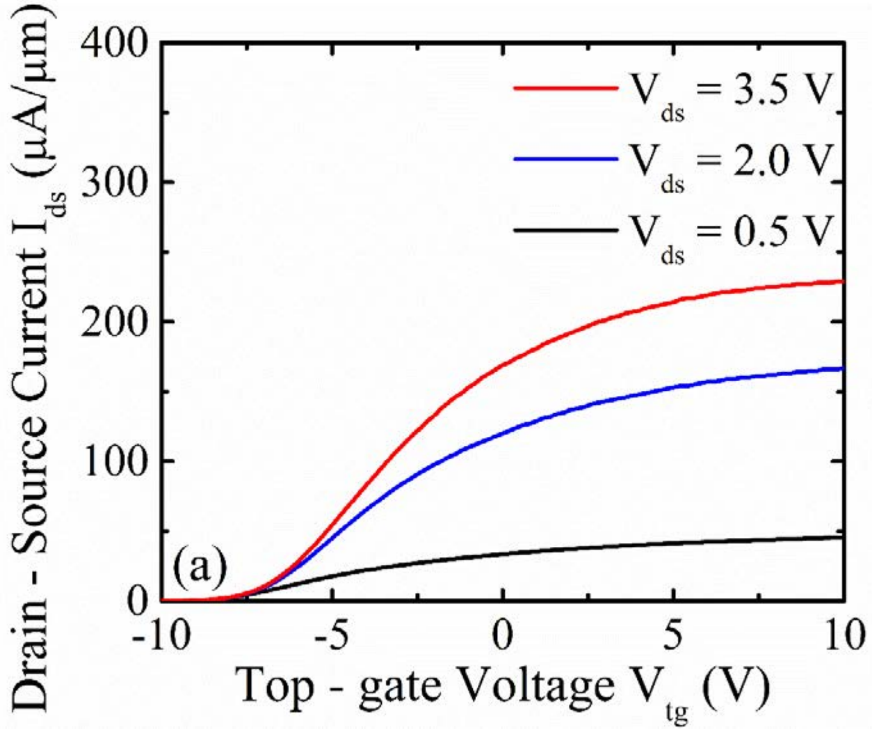


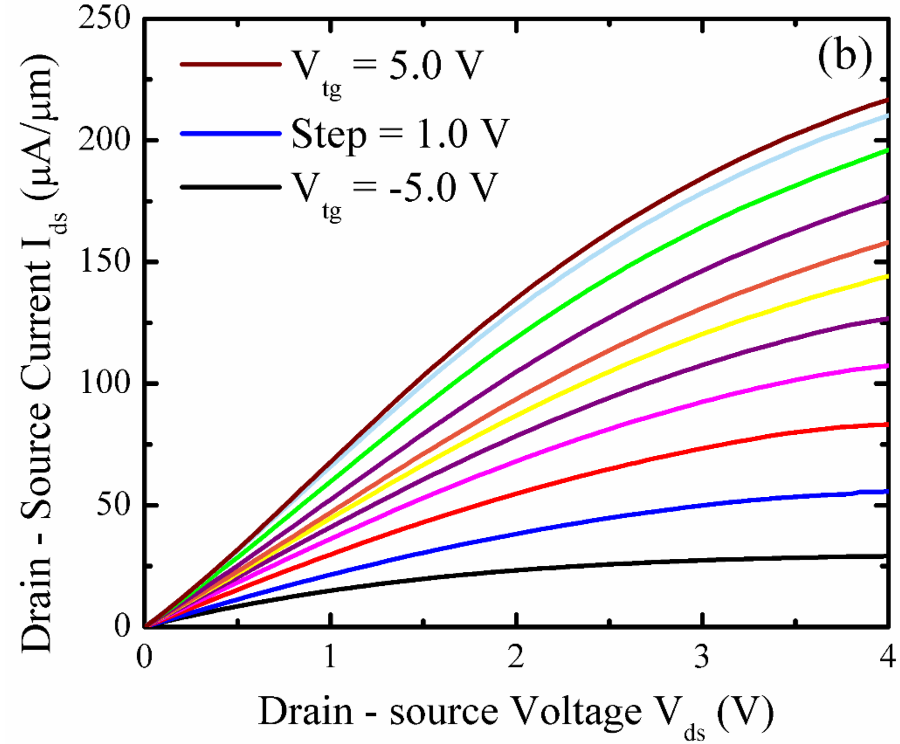


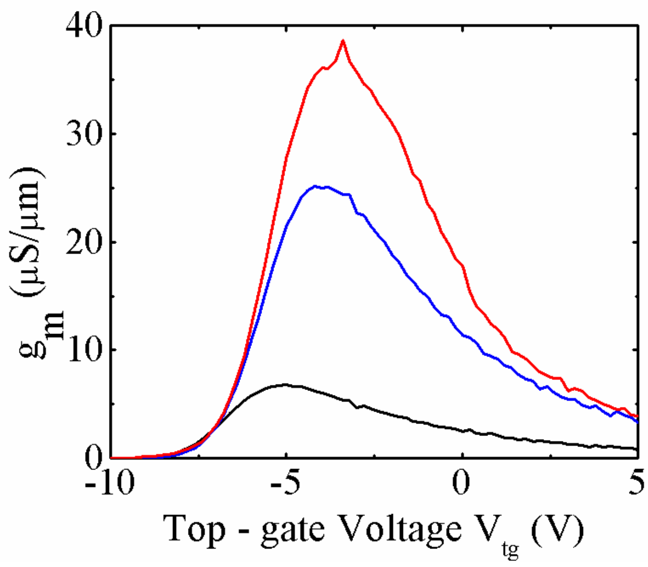
Similar results for Hf-termination and H –passivation, and other high-k (Al_2O_3, TiO_2)

Rai,Valsraj…. Register, Tutuc, Banerjee, Nanoletters (2015)

Top Gated MoS_2 DC Characteristics



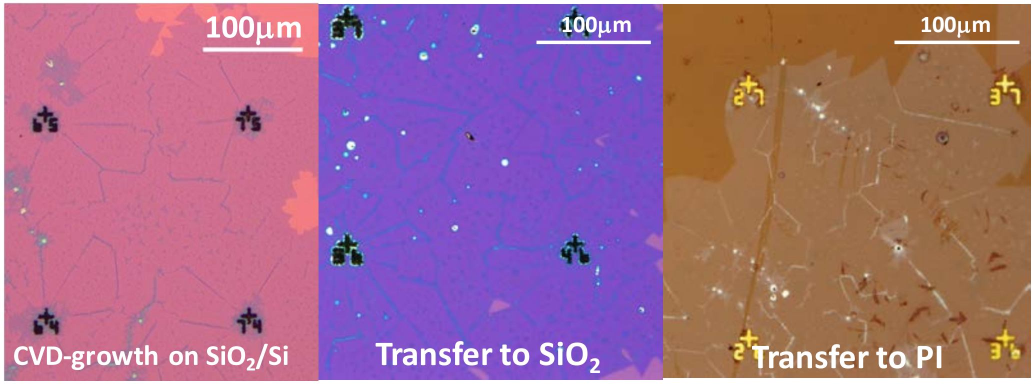


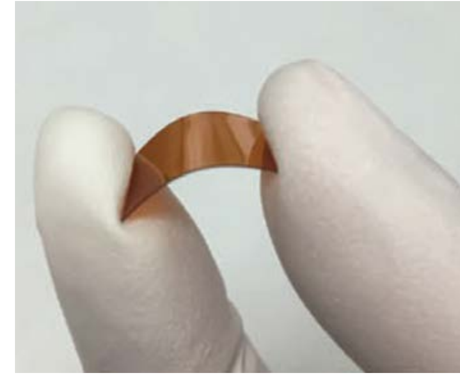


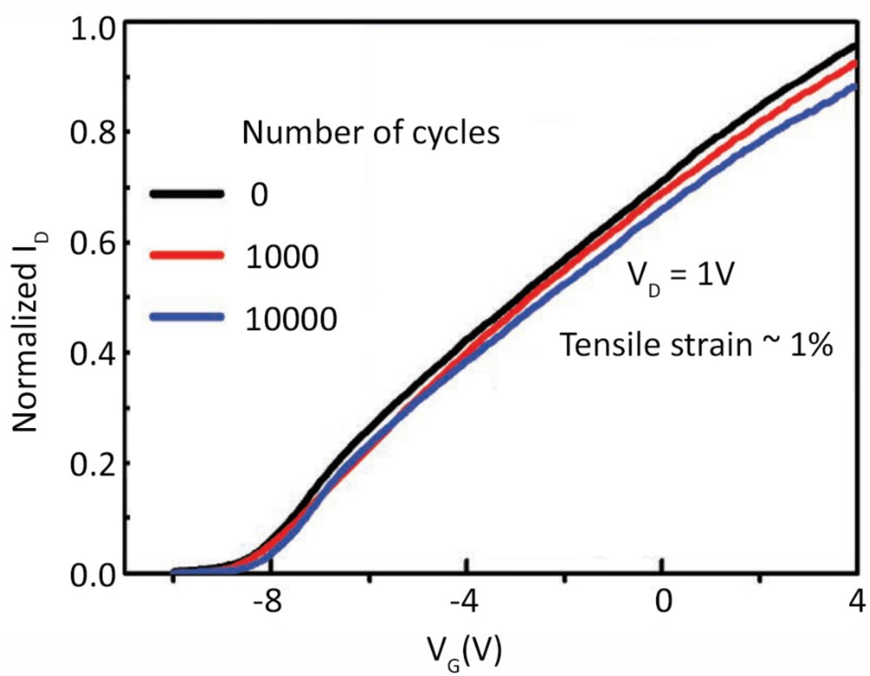
- Monolayer CVD MoS_2 on 285 nm SiO_2 on Si; L= 250 nm
- 30 nm ALD $HfO_{1.56}$; Ni gate (50 nm); V_T= -9V
- 20 nm Ag/30 nm Au S/D contacts
  Schottky barrier =0.07 eV; $R_{contact}$= 2kΩ- μm
- Highest peak g_m (at V_{tg}=-4.5V, V_{ds}=3.5 V) =38 $\mu S/\mu m$
  & mobility= 63 cm^2/Vs for CVD MoS_2; V_{sat}= 10^6cm/s

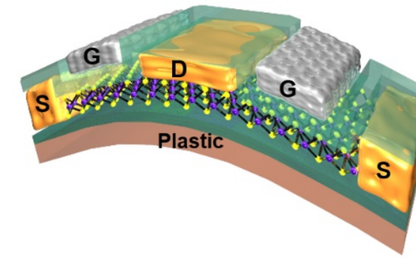
Sanne….Banerjee, Nano. Lett. 2015.

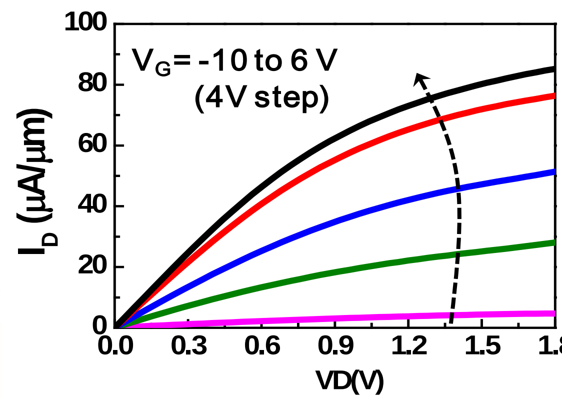
MoS_2 FET fabrication and characterization on flexible polyimide substrates





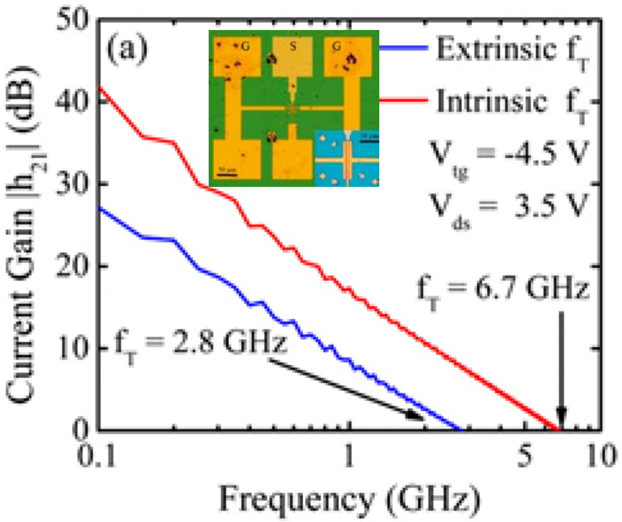


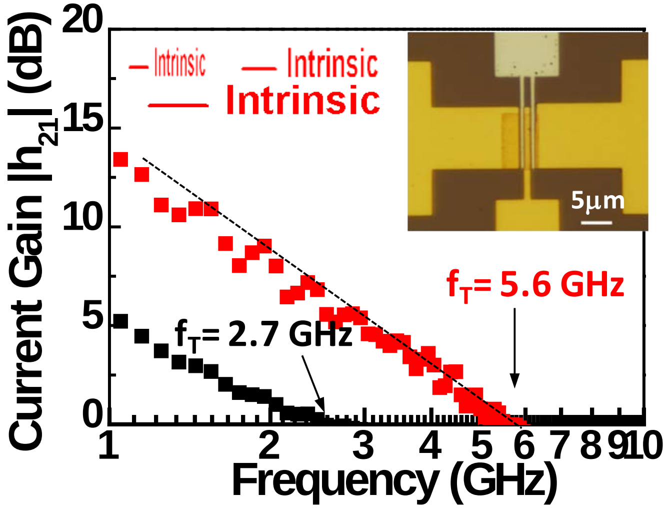


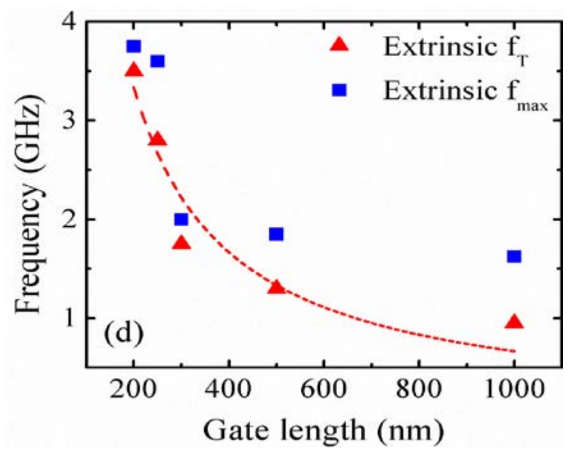


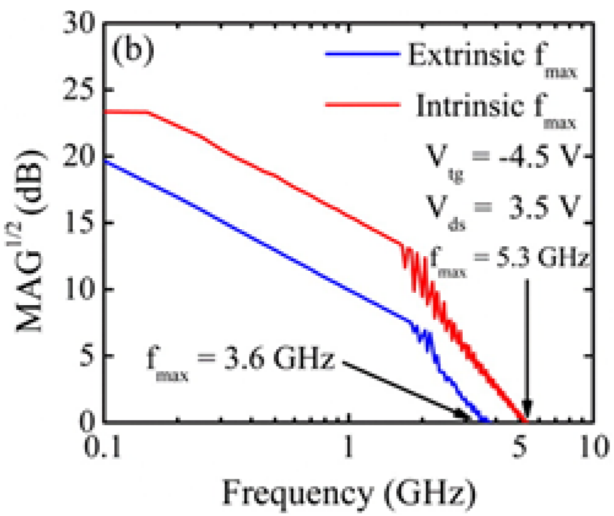
Chang,… Banerjee, Akinwande "**Large-area monolayer MoS2 for flexible low-power RF nanoelectronics in the GHz regime**; " Advanced Materials Dec 2015.

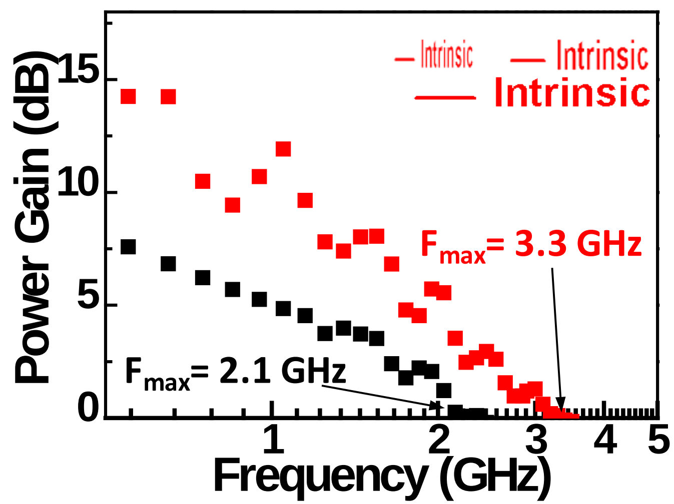
High Frequency Performance of MoS_2 Flexible RF FETs







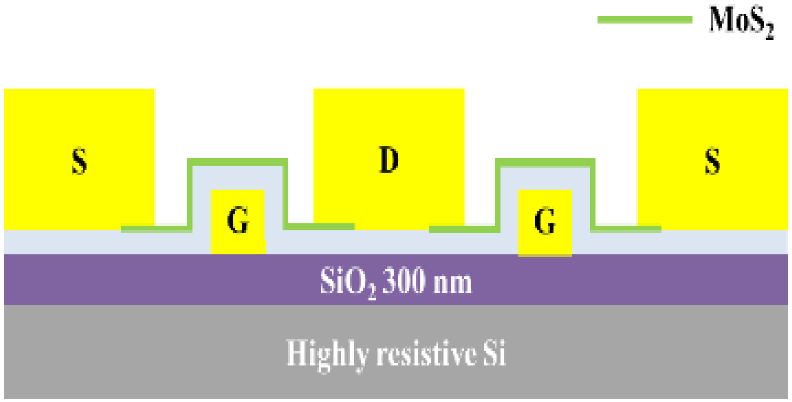


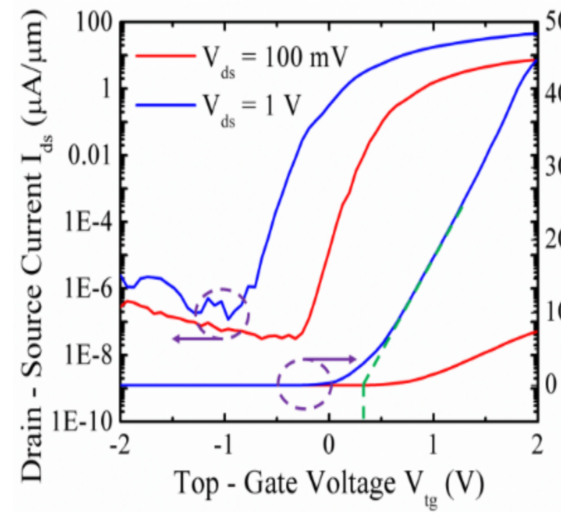


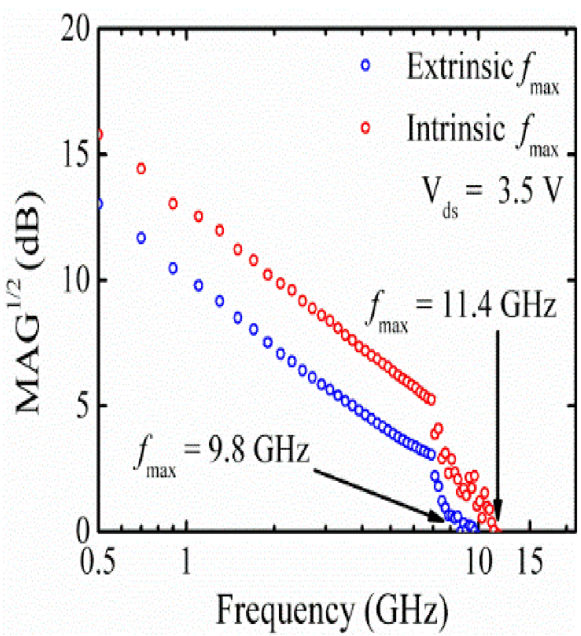
- **MoS_2 RF Transistor on SiO_2/Si**
- **MoS_2 RF Transistor on Polyimide**

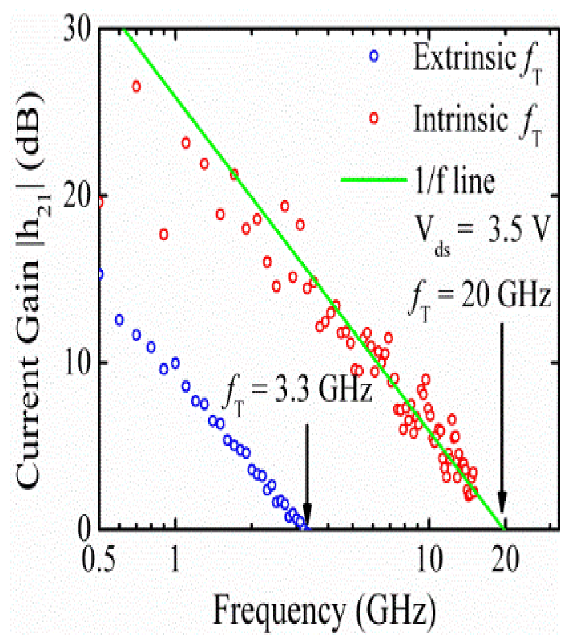
Sanne… Banerjee “Radio Frequency Transistors and Circuits Based on CVD MoS2**”;** *Nano Letters* 2015 *15* (8), 5039-5045
Chang.. Banerjee, Akinwande “Large-area monolayer MoS2 for flexible low-power RF nanoelectronics in the GHz regime; “ Advanced Materials Dec 2015.

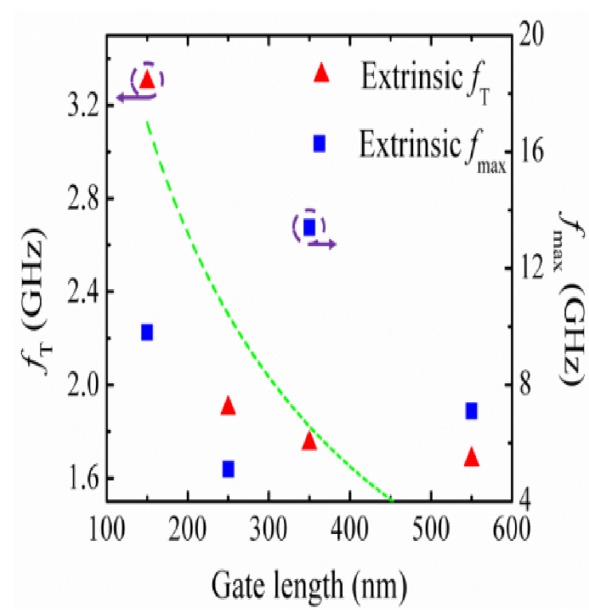
Back-gated CVD MoS_2 FETs



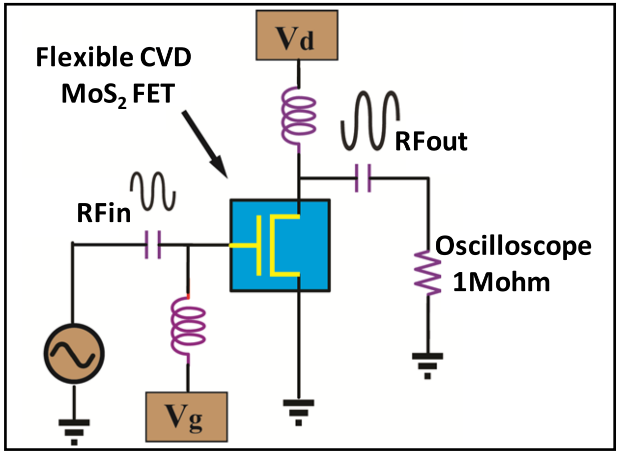


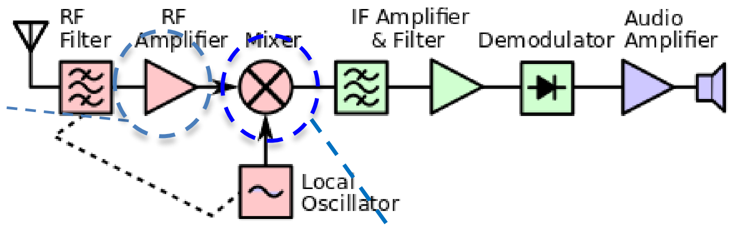


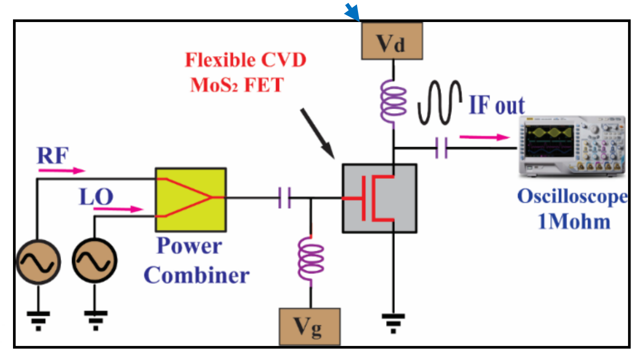


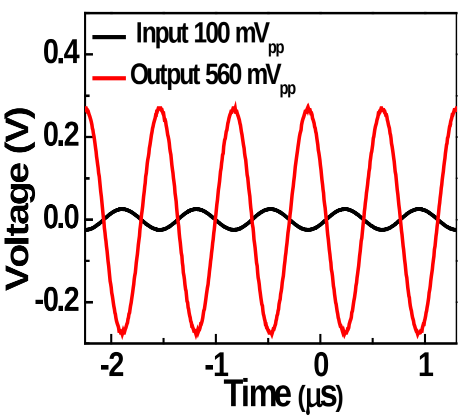


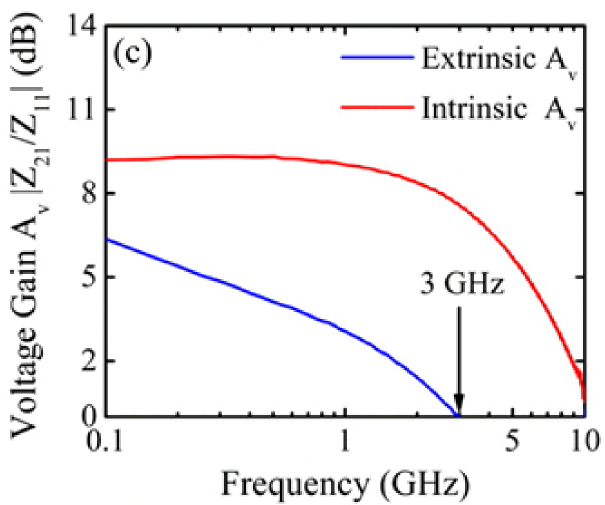
Flexible MoS_2 based RF circuits



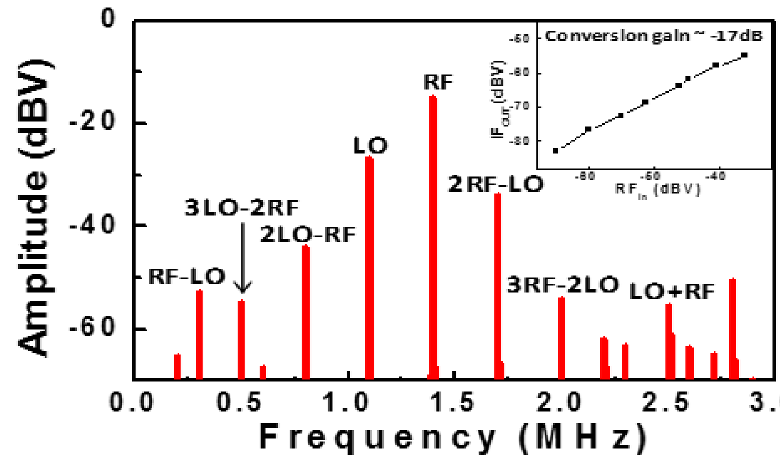






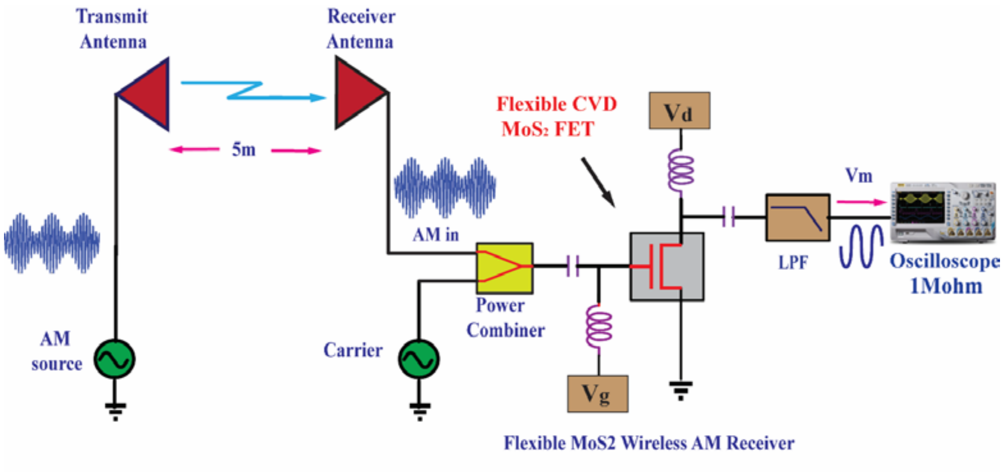


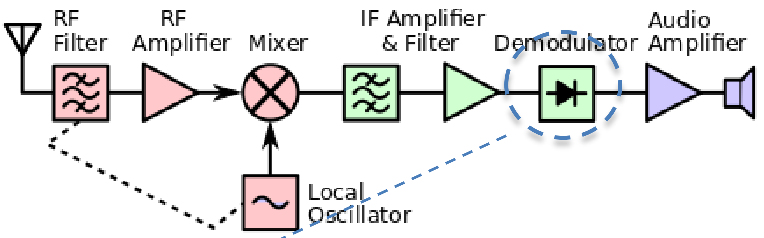
Flexible MoS_2 amplifier



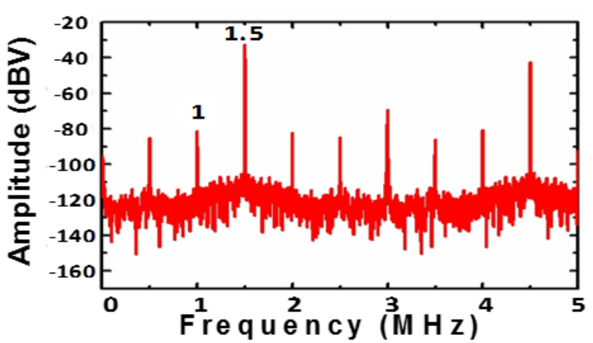
Flexible MoS_2 Mixer

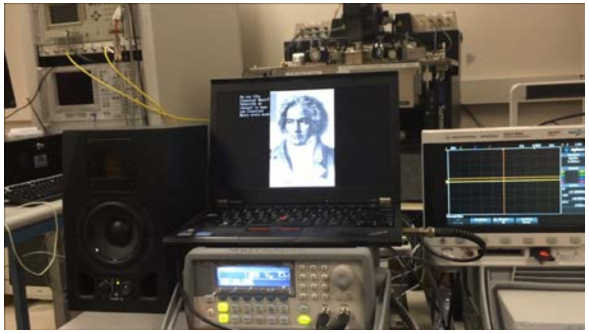
Flexible MoS_2 based Radio





Flexible MoS_2 AM Demodulator

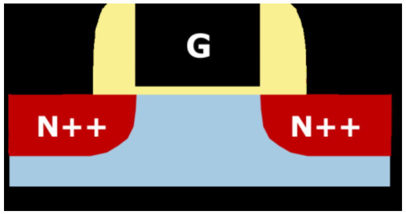


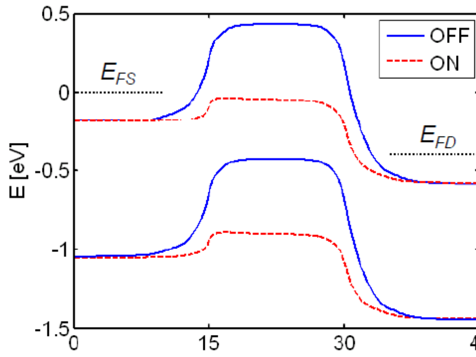


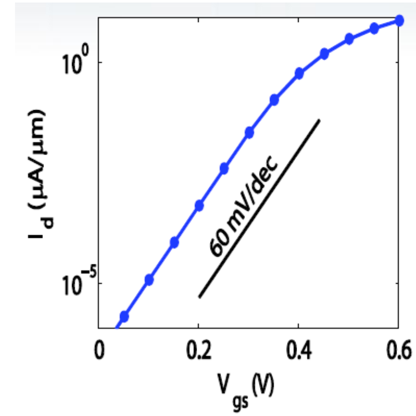
- **Flexible MoS_2 AM Receiver Output Spectrum**

MOSFETs vs. Steep Slope TFETs & Resonant TFETs

- MOSFETs

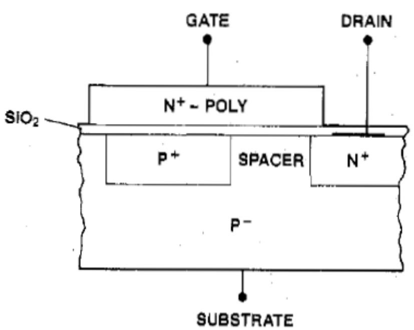


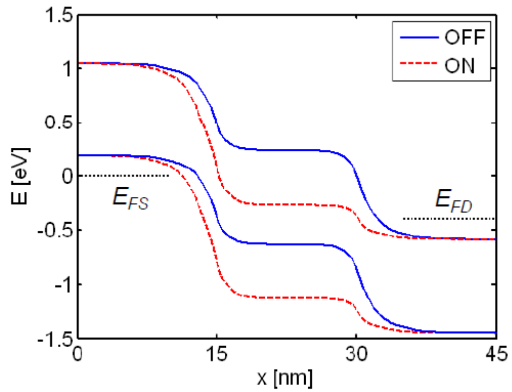


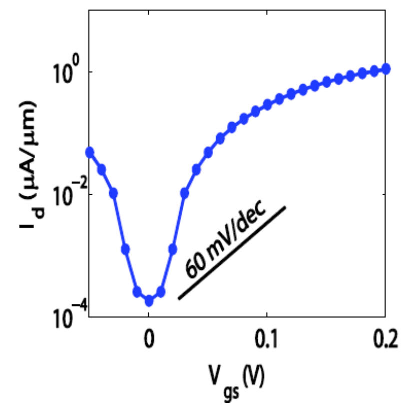


- Steep slope TFETs

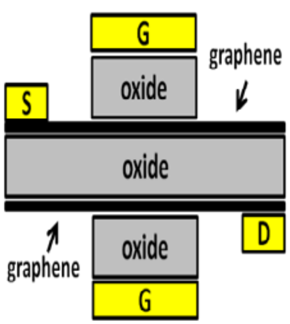
(Banerjee, ..EDL 1987)

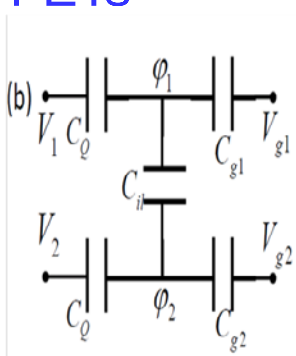


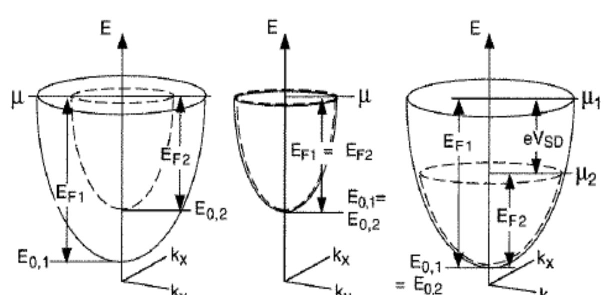


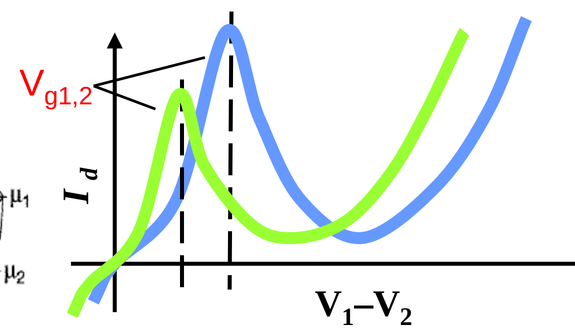


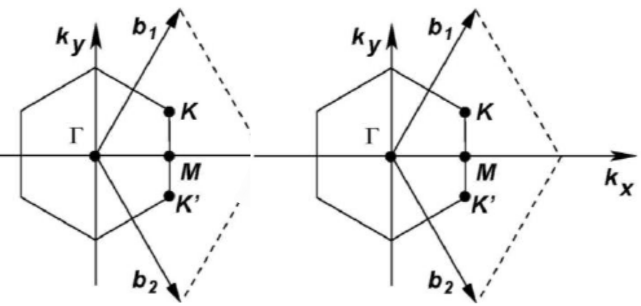
- Resonant ITFETs

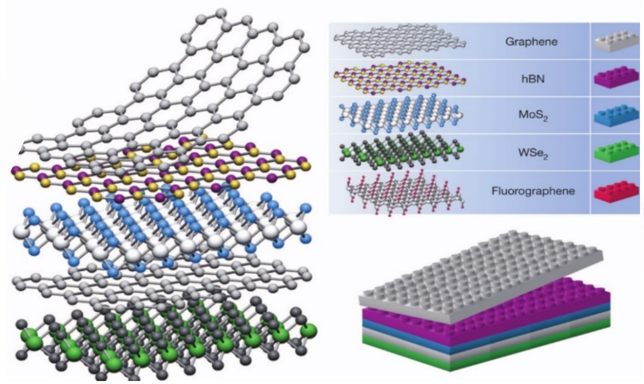


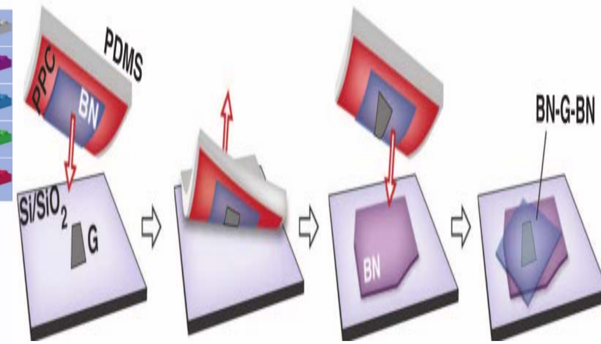


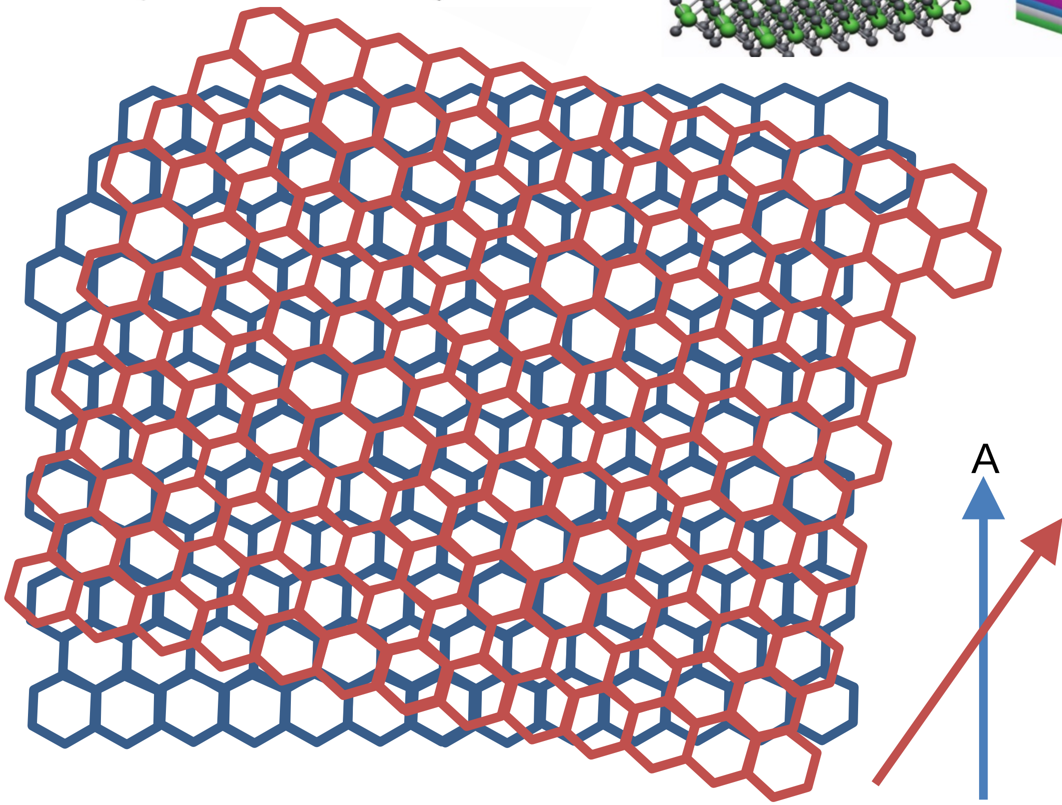


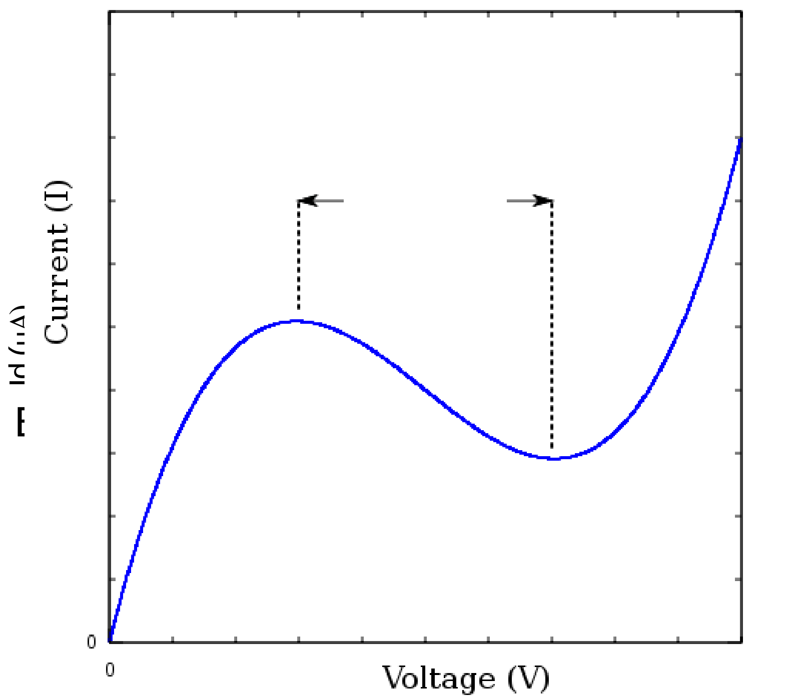












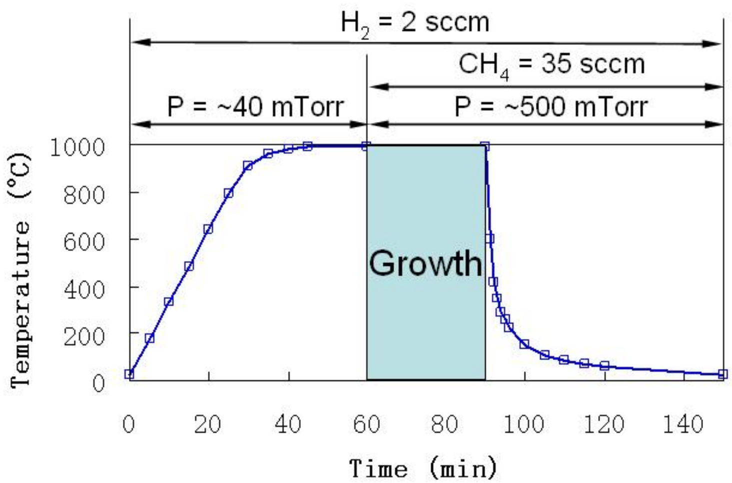
Rotationally misaligned 2D materials

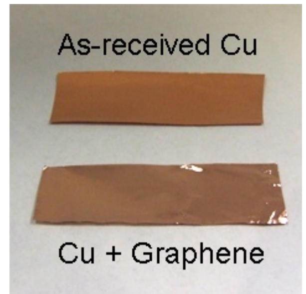
Rotationally **ALIGNED 2D materials**

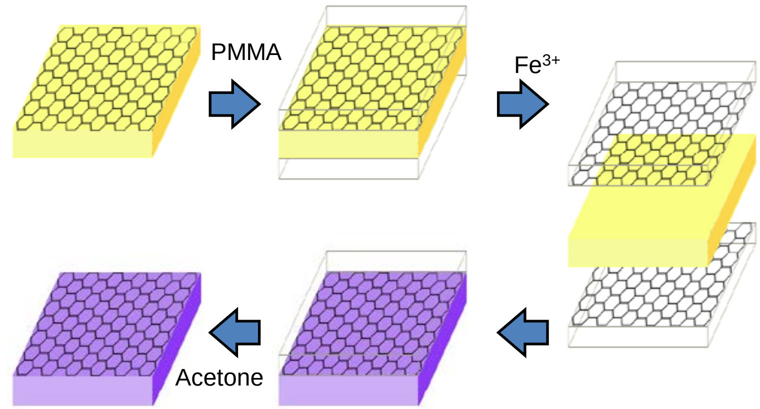
Negative differential resistance

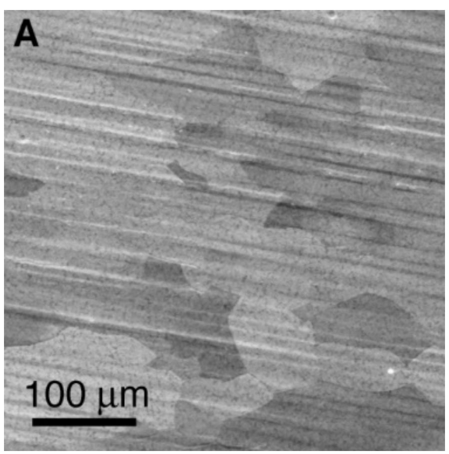
Tunneling behavior

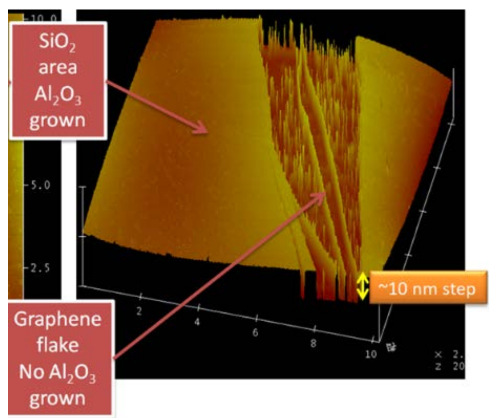
Large-Area Graphene Grown on Cu Foils and FETs with high-k

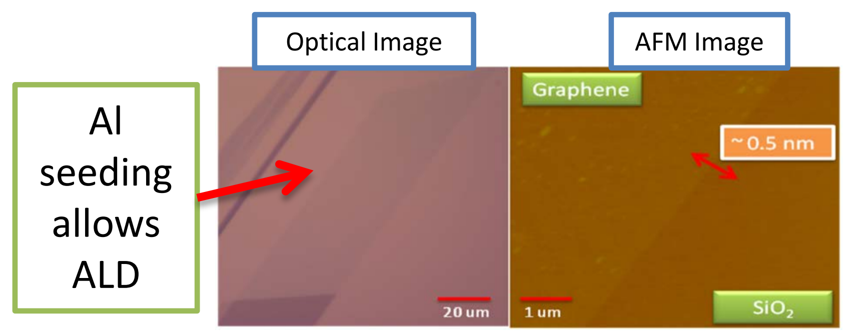






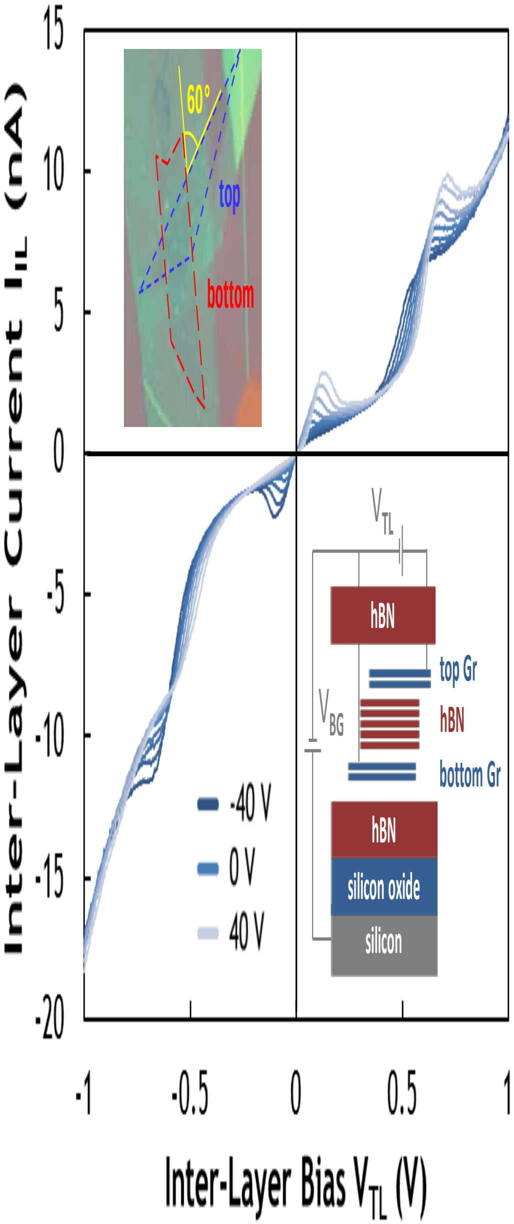


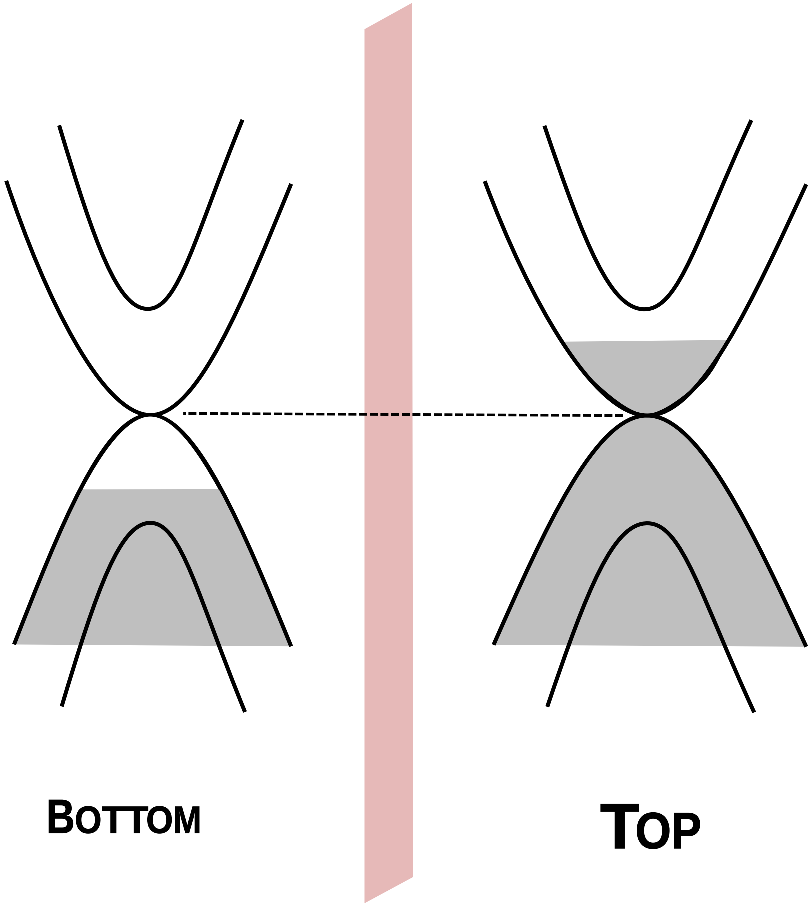




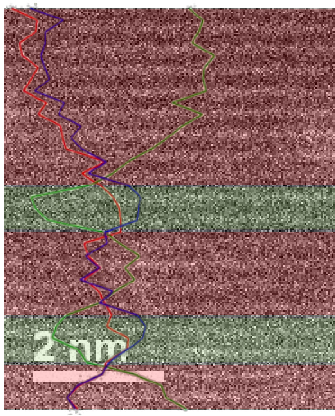
Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils
Xuesong Li, Weiwei Cai, Jinho An, Seyoung Kim, Junghyo Nah, Dongxing Yang, Richard Piner, Aruna Velamakanni, Inhwa Jung, Emanuel Tutuc, Sanjay K. Banerjee, **Luigi Colombo, Rodney S. Ruoff** *Science*, 2009 (6500 citations)

Origin of the First and Second NDR?





n-layer BN
2-layer Gr
4-layer BN
2-layer Gr
2-layer BN

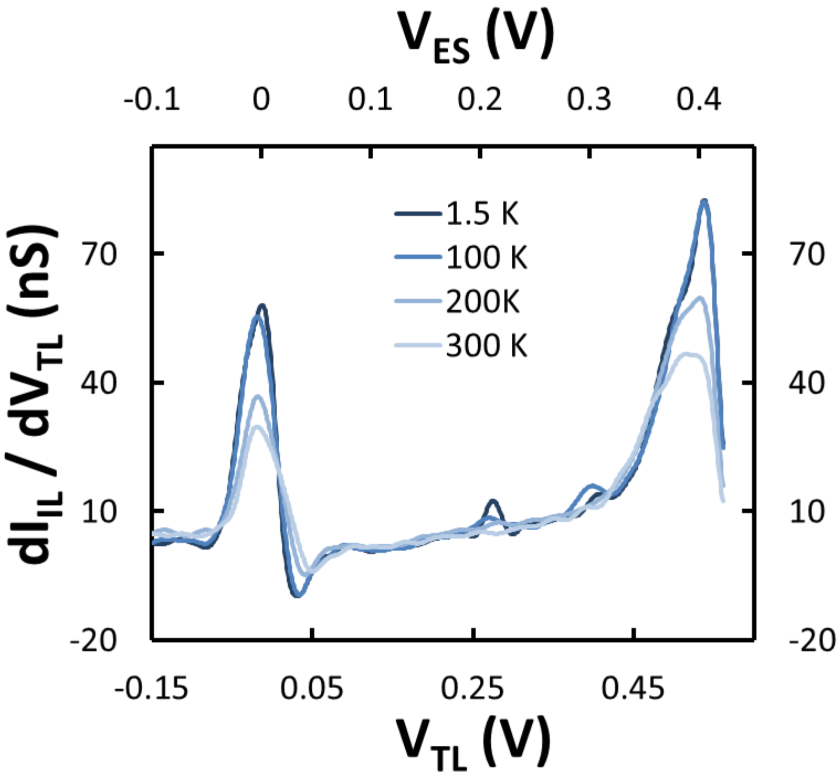


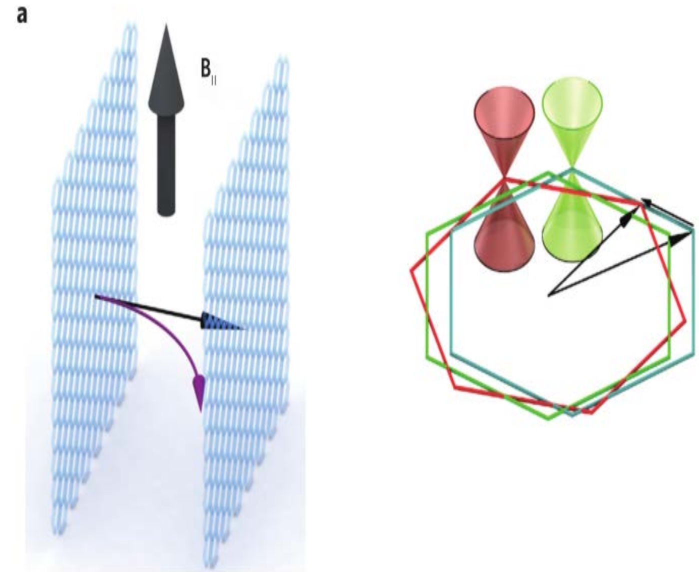
HRTEM AND EELS OF ITFET (COURTESY, M.KIM)

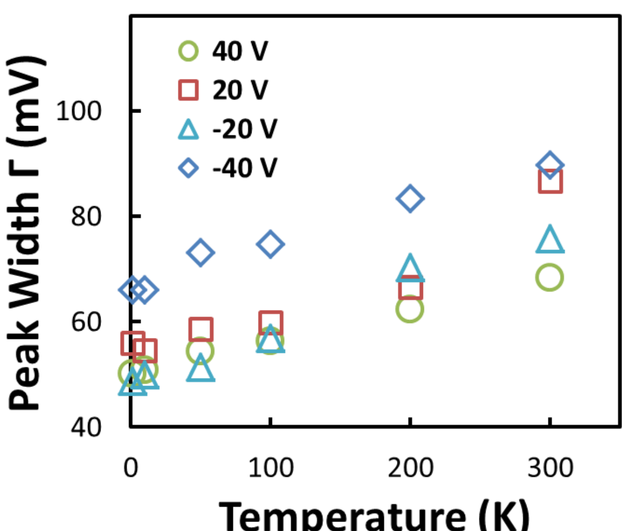
Fallahazad... Register, Banerjee, Tutuc Nano. Lett (2015)

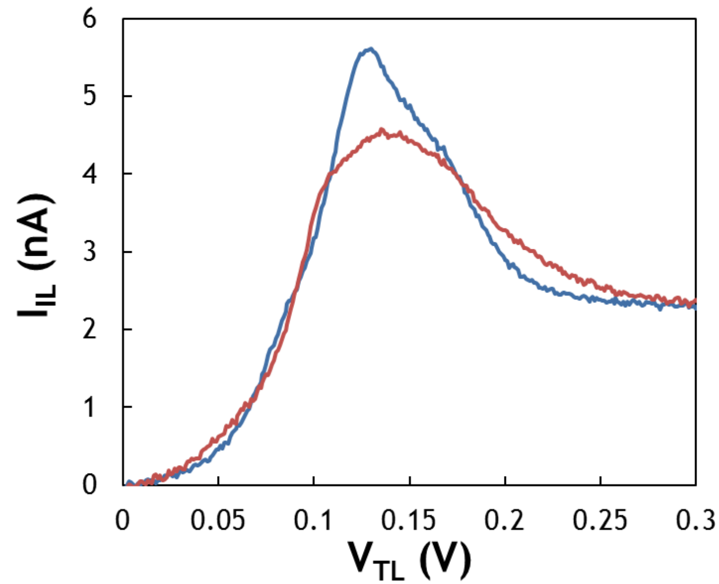
Kang.... Register, Tutuc, Banerjee, EDL (2015)

Tunneling vs. Temperature and Magnetic Field

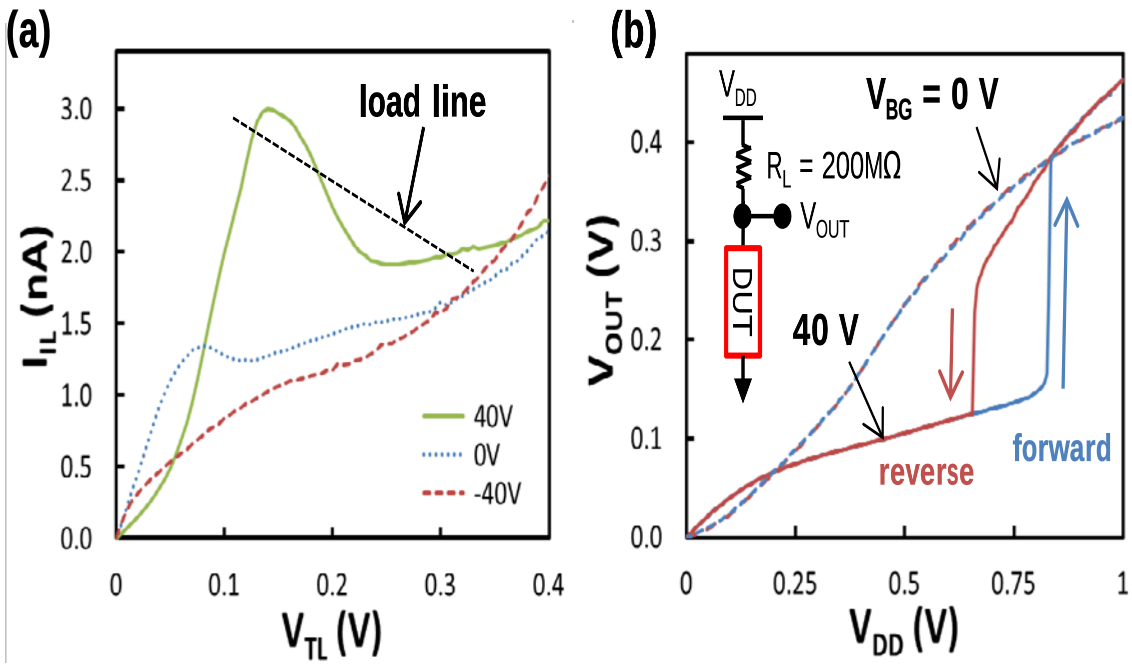


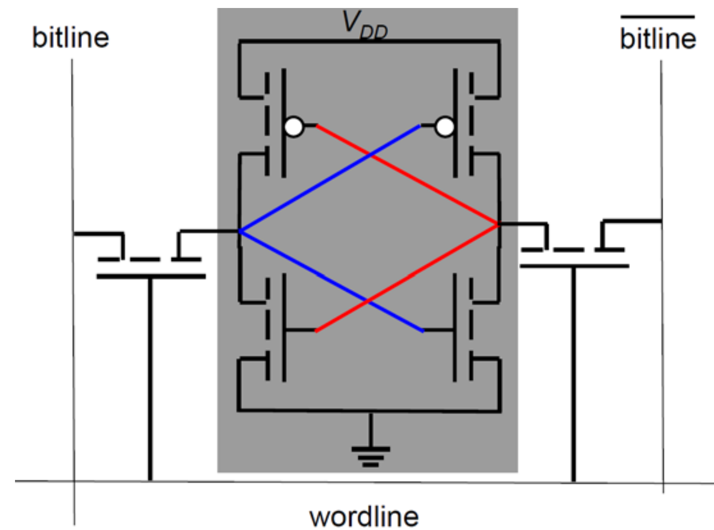




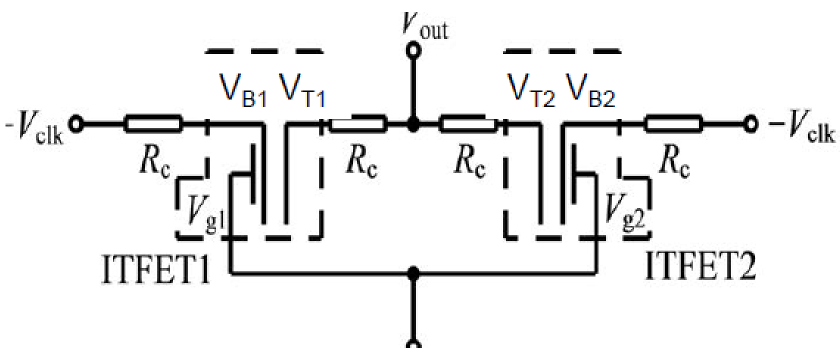


ITFET SRAM and Inverter



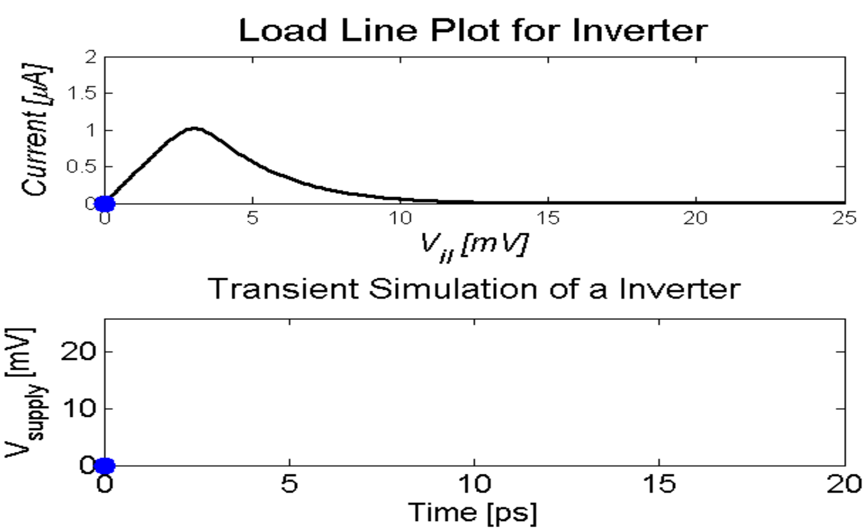


Kang.... Register, Tutuc, Banerjee, EDL (2015)

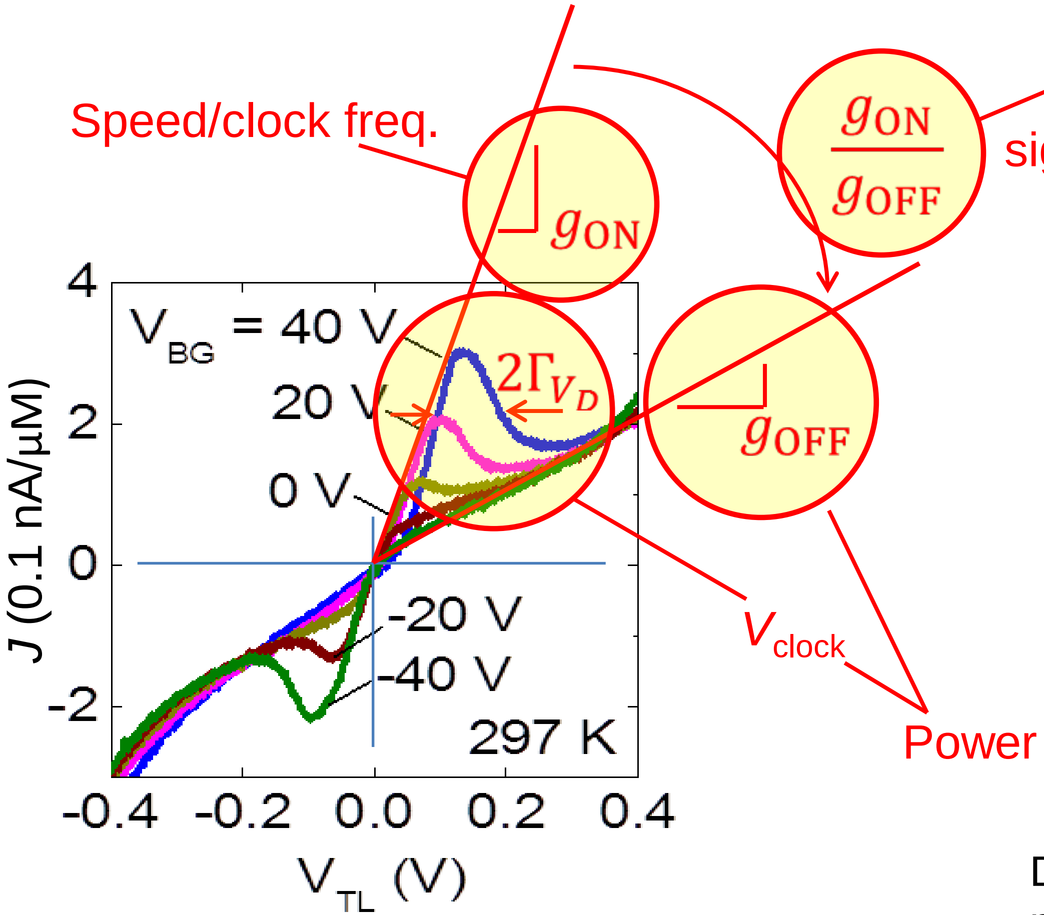


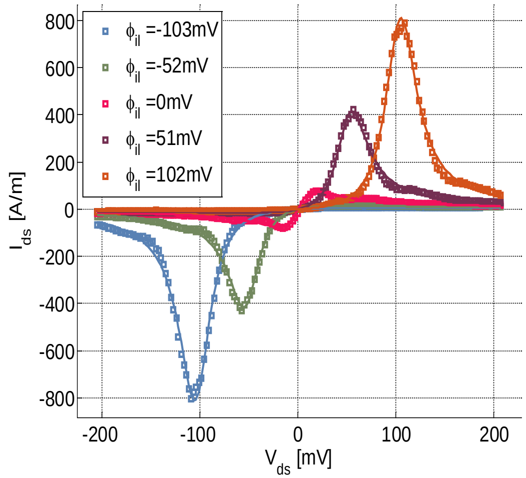
V_{in} = 0, 1

V_{out} = 1, 0



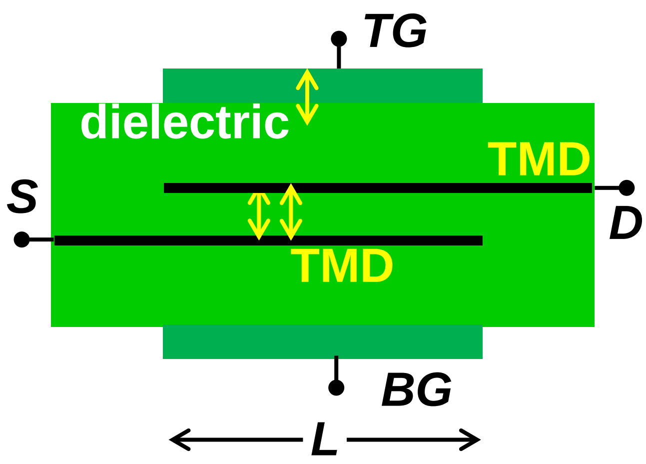
Effects of device characteristics on ITFET circuit performance

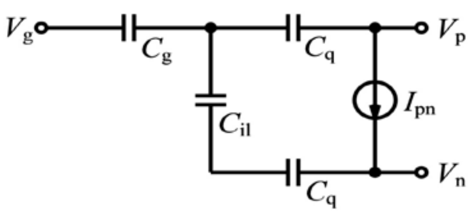




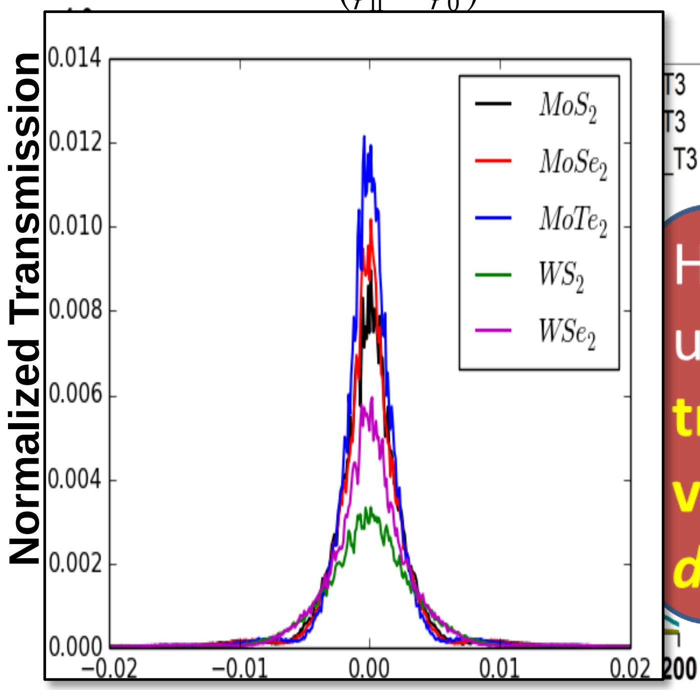
DFT + NEGF simulations predict higher ON/OFF
Need rotational alignment of electrodes *and tunnel barrier*

Resonance Broadening, Short-Channel Effects, Carrier Velocity, Scattering





$$I_{tun} = \frac{A\Gamma(V_p - V_n)}{\Gamma^2 + (\phi_{il} - \phi_0)^2}$$



Tunneling probability vs. interlayer potential $\pm\Delta V_c$ for 25 meV normally incident electrons in GaAs/AlAs and graphene ITFET

Heisenberg $\Delta k \Delta x$ uncertainty … **translated to $\Delta E \Delta x$ via carrier velocity $dE/d(\hbar k)$**

Short L

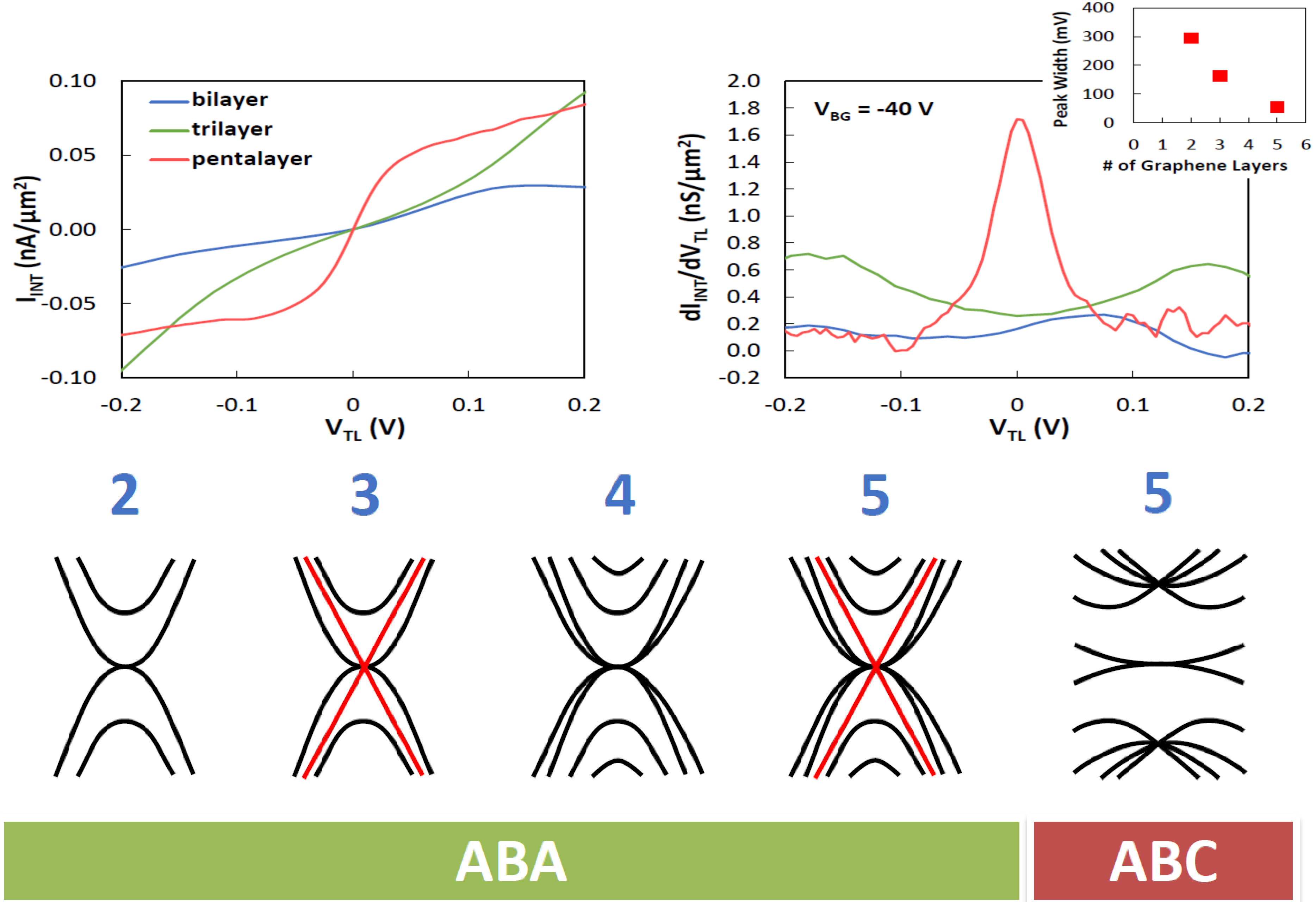
Fast carriers

Scattering

→ **Large energy broadening** → **High voltage, power**

Need *low defect* TMDs with *high* effective mass to reduce broadening Γ and power
Need vdWE with *clean* interfaces and rotational *alignment* to reduce OFF current

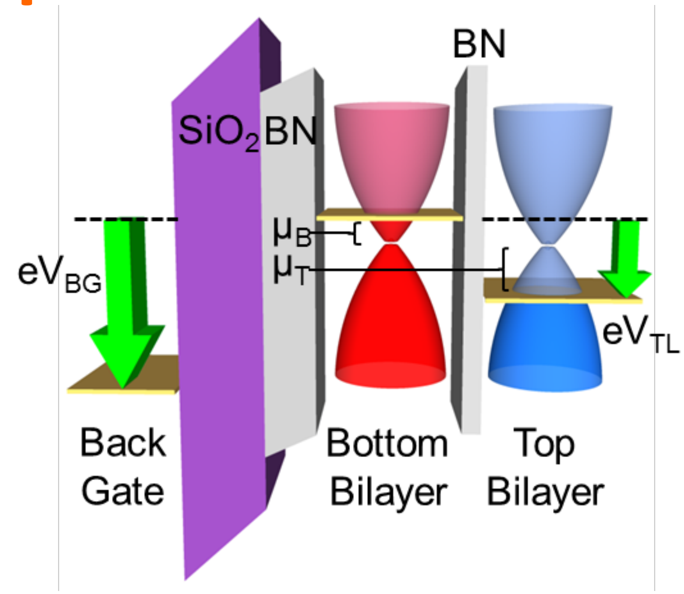
Graphene Thickness Dependence



Quantum vs Interlayer Capacitance

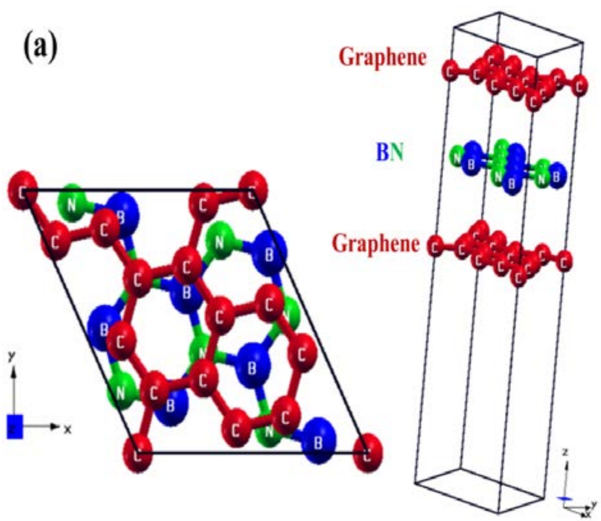
$$V_{TL} = \frac{-en_T}{C_{int}} + (\mu_B - \mu_T)/e$$

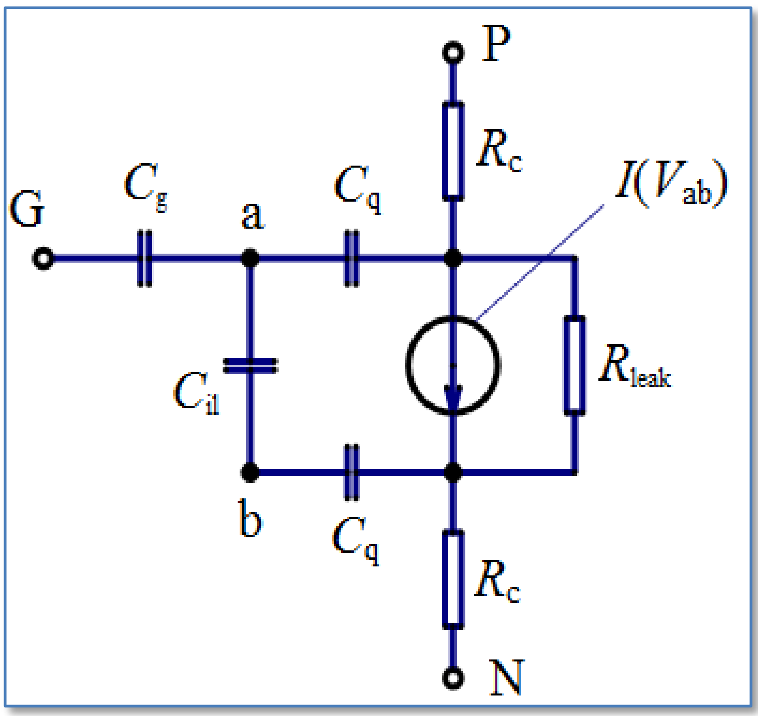
$$V_{ES} = V_{TL} - (\mu_B - \mu_T)/e = 0$$



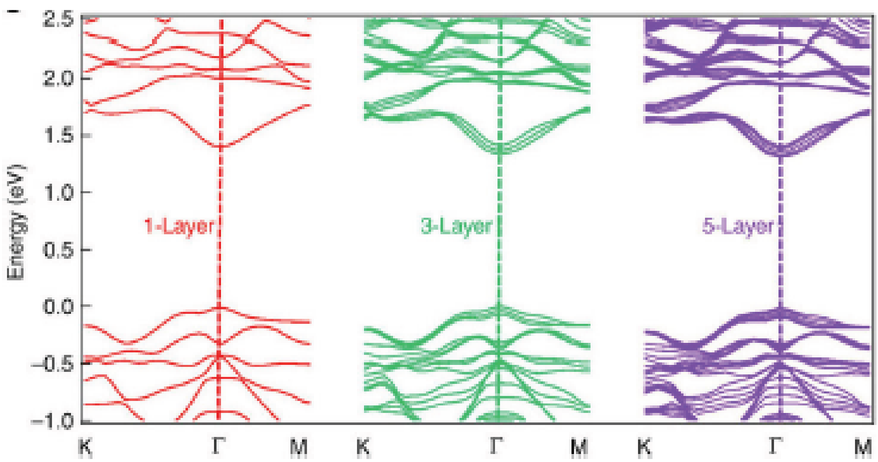
- Resonances occur when electrons momentum **and** energy are conserved:
- Using $\mu = \frac{n}{DOS} = \frac{e^2 n}{C_Q}$ $\quad V_{TL} = V_{ES}\left(1 + \frac{2C_{int}}{C_Q}\right)$
- Resonance width Γ "amplified" by $1 + \frac{2C_{int}}{C_Q}$ when measured as a function of V_{TL}

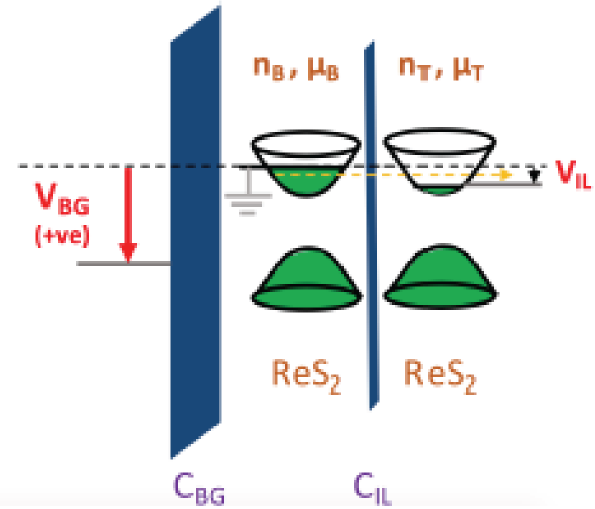
- Intrinsic resonance width (Γ) in V_{ES} determined by quasi-particle lifetime and rotational misalignment



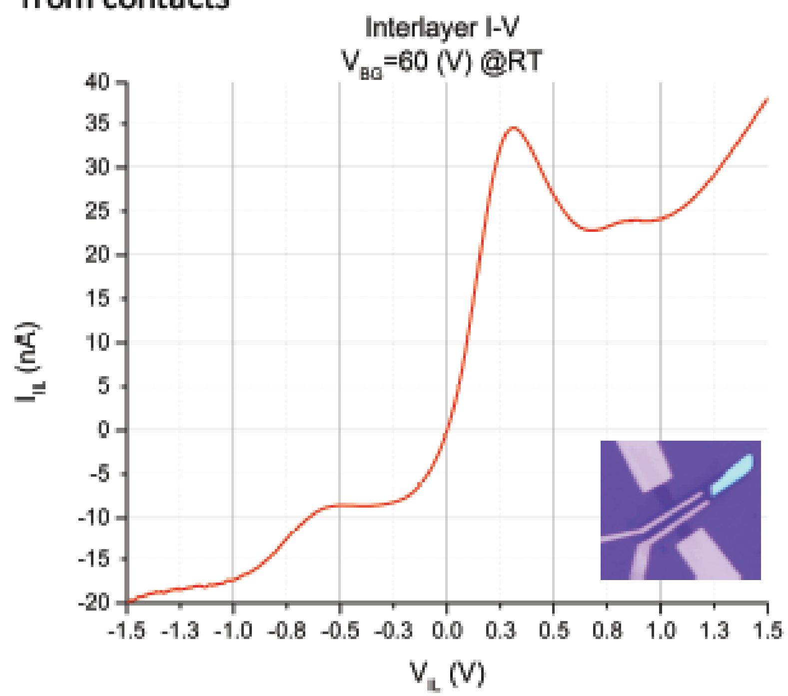


- ReS$_2$ is a stable, direct bandgap TMD material, regardless of the number of layers [1].
- Ab initio calculations indicate bandgaps of monolayer, tri-layer, and five-layer ReS$_2$ are 1.44, 1.4, and 1.35 eV, respectively [1].

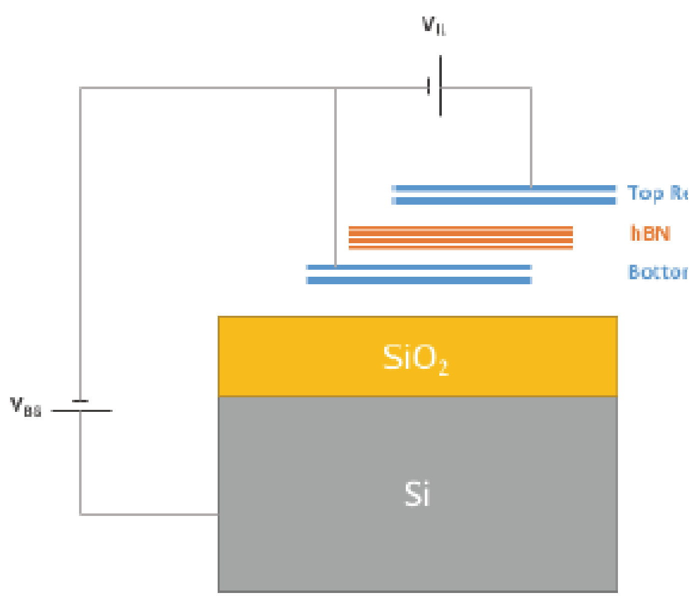




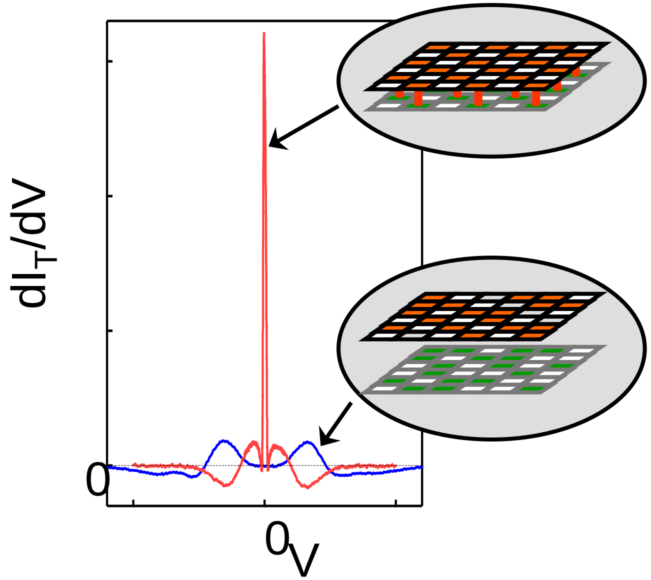
- Room temperature interlayer I-V characteristics showing multiple NDR. However, there could also be contribution from contacts

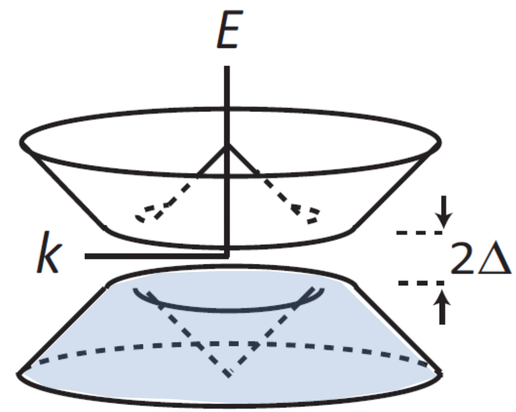


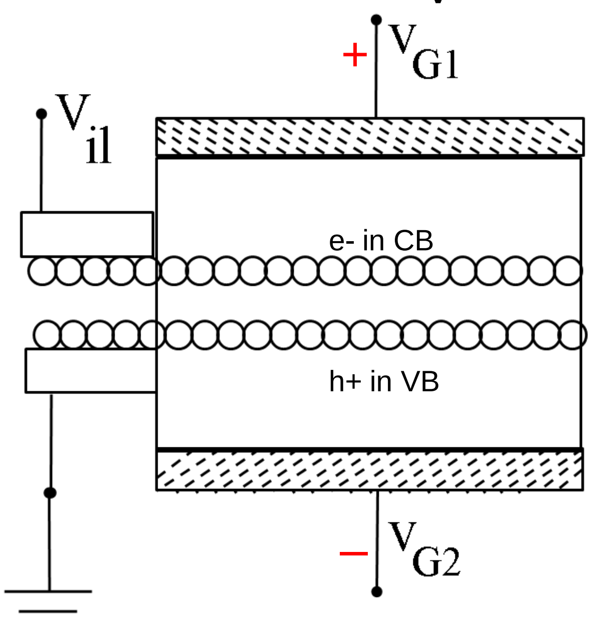
- Schematic and biasing scheme of the device; the n$^+$ Si substrate is used as the back gate while the top layer is biased and the bottom layer is at ground.

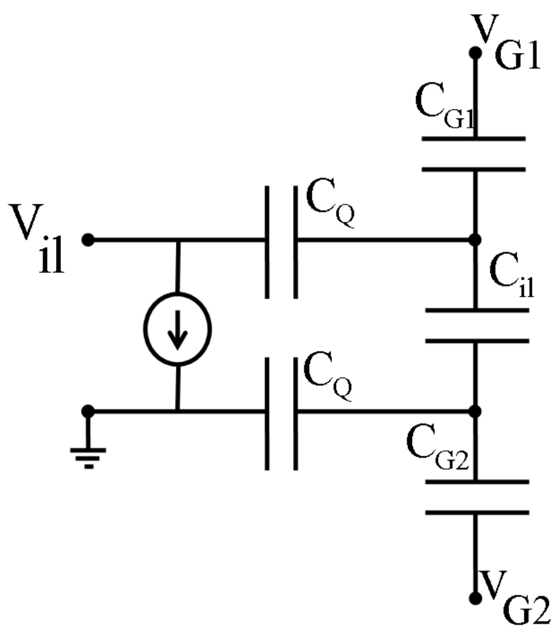


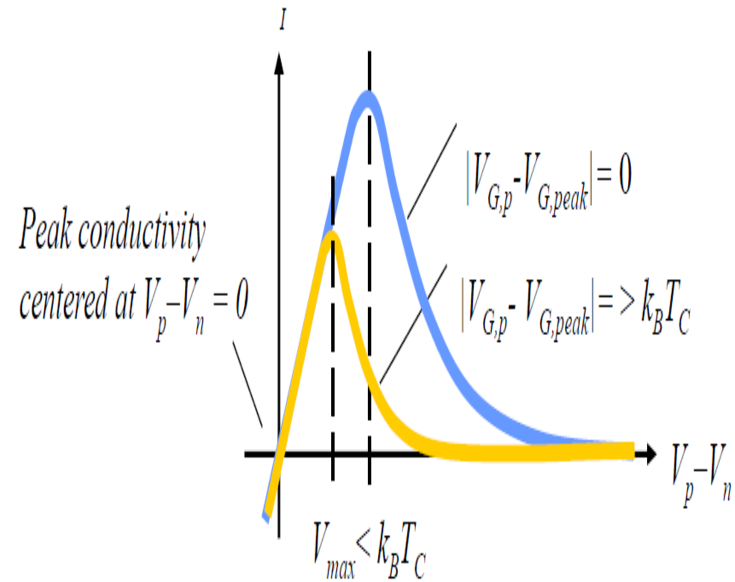
Bi-layer pseudoSpin Field Effect Transistor (BiSFET)

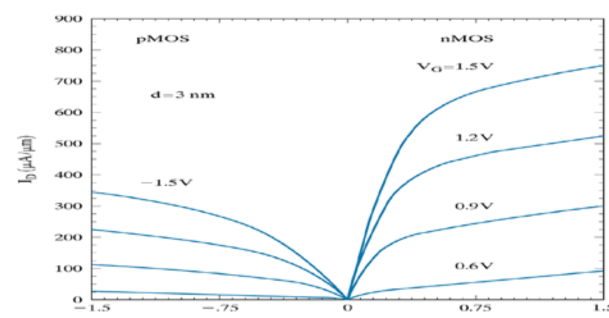






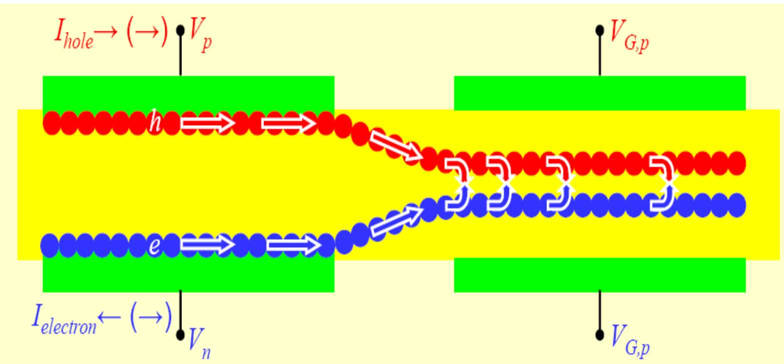


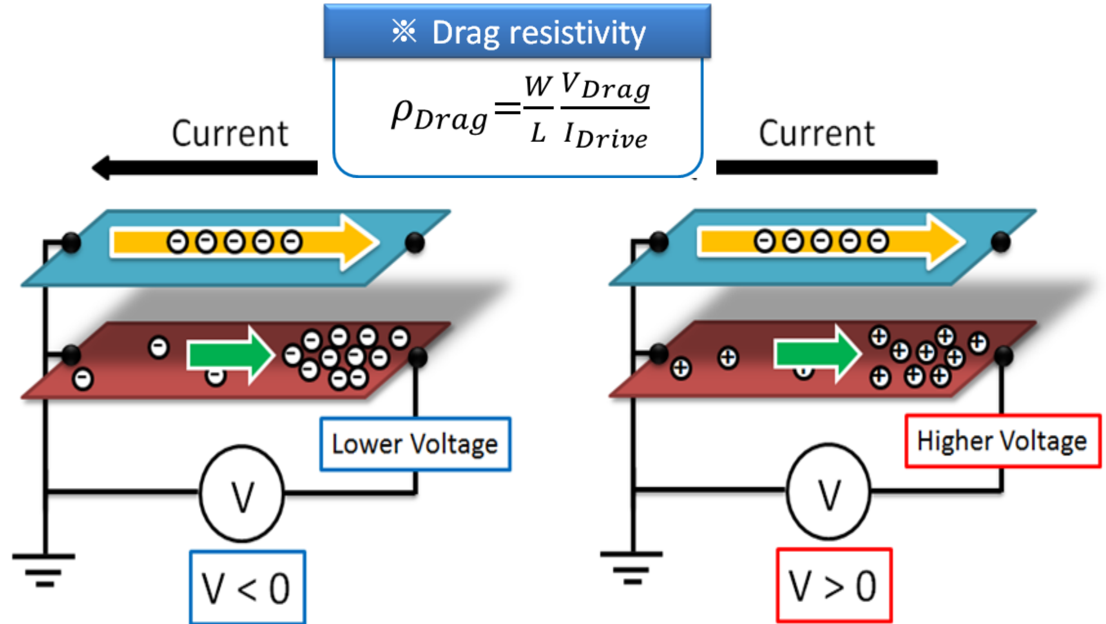


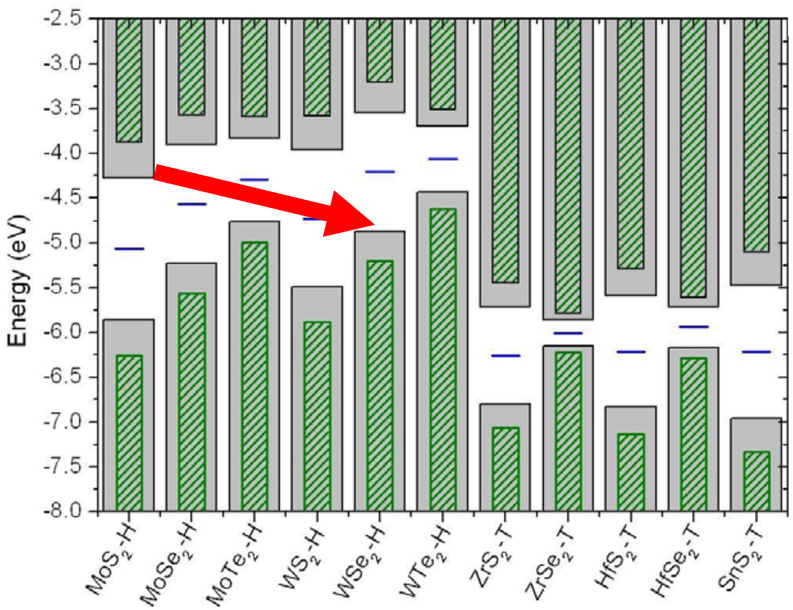


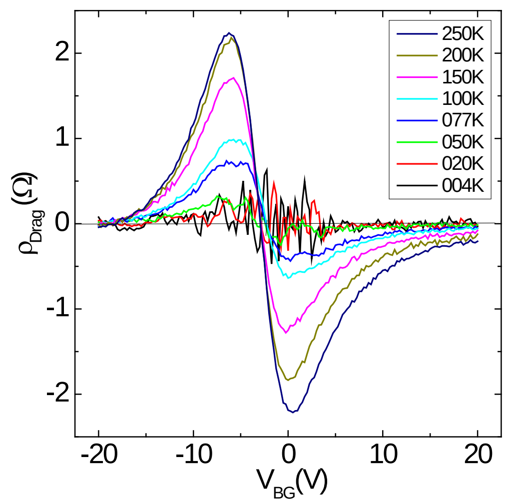
"Bilayer pseudoSpin Field Effect Transistor (BiSFET): a proposed new logic device"
Banerjee, Register, Tutuc, Reddy and Macdonald, IEEE EDL, Feb. 2009; also US patent

Bose Condensate in Graphene/TMD Heterostructures??





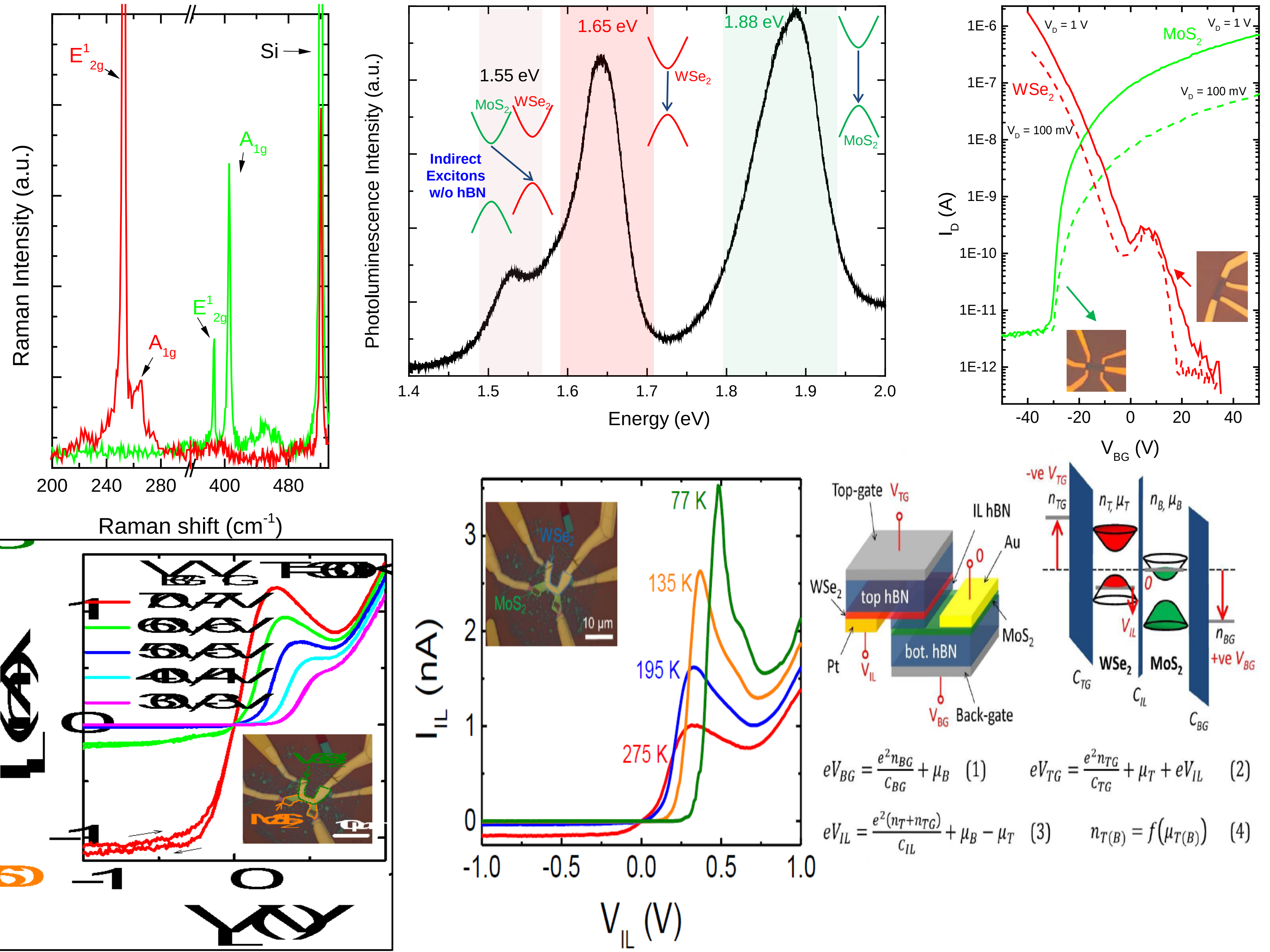




$$\frac{1}{\tau(\mathbf{k}_1)} \propto \sum_{\mathbf{k}_1'\mathbf{k}_2\mathbf{k}_2'} |W|^2 f_1 f_2 (1-f_{1'})(1-f_{2'})\delta(\epsilon_1+\epsilon_2-\epsilon_{1'}-\epsilon_{2'})\delta_{\mathbf{k}_1+\mathbf{k}_2,\mathbf{k}_1'+\mathbf{k}_2'}\,.$$

Gong,….Colombo, Wallace, Cho, APL, 2013

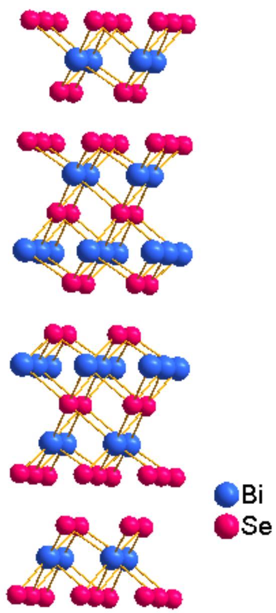
Kim, .. Banerjee, Tutuc, PRB 2011

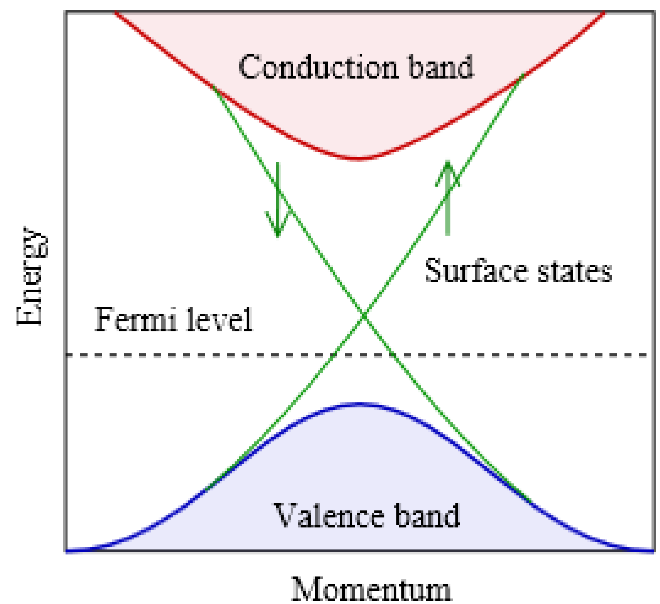


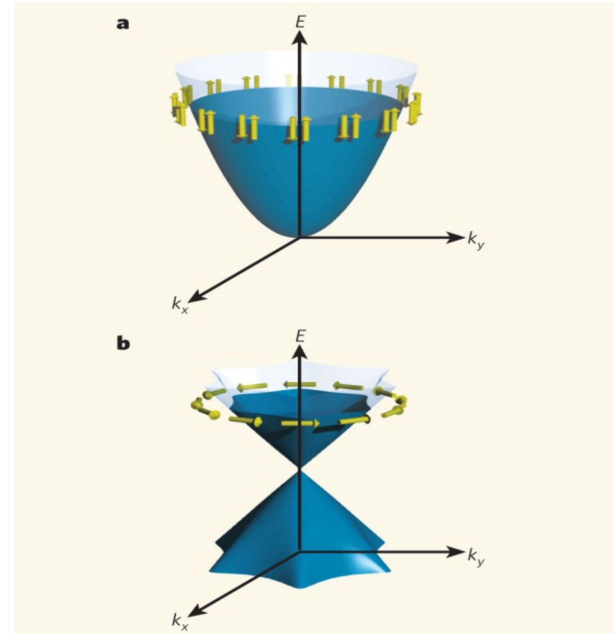
$$eV_{BG} = \frac{e^2 n_{BG}}{C_{BG}} + \mu_B \quad (1) \qquad eV_{TG} = \frac{e^2 n_{TG}}{C_{TG}} + \mu_T + eV_{IL} \quad (2)$$

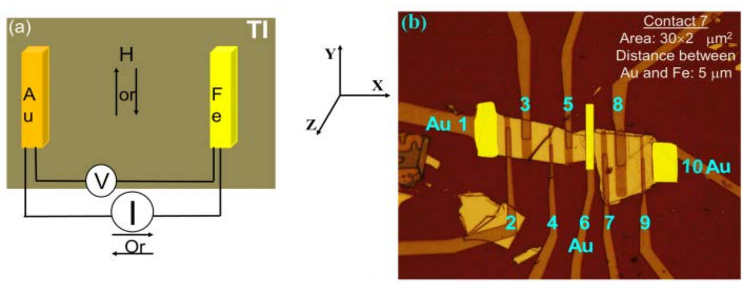
$$eV_{IL} = \frac{e^2(n_T + n_{TG})}{C_{IL}} + \mu_B - \mu_T \quad (3) \qquad n_{T(B)} = f(\mu_{T(B)}) \quad (4)$$

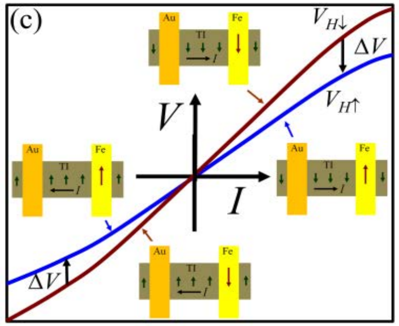
Spintronics with Topological Insulators

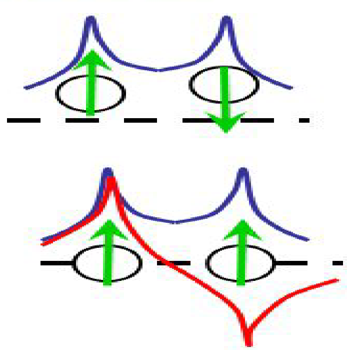


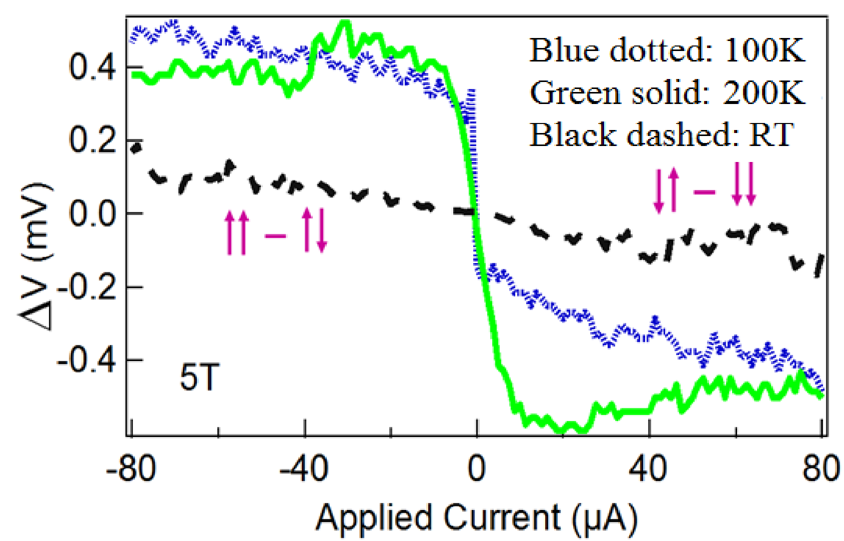




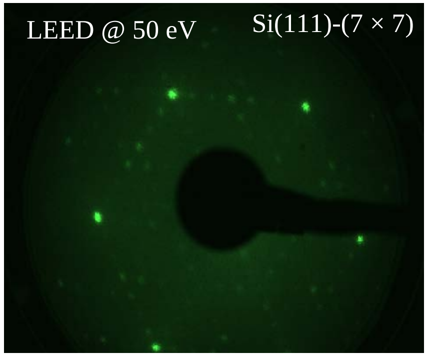


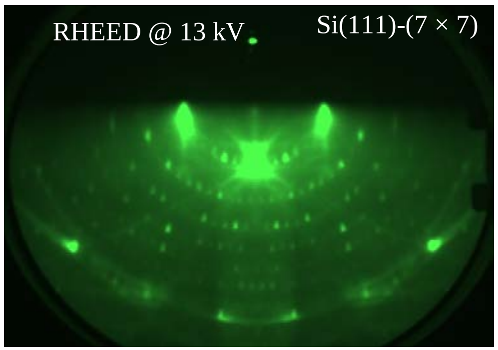


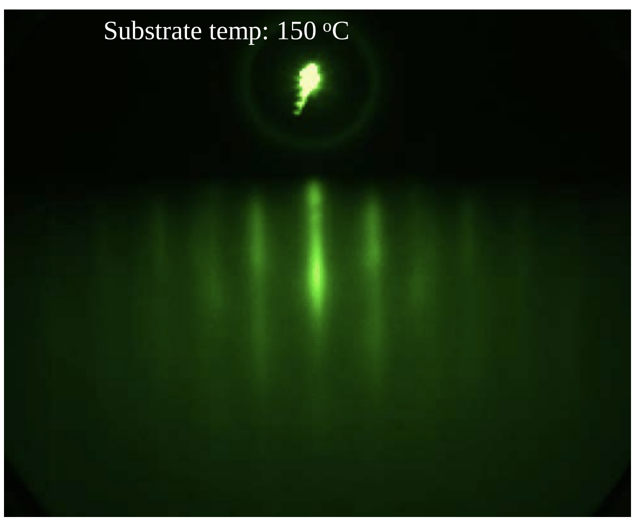




MBE of topological insulators

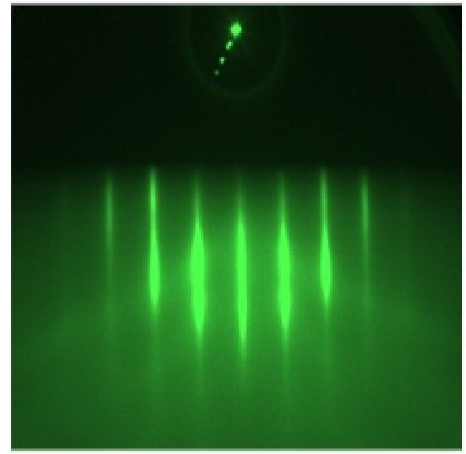


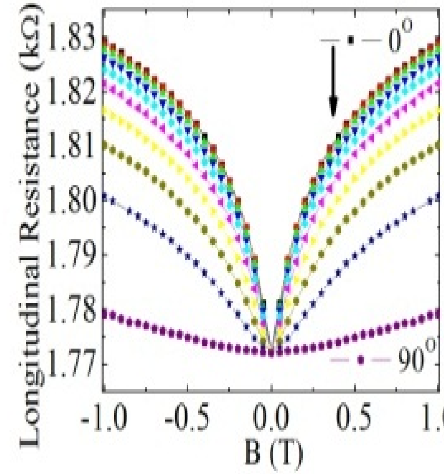




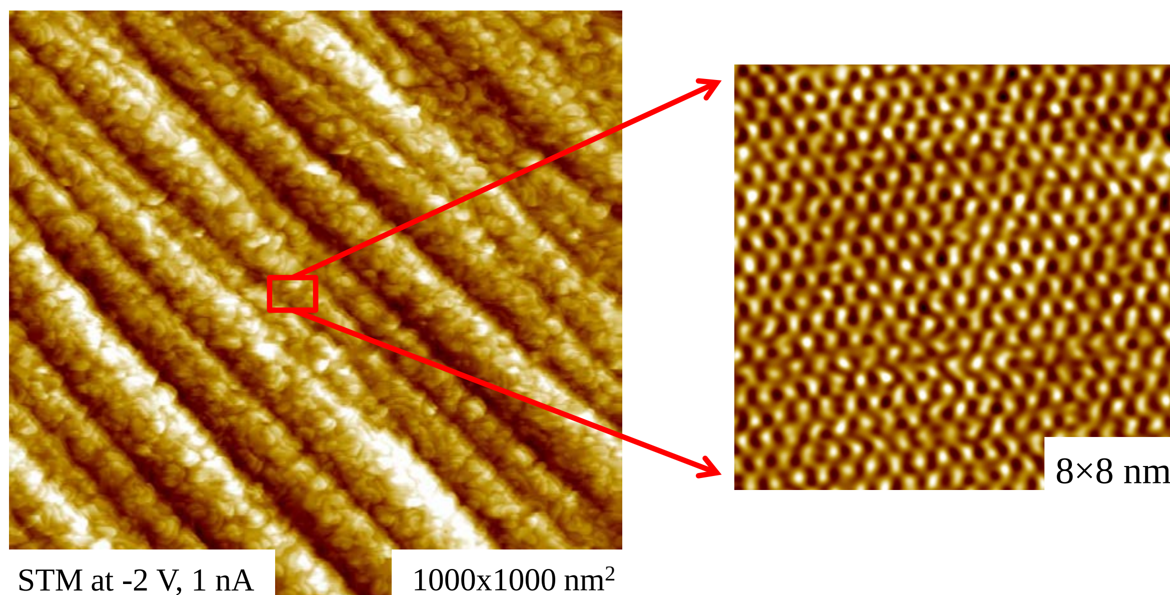
Sharp RHEED streaks

Bi_2Te_3 on Si(111)

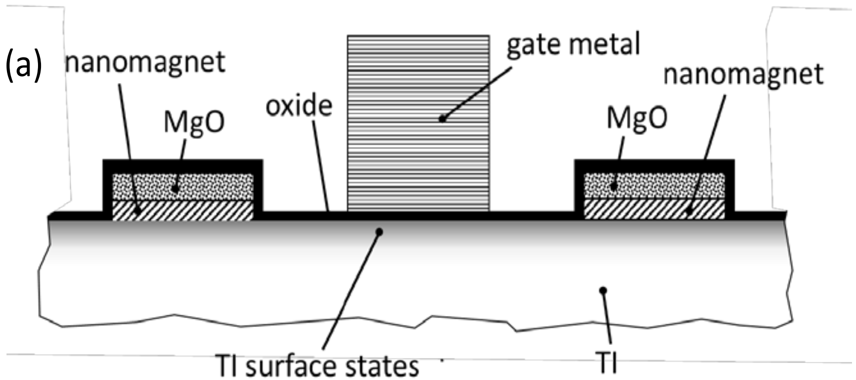




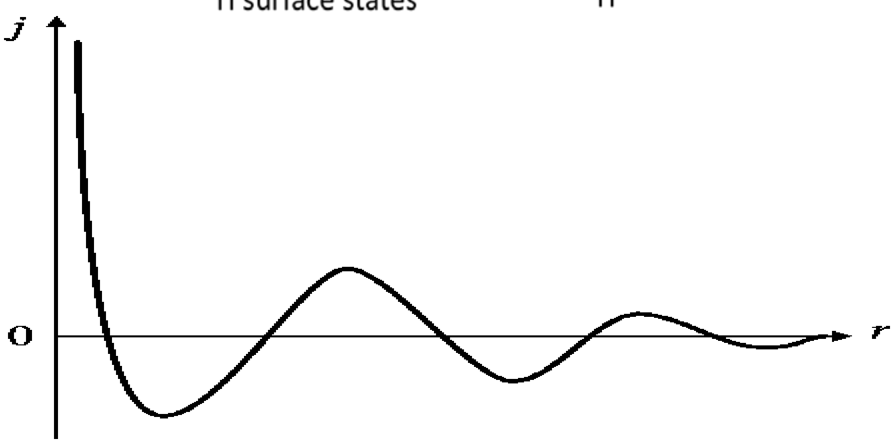
Bi_2Se_3 on Si(111)



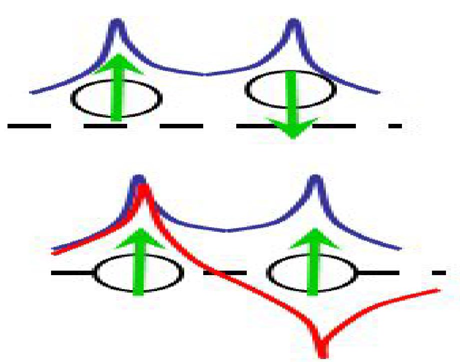
RKKY Coupling of Nanomagnets on TI

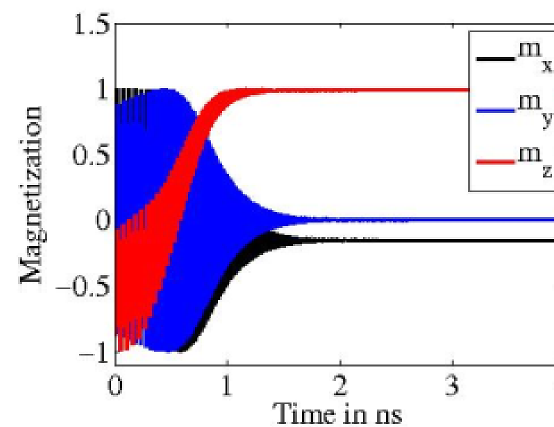


$$H^{\mathrm{RKKY}} = -\frac{J^2 \varepsilon_F}{2\pi^2 \hbar^2 v_F^2 R^2}\left[(S_1^x S_2^x + S_1^z S_2^z) \sin\left(\frac{2R\varepsilon_F}{\hbar v_F}\right) - (\mathbf{S}_1 \times \mathbf{S}_2)_y \cos\left(\frac{2R\varepsilon_F}{\hbar v_F}\right)\right]$$



$$\frac{d\hat{\mathbf{m}}}{dt} = -\gamma(\hat{\mathbf{m}} \times \mathbf{H}_{\mathrm{eff}}) + \alpha\left(\hat{\mathbf{m}} \times \frac{d\hat{\mathbf{m}}}{dt}\right)$$





$$\Delta = V[K_u - 0.5\,\mu_0 M_s^2 (N_{zz} - N_{xx})]$$

$$\tau = \tau_0 e^{\Delta/k_B T}$$

$$E_s = C_g V_g^2$$

Sub aJ energies possible

Ghosh, Register, Banerjee, JAP 2016; patent disclosure

Epilog

- **Need advances in vdW epitaxy of heterostructures, and in process modules such as doping and contacts**
- **Negative differential resistance (NDR) Tunnel FETs can lead to novel logic and memory**
- **Pseudospintronics and spintronics for ultra-power and non-volatile devices**
- **IoT devices need on chip power generation**