N. VLSI CAD 분과

2017년 2월 15일 (수), 15:25-17:10
Room H (다이아몬드1, 3층)

[WH4-N] Advances in Design Automation and Test

좌장: 정재용(인천대학교), 이종은(UNIST)

WH4-N-1 **15:25-15:40**	**High-Level Synthesis for Neuromorphic Computing: Convolutional Neural Network Case Study** Daewoo Kim and Jongeun Lee *School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology*
WH4-N-2 **15:40-15:55**	**Efficient Execution of Streaming Application by the Approach of Packet Structure based on Coarse-Grained Reconfigurable Architecture** Sangyun Oh and Jongeun Lee *School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology*
WH4-N-3 **15:55-16:10**	**Full-Chip Level Estimation of Temperature-Dependent Leakage Power** Suhyeong Choi[1], Seongbo Shim[2], and Youngsoo Shin[1] *[1]School of Electrical Engineering, KAIST, [2]Samsung Electronics Co., Ltd.*
WH4-N-4 **16:10-16:25**	**Cube-based TSV Redundancy Architecture for Yield Improvement of 3D-ICs** Minho Cheong, Ingeol Lee, Jaewon Jang, Jaeseok Park, and Sungho Kang *Department of Electrical & Electronic, Yonsei University*
WH4-N-5 **16:25-16:40**	**고장 그룹화 및 고장 그룹 분류 기반 메모리 수리 방법론** 이하영, 김주영, 김동현, 강성호 *Department of Electrical and Electronics Engineering, Yonsei University*
WH4-N-6 **16:40-16:55**	**다중 전원 영역 기반 SoC의 모듈러 스캔 테스트를 위한 IEEE std. 1149.1-2013 기반의 테스트 전원 제어 기술** 김영성, 김두영, 정지훈, 김진욱, 박성주 *Department of Computer Science and Engineering, Hanyang University*
WH4-N-7 **16:55-17:10**	**복수의 디코더들을 이용한 X-비트 제거 스캔체인 압축 법** 김새은, 양준성 *성균관대학교 반도체디스플레이공학과*