## F. Silicon and Group-IV Devices and Integration Technology 분과

2017년 2월 15일 (수), 10:10-11:40 Room E (루비, 2층)

## [WE2-F] Advanced CMOS Materials

좌장: 안동환(국민대학교), 전인상(한국알박)

<b>Metal/Al<sub>2</sub>O<sub>3</sub>/GeO<sub>2</sub>/Ge 구조의 열처리에 따른 유효 일함수에 대한 연구</b> Tae In Lee, Yujin Seo, Jungmin Moon, Hyun Jun Ahn, Hyun-Young Yu,
Wan Sik Hwang, and Byung Jin Cho School of Electrical Engineering, KAIST
$V_{TH}$ Modulation of HfO_2-MOSFETs with ALD TiN Using TiCl_4 and NH_3 $$
Younjin Kim <sup>1</sup> , Donghwan Lim <sup>1</sup> , Myeong Gyoon Chae <sup>1</sup> , Dongkyun Kang <sup>2</sup> , Jaesang Lee <sup>2</sup> , Hojin Cho <sup>2</sup> , Sunggon Jin <sup>2</sup> , Euiseong Hwang <sup>2</sup> , and Changhwan Choi <sup>1</sup> <sup>1</sup> Division of Materials Science and Engineering, Hanyang University, <sup>2</sup> SK Hynix Inc.
Metal-Interlayer-Semiconductor Structure Using Al-Doped ZnO for Non-Alloyed Ohmic Contacts on Silicon
Seung-Hwan Kim <sup>1</sup> and Hyun-Yong Yu <sup>1</sup> <sup>1</sup> School of Electrical Engineering, Korea University
An Analysis of Carrier Trapping at Grain Boundary of Polysilicon
Taejin Jang, Myung-Hyun Baek, Hyungjin Kim, and Byung-Gook Park Department of Electrical Engineering, Seoul National University
Study on Material Properties of Tensile-Strained Ge and Sn-Incorporated Ge through First-Principle Simulation for Advanced Si CMOS Technology
Yongbeom Cho <sup>1</sup> and Seongjae Cho <sup>1,2</sup> <sup>1</sup> Graduate School of IT Convergence Engineering, Gachon University, <sup>2</sup> Department of Electronics Engineering, Gachon University
Impact of Equivalent Oxide Thickness on Threshold Voltage Variation Induced by Work-Function Variation in FinFET
Youngtaek Lee, Gihun Choe, Hyunjae Lee, and Changhwan Shin
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