F. Silicon and Group-IV Devices and Integration Technology 분과

2017년 2월 15일 (수), 08:30-10:00 Room E (루비, 2층)

[WE1-F] Advanced CMOS Processing and Reliability

좌장: 신창환(서울시립대학교), 김춘환(SK 하이닉스)

WE1-F-1 08:30-08:45	Improvement of TDDB in 28nm Logic NFET Transistor by the Surface Oxidation of eWF Metal Seung Wook Ryu, Young Tae Yoo, Sung Hun Son, Hun Sung Lee, Tae Yong Park, Seon Haeng Lee, Sang-wan Jin, Moon Sig Joo, Seung Woo Jin, and Choon Hwan Kim SK Hynix Inc.
WE1-F-2 08:45-09:00	Substrate and Layout Engineering to Suppress Self-Heating SangHoon Shin ¹ , SangHyeon Kim ² , Seongkwang Kim ² , Heng Wu ¹ , P. D. Ye ¹ , and M. A. Alam ¹ ¹ Department of ECE, Purdue University, ² Korea Institute of Science and Technology
WE1-F-3 09:00-09:15	The Interaction of Fin Edge Roughness and Side Wall Roughness and Its Impacts on FinFET Sangheon Oh and Changhwan Shin Department of Electrical and Computer Engineering, University of Seoul
WE1-F-4 09:15-09:30	Effect of Process Induced Damage of Porous Low-k SiOCH Films on RVST and TDDB Performance of Logic BEOL Modules Sang-wan Jin, Tae Yeon Jung, Hyo Seok Lee, Hyunah Lee, Chai O Chung, In Cheol Ryu, Seong Wook Ryu, Jung Hyuk Kim, Seung Woo Jin, and Choon Hwan Kim SK Hynix Inc.
WE1-F-5 09:30-09:45	Novel Method to Form Thin Silicon Channel on Bulk Silicon Substrate for Low-Cost Tunnel Field Effect Transistor Fabrication Junil Lee, Dae Woong Kwon, Euyhwan Park, Sihyun Kim, Ryoongbin Lee, Taehyung Park, Hyun-Min Kim, Kitae Lee, and Byung-Gook Park Inter-University Semiconductor Research Center (ISRC), Seoul National University, Department of Electrical and Computer Engineering (ECE), Seoul National University
WE1-F-6 09:45-10:00	Laser Spike Anneal Impact on Bias Temperature Instability for 28nm Replacement Metal Gate CMOS Seon Haeng Lee, Myung Hee Nam, Yu Jun Lee, Seong Jun Lee, Hei Mi Kwon, Sang Eun You, Seung Wook Ryu, Jeong Soo Park, and Joong Smith Jeon SK Hynix Inc.