G. Device & Process Modeling, Simulation and Reliability 분과

2017년 2월 15일 (수), 10:10-11:40
Room C (사파이어, 2층)

[WC2-G] Device Modeling and Simulation 2

좌장: 박찬형(광운대학교), 나현철(동부하이텍)

WC2-G-1 **10:10-10:25**	**New Modeling Method for the Dielectric Relaxation of a DRAM Cell Capacitor** Sujin Choi, Wookyung Sun, and Hyungsoon Shin *Department of Electronic and Electrical Engineering, Ewha Womans University*
WC2-G-2 **10:25-10:40**	**Compact Model for Positive Gain-Embedded Voltage Transfer Curve of Inverter based on Novel I-V Curves for Multi-Peak NDR** Jaewon Jeong, Sunhae Shin, Esan Jang, and Kyung Rok Kim *School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology*
WC2-G-3 **10:40-10:55**	**Tunneling Current Density in Ge/GeO_2/Ge from First-Principles** Eunjung Ko[1], Liu Kai[1,2], and Jung-Hae Choi[1] *[1]Center of Electronic Materials, Korea Institute of Science and Technology, [2]Department of Materials Science and Engineering, Seoul National University*
WC2-G-4 **10:55-11:10**	**Interfacial Properties of Ge (111)/ La_2O_3 by Density Functional Calculations** Liu[1,2], Eunjung Ko[1], Cheol Seong Hwang[2], and Jung-Hae Choi[1] *[1]Center for Electronic Materials, Korea Institute of Science and Technology, [2]Department of Materials Science and Engineering, and Inter-university Semiconductor Research Center, Seoul National University*
WC2-G-5 **11:10-11:25**	**Universal Bias Stress-Induced Instability Model in the Inkjet-Printed Carbon Nanotube Network FETs** Haesun Jung, Sungju Choi, Jun Tae Jang, Bongsik Choi, Jinsu Yoon, Juhee Lee, Yongwoo Lee, Dong Myong Kim, Sung-Jin Choi, and Dae Hwan Kim *School of Electrical Engineering, Kookmin University*