G. Device & Process Modeling, Simulation and Reliability 분과

2017년 2월 15일 (수), 08:30-10:00
Room C (사파이어, 2층)

[WC1-G] Device Physics and Characterization 2

좌장: 김대환(국민대학교), 홍성민(광주과학기술원)

WC1-G-1 **08:30-08:45**	**Performance of Black Phosphorous Tunnel FETs under Uniaxial Strain: First-Principles Study** Sungwoo Jung, Junbeom Seo, and Mincheol Shin *School of Electrical Engineering, KAIST*
WC1-G-2 **08:45-09:00**	**Ab Initio Study on the Atomic and Electronic Structures of MoS_2/oxide Interface** Jaehong Park[1,2], Cheol Seong Hwang[2,3], and Jung-Hae Choi[1] *[1]Center for Electronic Materials, Korea Institute of Science and Technology, [2]Department of Materials Science and Engineering, Seoul National University, [3]Inter-University Semiconductor Research Center, Seoul National University*
WC1-G-3 **09:00-09:15**	**Determination of Bulk and Interface Density of States in a-IGZO TFTs** Chan-Yong Jeong[1], Hee-Joong Kim[1], Jong In Kim[2], Jong-Ho Lee[2], and Hyuck-In Kwon[1] *[1]School of Electrical and Electronics Engineering, Chung-Ang University, [2]School of Electrical Engineering and Computer Science, Seoul National University*
WC1-G-4 **09:15-09:30**	**Giant Electroresistance in Edge Metal-Insulator-Metal Tunnel Junction Induced by Electric Fringe Fields from Underlying Ferroelectric Layer** Sungchul Jung[1], Youngeun Jeon[2], Hanbyul Jin[2], Jung-Yong Lee[1], Jae-Hyun Ko[3], Nam Kim[4], Daejin Eom[4], and Kibog Park[1,2] *[1]Department of Physics, Ulsan National Institute of Science and Technology, [2]School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, [3]Department of Physics, Hallym University, [4]Korea Research Institute of Standar*
WC1-G-5 **09:30-09:45**	**Experimental Investigation of Physical Mechanism for Asymmetrical Degradation and Related Noise Properties in a-IGZO TFTs under Simultaneous Gate and Drain Bias Stresses** Hee-Joong Kim, Chan-Yong Jeong, and Hyuck-in Kwon *School of Electrical and Electronics Engineering, Chung-Ang University*