K. Memory (Design & Process Technology) 분과

2017년 2월 15일 (수), 12:40-14:25
Room B (토파즈, 2층)

[WB3-K] Resistance Switching Memories

좌장: 김수길(SK 하이닉스), 민경식(국민대학교)

WB3-K-1 **12:40-12:55**	**Atomic Layer Deposition of 14-15-16 Group Ternary and Quaternary Thin Films for Ovonic Threshold Switching Selector Device** Sijung Yoo, Taeyong Eom, Taehong Gwon, Sanggyun kim, Euisang Park, Chanyoung Yoo, and Cheol Seong Hwang *Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University*
WB3-K-2 **12:55-13:25**	**[초청]** **Memory Devices based on Self-Assembled Materials and Processes** Jang-Sik Lee *Department of Materials Science and Engineering, Pohang University of Science and Technology*
WB3-K-3 **13:25-13:40**	**A New Concept of Stateful Logic Using CRS//BRS Sub-Circuit** Nuo Xu[1,2], Kyung Min Kim[3], Kyung Jean Yoon[1], Hae Jin Kim[1], Xing Long Shao[1], Xi Wen Hu[1], Liang Fang[2], and Cheol Seong Hwang[1] *[1]Department of Materials Science and Engineering and Inter-University Semiconductor Research Center, Seoul National University, [2]State Key Laboratory of High Performance Computing, National University of Defense Technology, [3]Hewlett-Packard Laboratories,*
WB3-K-4 **13:40-13:55**	**Low Power and Forming-Free Resistive Switching Property of Pt/Al_2O_3/SiN_x/Ti Device** Daeeun Kwon, Jung Ho Yoon, Kyung Jean Yoon, Tae Hyung Park, Hae Jin Kim, Xinglong Shao, Yumin Kim, Young Jae Kwon, and Cheol Seong Hwang *Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University*
WB3-K-5 **13:55-14:10**	**Controllable Non-Reactive TaN Materials as a Promising Resistive Switches Electrode** Tae Yoon Kim[1], Gwang Ho Baek[2], and Jin Pyo Hong[1,2] *[1]Novel Functional Materials and Devices Lab, The Research Institute for Natural Science, Department of Physics, Hanyang University, [2]Division of Nano-Scale Semiconductor Engineering, Hanyang University*
WB3-K-6 **14:10-14:25**	**Improved Controllability of Conductance by Inserting Al_2O_3 in SiN-based Resistive Switching Memory** Sungjun Kim[1], Min-Hwi Kim[1], Hee-Dong Kim[2], Seongjae Cho[3], and Byung-Gook Park[1] *[1]Inter-university Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electrical Engineering, Sejong University, [3]Department of Electronic Engineering, Gachon University*