A. Interconnect & Package 분과

2017년 2월 15일 (수), 10:10-11:40
Room B (토파즈, 2층)

[WB2-A] Process Issues of Interconnect

좌장: 이웅선(SK 하이닉스), 이원준(세종대학교)

WB2-A-1 **10:10-10:25**	**Potential of Tungsten as Next-Generation Semiconductor Interconnects** Dooho Choi *School of Advanced Materials Engineering, Dong-Eui University*
WB2-A-2 **10:25-10:40**	**Effect of None-TMAH Based Chemical as Post-Clean Chemical on Cu CMP** Min Cehol Kang, Hee Jin Kim, Jong Hwa Baek, Young Jun Kim, Kyung Cheol Jung, Choon Hwan Kim, and Joo Young Lee *SK Hynix Inc.*
WB2-A-3 **10:40-10:55**	**개시제를 통한 고분자 기상증착기법을 활용한 다공성 초절연물질 (k = 2.0) 표면 실링 방법** Seong Jun Yoon[1], Kwanyong Pak[2], Taewook Nam[3], Alexander Yoon[4], Hyungjun Kim[3], Sung Gap Im[2], and Byung Jin Cho[1] *[1]Department of Electrical Engineering, KAIST, [2]Department of Chemical and Biomolecular Engineering, KAIST, [3]School of Electrical Engineering, Yonsei University, [4]Lam Research Corporation, Fremont*
WB2-A-4 **10:55-11:10**	**CMP Conditioning 조건 최적화를 통한 Pad Life Time 연장** Hong-joo Lee, Kyung-ho Hwang, Hyung-hwan Kim, and Chang-rock Song *DRAM C&C, Process Center, SK Hynix Inc.*
WB2-A-5 **11:10-11:25**	**Laser Source를 이용한 Wafer 가공 및 분리기술 최적화** 이강원, 민복규, 이중진, 안미래, 김재면 *NAND Package Development, SK Hynix Inc.*
WB2-A-6 **11:25-11:40**	**고 용량 메모리 모듈의 고속동작 특성 개선을 위한 Ci 저감기술 연구** 엄주일, 임상준, 김남석 *IPT Development Project, SK Hynix Inc.*