A. Interconnect & Package 분과

2017년 2월 15일 (수), 08:30-10:00
Room B (토파즈, 2층)

[WB1-A] Packaging and Design

좌장: 이후정(성균관대학교)

WB1-A-1 **08:30-08:45**	**Mechanical Reliability of Sn-Ag-Cu and Sn-Bi BGA Solder Joints with Epoxy During Temperature-Humidity Treatments** Kyung-Yeol Kim[1], Woo-Ram Myung[2], Haksan Jeong[1], and Seung-Boo Jung[1] *[1]School of Advanced Materials Science & Engineering, Sungkyunkwan University, [2]SKKU Advanced Institute of Nanotechnology, Sungkyunkwan University*
WB1-A-2 **08:45-09:00**	**Interposer-Level Wireless Power Transfer Scheme Design on Active Silicon Interposer in 2.5-D and 3-D IC** Jinwook Song, Seungtaek Jung, Shinyoung Park, Subin Kim, and Joungho Kim *Department of Electrical Engineering, KAIST*
WB1-A-3 **09:00-09:15**	**Signal Integrity Design of High Bandwidth Memory Interposer in 2.5D Terabyte/s Bandwidth Graphics Module** Hyunsuk Lee and Joungho Kim *School of Electrical Engineering, KAIST*
WB1-A-4 **09:15-09:30**	**New Verification Method Considering Process Variation in NAND Flash Memory** Young Sang Ahn, Gun Gi Song, Jin Yong Seong, Jae Won Cha, Seung Geon Yu, and Sang Hoo Hong *Nand Product Verification Team, Nand Tech Development Division, SK Hynix Inc.*
WB1-A-5 **09:30-09:45**	**3D Packaging System에서 저온 공정의 필요성 및 절연 박막의 특성 연구** 손성민, 안진호, 정덕영, 진정기, 장근호, 박병률, 이내인, 황기현, 강호규, 정은승 *삼성전자 반도체 연구소*
WB1-A-6 **09:45-10:00**	**Chip Guard Ring 구조 최적화 연구** Min-Soo Park, Jea Hyun Son, Young Geon Kwon, and Nam Seog Kim *SK Hynix Inc.*