F. Silicon and Group-IV Devices and Integration Technology 분과

2017년 2월 14일 (화), 16:00-17:30
Room E (루비, 2층)

[TE3-F] Flash and Si Memory Technologies

좌장: 이종호(서울대학교), 임준희(삼성전자)

TE3-F-1 **16:00-16:15**	**Intercell Trapped Charge (ITC) Suppression of Vertical NAND (VNAND) Flash Memory** Hyug Su Kwon[1], Sangmoo Choi[2], Sung-Yong Chung[2], Gyu-Seog Cho[2], Sung-Kye Park[2], and Woo Young Choi[1] *Department of Electronic Engineering, Sogang University*
TE3-F-2 **16:15-16:30**	**A Boosted Common Source Line Program Scheme in Channel Stacked NAND Flash Memory with Layer Selection by Multilevel Operation** Do-Bin Kim, Dae Woong Kwon, and Byung-Gook Park *Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University*
TE3-F-3 **16:30-16:45**	**Simulation Study of the Dependence of Word-Line Stacked NAND Flash Memory Electrical Characteristics on Grain Boundary Traps** Sang Ho Lee, Dae Woong Kwon, Seung Hyun Kim, Sangku Park, Myung Hyun Baek, and Byung-Gook Park *Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University*
TE3-F-4 **16:45-17:00**	**Compact Modeling of NAND Flash Memory Operation through Accurate Locating the Vertical Position of Trapped Charges** Seunghyun Kim[1], Do-Bin Kim[1], Sang-Ho Lee[1], Sang-Ku Park[1], Youngmin Kim[2], Seongjae Cho[2], and Byung-Gook Park[1] *[1]Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronics Engineering, Gachon University*
TE3-F-5 **17:00-17:15**	**Design and Operation of Capacitorless Si Volatile Memory Based on 2-Terminal Thyristor (2-T TRAM)** Youngmin Kim[1], Seongjae Cho[1], Hyungsoon Shin[2], and Byung-Gook Park[3] *[1]Graduate School of IT Convergence Engineering, Gachon University, [2]Department of Electronics Engineering, Ewha Womans University, [3]Department of Electrical and Computer Engineering, Seoul National University*
TE3-F-6 **17:15-17:30**	**Fabrication and Resistive Switching Characteristics of Silicon Nano-Wedge Structure RRAM** Min-Hwi Kim[1], Sungjun Kim[1], Suhyun Bang[1], Tae-hyeon Kim[1], Dong Keun Lee[1], Seongjae Cho[2], and Byung-Gook Park[1] *[1]Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University, [2]Department of Electronic Engineering, Gachon University*