F. Silicon and Group-IV Devices and Integration Technology 분과

2017년 2월 14일 (화), 10:10-11:40
Room E (루비, 2층)

[TE2-F] Advanced CMOS Devices II

좌장: 양지운(고려대학교), 정성웅(SK 하이닉스)

TE2-F-1 **10:10-10:25**	**Demonstration of CMOS with Gate-Bias Independent Junction Band-to-Band Tunneling Current for Standard Ternary Inverter** Sunhae Shin, Esan Jang, Jae Won Jeong, and Kyung Rok Kim *School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology*
TE2-F-2 **10:25-10:40**	**Switching Voltage Modeling of Nano-Electromechanical (NEM) Memory Switches** Ho Moon Lee and Woo Young Choi *Department of Electronic Engineering, Sogang University*
TE2-F-3 **10:40-10:55**	**Influence of Temperature and Doping Concentration on the Energy Filtering Effects of Tunnel Field-Effect Transistors** In Huh and Woo Young Choi *Department of Electronic Engineering, Sogang University*
TE2-F-4 **10:55-11:10**	**Optimal Design of Si Dual-Gate Junctionless Tunneling Field-Effect Transistor** Junsoo Lee[1] and Seongjae Cho[1,2] *[1]Graduate School of IT Convergence Engineering, [2]Department of Electronics Engineering Gachon University*
TE2-F-5 **11:10-11:25**	**Resistive Switching Characteristics of a Ni/WO_x/p^+-Si RRAM by Pulse Analysis** Tae-Hyeon Kim, Sungjun Kim, Min-Hwi Kim, Su-Hyun Bang, Dong Keun Lee, and Byung-Gook Park *Inter-University Semiconductor Research Center (ISRC) and the Department of Electrical and Computer Engineering, Seoul National University*
TE2-F-6 **11:25-11:40**	**Current-Voltage Characterization of Ultra-Thin Floating-Body MOSFETs** Eunseon Yu[1], Seongjae Cho[1,2], and Byung-Gook Park[3] *[1]Graduate School of IT Convergence Engineering, Gachon University, [1]Graduate School of IT Convergence Engineering, [2]Department of Electronics Engineering, Gachon University, [3]Department of Electrical and Computer Engineering, Seoul National University*