F. Silicon and Group-IV Devices and Integration Technology 분과

2017년 2월 14일 (화), 08:30-10:00
Room E (루비, 2층)

[TE1-F] Advanced CMOS Devices I

좌장: 김소영(성균관대학교), 이내인(삼성전자)

TE1-F-1 **08:30-08:45**	**Super Steep Switching FinFET Technology for Ultra-Low Power Operation** Eunah Ko and Changhwan Shin *Department of Electrical and Computer Engineering, University of Seoul*
TE1-F-2 **08:45-09:00**	**Approach for Advancement of Transistor: Vertically Integrated Gate-All-Around Junctionless Nanowire FET** Byung-Hyun Lee and Yang-Kyu Choi *School of Electrical Engineering, KAIST*
TE1-F-3 **09:00-09:15**	**Hump Effects of Triple-Gate Tunnel FETs Encapsulated with an Epitaxial Layer (EL TFETs)** Jang Woo Lee and Woo Young Choi *[1]Department of Electronic Engineering, Sogang University, [2]Flash Device Technology Team, SK Hynix Inc.*
TE1-F-4 **09:15-09:30**	**Fully Formed, Releasable Single-Crystal Silicon-Metal Oxide Field Effect Transistors based on (100) Silicon Bulk Wafer** Kyu-Bong Choi, Byung-Gook Park, and Jong-Ho Lee *Department of ECE and ISRC, Seoul National University*
TE1-F-5 **09:30-09:45**	**Vertical Gate-All-Around Transistor with Wrapped Contact and Vertically-Stacked Dual Metal Gate for High Current Memory Applications** Dongyean Oh, Junkyo Suh, Kangsik Choi, Sangyong Kim, Seong-Dong Kim, Seokkiu Lee, and Sungjoo Hong *R&D Division, SK Hynix Inc.*
TE1-F-6 **09:45-10:00**	**Improved Characteristics and V_{TH} Modulation of FD-SOI Tunnel Field Effect Transistor (TFET) Using ALD $HfAlO_x$ and TiN Gate Stack** Donghwan Lim, Jae Ho Lee, Myeong Gyoon Chae, Hoon Hee Han, Yu-Rim Jeon, Andrey Sokolov Sergeevich, and Changhwan Choi *Division of Materials Science and Engineering, Hanyang University*