S. Chip Design Contest 분과

2017년 2월 14일 (화), 08:30-10:00
Room D (크리스탈, 2층)

[TD1-S] Chip Design Contest

좌장: 김태욱(연세대학교), 심재윤(포항공과대학교)

TD1-S-1 **08:30-08:45**	**A Process Compensating Analog PIE Decoder for EPC Gen2 UHF RFID Tag IC** Jae-Hun Lee, Dasom Park, Hyun-Sik Lee, Woo-Jin Jo, and Jong-Wook Lee *Department of Electronics and Radio Engineering, Kyung Hee University*
TD1-S-2 **08:45-09:00**	**300 GHz 7×7 배열 CMOS 이미지 검출기** 송기룡, 김정수, 서명교, 이재성 *고려대학교 전기전자공학과*
TD1-S-3 **09:00-09:15**	**10Gbps Serial-link Transmitter for 10G-EPON** Dong-Hyun Yoon, Yo Han Hong, Dong-Gyu Jung, Ngoc-Son Pham, and Kwang-Hyun Baek *School of Electrical and Electronics Engineering, Chung-Ang University*
TD1-S-4 **09:15-09:30**	**A Single-Ended 6T1D SRAM Cell With Feedback-fade Write Access** Kyungho Shin and Jongsun Park *School of Electrical Engineering, Korea University*
TD1-S-5 **09:30-09:45**	**1GHz에서 동작하는 고성능 EISC 프로세서 설계** 김창현, 전재영, 김인식, 민경일, 김선욱 *고려대학교 전기전자공학과*
TD1-S-6 **09:45-10:00**	**A Mixed-Signal ASIC Chip Design for Peripheral Neural Stimulation for Miniaturized Implantable Devices** Jungmin Seo, Jeong-Hoan Park, and Sung June Kim *Department of Electrical and Computer Engineering, Seoul National University*