

G. Device & Process Modeling, Simulation and Reliability **분과**

2017년 2월 14일 (화), 16:00-17:30
Room C (사파이어, 2층)

[TC3-G] Device Modeling and Simulation 1

좌장: 김대환(국민대학교), 최성진(국민대학교)

TC3-G-1 16:00-16:15	Surface Potential Model for L-shaped Tunnel Field-Effect-Transistor Faraz Najam and Yun Seop Yu <i>Department of Electrical, Electronic and Control Engineering and ITC, Hankyong National University</i>
TC3-G-2 16:15-16:30	Density-Functional Theory Based Simulation of Biaxial Strained Silicon Ultra-Thin-Body FETs Seonghyun Heo, Hyo-Eun Jung, and Mincheol Shin <i>Department of Electrical Engineering, KAIST</i>
TC3-G-3 16:30-16:45	TCAD-based Analysis on the Relationship between the Physical Parameters in charge Trapping and the Stretched Exponential Model Parameters in Amorphous InGaZnO TFTs under the Positive Gate Bias Temperature Stress Jihyun Rhee, Sungju Choi, Hara Kang, Jae-Young Kim, Jun Tae Jang, Daehyun Ko, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i>
TC3-G-4 16:45-17:00	Simulation Study on Drain Current Characteristics in Linear and Saturation Region of Tunnel Field Effect Transistor (TFET) Ryoongbin Lee, Dae Woong Kwon, Euyhwan Park, Junil Lee, Sihyun Kim, and Byung-Gook Park <i>Department of Electrical and Computer Engineering, Seoul National University</i>
TC3-G-5 17:00-17:15	A Development of New CDM SPICE Simulation Model Jung-woo Han, Young-chul Kim, Young-sang Son, Joong-hyeok Byeon, Joon-tae Jan, Geun-tae Kwon, and Yoon-jong Lee <i>TE team, Dongbu HiTecks Co., Ltd.</i>
TC3-G-6 17:15-17:30	TCAD-based Comparative Study on the Positive Bias Stress Instability between the Single-Gate and Double-Gate Structured In-Ga-Zn-O TFTs Sungju Choi, Jun Tae Jang, Hara Kang, Jae-Young Kim, Daehyun Ko, Jihyun Rhee, Jun Tae Jang, Hye Ri Yu, Jisun Park, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim <i>School of Electrical Engineering, Kookmin University</i>