G. Device & Process Modeling, Simulation and Reliability 분과

2017년 2월 14일 (화), 10:10-11:40
Room C (사파이어, 2층)

[TC2-G] Reliability Analysis

좌장: 김성동(SK 하이닉스), 유현용(고려대학교)

TC2-G-1 **10:10-10:25**	**3차원 시뮬레이션을 이용한 Gate-All-Around Nanowire FET의 PVE(Process Variation Effect)에 의한 GIDL분석** 김신근[1], 서영수[1], 강명곤[2], 신형철[1] *[1]School of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Electronics Engineering, Korea National University of Transportation*
TC2-G-2 **10:25-10:40**	**Mitigation of Grain Boundary Effect in 3D Vertical NAND Flash with Macaroni Structure** Hyeongwan Oh[1], Jiwon Kim[1], Seabyuk Jeong[2], Taehee Kim[1], Hojoon Lee[1], Junyoung Lee[1], Wonyeong Choi[1], and Jeong-Soo Lee[1] *[1]Department of Electrical Engineering, Pohang University of Science and Technology, [2]Division of IT Convergence Engineering, Pohang University of Science and Technology*
TC2-G-3 **10:40-10:55**	**Low Leakage III-V/Ge CMOS FinFET Design with High-K Spacer Technology** E-San Jang, Sunhae Shin, Jae Won Jung, and Kyung Rok Kim *Department of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology*
TC2-G-4 **10:55-11:10**	**ESD Damage Caused by Non-Uniform Metal Resistance in Big Switch** Youngchul Kim, Jungwoo Han, Jowoon Lee, Youngsang Son, Joonghyeok Byeon, Joontae Jang, Geuntae Kwon, and Yoonjong Lee *TE team, Dongbu HiTecks Co., Ltd.*
TC2-G-5 **11:10-11:25**	**Field-Effect-Passivation for Backside Illuminated CMOS Sensor by High K Material** Jin-woo Sung *Department of Process integration, SK Hynix Inc.*