## N. VLSI CAD 분과

**Room I**
**육백II(6층)**

**2016년 2월 24일(수) 08:30-10:00**
**[WI1-N] Architecture-Level Design Techniques**
**좌장 : 이종은(UNIST), 정재용(인천대학교)**

**WI1-N-1** **08:30-08:45** **Power-Optimized Design of N:1 Serializer in 65-nm CMOS**
Tongsung Kim and Woo-Young Choi
*Department of Electrical and Electronic Engineering, Yonsei University*

**WI1-N-2** **08:45-09:00** **CAM Structure of Built-in Redundancy Analysis Hardware**
Jooyoung Kim, Keewon Cho, Woosung Lee, Soyeon Kang, and Sungho Kang
*Department of Electrical and Electronic Engineering, Yonsei University*

**WI1-N-3** **09:00-09:15** **Cascaded Propagation Technique for Fault Binary Decision Diagram in Single-Event Transient Analysis**
Jong Kang Park, Myoungha Kim, and Jong Tae Kim
*School of Electronic and Electrical Engineering, Sungkyunkwan University*

**WI1-N-4** **09:15-09:30** **The Techniques for Exploiting The Plane-level Parallelism in NAND Flash Based Storage Device**
Wontaeck Jung[1,2] and Eui-Young Chung[1]
*[1]School of Electrical and Electronic Engineering, Yonsei University, [2]Samsung Electronics Co., Ltd.*

**WI1-N-5** **09:30-09:45** **Exploring Synchronous/Asynchronous Communication and Computation for Mapping Streaming Applications onto CGRA-based System**
Hongsik Lee, Sangyun Oh, and Jongeun Lee
*Department of Computer Science Ulsan National Institute of Science and Technology*

**WI1-N-6** **09:45-10:00** **Toward Neuromorphic Execution of Deep Learning Models**
Taehwan Shin, Yongshin Kang, Seungho Yang, Seban Kim, and Jaeyong Chung
*Department of Electronic Engineering, Incheon National University*