

# 제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

## G. Device & Process Modeling, Simulation and Reliability 분과

Room D

함백II+III(5층)

2016년 2월 24일(수) 08:30-10:00

[WD1-G] Device Physics and Characterization 2 : Memory Devices

좌장 : 이석규(SK 하이닉스), 이재규(삼성전자)

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| WD1-G-1 | 08:30-08:45 | <b>Data Retention of Select Gate Lateral Coupling eNVM Array</b><br>Yong-Seop Lee, Kwang-Il Choi, Do-Hee Kim, Nam-Yoon Kim, and Sung-Kun Park<br><i>System IC Platform Technology Development Team, SK hynix Inc.</i>                                                                                                                                                                                                                                                                            |
| WD1-G-2 | 08:45-09:00 | <b>Charge Trapping Characteristics of FG NAND Flash Tunneling Oxide under Program and Erase Operation</b><br>Sangu Park <sup>1,2</sup> , Myung-Hyun Baek <sup>1</sup> , and Byung-Gook Park <sup>1</sup><br><sup>1</sup> <i>Inter-university Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University,</i><br><sup>2</sup> <i>Samsung Electronics Co., Ltd.</i>                                                                            |
| WD1-G-3 | 09:00-09:15 | <b>Effect of Trap in Hysteresis Phenomenon of Floating-Gate NAND Flash Memory Cells</b><br>Nagyong Choi <sup>1</sup> , Ho-Jung Kang <sup>1</sup> , Sung-Min Joe <sup>2</sup> , Byung-Gook Park <sup>1</sup> , and Jong-Ho Lee <sup>1</sup><br><sup>1</sup> <i>Department of Electrical Engineering and Computer Science and Inter-University Semiconductor Research Center, Seoul National University,</i> <sup>2</sup> <i>Flash Design Team, Memory Division, Samsung Electronics Co., Ltd.</i> |
| WD1-G-4 | 09:15-09:30 | <b>An Analysis of AC-gm Dispersions due to Traps in Nitride Storage Layer in 3-D NAND Flash Memory</b><br>Ho-Jung Kang, Nagyong Choi, Byung-Gook Park, and Jong-Ho Lee<br><i>Department of Electrical Engineering and Computer Science and Inter-University Semiconductor Research Center, Seoul National University</i>                                                                                                                                                                         |
| WD1-G-5 | 09:30-09:45 | <b>Nanowire Width-Dependent Low-Frequency Noise Characteristics in SiNW-Based GAA JL Flash Memory with Extremely Small Dimension</b><br>Tewook Bang <sup>1</sup> , Ui-Sik Jeong <sup>2</sup> , Choong-Ki Kim <sup>1</sup> , Hagyoul Bae <sup>1</sup> , Gun-Hee Kim <sup>1</sup> , Da-Jin Kim <sup>1</sup> , and Yang-Kyu Choi <sup>1</sup><br><sup>1</sup> <i>School of Electrical Engineering, KAIST,</i> <sup>2</sup> <i>Samsung Electronics Co., Ltd.</i>                                     |
| WD1-G-6 | 09:45-10:00 | <b>Verilog-A Model of Phase Change Memory for Cell Distribution</b><br>Sung-Su Kim, Hye-Jung Choi, Dong-Jae Lee, and Seok-Kiu Lee<br><i>DMR. Research and Development Division, SK hynix Inc.</i>                                                                                                                                                                                                                                                                                                |