제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

D. Thin Film Process Technology 분과

Room B 태백**피**+피(5층)

2016년 2월 24일(수) 10:10-11:40

[WB2-D] Thin Films for Emerging Devices II

좌장: 전상훈(고려대학교), 최창환(한양대학교)

11:25-11:40

WB2-D-6

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| WB2-D-1 | 10:10-10:25 | Low-Temperature P-Type Poly-Ge Thin-Film Transistor Fabricated by Metal-Induced Lateral Crystallization for High Hole Mobility Jae Hyo Park ¹ , Yoonyoung Bae ² , Seung Ki Joo ¹ , and Donghwan Ahn ² ¹ Department of Material Science and Engineering, Research Institute of Advanced Materials, Seoul National University, ² Department of Advanced Materials Engineering, Kookmin University |
| WB2-D-2 | 10:25-10:40 | Wearable Transparent Oxide Thin-Film Transistor Via Inorganic-Based Laser Lift-Off Han Eol Lee and Keon Jae Lee Department of Materials Science and Engineering, KAIST |
| WB2-D-3 | 10:40-10:55 | Atomic Layer Deposition of GeTe and GexSbyTez Alloys Using Ge(N((CH ₃) ₃ Si) ₂) ₂ Precursor Taehong Gwon ¹ , Taeyong Eom ¹ , Sijung Yoo ¹ , Eui-sang Park ¹ , Sanggyun Kim ¹ , Moo-sung Kim ² , Iain Buchanan ³ , Manchao Xiao ³ , Sergei Ivanov ³ , and Cheol Seong Hwang ¹ ¹ Department of Materials Science and Engineering and Inter- University Semiconductor Research Center, ² Air Products Korea, ³ Air Products and Chemicals, Inc. |
| WB2-D-4 | 10:55-11:10 | Decreasing Interfacial Layers of The Ferroelectric Hf _{0.5} Zr _{0.5} O ₂ Film Capacitors by Wake-Up Effect Han Joon Kim, Min Hyuk Park, Yu Jin Kim, Taehwan Moon, Keum Do Kim, Young Hwan Lee, Seung Dam Hyun, and Cheol Seong Hwang Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University |
| WB2-D-5 | 11:10-11:25 | Transparent Poly-Si Gate Thin-Film Transistors by NiSi ₂ Seed-Induced Lateral Crystallization for Display Applications. Ji Su Han, Jae Hyo Park, Hyung Yoon Kim, Ki Hwan Seok, Zohreh Kiaee, and Seung Ki Joo Department of Material Science and Engineering, Research Institute |

of Advanced Materials, Seoul National University

A New Method To Form NiGeSn Layer To Reduce Contact

Resistance in Source/Drain Region for Future Ge CMOSFET Jeyoung Kim¹, Meng Li¹, Jungwoo Oh², and Hi-Deok Lee¹ ¹Department of Electronics Engineering, Chungnam National University, ²School of Integrated Technology, Yonsei University