The 23rd Korean Conference on Semiconductors (KCS 2016)

제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

K. Memory (Design & Process Technology) 분과

Room J 청옥 I (6층)

2016년 2월 23일(화) 08:30-10:30

[TJ1-K] Memory Processing and RRAM Operation

좌장 : 김수길(SK 하이닉스), 백승재(한경대학교)

| ТЈ1-К-1 | 08:30-08:45 | Reliability of Hour-Glass Shaped Filament in a Cu-based Al2O3/WO3 Conductive Bridge RAM System Jiyong Woo and Hyunsang Hwang Department of Materials Science and Engineering, Pohang University of Science and Technology |
|---------|-------------|---|
| ТЈ1-К-2 | 08:45-09:15 | [초청] ALD Technologies and Applications in Memory Device Fabrication Han-Jin Lim, Seok-Woo Nam, Siyoung Choi, and Ho-Kyu Kang Semiconductor R&D Center, Samsung Electronics Co. Ltd. |
| TJ1-K-3 | 09:15-09:30 | Suppression of the Reset Breakdown Failure by using RuO ₂ Electrode in HfOx-based RRAM Jaesung Park, Jiyong Woo, Amit Prakash, Kibong Moon, Changhyuck Sung, and Hyunsang Hwang Department of Materials and Science Engineering, Pohang University of Science and Technology |
| TJ1-K-4 | 09:30-09:45 | Effects of N-GST Buffer Layer on Switching Characteristics of CBRAM Seokjae Lim, Sangheon Lee, Jiyong Woo, and Hyungsang Hwang Department of Materials and Science Engineering, Pohang University of Science and Technology |
| TJ1-K-5 | 09:45-10:00 | Exploring Non-polar and Bipolar Resistance Switching Mechanisms from TiN/TiO₂/Al Memory Xing Long Shao ¹ , Kyung Min Kim ² , Kyung Jean Yoon ¹ , Seul Ji Song ¹ , Jung Ho Yoon ¹ , Tae Hyung Park ¹ , Dae Eun Kwon ¹ , Young Jae Kwon ¹ , Hye Jin Kim ¹ , and Cheol Seong Hwang ¹ ¹ Korea ¹ Department of Materials Science and Engineering and Inter- university Semiconductor Research Center, Seoul National University, ² Hewlett-Packard Laboratories, Hewlett-Packard Company Palo Alto, |
| TJ1-K-6 | 10:00-10:15 | <i>USA</i> Enhancement of Switching and Endurance Characteristics of ReRAM by Control of Forming Conditions 이재연, 하태정, 박우영, 김경완, 박용택, 배윤철, 김종일, 김수길 <i>NM 공정개발그룹, R&D 부문, SK hynix Inc.</i> |
| ТЈ1-К-7 | 10:15-10:30 | Effects of Gate Bias on Reset Failure in HfO ₂ based 1T1R ReRAM Cell |

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