## N. VLSI CAD 분과

**Room I**
**육백II(6층)**

**2016년 2월 23일(화) 15:10-17:10**
**[TI1-N] Advances in Design Technology**
**좌장 : 이종은(UNIST), 김영민(광운대학교)**

**TI1-N-1** **15:10-15:25** **Power Grid and Bump Optimization for Minimizing IR Drop in an Early Design Stage**
Minjee Lee, Yongchan Ban, Changseok Choi, Kyeongmin Kim, Yongseok Kang, and Woohyun Paik
*System IC R&D Center, LG Electronics Inc.*

**TI1-N-2** **15:25-15:40** **Framework of Scan Mode IR-Drop Simulation with Accuracy**
Kyeongmin Kim, Yongchan Ban, Minjee Lee, Changseok Choi, Yongseok Kang, and Woohyun Paik
*System IC R&D Center, LG Electronics Inc.*

**TI1-N-3** **15:40-15:55** **Automatic Placement for Directed Self-Assembly Lithography**
정우현, 심성보, 신영수
*KAIST 전기및전자공학부*

**TI1-N-4** **15:55-16:10** **Optimizing the Number of Routing Tracks for Timing Closure and Circuit Area**
Inhak Han and Youngsoo Shin
*School of Electrical Engineering, KAIST*

**TI1-N-5** **16:10-16:25** **Optimizing Timing Margin for Timing Closure, Area, and Power**
Inhak Han, Jinwook Jung, and Youngsoo Shin
*School of Electrical Engineering, KAIST*

**TI1-N-6** **16:25-16:40** **Pin Congestion-aware Legalization for Area Efficiency**
Taeil Kim, Sungmin-Bae, Hyung-Ock Kim, Jung Yun Choi, Sungho Park
*Samsung Electronics Co., Ltd.*

**TI1-N-7** **16:40-16:55** **Path Ordering for Delay Testing under Process Variation**
Heetae Kim, Jaeil Lim, Inhyuk Choi, Hyunggoy Oh, and Sungho Kang
*Department of Electrical and Electronic Engineering, Yonsei University*