제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

F. Silicon and Group-IV Devices and Integration Technology 분과

Room G

봉래표+표(6층)

2016년 2월 23일(화) 15:10-17:10

[TG3-F] Novel Si Devices and Integrated Circuits (3)

좌장: 전인상(Ulvac Korea), 최우영(서강대학교)

TG3-F-1	15:10-15:25	Integrate-and-Fire(I&F) Neuron Circuit using Resistive-switching Random Access Memory(RRAM) Min-Woo Kwon, Sungjun Kim, Min-Hwi Kim, Jungjin Park, Hyungjin Kim, and Byung-Gook Park Inter-university Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University
TG3-F-2	15:25-15:40	Effects of Pocket Doping Concentration on 1T DRAM based on Pillar Type Tunneling Field-effect Transistor with Surrounding Gate Structure Hyungjin Kim and Byung-Gook Park Department of Electrical and Computer Engineering and Interuniversity Semiconductor Research Center, Seoul National University
TG3-F-3	15:40-15:55	Hole Trapping Phenomenon at Grain Boundary of 3D NAND Flash Memory Myung-Hyun Baek, Sang-Ho Lee, Dae Woong Kwon, Joo Yun Seo, and Byung-Gook Park Department of Electrical and Computer Engineering, Seoul National University
TG3-F-4	15:55-16:10	Resistive Switching Characteristics of RRAM with WO _x Switching Layer Prepared by Rapid Thermal Oxidation Tae-Hyeon Kim, Hyungjin Kim, Sungjun Kim, Suhyun Bang, and Byung-Gook Park Inter-university Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University
TG3-F-5	16:10-16:25	Synaptic Device based on Memristor using Cu/ITO/Si Structure Suhyun Bang, Sungjun Kim, Hyungjin Kim, Tae-Hyeon Kim, and Byung-Gook Park Inter-university Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University
TG3-F-6	16:25-16:40	Highly Accurate Circuit-level Macro Modeling of Charge-trap Flash Memory Seunghyun Kim ¹ , Min-Hwi Kim ¹ , Sang-Ho Lee ¹ , Youngmin Kim ² , Hyung-Min Kim ³ , Young Goan Kim ³ , Seongjae Cho ² , and Byung-Gook Park ¹ **Department of Electrical and Computer Engineering, Seoul National**

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University, ²Department of Electronic Engineering, Gachon University, ³Novachips

TG3-F-7 16:40-16:55 DC and Pulse Switching Characteristics of Fully Si Processing-Compatible SiN-based RRAM

Min-Hwi Kim¹, Sungjun Kim¹, Sunghun Jung¹, Seongjae Cho², and Byung-Gook Park¹

¹Inter-university Semiconductor Research Center and Department of Electrical and Computer Engineering, Seoul National University, ²Department of Electronic Engineering, Gachon University

TG3-F-8 16:55-17:10 Thyristor Technology for Ultra-sharp-switching Logic and Capacitorless Dynamic Random-access Memory (DRAM) Applications

Seongjae Cho^{1,2}

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