제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

F. Silicon and Group-IV Devices and Integration Technology 분과

Room G

봉래표+Ⅲ(6층)

2016년 2월 23일(화) 08:30-10:30

[TG1-F] Novel Si Devices and Integrated Circuits (1)

좌장: 이내인(삼성전자), 이종호(서울대학교)

TG1-F-1	08:30-09:00	[초청] Novel Circuit Design Methodology by using of Multi-Gate Transistors Youngmin Kim Department of Computer Engineering, Kwangwoon University
TG1-F-2	09:00-09:15	Improved Hetero-Gate-Dielectric Tunnel Field-Effect Transistors Woo Young Cheon, Jangwoo Lee, and Woo Young Choi Department of Electronic Engineering, Sogang University
TG1-F-3	09:15-09:30	Hysteresis-Free Negative Capacitance Field Effect Transistor with Sub-kT/q(ln10) Switching Hyunseo Park, Jaesung Jo, Kihun Choi, Seunghoon Han, Sungjin Lee, and Changwhan Shin School of Electrical and Computer Engineering, University of Seoul
TG1-F-4	09:30-09:45	Optimal Design of 10-nm Junctionless Field-effect Transistor with Poly-Si Channel in Consideration of Quantum-mechanical Drift-diffusion Models Junsoo Lee, Youngmin Kim, and Seongjae Cho Department of Electronic Engineering, Gachon University
TG1-F-5	09:45-10:00	Bias-Dependent On-Current Modeling of Ultra Short-Channel PMOSFETs with Hot-Carrier Stress Effects In Eui Lim ¹ , Heesauk Jhon ¹ , Gyuhan Yoon ¹ , Byung Kil Choi ² , Heung Sik Park ² , Seok Kiu Lee ² , and Woo Young Choi ¹ ¹ Department of Electronic Engineering, Sogang University, ² R&D Division DMR Team, SK hynix Inc.
TG1-F-6	10:00-10:15	Nanowire PMOSFET Having Si Core and Ultra-thin Ge Peripheral Channel Eunseon Yu ¹ , Mina Yun ¹ , and Seongjae Cho ^{1,2} ¹ Department of Electronic Engineering, Gachon University, ² Graduate School of IT Convergence Engineering, Gachon University
TG1-F-7	10:15-10:30	Experimental Demonstration of Sub-60-mV/decade Steep Switching FinFET using Negative Capacitance Effects Jaesung Jo and Changwhan Shin School of Electrical and Computer Engineering, University of Seoul