

제23회 한국반도체학술대회

2016년 2월 22일(월)-24일(수), 강원도 하이원리조트

Q. Metrology, Inspection, and Yield Enhancement 분과

Room F
봉래 I (6층)

2016년 2월 23일(화) 15:10-17:10

[TF3-Q] Metrology and Inspection I

좌장 : 박병천(한국표준과학연구원), 유형원(SK 하이닉스)

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| TF3-Q-1 | 15:10-15:25 | 요소 트리를 이용한 반도체 SEM 영상의 결함 자동 검출
김성현 ¹ , 김민우 ² , 오일석 ^{1,2}
<i>¹전북대학교 나노과학기술학과, ²전북대학교 컴퓨터공학과</i> |
| TF3-Q-2 | 15:25-15:40 | Methodology of Stress Measurement in Copper and Silicon around Through-Silicon via using Nanoindentation and Micro Raman Spectroscopy for 3D IC Interconnects
Jaehyun Kim ^{1,2} , Changhwan Lee ¹ , Hyungwon Yoo ¹ , Yeojin Yoon ¹ , Jinsan Yoo ¹ , and Seungmin Han ²
<i>¹SK hynix Inc., ²KAIST</i> |
| TF3-Q-3 | 15:40-15:55 | Identifying the Systematic Failure Mechanism using Volume Diagnostics Methodology
Jeongsu Park ¹ , Joochan Kim ² , Sunghun Kim ² , and Sunggun Kang ²
<i>¹Yield and Failure Analysis, Synopsys, Inc., ²Process Architecture Team, System LSI, Samsung Electronics Co., Ltd.</i> |
| TF3-Q-4 | 15:55-16:10 | Methodology Study for Real Cell Overlap Control Under sub-1_x-nm Device Era
Jun-Beom Park, Hong-Boo Lee, Sang-Jun Han, Young-Sik Kim, and Noh-Jung Kwak
<i>R&D Division, SK hynix Inc.</i> |
| TF3-Q-5 | 16:10-16:25 | Study on the Interferometric Measurements of Wafer Warpage for Correction of Overlay Error
Seung-Il Lim ^{1,2,3} , Jae-Jun Choi ^{1,2,3} , Sung-Min Yoon ^{1,2,3} , Woo Sung Jung ^{1,2,3} , Seung Chul Oh ^{1,2,3} , Jae Yong Lee ^{1,2,3} , and Jaison Kim ^{1,2,3}
<i>¹Department of Physics, Myong-ji University, ²AUROS Technology, ³KRISS</i> |
| TF3-Q-6 | 16:25-16:40 | Reliability Analysis of Protective Anodizing Film for Contamination Free Manufacturing under Etching
Je-Boem Song ^{1,2} , Jin-Tae Kim ¹ , Seung-Su Lee ¹ , SinHo Choi ¹ , Seong-Geun Oh ² , and Ju-Young Yun ¹
<i>¹Vacuum Center, Korea Research Institute of Standards and Science, ²Department of Chemical Engineering, Hanyang University</i> |