Nonvolatile Memory Technology beyond 20 nm: Dilemma and Challenge

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For a last decade, mobile devices such as cellular phone, tablet, and note book etc. have driven the memory technology to be a higher integration density, a lower power consumption, and a faster speed, which has been deployed by scaling-down conventional DRAM and NAND flash memory. Currently, DRAM has been scaled down up to 18-nm technology node by using novel process integration technologies such as smaller memory-cell feature-size design, 3dimensional transistor, higher capacitance material design, and smaller bit-to-bit parasitic capacitor design etc..[1] However, the speed of the DRAM scaling-down has become slower, which would meet a physical scaling-down limit with several years. In addition, currently, NAND flash memory has been scaled down up to 14-nm technology node by changing planar memory-cell integration to 3 dimensional memory-cell integration, which would meet a physical scaling-down limit when the floor number of the vertically stacked memory-cells reaches more than 128 floors.[2] For a coming decade, mobile devices as well as data cloud, big data, and Internet-of-Thinks would drive strongly the memory technologies to be scaled down close to a physical scaling-down limit of current DRAM and NAND flash memory. As a solution of a physical scaling-down limit, for a last decade, nonvolatile memories such as PCM (phase change memory), ReRAM (resistive random-access memory),and p-STTMRAM (perpendicularspin-transfer-torquemagneticrandom-access-memory), called emerging memories, have been intensively researched. Current technology level of these nonvolatile memories could not replace current DRAM and NAND flash memory because of relative high bit-cost, low integration density, and pre-mature reliability. However, recently, Storage Class Memory (SCM), has been proposed as a new challenging business for nonvolatile emerging memories.[3] Two types of SCM has been proposed; the memory mapped SCM (memory performance between DRAM and the storage mapped SCM) and the storage mapped SCM (memory performance between the memory mapped SCM and SSD). The mapped SCM is preferring to p-STT MRAM while the storage mapped SCM is preferring to PCM and ReRAM. First of all, as a storage mapped SCM, PCM has used chalcogenide materials (i.e., Ge doped SbTe etc.) as restive change material via phase transforming, but it has several potential issues such as Resistance-drift during set/reset endurance cycles (called stuck failure) and scaling-down limit of the current driving transistor since the set and reset process require relatively high current, which would be challenging issue

to move a real storage mapped SCM market. Second, as a storage mapped SCM, two types of ReRAM, binary oxide based ReRAM and CBRAM (conductive bridge random access memory) using solid electrolyte, have been intensively studied. ReRAM also has presented several potential issues such as small set/reset margin, large high-resistance-state distribution, and short set/reset endurance cycles. CBRAM also has ReRAM also has showed several potential issues such as small large high-resistance-state distribution and short set/reset endurance cycles. These potential issues for ReRAM and CBRAM would be solves for entering a real storage mapped SCM market.Dislike 3D NAND flash memory, since PCM and ReRAM could not achieve the MLC (multi-level-cell) operation, they need to be designed by 3 dimensional cross-bar memory-cell integration. Because of severe sneak current during set/reset programming and data reading, a cross-bar memory cell should contain a vertically stacked selector. Several selectors have been proposed: AsTeGeSiNthreshold switch1[4], Mixed Ionic Electronic Conduction (MIEC)[5], Field Assisted Super-linear Threshold (FAST)[6], self-selecting ReRAM[7], oxide pnp selector[8], which need further to research the high density integration of PCM or ReRAM including selectors. Otherwise, as a memory mapped SCM, p-STT MRAM has been widely researched, which essentially need to achieve a high tunneling-magneto-resistance (TMR) ratio (> 150%) , thermal stability (Δ) (>74), and switching current (J_c) (~$1x10^2$ MA/cm^2) at the back end of line (BEOL) temperature of 400 ^oC. As a solution, recently, a p-STT MRAM cell fabricated with double MgO based p-MTJ spin-valve with a top free CoFeB layer has been intensively researched, which would be challenging issue to move a real memory mapped SCM market.

References

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