Future Memory Technology
with Vertical MOSFET and STT-MRAM for Ultra Low Power Systems

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Recently in semiconductor memories, it is becoming difficult to meet the target performance requirements by technology development based solely on device scaling. Firstly, the speed gap between each memory levels in addition to the speed gap between the operation speed of logic and that of memory have expanded year by year. Moreover, the power consumption due to the increase in memory capacity and increased operation speed is rapidly increasing.

In this invited talk, the directionality of the revolution of the semiconductor memory hierarchy structure in the future from the background mentioned above is discussed. The realization of this revolution in the memory layers with Vertical MOSFET and STT-MRAM, which solve both the issues of cell density, speed gap and power consumption simultaneously, is introduced. In addition, from the viewpoint of future high-end memory system, the impact of hybrid memory technology with 3D structured device technology and spin devices technology is discussed. Finally, nonvolatile logic as one of application technology of leading edge memory technology is shown.

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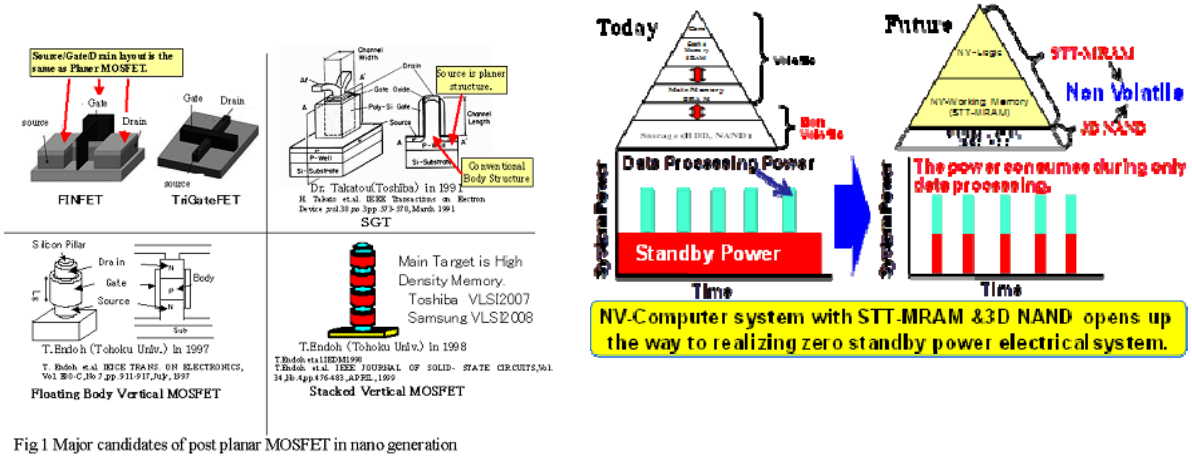

Fig 1 Major candidates of post planar MOSFET in nano generation

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