N. VLSI CAD 분과

Room D
1F / 107호

2015년 2월 11일(수) 13:00-14:30
[WD2-N] System Level Design & Test
좌장: 정재용 (인천대학교), 김윤진 (숙명여대)

WD2-N-1	**13:00-13:30**	**Managing Power Consumption and Clock Skew using Mesh Clock Network with Multiple Subtrees** Jinwook Jung and Youngsoo Shin Department of Electrical Engineering, KAIST
WD2-N-2	**13:15-13:30**	**Efficient Configuration-Data Assignment Algorithm for CGRA-based Multi-Core Architecture1** So Hyun Yoon, Hyejin Joo, and Yoonjin Kim Department of Computer Science, Sookmyung Women's University
WD2-N-3	**13:30-13:45**	**Pipelining Nested Loops with Triangular Iteration Space for High-Level Synthesis** Atul Rahman, Hyeonuk Sim, and Jongeun Lee School of ECE, Ulsan National Institute of Science and Technology
WD2-N-4	**13:45-14:00**	**Fast Verification Flow with High-Level Synthesis - Case Study** Ganghee Lee, Changsoo Park, Kyungah Jeong, Jinhong Oh, and Jinaeon Lee Multimedia Core Development Team, System LSI, Samsung Electronics Co., Ltd.
WD2-N-5	**14:00-14:15**	**UVM based Register Test Automation Flow** Jaehun Woo, Yongkwan Cho, and SunKyu Park Design Solution Lab, DMC R&D, Samsung Electronics Co., Ltd.
WD2-N-6	**14:15-14:30**	**Fault-Recoverability Evaluation of CGRA-based Multi-Core Architecture1** Seungyeon Sohn and Yoonjin Kim Department of Computer Science, Sookmyung Women's University