## N. VLSI CAD 분과

**Room D**
**1F / 107호**

**2015년 2월 11일(수) 09:00-10:30**
**[WD1-N] VLSI Design & Automation**
**좌장: 김윤진 (숙명여대), 이종은 (UNIST)**

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| **WD1-N-1** | **09:00-09:15** | **Analysis of Characterizing Feasible Design Space of LC-VCO Using SVM Classifiers**<br>Jiho Lee and Jaeha Kim<br>Department of Electrical and Computer Engineering, Seoul National University |
| **WD1-N-2** | **09:15-09:30** | **Local Density-aware Metal Retargeting for Preventing Topological CMP Failure in Sub-28nm Node Designs**<br>Yongchan Ban, Eunjoo Choi, Yongseok Kang, and Woohyun Paik<br>System IC R&D Lab., LG Electronics |
| **WD1-N-3** | **09:30-09:45** | **Reducing Routing Congestion and Chip Area by Post Placement Optimization Utilizing Redundant Inter-Cell Margin**<br>Woohyun Chung, Seongbo Shim, and Youngsoo Shin<br>Department of Electrical Engineering, KAIST |
| **WD1-N-4** | **09:45-10:00** | **Comparative Study of Capacitor-Less LDO Regulator Designs Based on Pass Transistor Types**<br>Soyeon Joo[1], Jintae Kim[2], and SoYoung Kim[1]<br>[1]College of Information and Communication Engineering, Sungkyunkwan University, [2]Department of Electronics Engineering, Konkuk University |
| **WD1-N-5** | **10:00-10:15** | **Simultaneous Fixing Hold Violations of Best and Worst Corners**<br>Inhak Han, Jinwook Jung, and Youngsoo Shin<br>Department of Electrical Engineering, KAIST |
| **WD1-N-6** | **10:15-10:30** | **Clock Domain Crossing Aware Sequential Clock Gating Optimization**<br>Jianfeng Liu, Mi-Suk Hong, Kyungtae Do, Jung Yun Choi, and Jaehong Park<br>Design Technology Team, Samsung Electronics Co. Ltd. |