G. Device & Process Modeling, Simulation and Reliability 분과

Room C
1F / 106호

2015년 2월 11일(수) 09:00-10:30
[WC1-G] Device Modeling and Simulation
좌장: 이재규 (삼성전자), 조인욱 (SK Hynix Inc.)

WC1-G-1	**09:00-09:15**	**A Newly-Proposed Vacuum-Channel Transistor** In Jun Park and Changhwan Shin School of Electrical and Computer Engineering, University of Seoul
WC1-G-2	**09:15-09:30**	**DFT-NEGF Simulation of Si Nanowire Transistors using Reduced-Sized Hamiltonian** Woo Jin Jeong, Jaehyun Lee, and Mincheol Shin Department of Electrical Engineering, KAIST
WC1-G-3	**09:30-09:45**	**Multiple Negative Differential Resistance Device by using the Ambipolar Behavior of TFET with Fast Switching Characteristics** Jaewon Jung, Sunhae Shin, Esan Jang, and Kyung Rok Kim School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology
WC1-G-4	**09:45-10:00**	**Analysis of Stress Effect on (110)-oriented Single Gate SOI nMOSFETs using Silicon-Thickness-Dependent Deformation Potential** Sujin Choi, Wookyung Sun, Injae Lee, and Hyungsoon Shin Department of Electronics Engineering, Ewha Womans University
WC1-G-5	**10:00-10:15**	**Effects of Ferroelectric Thickness on Negative Capacitance FET Inverters** Junbeom Seo, Jaehyun Lee, and Mincheol Shin Department of Electrical Engineering, KAIST
WC1-G-6	**10:15-10:30**	**Design and Analysis of Gate-recessed AlGaN/GaN Fin-type Field-Effect Transistor** Young In Jang, Jae Hwa Seo, Young Jun Yoon, Hye Rim Eun, Ra Hee Kwon, Jin Su Kim, Jung-Hee Lee, and In Man Kang School of Electronics Engineering, Kyungpook National University