

# 제22회 한국반도체학술대회

2015년 2월 10일(화) - 12일(목), 인천 송도컨벤시아

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## B. Patterning 분과

Room B  
1F / 105호

2015년 2월 11일(수) 09:00-10:30

[WB1-B] Patterning

좌장: 유원종 (성균관대학교), 정지원 (인하대학교)

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| WB1-B-1 | 09:00-09:15 | <b>Deep Contact Hole Patterning for 3D NAND Flash</b><br>구분왕, 김종훈, 김영식<br>SK Hynix Inc. 미래기술 연구원 PHOTO Technology Team   |
| WB1-B-2 | 09:15-09:30 | <b>EUV Multilayer Defect Compensation in Computational Lithography</b><br>김상곤<br>한양대학교   |
| WB1-B-3 | 09:30-09:45 | <b>Negative Tone Development Process Window according to Pattern Size</b><br>Doyoun Kim, Seyoung Oh, Hyoungsoon Yune, Daejin Park, Woosung Moon, Hyunjo Yang, and Donggyu Yim<br>Research & Development Division, SK Hynix Inc.  |
| WB1-B-5 | 10:00-10:15 | <b>Overlay Metrology In Cell Area with Design based Metrology</b><br>Gyoyeon Jo <sup>1</sup> , Jungchan Kim <sup>1</sup> , Sunkeun Ji <sup>1</sup> , Chanha Park <sup>1</sup> , Minwoo Park <sup>1</sup> , Hyunwoo Kang <sup>1</sup> , Hyunjo Yang <sup>1</sup> , Donggyu Yim <sup>1</sup> , Masahiro Yamamoto <sup>2</sup> , Kotaro Maruyama <sup>2</sup> , and Byungjun Park <sup>1</sup><br><sup>1</sup> Research & Development Division, SK Hynix Inc., Korea, <sup>2</sup> NGR Inc. Japan |
| WB1-B-6 | 10:15-10:30 | <b>Study and Control of Reticle Heating Contribution to Total Overlay Error Budget for Sub-20-nm Devices</b><br>Byong-Seog Lee, Honggoo Lee, Sangjun Han, Wontaik Kwon, and Myoungsoo Kim<br>R&D Div., SK Hynix Inc. Semiconductor Inc.  |