F. Silicon Device and Integration Technology 분과

Room G
1F / 109호

2015년 2월 12일(목) 13:10-14:40
[TG2-F] Emerging Devices (2)
좌장: 정성웅 (SK Hynix Inc.), 이희덕 (충남대학교)

TG2-F-1	**13:10-13:25**	**Effect of Double Patterning on Performance Variation Induced by Gate Line-Edge-Roughness (LER) in Germanium FinFET** Seulki Park[1], Hyun-Yong Yu[2], and Changhwan Shin[1] [1]School of Electrical and Computer Engineering, University of Seoul, [2]Department of Electrical Engineering, Korea University
TG2-F-2	**16:05-16:20**	**Heterojunction Symmetric Tunnel Field-Effect Transistor (S-TFET)** Hyohyun Nam and Changhwan Shin School of Electrical and Computer Engineering, University of Seoul
TG2-F-3	**13:40-13:55**	**Optimal Design of an Electrically Self-Isolated GaN-on-Si Junctionless Field-Effect Transistor for Beyond-CMOS Low-Power Applications** Seongmin Lee[1], Jeongmin Lee[1], Jisun Lee[2], Young Jun Yoon[3], In Man Kang[3], and Seongjae Cho[1,2] [1]Department of IT Convergence Engineering, [2]Department of Electronic Engineering, Gachon University, [3]School of Electronics Engineering, Kyungpook National University
TG2-F-4	**13:55-14:10**	**A Novel Sampling Method Using Confidence Ellipse Conceptto Estimate the Impact of Random Variation on Static Random Access Memory (SRAM)** Sangheon Oh and Changhwan Shin School of Electrical and Computer Engineering, University of Seoul
TG2-F-5	**14:10-14:25**	**Negative Capacitance Field-Effect Transistor for Sub-60-mV/Decade Steep Switching Device** Jaesung Jo[1], Woo Young Choi[2], and Changhwan Shin[1] [1]School of Electrical and Computer Engineering, University of Seoul, [2] Department of Electronic Engineering, Sogang University
TG2-F-6	**14:25-14:40**	**Germanium-Source Vertical Tunnel Field-Effect Transistor** Hyunjae Lee and Changhwan Shin School of Electrical and Computer Engineering, University of Seoul