Tackling High Volume Production of 3DI/TSV Packages

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The omni-presence of 3DI/TSV packages has been proposed since almost a decade, but the tremendous package costs inhibited for a long time a general break-through of this technology. But, driven by super-computing applications, the need for low-power consuming, high-speed memory stacks has evolved fast and since two years we see such kind of packages in volume production.

Since thermo-compression bonding is typically a slow process, the cost of ownership of thermo-compression equipment is always under focus. Based on a dual bond head approach implemented on a fast machine architecture an attractive cost-of-ownership can be offered on a minimum of floor-space, and 1000 UPH per TC bonder is now a benchmark performance.

Beyond the high level of capabilities that thermo-compression bonders must provide for 3DI/TSV applications there are special challenges like tool-2-tool repeatability, recipe portability, enhanced machine capability tests for thermo-compression equipment which must be tackled in a high volume production environment. Finally a major challenge is addressing the graphical user interface (GUI) which has to offer an easy access to the equipment and has to hide the complexity of the machine.

Characteristics of Through-Si-Via(TSV) Filling by Electrodeposition with Pulse Wave Form Current

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Recently, TSV interconnection was intensively investigated to achieve the excellent performance and high efficiency for semiconductor devices. However, several issues such as reliability and slow process rate make it hard to be applied in industry. Especially, via filling process using Cu electrodeposition has been a core process in the total TSV process because of its high processing cost. Therefore, increasing the via filling rate is a necessary task for commercializing the TSV technology in industry. In the case of the via filling process using the direct current, the via filling rate should be limited due to the slow diffusion rate of cupric ion resulting in the limitation of the current density. If the current density is increased over the limiting current to increase the rate of via filling, entrance of the via should be blocked and huge void should be formed because of the fast deposition rate both at the top and on the side wall of the via. However, in the case of via filling using the pulse wave form current, the thickness of the ion depleted layer could be controlled by relaxation time. Thin ion depleted layer on the side wall and at the top of the via decreases the surface overpotential and preserves the effect of suppressor. Therefore, ion diffusing into the via could effectively deposited at the bottom of the via. In this research, significant improvement in via filling rate was achieved by applying the pulse wave form current as shown in the figure 1.

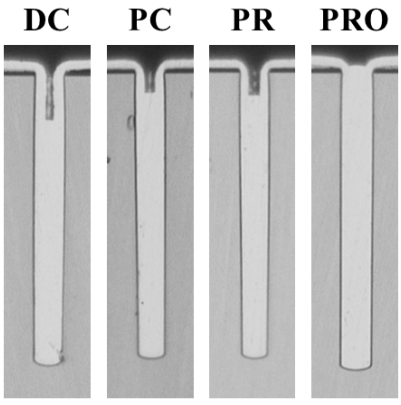

Figure 1. Cross-sectional images of Cu filled via by direct current (DC), pulse current (PC), pulse-reverse current (PR) and pulse-reverse-off current (PRO).

Temporary Bonding and Debonding Technology to Enable Cost-Effective Fabrication of Through-Glass-Via Interposers

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Temporary bonding and debonding technologies designed for use in fabricating silicon interposers have been widely discussed at conferences. Despite tremendous efforts to overcome several technical hurdles such as wafer chipping, cracking, and warpage, the complexity of the processes, which leads to high costs for manufacturing silicon interposers, remains the primary concern.

A through-glass-via (TGV) interposer process flow involving simplified temporary bonding and debonding technology will be presented here as an example of a simple and cost-effective solution for realization of 2.5-D integrated circuit technology. A TGV interposer wafer with 30-µm-diameter vias to eliminate the isolation layer is combined with polymer-based polybenzoxazole (PBO) as passivation to build one to two redistribution layers (RDLs) with 20-µm line width on both sides after thinning to 100 µm utilizing a simplified temporary bonding and debonding technology. As shown in fig. 1, this technology includes only a release layer on a glass carrier and another layer of bonding material on the TGV wafer to enable fabrication of the TGV interposer.

A process flow for fabricating TGV interposers utilizing this simplified temporary bonding and debonding technology will be presented in detail, including carrier treatment, bonding material coating, bonding, Ti/Cu (seed layer) deposition, Cu plating, RDL deposition, under-bump material (UBM) formation, debonding, and silicon chip stacking on the TGV interposer.

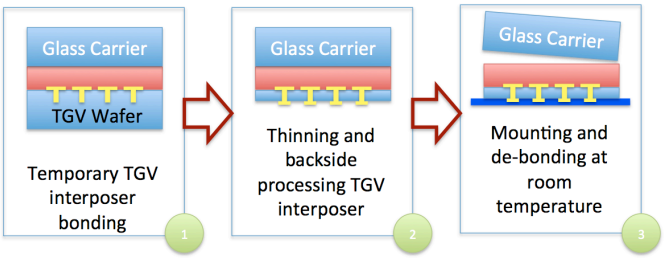

Figure 1: Generalized process flow for TGV interposer wafer thinning and processing

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Mechanisms of improving thermal cycling reliability with pad finish & solder alloying effect on solder grains

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Abstract—in present work, solder alloys for memory and EDP packages were investigated on the effect of high thermal cycling reliability. The difference mechanisms were also clarified on alloying effect and pad finish effect. Solder grains and mis-orientations between adjacent grains were defined by electron backscatter diffraction (EBSD). The additives change the grain mis-orientations and grain sizes after reflow process and thermal cycling. The high mis-orientation angle between the adjacent grains is effective on the high thermal cycling reliability.

I. Introduction

Sn based solder alloys have been researched actively for a few decades, due to its wonderful merits on electro-devices for joining components. Especially, Sn-Pb solder was only a representative solder alloy for over the forty years [1-4.] However using Sn-Pb has been prohibited by RoHS regulations in 2005 for toxic of Pb to human [5]. Therefore, Pb-free solder paste and ball has been developed to replace Sn-Pb [6-11]. However the development of lead-free solder has been brought many reliability problems on electro packaging such as Sn whisker, decreasing joint reliability, increasing reflow temperature and so on. Moreover, the trend miniaturization and thinning of mobile electronics faces the high reliability challenges, such as high thermal cycling and humidity conditions under low cost manufacturing. Recently, the mechanical drop reliability is reinforced by changing solder mask defined (SMD) structure on board on solder pad from None SMD (NSMD). However the thermal cycling (TC) reliability is decreased by SMD structure. Figure 1 shows each structure of (a) SMD and (b) NSMD for solder on pad. Therefore, the changing SMD structure is essential for strengthen to TC reliability. In this research, various pad finishes; OSP, Ni/Au, ENIG have been compared by EBSD analysis before and after TC. The various solder balls have been also clarified to develop high TC solder ball for SMD structure.

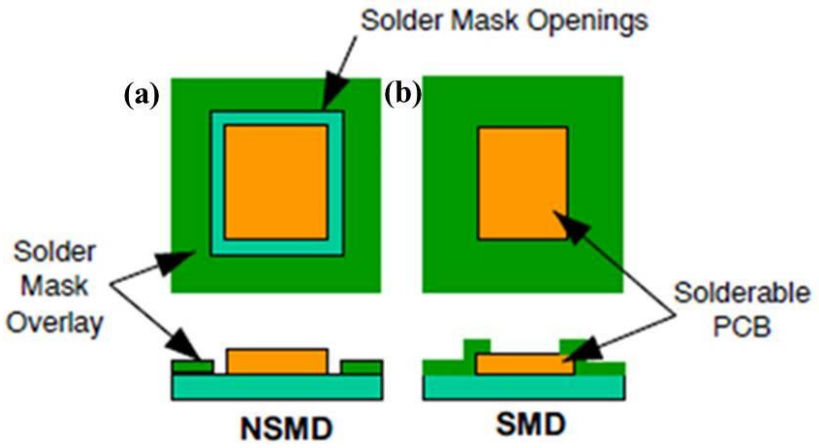

Figure 1. (a) NSMD structure (b) SMD structure

The different grain size and their mis-orientation angles are important to strengthen the TC reliability. The details of the mechanisms about a high TC reliability will be discussed.

II.Experimental procedures

Three kinds of finishes; OSP, Ni/Au and ENIG were prepared on the PCB board to evaluate the pad finish effect. Sn-3.0Ag-0.5Cu (SAC305) and Samsung Solder ball; SS1 were reflowed for top package bonding on the different pad finishes. Table 1 displays the details of variables in this study.

Top Package	Solder ball	Pad finish on Board Side
Ni/Au	SAC302	OSP
		Ni/Au
		ENIG
Ni/Au	SS1	OSP
		Ni/Au
		ENIG

Table1. The variables of pad finish and solder ball composition.

#	Package side	Solder Ball	Pad finish	1% accumulate failure (cycles)	Scale	Shape
1	Ni/Au	SAC302	OSP	1438	1926	15.7
2			Ni/Au	2265	3014	16.1
3			ENIG	2052	2902	13.3
4	Ni/Au	SS1	OSP	1580	2033	18.2
5			Ni/Au	2675	3054	34.7
6			ENIG	2639	3241	22.4

Table Results of TC reliability calculating by minitab14 software.

Top package and board were reflowed with two kinds of solder balls for bonding. The numbers of sample were 100ea on each condition. After reflowed, all the samples were tested TC from -25 ℃ up to 125 ℃ in the TC camber. The dwell times are about 15 minutes respectively at each low and peak temperature. Every after 100 cycles, all the samples were measured by electrical probe. TC test was performed up to 3500 cycles and the reliability distribution with arbitrary censoring was calculated by Minitab 16. The calculated data are arranged in Table 2.

III. Results

TC reliability results indicate Ni/Au pad finish effect for TC is far superior to the others irrespective of solder ball. SS1 is more effective at the TC reliability than the conventional SAC302. Therein, the TC reliability is more dependent on the pad finish than the solder ball. Au composition is good to dissolve in Sn solder and block to growth intermetallic compounds (IMCs) between joint interfaces. It is well coincident with the Ni/Au, ENIG results after TC test. The detail mechanisms will be explained by EBSD analysis.

IV. Discussion i: EBSD interpretation

To clarify detail mechanisms of pad finish and solder ball, the cross sectioned plane were analyzed by EBSD with each orientation. Each grain sizes were also defined.

Figure 2 indicates the crystal orientations of each condition. The each colors indicate each separated grain of Sn. As shown in figure2, Ni/Au pad finish shows smaller grains than the others irrespective of solder balls. Even more, the orientation distributions well indicated in figure 3. The concentrations of orientation, especially at the

001 plane to 110 are well shown in OSP finishes which marked with red dotted circle in Fig.3. however, in case of Ni/Au, omnidirectional orientation distributions can be defined. These results well explain the TC results i.e., small grains and omnidirectional orientation is effective at TC reliability. Furthermore, the correlations between grains are defined by mis-orientation angle as shown in figure 4.

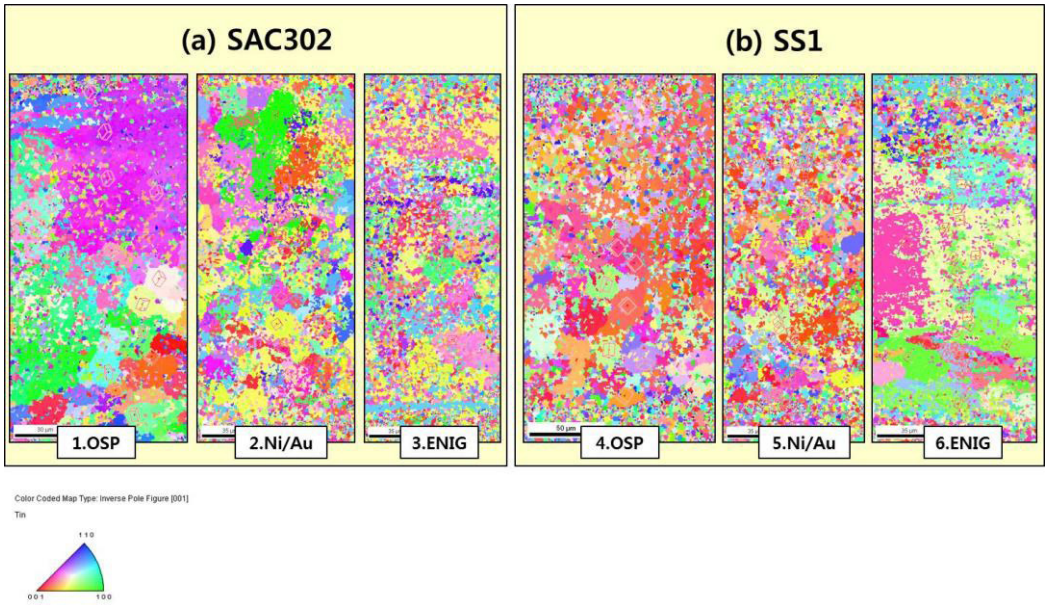

Figure 2. The crystal orientation of (a) SAC302 and (b) SS1 after 2000 cycle.

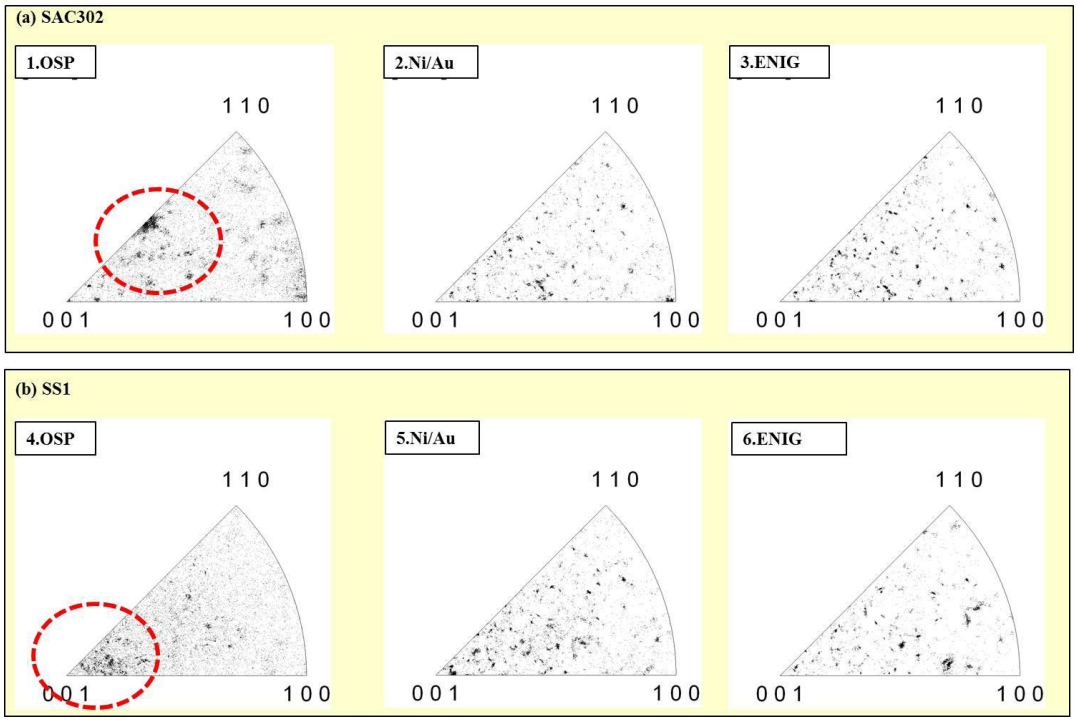

Figure 3. Inverse pole figures of (a) SAC302 and (b) SS1 after 2000 cycle.

The mis-orientation is the difference in crystallographic orientation between two crystallites in a polycrystalline material [12].

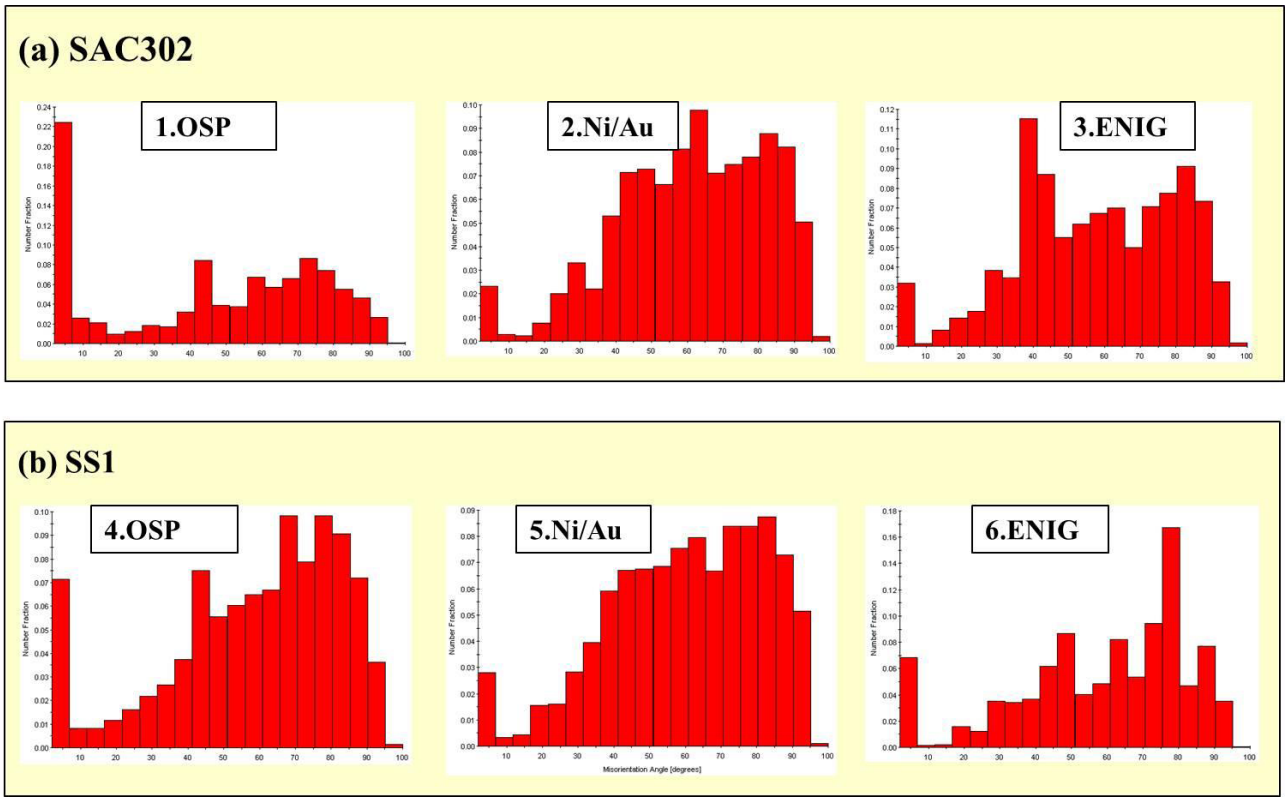

Figure 4. Mis-orientation angle of (a) SAC302 and (b) SS1

Mis-orientation angle of Ni/Au finishes are larger than those of the others irrespective of solder ball as shown in Fig.4. Note that distributions of mis-orientation angle are different from SAC302 and SS1 in case of OPS finishes. Indicating that SS1 solder ball have finer grains and larger mis-orientation angle than that of SAC302. TC reliability has been increasing as finning grain size and increasing mis-orientation angle. EBSD results i.e., grain size, orientation and mis-orientation distributions well explain the TC reliability results.

IV. Discussion ii: reinforcing TC reliability mechanism

TC reliability has been lengthened by changing grain properties on grain refinement and mis-orientation. Grain refinement during reflow process causes grain orientation omnidirectional. These relocated grains have larger mis-orientation than that before grain refinement. Fig.5 demonstrates briefly the mechanism of improving TC reliability by grain refinement.

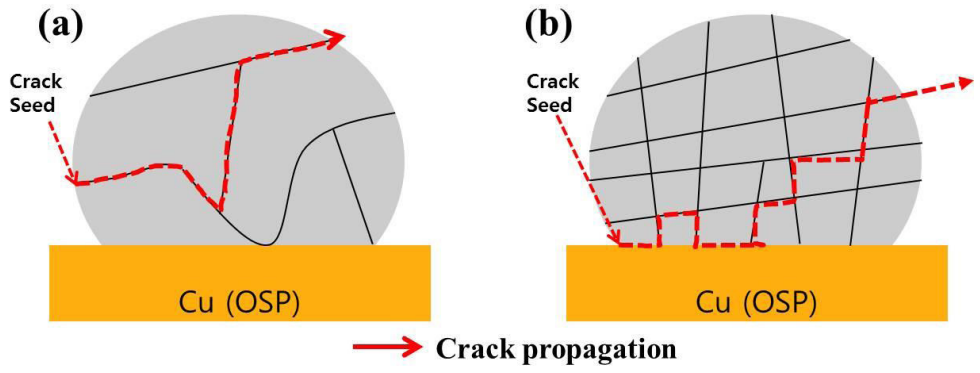

Figure 5 Schematic of crack propagation during TC; (a) SAC302 solder and (b) SS1 solder

The cracking, in general, initiates and propagates to the grain boundaries. In fig.5, SS1 shown in (b) has longer crack propagation line than the (a) OSP. Indicating grain refinement is effective for the TC reliability with increased grain boundaries. Considering 3-dimensional crack propagation, the differential TC reliability between SAC302 and SS1 far outweigh. Suggesting conclusive mechanism that increased grain boundaries and mis-orientation effectively hinder crack propagation following to the grain boundaries during TC.

V. Conclusion

Pad finish and solder balls effects have been investigated on TC reliability. Ni/Au effectively refines grain after reflow process comparing to the OSP (Cu) pad finish. However, even OSP pad finish reflowed by SS1 solder, more effective grain refinement and more larger mis-orientation angle have been showned than those of SAC302 solder. Grain refinement rolls to relocate grain orientation to omnidirectional distributing larger mis-orientation between grains than before re-location.

Consequently, refined grains and increased mis orientation angle is effective for TC reliability disturbing crack propagation followed to grain boundaries.

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Comparison of Creep Models for Solder Alloys

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ABSTRACT

Demand for long-term reliability of electronic packaging has lead to a large number of studies on visco-plastic behavior of solder alloys. In order to explain the visco-plastic behaviors of solder joints, various creep models for solder alloys have been proposed by using the main factors, such as temperature, strain rate, and stress. They range from purely empirical to mechanism based models where dislocation motion and diffusion processes are taken into account. In this study, most commonly used creep models for solder alloys are compared with the test data and implemented in numerical simulation by using ABAQUS in order to compare their performance in cycling loading. Finally, a new creep model is proposed that combines best features of many models. It is also shown that, while two creep models may describe the same material stress-strain rate curves equally well, they may yield very different results when utilized for cycling loading. One interesting observation of this study is that the stress exponent, *n,* also depends on the grain size.

Deep Contact Hole Patterning for 3D NAND Flash

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NAND 제품개발이 2D NAND 제품에서 3D NAND FLASH 제품개발로 빠르게 변모하고 있다. 또한 제품별 Generation 이 진행됨에 따라 평면적인 Critical Dimension 감소보다 Depth 가 깊어지면서 공정 개발 난이도가 훨씬 더 어렵고 중요한 시기로 변모하고 있다. 특히 Deep Contact Patterning 에서의 안정된 Process Margin 을 확보하는 것이 무엇보다도 중요한 Item 으로 나타나고 있다.

3D NAND FLASH 에서 Deep Contact Patterning 은 난이도가 높은 핵심공정중의 하나로서 Contact Hole 의 Depth 가 30kÅ 이상의 High Aspect Ratio 를 가지고 있다. 식각 공정에서 형성된 30kÅ Depth 이상의 Deep Contact Hole Pattern 위에 MASK 공정을 진행 시 Contact Hole 바닥부분에 남아있는 Exposed Resist 가 Develop 과정에서 완전히 제거 되지 못한 Scum 성 Residue 불량 문제가 발생 하고 있다.

본 논문은 Deep Contact Hole 에서의 Resist Scum 을 제어할 수 있는 방법으로 Develop Performance 강화, 수용성 Gap Fill Material 적용 등의 기술 개발로 Scum 문제에 대한 개선방법을 제시하여 3D NAND 제품수율 향상에 기여할 수 있도록 하였다.

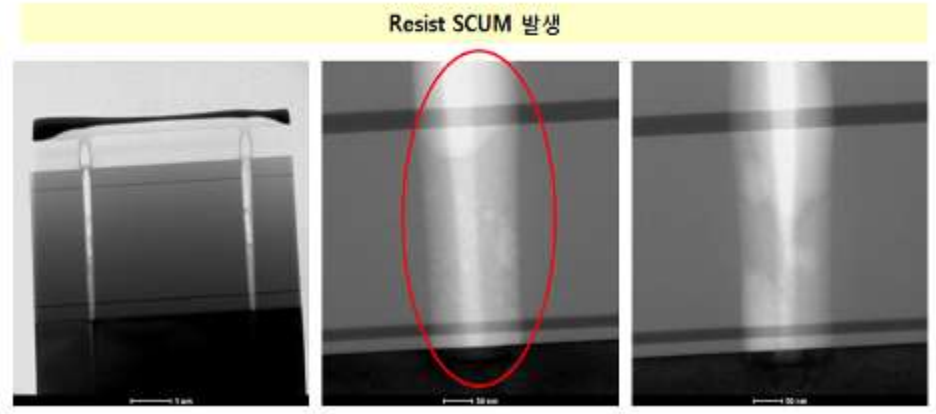

Fig 1. Deep Contact Hole Resist Scum

EUV Multilayer Defect Compensation in Computational Lithography

According to the international technology roadmap for semiconductors (ITRS), the extreme ultraviolet lithography (EUVL) is the leading candidate for semiconductor patterning. One of the most critical problems in EUVL development is EUV mask defects, specifically buried multilayer (ML) defects. Different types of mask defects manifest their effects differently during resist patterning in terms of the defect size and defect position. Repair and other mitigation strategies are essential because the near zero-defect mask blanks cannot be fabricated.

In this paper, a new defect printability simulator (DPS) is introduced to predict the effects of ML defects on aerial images in EUV and to reduce the effects in terms of mask repair. ML defects are simulated by using a combining the multi-thin layer method with a rigorous coupled-wave analysis (RCWA) of S-matrix. The compensation of ML defects is investigated from the viewpoint of simulation results. This DPS can be helpful in understanding EUV defect and also give insight into the EUV defect compensation for the device volume production.

Negative Tone Development Process Window according to Pattern Size

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반도체 산업이 발달 됨에 따라 Bit Growth 를 위해 Technology Node 는 점점 줄어들고 있으며, 그와 더불어 높은 생산성을 유지하기 위해 다양한 기술 개발이 이루어지고 있다. 한편 Patterning 관점에서 193nm 1.35NA ArF Immersion 기술의 한계에 봉착하면서 이를 극복하고자 EUV, MPT, ILT 등 다양한 기술들이 개발되고 있지만, 아직 양산에 적용하기엔 몇 가지 해결해야 할 숙제들이 있다. 모든 기술 개발은 Define 능력과 함께 넓은 Process Window 를 가지는 방향으로 이루어지고 있는데 이러한 기술 중 하나가 바로 현재 많이 쓰이고 있는 Negative Tone Development (이하 NTD) 이다. NTD 는 Bright Field Mask 를 사용하여 Dark Field Mask 특성을 가지는 Pattern 을 형성할 수 있는 기술로 Developer 를 Negative Tone 으로 바꾸어 Lithography 을 진행하는 방식이다. PTD 에서는 노광된 영역의 PR Pattern 이 현상되어 제거되었다면, NTD 에서는 노광되지 않은 영역의 PR Pattern 이 제거된다는 점에서 반대의 결과를 얻을 수 있다. 이러한 NTD 는 기존의 다양한 논문과 실험을 통해 Small Feature 의 Contact Hole 과 Narrow Trench 구조에서 PTD 에 비해 Depth of Focus (이하 DOF) Margin, Mask Error Enhancement Factor (이하 MEEF), Line Edge Roughness (이하 LER) 측면에서 더욱 좋은 특성이 있다는 것이 밝혀졌다. 본 논문에서는 이러한 NTD Process 를 이용해 1D, 2D Pattern 을 Size 별로 노광해서 평가함으로써 NTD Process 의 기본적인 Back Data 를 수집하여 그 특성을 이해할 수 있다. 그리고 Pattern 들의 Process Window 를 정리하여 Layer 의 Pattern Size 및 구조 특성에 따라 NTD Process 의 사용 여부를 결정하는 좋은 Guide Line 을 제시해 줄 것이며, Pattern Size 가 큰 경우 Margin 이 적은 경우가 있는데 이러한 부분 역시 실험을 통해 분석해볼 것이다.

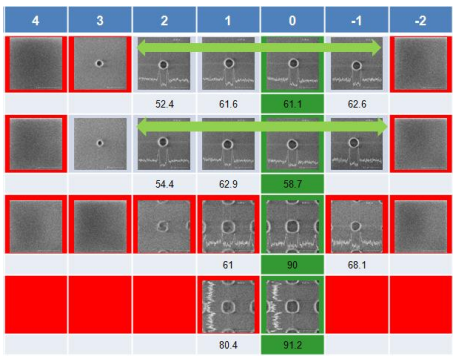

그림 1. Contact Hole Size 별 DOF Margin 비교

Overlay metrology in cell area with design based metrology

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반도체 소자의 고집적화 및 제품 특성 확보를 위해 deisgn rule 감소에 대한 요구는 끊임없이 이어지고 있으며 이를 위해서는 미세패턴 구현 능력과 함께 복잡한 process를 거쳐 형성되는 layer간 정밀한 중첩도 (이하 overlay)의 유지 또한 더욱 중요해지고 있다. 본 논문에서는 DBM (Design Based Metrology) tool을 이용하여 특정 mark가 아닌 real pattern을 측정하는 overlay분석 방법의 개발 및 적용 내용에 대해 소개하도록 한다. 현재 Fab에서는 frame 외곽에 layer별로 형성되는 mark를 통해서 overlay값을 측정하는 방식이 주로 사용되고 있으나 process에 기인된 mark의 왜곡, real pattern과의 size 차이 등으로 실제 pattern의 overlay 값을 대변하지 못하는 문제점이 있다. 이를 보완하기 위해 최근 CD-SEM 계측 장치를 이용, 실제 pattern을 측정하는 방식 또한 활용되고 있으나 data volume 부족과 coordinate accuracy 부족에 따른 분석 정확도 측면에서 개선이 필요하다. 이러한 측면에서 e-beam을 사용하며 target lay-out과 wafer pattern간 matching 분석으로 대량 data 확보가 가능한 NGR2170 DBM tool을 사용, DRAM과 Flash 제품의 critical layer에서 Overlay를 측정하였다. DRAM cell array의 contact과 하부에 형성되는L/S pattern간 Inter/Intra field overlay 분석 결과 wafer edge die에서 L/S pattern 대비 contact의 ~7nm shift 검출이 가능하였다. 이와 같은 분석 방법을 통해 기존 metrology 기법의 한계를 극복하는 것이 가능하다.

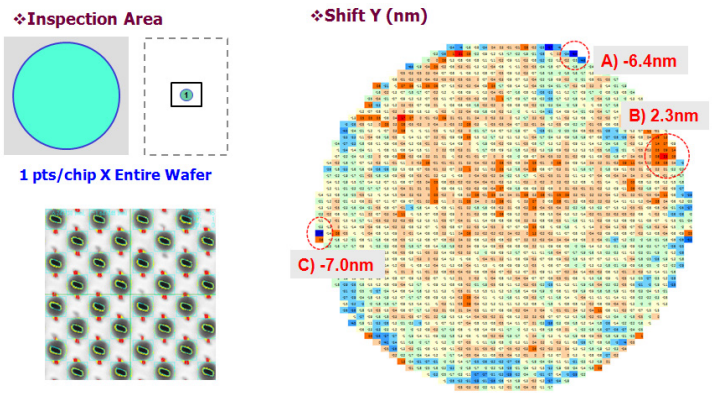

Figure 1. Inter field overlay measurement result for (Contact)

Study and Control of Reticle Heating Contribution to total Overlay Error Budget for sub-20-nm devices

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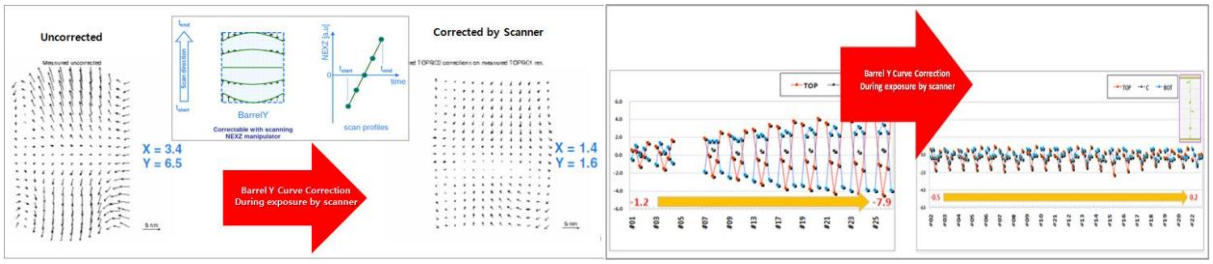
According to the 20013 HTRS for Semiconductors of DRAM, the overlay budget of T2z nm memory devices is 3.5 nm. To meet such a tight requirement, the total overlay error budget should be controlled carefully. There are many ways to analyze overlay budget; here, however, a simple but classic methodology is used. In this study, total overlay error budget consists of four major contribution categories: system, process, metrology, and mask contributions. Major three Overlay Budget items of sub-20-nm era devices are Heating of Scanner System, Process Fingerprint, total measurement Uncertainty of metrology tool. Especially, Uncontrollable Reticle Heating Error is recently emerged and must be minimized at ultimate sub-20-nm device era. In this article, optimum control of Reticle heating is investigated.



(a)Schematic diagram of Reticle heating curve correction (b)T2y M0C INTRA Residual Improvement with Scanner Option

Fig 1. Measure of Reticle heating curve and correction by scanner option

1]SeungYoon Lee,"Overlay Strategy of EUV Lithography era" 2010 International Symposium on Extreme Ultraviolet Lithography

[2] Amr Y. Abdo “Effects of Cr Pattern Characteristics on Image Placement due to the Thermomechanical Distortion of Optical Reticles During Exposure” SRC Program Review 2003

[3] Pierluigi Rigolli1," Double patterning overlay budget for 45 nm technology node single and double mask approach,"
J. Vac. Sci. Technol. B 25, 2461 (2007)

A Newly-Proposed Vacuum-Channel Transistor

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Recently, vacuum-channel transistor has been studied because of its possible application for high frequency operation [1]. However, previous studies [2, 3] are not suitable for digital integrated circuits (ICs) for two reasons: **i)** the anode voltage is much higher than the gate voltage when gate leakage current is small, and **ii)** scaling the proposed devices in [2, 3] down to the nanometer scale by using current CMOS technology is challenging. We report a new vacuum-channel transistor (*i.e.,* a *slit-type vacuum transistor*) with a carbon nanotube cathode and nanometer-scale channel length. Because of its geometrical characteristics, the device enables to be operated when the anode bias is almost the same as the gate bias with a negligible gate oxide leakage current. Moreover, its channel length is almost the same as the mean free path of carriers in air, meaning that the device can operate in vacuum as well as in air, without any performance degradation.

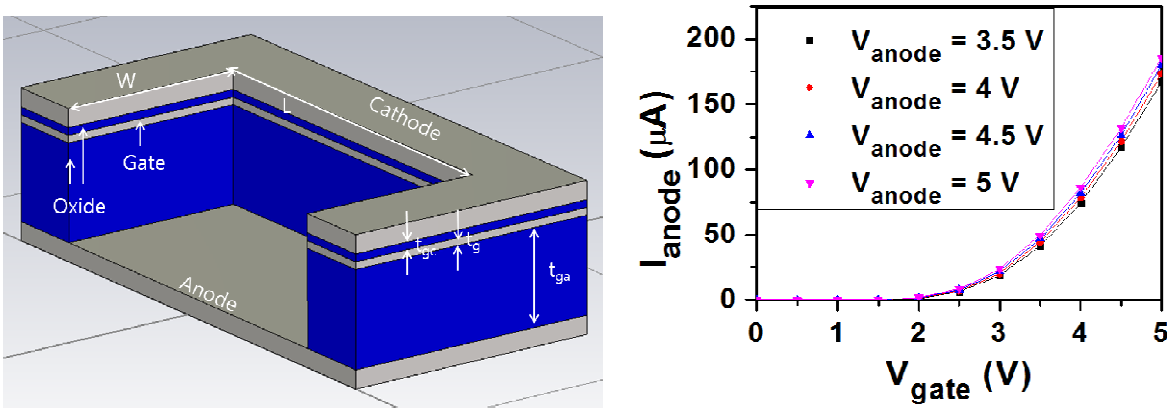

Fig. 1. Proposed device structure (left) and its input characteristic (right)

References

[1] J.-W. Han, J. S. Oh, and M. Meyyappan, *App. Phys. Lett.,* 100, 213505 (2012).
[2] S. H. Hsu, W. P. Kang, S. Raina, and J. H. Huang, *App. Phys. Lett.*, 102, 203105 (2013).
[3] S. H. Hsu, W. P. Kang, J. L. Davidson, J. H. Huang, and D. V. Kems, *J. Appl. Phys.,* 111, 114502 (2012).

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637).

DFT-NEGF simulation of Si nanowire transistors using reduced-sized Hamiltonian

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The ab-initio method[1] is the most rigourous method to simulate ultra-scaled nano devices because material-dependent input parameters are not required. However, due to the huge computational burden, it is impractical to directly apply the ab-initio method to the device-level carrier transport problem. In this work, we propose an efficient simulation method for the quantum transport in the nanowire field effect transistors (NWFET), using device Hamiltonians constructed via the density function theory (DFT) and the carrier transport calculated by the non-equilibrium Green's function (NEGF) method. The basic principle is to reduce the basis set of the original Hamiltonian by a unitary transformation[2]. We first extracted both the Hamiltonian and overlap matrices of Si NW from the DFT calculations (Fig.1). Their sizes were reduced following the transformation algorithm shown in Fig. 2. Then, with much reduced-sized Hamiltonian matrices, it is possible to simulate Si NWFET efficiently using our in-house Poisson-NEGF solver.

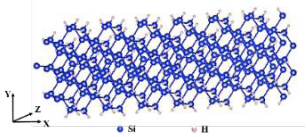

Figure 1

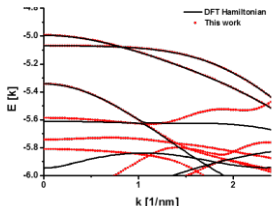

Figure 3

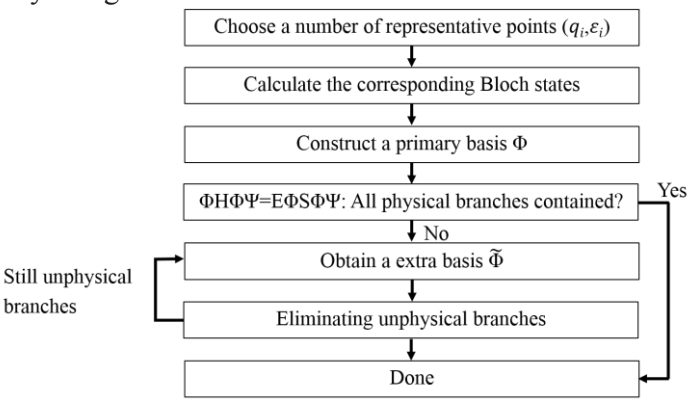

Figure 2

Figure 1. Schematic of the Si nanowire

Figure 2. Flow chart illustrating the algorithm of obtaining reduced basis set

Figure 3. The band structure of DFT Hamiltonian (black solid lines) and this work (red circle symbols)

[1] M. Brandbyge, J.-L. Mozos, P. Ordejón, J. Taylor, and K. Stokbro, Phys. Rev. B, 65, 165401 (2002).

[2] G. Mil'nikov, N. Mori and Y. Kamakura, Phys. Rev. B, 85, 035317 (2012).

Multiple Negative Differential Resistance Device by using the Ambipolar behavior of TFET with fast switching characteristics

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The negative differential reistance (NDR) devices have recived much attention as promising alternative device owing to its nonmonotonic behavior, however, its low peak-to-valley current ratio (PVCR) or CMOS imcompatible process restrict practial applications. For the improvement of PVCR in the CMOS compatible process, many reserach works have been reported focusing on the MOSFET structure and suceed to obatined high PVCR based on single-peak MOS-NDR circuit [1]. In our previous works, ultra-high 2nd PVCR was obatined with double peaks by using the gate-induced drain leakage (GIDL) on conventional MOS-NDR circuit [2]. In this work, we report more improved 1st and 2nd peaks and PVCRs by replacing GIDL-enhanced CMOS inverter with complementary *n/p*TFET (*Tn* and *Tp*) having ambipolar characteristics. Figure 1 shows much steeper voltage transfer characteristics (VTC) with TFET inverter compared with GIDL-enhanced CMOS inverter. The ambipolar characteristics of TFET make faster transiton of VTC on positive direction, while the transition to negative direction is caused from high subthreshold swing. When the improved VTC of Fig.1 is applied on conventional 32nm *n*MOS (*Mn*) with circuit composition in the inset of Fig. 1, the 1st and 2nd PVCRs are enhanced from 17 and 5.8×10^4 to 6.17×10^4 and 5×10^5 respectively, owing to high 1st and 2nd peaks of 0.3 and 1.4mA and fully suppressed valleys with MOSFET off current level (~1nA). Therefore, double-peak NDR with both ultra-high PVCRs (~ 10^5) based on TFET inverter has been successfully demonstrated.

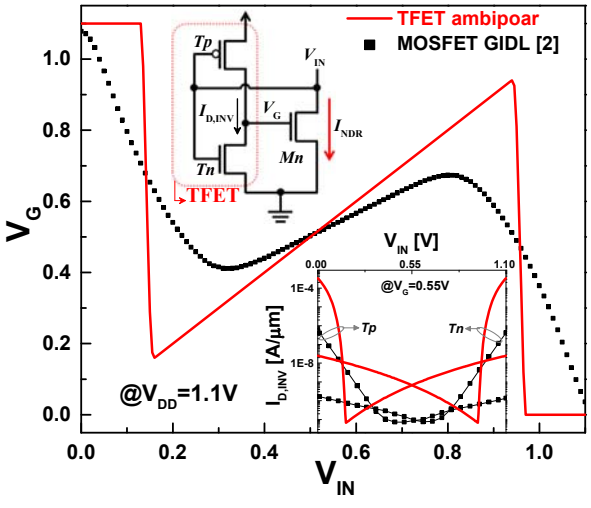

Fig. 1 Voltage transfer characteristics (VTC) of inverter based on ambipolar TFET compared with GIDL-enhanced MOSFET [2].

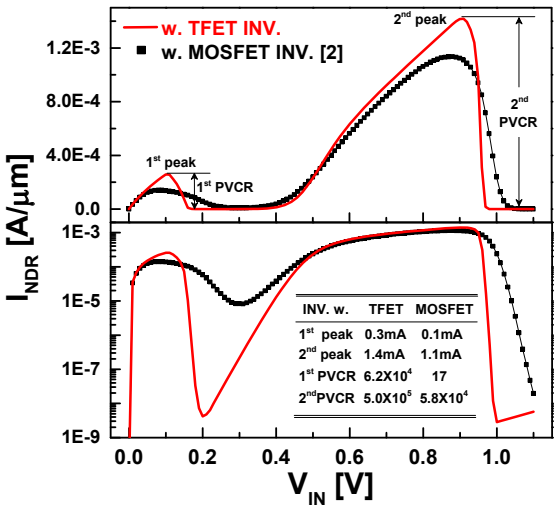

Fig. 2 Multiple NDR characteristics according to linear (top) and log scale (bottom) based on VTC of Fig. 1

[1] J. Nunez, et. al, *IET Electron Lett.*, 45(23), p.1158 (2009)
[2] S. Shin, et. al, *IEEE SISPAD*, p.316 (2013)

Analysis of Stress Effect on (110)-oriented Single Gate SOI nMOSFETs using Silicon-Thickness-Dependent Deformation Potential

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As device dimensions shrink, the enhancement of carrier mobility by strain has been investigated to improve device performance. In this paper, stress effect in uniaxially strained single gate (SG) silicon-on-insulator (SOI) n-type Metal Oxide-Semiconductor Field Effect Transistors (MOSFETs) with (110) wafer orientation is analyzed. The concept of silicon-thickness-dependent deformation potential (D_{ac_Tsi}) is introduced [1] to accurately calculate the mobility using Schrödinger-Poisson solver. Electron mobility enhancements with longitudinal tensile stress condition is simulated as a function of silicon thickness (T_{si}). It is newly found that strain technology in (110) orientation is still effective in extremely thin T_{si}, unlikely in (100) orientation. Due to different Δ2 valley occupancy enhancement and τ enhancement as a function of silicon thickness, mobility enhancements in (110)/<110> shows different silicon thickness dependency compared to (100)/<110>. It should be noticed that higher mobility enhancement by strain is achieved in (110)/<110> from thick T_{si} to extremely thin T_{si}.

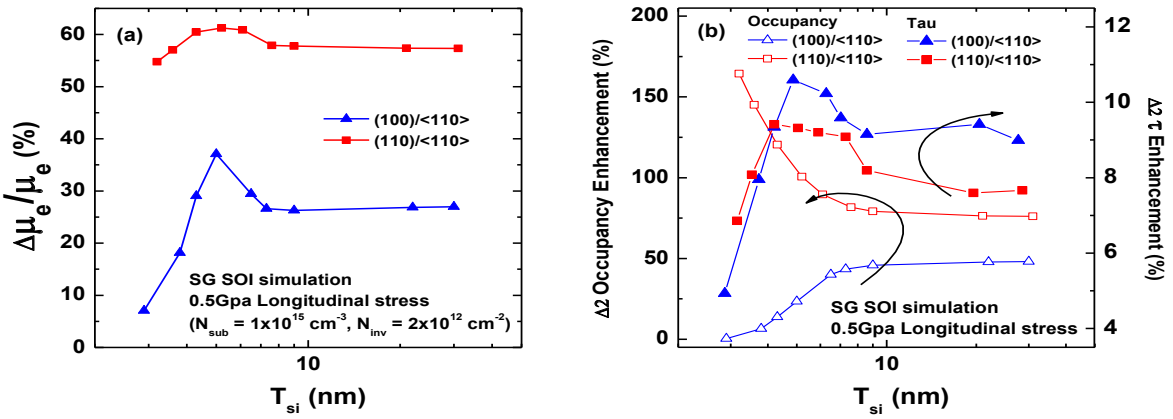

Fig 1. (a) T_{si} dependence of the mobility enhancement and (b) Δ2 valley occupancy enhancement and momentum relaxation time (τ) enhancement induced by uniaxial longitudinal tensile strain in (100)/<110> and (110)/<110> SG SOI MOSFETs.

[1] Ohashi T, Oda S, and Uchida K. Journal of Appl. Phys. 52: 04CC12-1 - 04CC12-6 (2013)

Effects of Ferroelectric Thickness on Negative Capacitance FET Inverters.

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Ferroelectric negative capacitance FETs (NCFETs) are promising candidates to realize steep subthreshold swing (SS) (<60mV/dec) [1]. The NCFETs have been mostly studied in the device level, whereas logic circuits using NCFETs have not been investigated much. In this work, we study the performance of NCFET inverters and the effects of ferroelectric thickness (T_{FE}). In our simulations, current and charge density were obtained by self-consistently solving the Poisson equation and non-equilibrium Green's function with the parabolic effective mass and k•p Hamiltonians for n-type and p-type devices, respectively [2]. $SrBi_2Ta_2O_9$ was assumed as the ferroelectric materials. Our results show that, although the I_{DS}-V_{GS} characteristics of n- and p-type NCFETs do not have any hysteresis, the hysteresis behaviors are seen in the inverters because the charge in the channel and C_{MOS} are altered by V_{DS} [3]. The upper and lower threshold voltages in the inverter characteristics can be adjusted by T_{FE}. It is noteworthy that devices with thinner T_{FE} suppress not only the on-state current (Fig. 1) but also hysteresis behavior (Fig. 2). Since there is a tradeoff between hysteresis and speed, optimization of T_{FE} is a very important aspect in the design of NCFET-based inverters.

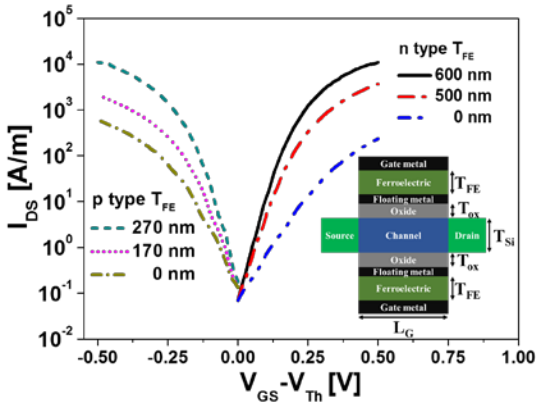

Fig 1. I_{DS} – (V_{GS}-V_{th}) characteristics. Inset shows the structure of the double-gate UTB NCFET with T_{Si} = 5nm and L_G = 20nm.

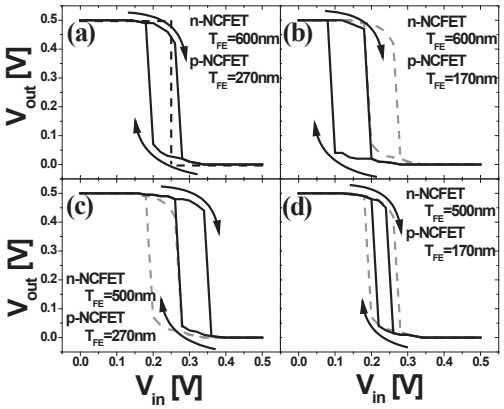

Fig 2. Inverter characteristics for different T_{FE} for n-NCFETs and p-NCFETs.

[1] Salahuddin, Sayeef, and Supriyo Datta, Nano lett, 8(2), 147 (2008).
[2] Mincheol Shin, Nanotechnology, IEEE Transactions on, 6(2), 230 (2007)
[3] Khan, Asif I., et al, Electron Devices Meeting (IEDM), 2011 IEEE International. IEEE (2011)

Design and Analysis of Gate-recessed AlGaN/GaN Fin-type Field-Effect Transistor

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AlGaN/GaN-based transistors have been researched and purposed for high-power, high-temperature, and high-frequency applications due to their inherent material properties such as high electron saturation velocity, wide bandgap and high 2-D electron gas (2-DEG) density at AlGaN/GaN heterojunction. However, the conventional high electron mobility transistors (HEMTs) usually operate at the normally-on state. To realize the normally-off operation, Fin-type FETs(FinFETs) with the recessed gate structure is used in this work [1]. Figure 1 illustrates the structure of the gate-recessed AlGaN/GaN FinFETs. The gate insulator is Al_2O_3 of 30 nm. Parameters used for the optimization are the gate length (L_G), gate-drain length (L_{GD}), fin width (W_{fin}), and GaN layer height (H_{GaN}). The doping concentration of both GaN layer and AlGaN layer is 5×10^{16} cm^{-3}. Figure 2 shows the I_{DS}-V_{GS} transfer curves of gate-recessed AlGaN/GaN FinFETs having various gate length (L_G). The values of I_{DS} for devices with L_G of 200 nm, 500 nm, and 800 nm are 331, 317, and 304 mA/mm, respectively.

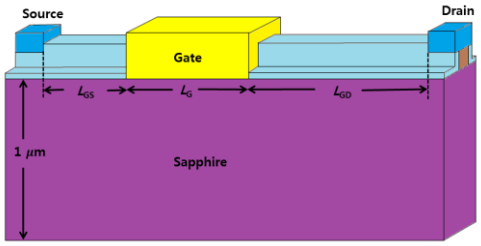

Fig. 1 Structure of the gate-recessed AlGaN/GaN FinFETs.

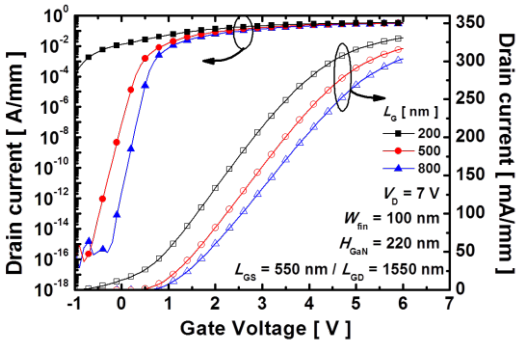

Fig. 2 I_{DS}-V_{GS} curve for various gate length (L_G).

[1] Ki-Sik Im, Jong-Bong Ha, Ki-Won Kim, Jong-Sub Lee, Dong-Seok Kim, Sung-Ho Hahm, and Jung-Hee Lee, IEEE Electron Device Letters, 31, 192 (2010).

Analysis of Characterizing Feasible Design Space of LC-VCO Using SVM Classifiers

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Recently, various machine learning algorithms are being adopted by analog design tools and among them, support vector machine (SVM) classifiers are well known for their efficiency and flexibility [1]. This paper applies the C-SVM classification algorithm to characterizing the feasible design space of an LC-tank voltage controlled oscillator (LC-VCO) and investigates the effects of the learning parameters on the classification accuracy and model complexity. The circuit has 6 dimensional design space and the constraints with the startup criteria and oscillation frequency charecterize the feasible design region. The use of Gaussian kernels showed the better accuracy and complexity than that of linear kernels, as it can more easily express nonlinear boundaries for the feasible space. With Gaussian kernels, the complexity and accuracy improve with the larger penalty parameter and stronger correlation, while it demands careful determination of the correlation parmeters. This study can be further extended to the advanced design methodologies of determining the optimal learning parameters as well as leveraging the classification results to the yield-aware circuit optimization and testing problems [2].

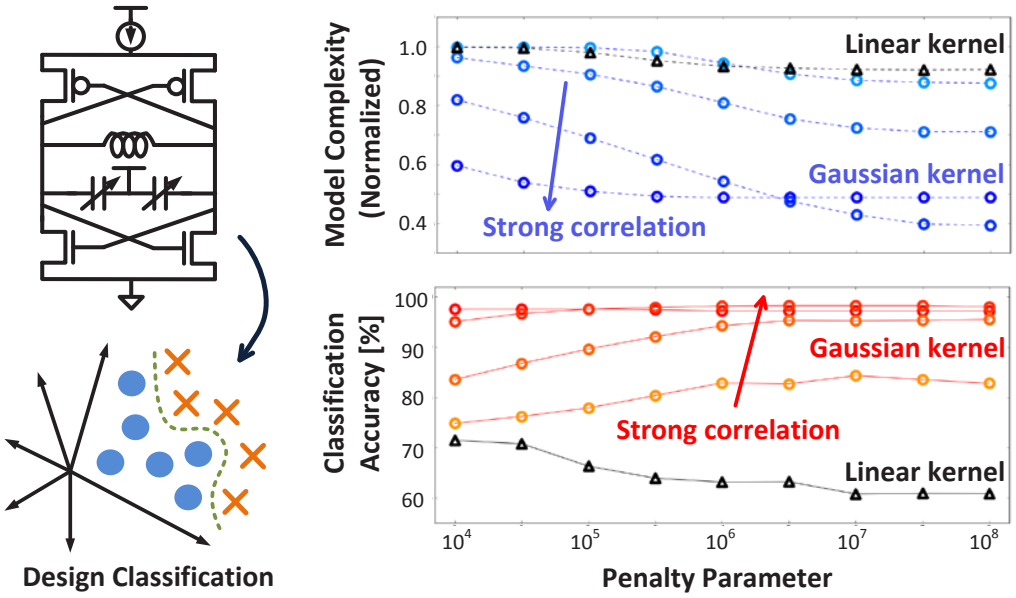

Fig 1. Complexity and accuracy of classifying feasible design space for an LC-VCO

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[2] D. Boolchandani, L. Garg, S. Khandelwal, and V. Sahula, Analog Integrated Circuits and Signal Processing. 73, 77–87 (2012).

Local Density-aware Metal Retargeting for Preventing Topological CMP Failure in Sub-28nm Node Designs

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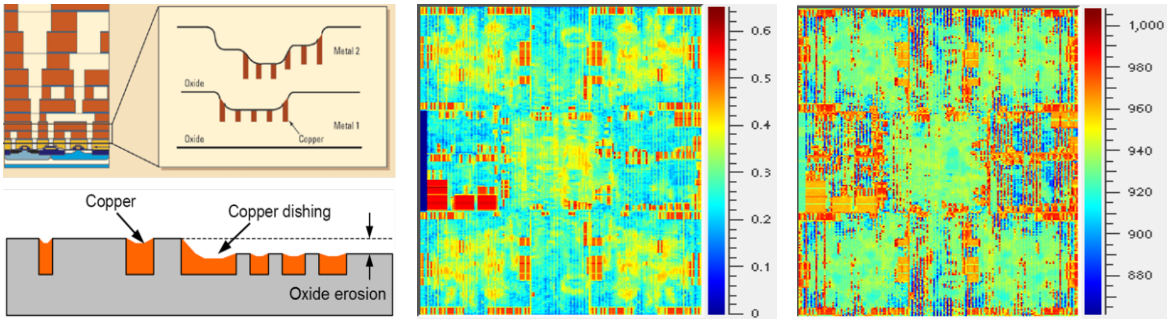
CMP (chemical-mechanical polishing) is a must-have planarization solution for back-end metallization in the past decade and a full-chip level CMP check has become a mandatory option in 28nm and bellow node sign-off. CMP varies the interconnect thickness which results in degradation of transistor characteristics, electrical shorts or increased wire resistance [1]. Since CMP heavily depends on the underlying pattern density, the insertion of dummy metal fill is commonly used into the layout to uniformly control the metal density [2]. Even though dummy metal fill with a rule-based manner is inserted after placement and routing stage, it is still hard to satisfy all density requirements since the dummy metal insertion is highly dependent upon the design rule: neighboring geometries. For avoiding all possible systematic failure due to CMP, this paper proposes a way of local density-aware metal retargeting, where the amount of metal retargeting/biasing can be differentiated by interconnect criticality in terms of timing. This approach is first to check CMP hotspots with a model-based CMP simulation, then to decide whether additional dummy can be put or not. If none of dummy metal is inserted, yet there is still CMP non-compliant, then metal retargeting is applied. The retargeting bias is varied with the space between metals, and it can be saved into look-up tables for faster referring. With this new methodology, we can prevent all CMP errors in wafer without compensating timing margin.



(a) CMP process induced variation (b) density map of a metal (c) simulation of a metal thickness

Fig 1. Process variation due do metal density and model-based full-chip CMP simulation

[1] A. Kahng, K. Samadi, and R. Topaloglu. Recent Topics in CMP-Related IC Design for Manufacturing. In Proc. Materials Research Society, Sep 2008.
[2] Yongchan Ban, et al., Analysis and Optimization of Process-Induced Electromigration on Signal Interconnects in 16nm FinFET SoC, Intl. Symp. SPIE Advanced Lithography, Feb 2014.

Reducing Routing Congestion and Chip Area by Post Placement Optimization Utilizing Redundant Inter-Cell Margin

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32-nm 및 28-nm 미세공정의 standard cell 양 끝에는, 그림 1(a)와 같이 원활한 lithography 를 위한 여백 (inter-cell margin)이 있다. 이 여백은 일부 cell pair 사이에서 불필요하며, 그림 1(b)와 같이 제거할 수 있다. 그러나, library 내의 모든 cell pair 에 대한 lithography simulation 은 runtime 상 실질적으로 불가능하다. 그 대신, cell pair 들을 경계 레이아웃 패턴에 따라 분류한 후, 각 그룹의 대표들에 대한 lithography simulation 를 통해 전체 margin 의 redundancy 를 사전에 알 수 있다[1].

면적이 작은 칩은 congestion overflow 가 높아 생기는 전선의 detour 등으로 인해 timing 조건을 만족하기가 어렵고, 이를 해결하기 위해 일반적으로 칩의 면적을 넓힌다. 본 논문에서는 redundant margin 을 이용해 congestion overflow 를 줄여, 칩의 면적을 넓히지 않고도 timing 조건을 만족하게 하여 궁극적으로 칩의 면적을 줄이고자 한다. 칩의 면적을 결정할 때는, 그림 1(c)와 같이 작은 면적에서 시작해 placement and routing (P&R) 후 timing 조건을 확인한다. 이 때 timing 을 만족하지 않으면, 칩의 면적을 넓힌 후 다시 진행한다. 본 논문에서는 P&R 후 redundant margin 을 이용해 congestion overflow 를 줄이기 위해 그림 1(d)와 같은 과정을 추가했다. 먼저 congestion 이 낮은 곳의 local placement 를 변경해 redundant margin 을 최대한 생성해 제거한 후, 그 때 생긴 whitespace 를 이용해 congestion 이 높은 곳의 cell 들을 퍼뜨렸다. 이 과정에서 placement 가 변경되었기 때문에 clock tree 를 다시 최적화하고, ECO routing 을 진행하였다. 제안한 방법을 28-nm 공정에 적용한 결과 평균 7.5% 의 칩 면적을 줄일 수 있었다.

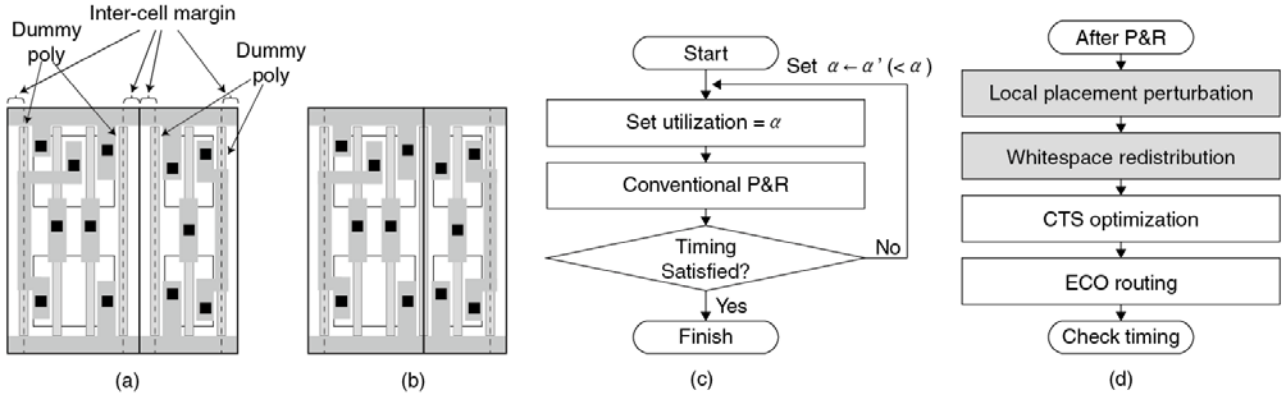

그림 1. (a) 32-nm 공정의 NAND2, INV 의 layout 과 (b) cell 사이의 inter-cell margin 을 제거한 후의 모습, 그리고 (c) 칩의 면적을 결정하는 과정과 (d) redundant margin 을 이용해 congestion overflow 를 줄이는 과정.

[1] S. Shim et al., “Lithographic defect aware placement using compact standard cells without inter-cell margin,” Proc. ASP-DAC, Jan. 2014.

Comparative Study of Capacitor-Less LDO Regulator Designs Based on Pass Transistor Types

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Low dropout (LDO) regulators are widely used in Power Management ICs(PMICs) because of its small size and low noise characteristics. LDO regulator consists of an error amplifier (EA), a feedback resistor, and a pass transistor. The pass transistor of an LDO regulator can be either an n-type or a p-type. Generally, for the same size, an n-type transistor can drive larger load current than p-type, while p-type transistor has lower dropout voltage than n-type [1]. In addition, quiescent current, PSR (Power-Supply Rejection), and transient response performances are different according to the pass transistor types. In this research, depending on the output voltage and PSR specification of LDO regulator, we perform a comparitive study of p-type and n-type pass transistor LDO designs. By deriving the analytical equations for the performance of LDOs that can be handled by Geometric Programming [2], the LDO design optimization can be performed using convex optimization. We will provide design guidelines for choosing the pass transistor types for optimal design of LDO regulators considering stability, PSR, and transient performance metrics.

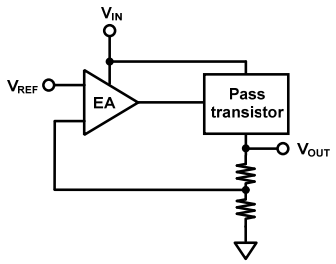

Fig. 1. Capacitor-less LDO regulator

Table 1 Optimization results

	N-type	P-type
Iq (mA)	0.829	3.2
PSR (V/V)	0.003	0.003
ΔVout (mV)	196.8	21.2

Acknowledgments : This research was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No.NRF-2014R1A2A2A01006595).

[1] Y. Li, “A NMOS Linear Voltage Regulator for Automotive Applications, ” M.S. thesis, Delft university of Technology, 2012.

[2] M. Hershenson, S. Boyd, and T. H. Lee, “Optimal design of a CMOS op-amp via geometric programming,” IEEE Trans. CAD, vol. 20, no. 1, pp. 1-21, Jan. 2001.

Simultaneous Fixing Hold Violations of Best and Worst Corners

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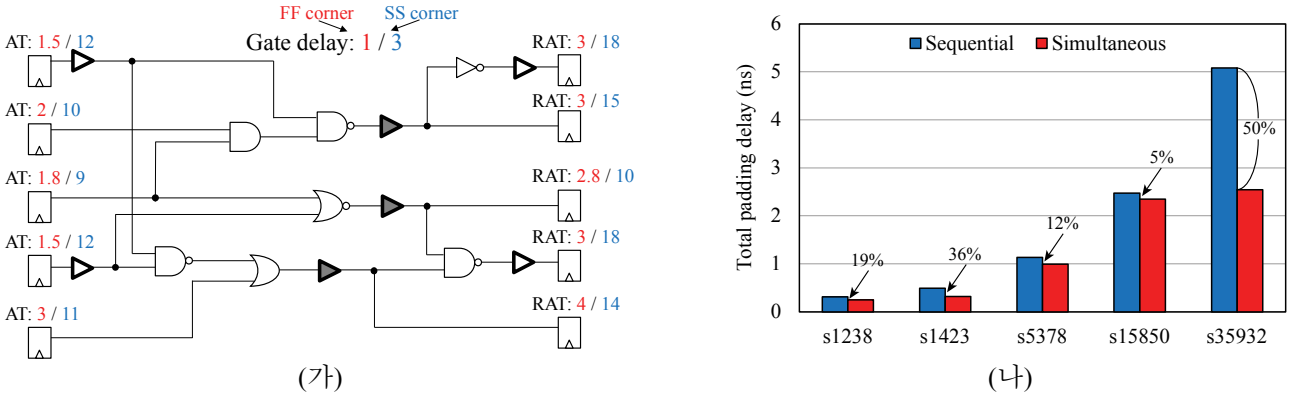
Time closure 중에 die-to-die variation이 고려돼야 하는데, 이를 위해서 현대 설계 방법은 모든 gate들의 delay 정보를 두 process corner (FF와 SS)에서 모델링한 후, 두 corner 모두에서 회로의 timing 조건을 만족하게 하는 방법을 사용하고 있다. Timing 조건은 setup time과 hold time 조건이 있는데, setup time 조건의 경우, 클럭 주기가 FF corner에서의 gate delay에 비해 충분히 크기 때문에 SS corner에서만 확인하고, 클럭 주기와 상관없는 hold time 조건은 두 corner 모두에서 확인하고 있다. Hold violation의 경우, 버퍼 삽입을 통해서 없애는데, industry에서는 한 corner에서 먼저 버퍼 삽입을 한 후, 다른 corner에서 버퍼 삽입을 하는 방법 (Sequential)을 사용하고 있다. 하지만 이 방법은 두 corner의 timing 정보를 동시에 고려하는 방법 (Simultaneous)에 비해 버퍼가 더 많이 사용된다. 그림 1(가)는 Sequential 적용 시 4개의 (흰색) 버퍼들이 필요했던 회로가 Simultaneous 적용 시 3개의 (회색) 버퍼들만 사용한 것을 보여주고 있다.

일반적인 버퍼 삽입은 두 단계로 이루어진다. 처음은 각 net에 삽입할 delay의 양을 할당하는 것이고, 다음은 할당된 delay에 맞춰 실제로 버퍼를 삽입하는 것이다. 우리는 첫 단계인 delay를 할당하는 문제를 다루는데, 이 문제의 목표는 두 corner에서 삽입되는 delay의 총량 (total padding delay)을 최소화하는 것이다. 이 문제에서 두 corner를 동시에 고려하는 경우, buffer가 삽입될 net에 FF corner delay와 SS corner delay를 동시에 할당해야 하는데, 두 delay가 한 버퍼에서 온 것이기 때문에 두 delay의 관계를 정의한 후, delay를 할당할 net과 그 할당량을 정해야 한다. 우리는 두 delay의 관계를 SS corner delay와 FF corner delay의 비[1] (SS/FF ratio)로 정의한다. SS/FF ratio는 한 test 회로 (s35932)에서 1.2~17.5까지 매우 다양하게 나타났다. 한 net의 SS/FF ratio가 17.5인 경우를 생각해보자. 우리가 그 net에서 고쳐야 할 hold violation의 양이 FF corner와 SS corner에서 각각 1과 5라면, SS corner에서 무려 12.5만큼 불필요한 delay가 삽입된다. 그래서 우리는 SS/FF ratio가 작으면서도 한 번에 많은 양의 hold violation을 고치는 net에 차례대로 delay를 할당하는 Simultaneous 방법을 제안한다. 이 방법은 각 net의 weight를 1+(SS/FF ratio)로 할당한 후, netlist를 PI쪽 부분과 PO쪽 부분으로 이등분하는 minimum weighted cut에 차례로 delay를 할당한다. 우리가 제안하는 Simultaneous는 Sequential에 비해 최대 50%만큼 total padding delay를 줄이는 결과를 보였다.



(가) (나)

그림 1. (가) Motivational example: Sequential의 결과인 4개의 흰색 버퍼들과 simultaneous의 결과인 3개의 회색 버퍼들, (나) sequential과 simultaneous의 total padding delay 비교.

[1] P. Wu et al., "On timing closure: buffer insertion for hold-violation removal," DAC, June 2014

Clock Domain Crossing Aware Sequential Clock Gating Optimization

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Recently, sequential clock gating optimization [1] has emerged as a powerful technique to aggressively reduce the dynamic power for mobile chips. In modern SoCs, multiple clocks have become common and data is frequently transferred from one clock domain to another. The sequential clock gating optimizations can use signals from across clock domain boundaries and therefore introduce new clock domain crossings (CDC) violations, which can cause catastrophic functional issues in the fabricated chip.

The state-of-art solution for this problem is to remove clock gating logic having CDC violations, which incurs severe loss of power savings and TAT increase. In this paper, as illustrated in Fig. 1, a new approach by using CDC aware sequential clock gating optimization was proposed, where CDCs were natively modeled as a cost function in the power optimization objective function. The proposed CDC aware algorithm performs fast and incremental CDC analysis, and supports different types of CDC problems extensively. As shown in Table 1, the CDC aware flow achieves register power savings of about 22.1% on average for six designs, which is significantly superior to about 6.1% average register power saving in the original flow. Furthermore, the runtime is also significantly improved in the proposed solution by minimizing the iterations between sequential clock gating optimization and CDC check.

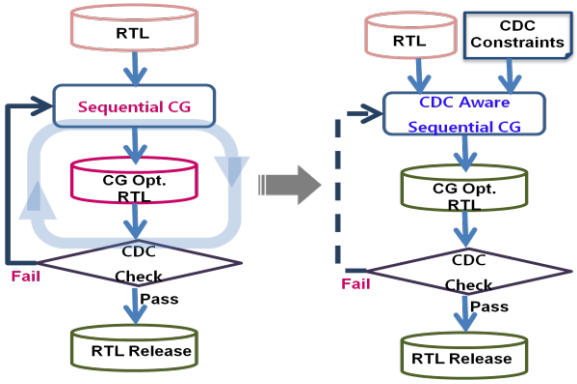

Fig 1. Original Flow vs CDC-Aware Flow

Design	Total Flops	Original Flow		Proposed Flow	
		Gated Flops	Register Power Savings	Gated Flops	Register Power Savings
Design1	204647	3028	1.2%	44876	16.8%
Design2	298757	3741	1.1%	119850	26.5%
Design3	83378	2053	2.0%	19113	22.5%
Design4	54895	2773	3.9%	15837	32.9%
Design5	121516	1470	1.8%	24224	7.3%
Design6	35492	4546	26.4%	4527	26.6%
Average	**133114**	**2935**	**6.1%**	**38071**	**22.1%**

Table 1. QoR improvement by CDC-Aware Flow

[1] S. Jairam, M. Rao, J. Srinivas, P. Vishwanath, H. Udayakumar, and J. Rao, “Clock Gating for Power Optimization in ASIC Design Cycle: Theory & Practice”, Proc. ISLPED 2008, pp. 307-308.

Extraction of Interface Trap Density by using frequency dispersion of C-V in Normally-off Gate-recessed AlGaN/GaN HFETs

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The gate-recessed metal-oxide-semiconductor (MOS) structured AlGaN/GaN hetero-structure field-effect transistor (HFET) is a promising candidate for the normally-off GaN-based HEMTs with advantages such as a thin barrier layer, low gate leakage, low gate swing, low turn on voltage and high break down voltage [1]. Here, it should be also considered that the operation of normally-off condition of GaN-based devices is important for commercializing the conventional CMOS circuit-based applications [2]. Furthermore, the interface trap density (D_{it}) should be exactly characterized especially in the gate-recessed AlGaN/GaN HFETs since they would undergo the etching damage-induced trap generation in each interfacial layer.

In this work, we demonstrated the D_{it} extraction by using the frequency-dispersion of capacitance-voltage (C-V) characteristics in the gate-recessed normally-off AlGaN/GaN HFETs [Fig. 1]. The $D_{it}(E)$ extracted by proposed method was verified to be consistent with the $D_{it}(E)$ extracted through the conventional conductance method (CM) [Fig. 1(d)]. In addition, the consistency between the proposed method and CM was also discussed in the case of the $D_{it}(E)$ of conventional MOSFETs [Fig. 1(d)]. The proposed technique is much simpler than CM because the proposed method requires only three different frequencies conditions while the CM many different frequencies.

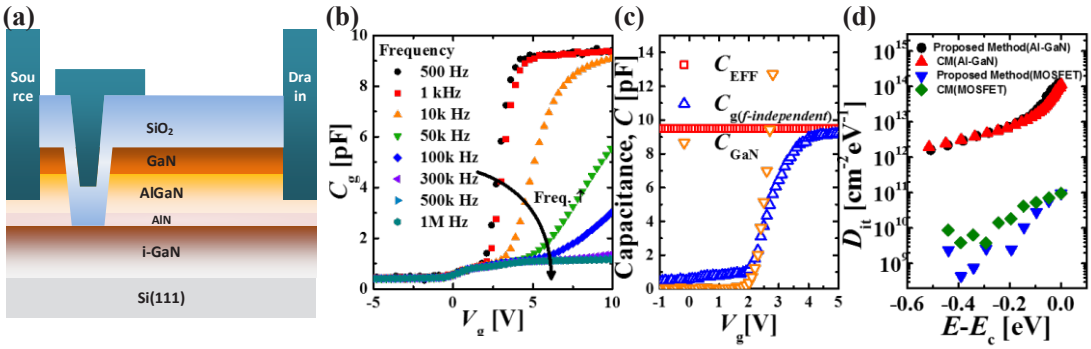

Fig. 1. (a) The structure of normally-off gate-recessed AlGaN/GaN HFETs, (b) capacitance-voltage curve with various small-signal frequencies, (c) the frequency-independent C_g, C_{eff}, and C_{GaN} as a function of V_g, (d) the comparison of D_{it}(E) between CM and proposed method in AlGaN/GaN HFETs and conventional MOSFETs.

References: [1] T. Palacios, et al., IEEE Electron Device Lett., vol. 26, p. 781 (2005). [2] J. Shi, et al., Appl. Phys. Lett., vol. 95, p. 042103 (2009).
Acknowledgment: This work was supported by BK21+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No. 22A20130000042) and in part by the Ministry of Science, ICT and Future Planning (Grant No. 2013065339).

Interfacial reactions of Si/Ti/Al/Cu Ohmic metallization on AlGaN/GaN heterostructures

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The electrical and physical characteristics of complementary metal-oxide semiconductor (CMOS)-compatible Si/Ti/Al/Cu Ohmic contacts to undoped AlGaN/GaN on Si were investigated. The Si/Ti/Al/Cu metallization exhibited specific contact resistivity of 3.5×10^{-6} Ω-cm^2 and contact resistance of 0.46 Ω mm after optimizing Si interfacial layer. HR-TEM confirmed AIN formation at the boundary of TiN and GaN after annealing at 870°C. Besides TiN formation in GaN, AlN formation is attributed to low contact resistance by lowering Schottky barrier height [1]. Without using a designated diffusion barrier in the metallization, negligible Cu was detected in the AlGaN/GaN heterostructure. Island-like $TiSi_x$ blocks formed in the metallic region is believed to act as a diffusion barrier. $TiSi_x$ blocks suppressed unnecessarily metallic reactions as well, which resulted in a smooth RMS roughness of 24nm. Low contact resistance and smooth surface morphology of Si/Ti/Al/Cu metallization using $TiSi_x$ barrier advances CMOS compatible AlGaN/GaN power transistor technologies.

[1] Luther, B. P., Mohney, S. E., Jackson, T. N., Khan, M. A., Chen, Q., & Yang, J. W., 70(1), 57-59. (1997)

AlN/GaN 이종접합구조의 성장 및 소자제작을 통한 특성 확인

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AlGaN/GaN HFETs (heterostructure field effect transistors) 는 고주파, 고전력 소자 분야에서 많은 연구가 이루어지고 있다. 특히, 최근에는 초고주파 동작을 위해 매우 짧은 채널 길이가 요구되고 있어, 이로 인해 발생할 수 있는 SCEs (short channel effects) 를 완화하기 위해 barrier의 두께를 얇게 성장하는 기술 또한 요구되고 있다. 하지만 AlGaN barrier의 두께가 너무 얇아지면 2-DEG (이차원전자가스)의 농도가 줄어드는 문제가 발생하여, 전류가 급격히 감소하게 된다. 이를 해결하기 위해 더 큰 밴드 불연속성 및 더 강한 분극 현상을 유발하는 AlN barrier가 각광받고 있으며, 이러한 특성으로 인해 barrier의 두께가 매우 얇아 지더라도 AlGaN barrier를 썼을 때보다 약 2배의 2-DEG 농도를 얻을 수 있어 고주파 소자에 매우 적합한 구조이다 [1, 2].

본 연구에서는 우수한 2DEG 특성을 가지는 AlN barrier를 성장하기 위해 indium을 계면활성제로 사용하였고, 그림 1과 같은 구조를 기반으로 성장 온도를 최적화하기 위해 750 ℃에서 1070 ℃까지 온도를 변화시켜 표 1의 결과를 확인하였다. 표 1에서 볼 수 있듯이 800 ℃에서 가장 우수한 특성이 확인 되었고, 온도가 높아질수록 2-DEG 농도가 증가하고, 이동도가 감소함을 확인할 수 있는데, 이는 표면이 거칠어 졌기 때문으로 판단된다. 단, 750 ℃와 1070 ℃에서는 표면이 매우 거칠고 2-DEG 특성이 매우 저하되었는데, 이 두 온도는 적절한 성장 조건 범위에서 벗어났기 때문으로 판단된다. 가장 우수한 2-DEG 특성을 나타낸 800 ℃의 결과에서 2-DEG 농도를 더 증가시키기 위해 AlN barrier 두께를 5 nm에서 7 nm로 증가시켜 244 ohm/sq의 면저항, 1220 $cm^2/V \cdot s$의 2-DEG 이동도 및 2.09 x 10^{13} $/cm^2$의 농도를 얻었으며, 이 기판으로 제작된 HFET의 특성을 측정한 결과, 900 mA/mm의 최대 드레인전류, 269 mS/mm의 최대 트랜스컨덕턴스, 그리고 40 GHz의 차단 주파수를 확인하였다. 이는 AlGaN/GaN 이종접합구조를 이용하여 만든 HFET의 특성과 비교하여 볼 때 고주파 소자에 매우 적절하다고 할 수 있다.

표 1. AlN barrier의 성장온도에 따른 특성 변화

Growth temperature (℃)	Sheet resistance (Ω/sq)	Electron mobility ($cm^2/V \cdot s$)	Sheet electron density ($/cm^2$)	RMS roughness (nm)
750	17520	32	1.11 x 10^{13}	2.445
800	323	1280	1.51 x 10^{13}	0.601
800 (7 nm)	244	1220	2.09 x 10^{13}	-
850	350	1110	1.61 x 10^{13}	1.097
950	632	569	1.73 x 10^{13}	1.254
1070	18020	37	0.93 x 10^{13}	3.053

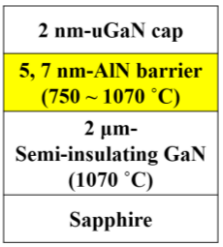

그림 1. 성장 구조도

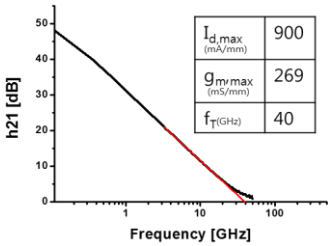

그림 2. 제작된 소자의 특성

[1] C.Y. Chang, S. J. Pearton, C. F. Lo, P. P. Chow, Appl. Phys. Lett. 94, 263505, (2009)
[2] A. Bairamis, Ch. Zervos, A. Adikimenakis, Appl. Phys. Lett, 105, 113508, (2014)

Correlation between 2-DEG mobility and crystal quality in AlGaN/GaN HEMT structure grown on 4H-SiC

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Group Ⅲ-Nitrides has a strong impact in the semiconductor industry compared to GaAs, Si, and SiC because of their potential in applications such as power devices, amplifiers, light-emitting diodes (LEDs), and photo-detectors due to its wide band-gap, high thermal stability, high saturation velocity, and high break-down voltage.[1]

GaN layer mainly grown on sapphire substrate is not suitable for high power device because sapphire substrate has low thermal conductivity and it has high defect density caused by a large lattice mismatch (GaN=16 %) between GaN layer and sapphire substrate. However, SiC substrate has excellent thermal conductivity (4.9 $W/cm^{-3}K^{-1}$) as well as low lattice mismatch with III-Nitride compounds (GaN=3.5%, AlN=1%). [2] The AlGaN/GaN high electron mobility transistor (HEMT) structures grown on SiC have superior electrical property for high power device due to two-dimensional electron gas (2DEG) which is occurred by spontaneous, piezoelectric polarization effect, and discontinuous bandgap at AlGaN/GaN interface. One of the major issues of AlGaN/GaN HEMTs which limit the performance is the presence of trap level arising from defect in GaN buffer layer. The trap level in GaN buffer layer leads to deterioration of performance in HEMTs due to electron capture at trap as shown in Fig.1. [3, 4]

In this study, first, we investigated the quality of the GaN buffer layers with different V/III ratio and growth temperature of AlN nucleation layer (NL) in AlGaN/GaN HEMT structure on 4H-SiC using metal organic chemical vapor deposition (MOCVD). Secondly, the 2-DEG Mobility of AlGaN/GaN HEMTs was observed with quality of the GaN buffer layer. Finally, we obtained GaN buffer layer of high quality by optimizing AlN NL as shown in Figure 2. These results suggest that HEMT structure will be fabricated by using these GaN buffer layer.

It was measured by Atomic force microscopy (AFM), high resolution X-ray diffractometer (HR-XRD), photoluminescence (PL), and transmission electron microscopy (TEM) to analyze the characteristics of the GaN buffer layers and the AlN NLs. Also, Electrical properties of

AlGaN/GaN HEMT structure were measured by Hall measurement. They will be discussed at the conference.

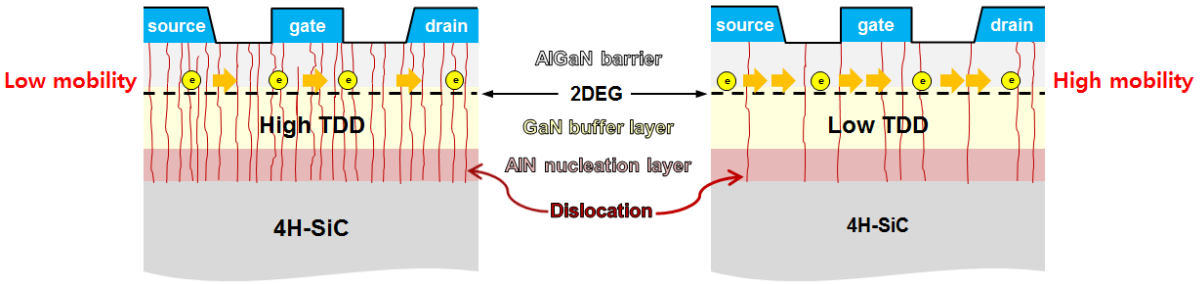

Fig 1. Schematic image of 2DEG mobility related to dislocations in AlGaN/GaN HEMT structure grown on SiC

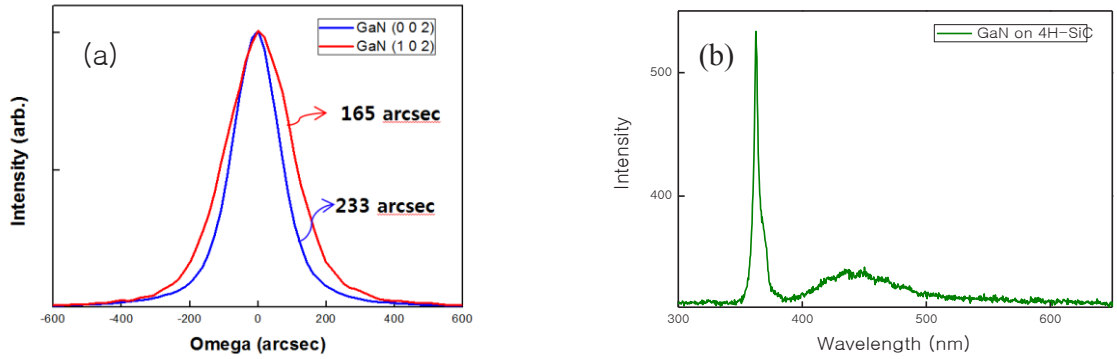

Fig 2. (a) FWHM profiles of the X-ray rocking curve (XRC) from symmetric (002) and asymmetric (102) planes and (b) room temperature PL of GaN grown on 4H-SiC

[1] S.J. Pearton et al. Mater. Sci. Eng., R. Rep., vol. R30, (2000)
[2] Raymond S. Pengelly et al, IEEE Trans. Microw. Theory Tech., VOL. 60, NO. 6, (2012).
[3] Takeshi Tanaka et al, Thin Solid Films 550, 207–211, (2014).
[4] Debdeep Jena et al Appl. Phys. Lett. 76, 1708 , (2000)

Fabrication of through-hole n-electrode for GaN buffer layer removed UV flip chip LED

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GaN-based 365 nm ultraviolet (UV) range LEDs have various applications: curing, molding, purification, deodorization and disinfection etc. However, their usage is limited by very low output power, because of the light absorption in the GaN buffer layer. The GaN buffer layer removed flip chip (BRFC) technique is one of the efficient ways to improve the output power of 365 nm UV LEDs. In this study, n-GaN is exposed by using through-hole etching technique for the fabrication of n-electrode on Si substrate bonded GaN-based 365 nm UV flip chip LEDs. GaN-based 365 nm UV LED epilayers grown on the sapphire substrate are bonded to Si substrate using Au-Sn bonding metal followed by laser lift-off. Subsequently, buffer GaN is removed by using dry etching. The indium-tin-oxide (ITO)/Al are deposited on p-GaN for the transparent ohmic contact and the optical reflection, respectively. The light emitting from the active region towards the silicon substrate could be reflected and escaped from the semiconductor through the top surface without absorption in GaN buffer layer, since GaN buffer layer is removed. Prior to the contact metal deposition, through-hole sidewall isolation is made. N-contact metals are deposited on the sidewalls of the through-hole, later through-hole is filled with Cu. The detailed through-hole etching processe as well as the electrical and optical performance of the GaN BRFC are presented.

InGaAs-on insulator transistors with Y_2O_3 buried oxide layer

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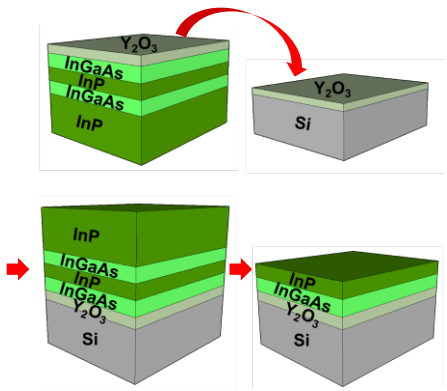
Recently, III-V semiconductors have been attracted as the possible channel material for n-channel transistors in future logic devices. To fully utilize the potential of III-V channel materials, short channel effects (SCEs) control is important. For this purpose, III-V-on insulator (III-V-OI) transistors have been actively studied [1]-[2]. Current many studies typically use Al_2O_3 buried oxide (BOX) layer due to their fairly good MOS interface. However, for ultimate equivalent oxide thickness (EOT) scaling, insulator with a higher dielectric constant than that of Al_2O_3 is required. Therefore, we have fabricated InGaAs-OI MOSFETs with Y_2O_3 as BOX layer using direct wafer bonding (DWB). Here, we have used Y_2O_3 layer due to their good MOS interfacial properties, high dielectric constant of around 16, and high bonding strength. Fig. 1 shows process flow of InGaAs-OI on Si wafer fabrication by DWB. After layer growth (InGaAs(10 nm)/InP/InGaAs/InP substrate), 10 nm-thick Y_2O_3 is deposited on both of III-V and Si by electron beam evaporation. Then, two wafers were manually bonded each other with a hand pressure. Finally, InP substrate and InGaAs etching sacrificial layer were etched by HCl and H_3PO_4-based solutions, respectively. Using InP/InGaAs-OI substrate, back gate-type transistors have been fabricated as shown in inset of Fig. 2 by source/drain metal deposition and mesa etching. Fig. 2 shows the output characteristics of fabricated transistors. It shows good transistor behaviors with clear current saturation. These results present first demonstration of InGaAs-OI transistor with Y_2O_3 BOX layer. Further electrical charateristics will be discussed.



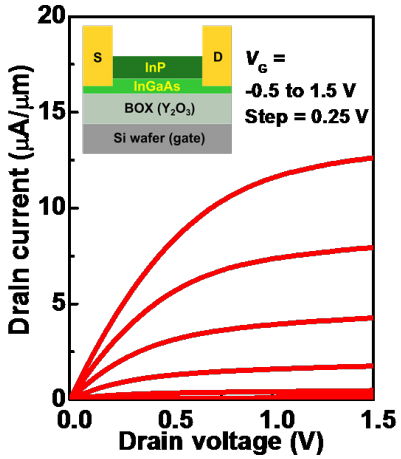


Fig 1. Process flow of InGaAs-OI on Si wafer by DWB **(left)**. Fig 2.The output characteristics of InGaAs-OI transistors **(right)**

[1] S. H. Kim *et al.*, *IEEE Trans. Electron Devices* **61**, p. 1354 (2014) [2] S. H. Kim *et al.*, *Appl. Phys. Lett.* **105**,043504 (2014) [3] N. Daix *et al.*, *APL materials* **2**, 086104 (2014)

Area-Efficient and High-Throughput Architecture for Galois/Counter Mode (GCM)

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In this paper, we present an area-efficient and high-throughtput Galois/Counter Mode (GCM) [1] core, which is optimized for IEEE 802.11ad [2] operating in the 60 GHz millimeter wave spectrum. The GCM is a mode of operation for symmetric key cryptographic block ciphers that has been adopted in 802.11ad to provide data confidentiality, authentication, integrity, and replay protection. As depicted in Fig. 1, the GCM core consists of two major function units: GCTR and GHASH. The GCTR unit performs a block cipher operation based on Advanced Encryption Standard (AES) [3], and the GHASH unit performs 128-bit parallel multiplication over Galois field. The GCM core just requires 12 clock cycles per 128-bit block for data encryption/decryption and authentication, when processing input data streams with 128-bit cipher key. To archieve the highest throughput (6,756.75 Mbps) of 802.11ad, we apply unrolling and pipelining to the AES unit, which olny uses five round logics for 10 AES rounds per 128-bit block. As a result, we have met the highest throughput at 106 MHz. Furthermore, the GCM design was described using verilog, and synthesized using a 65nm CMOS standard cell library that has 113,604 gates and occupies 163,590 um^2.

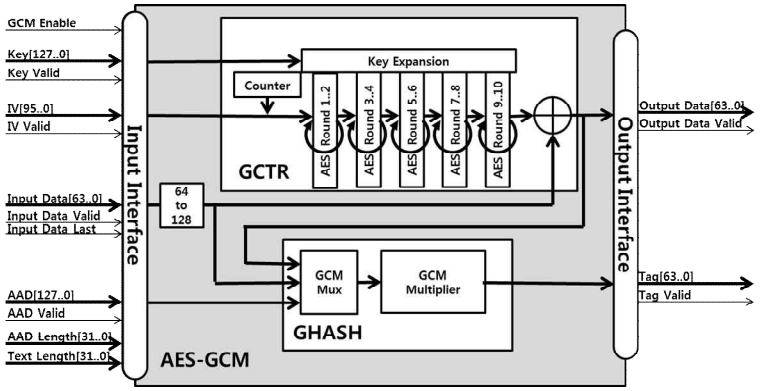

Fig. 1. The architecture of GCM core

[1] NIST Special Publication 800-38D, Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC, November (2007).
[2] IEEE Std 802.11ad, IEEE Standards for Local and Metropolitan Area Networks, December (2012).
[3] FIPS PUB 197, Advanced Encryption Standard (AES), November (2001).

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Efficient Successive-Cancellation Polar Decoder

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터키의 Arikan 교수가 2008 년 제안한 극 부호(Polar code)는 부호의 길이가 매우 길다는 가정하에 이진 입력 이산 무기억 채널에서 샤논의 채널 용량을 달성할 수 있는 최초의 부호로 최근 큰 주목을 받고 있다. 현재 극 부호의 하드웨어 연구로 가장 중요한 이슈는 낮은 하드웨어 복잡도와 높은 데이터 처리량을 가지는 것이다. 본 논문에서는 1 의 보수와 Saturation Adder 를 사용한 새로운 병합처리 연산부, 최적화된 양자화 비트를 사용한 주 프레임 연산부 및 최적화된 피드백 구조를 사용한 Successive-Cancellation 극 부호 복호기(1024,512) 구조를 제안한다.

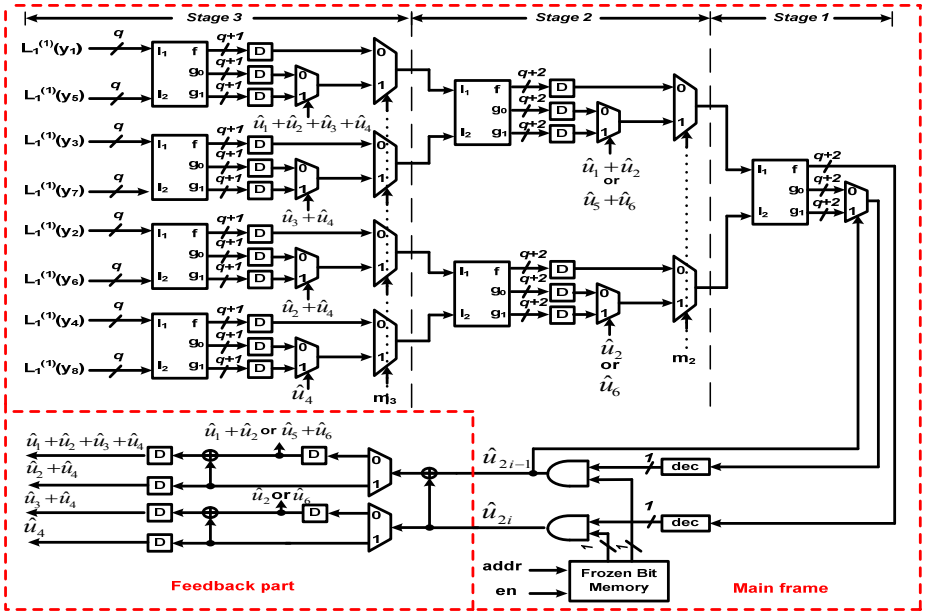

그림 1. 제안된 N=8 SC 극 부호 복호기 구조

[1] C. Zhang and K. K. Parhi, "Low-latency Sequential and Overlapped Architectures for Successive Cancellation Polar Decoder," IEEE Trans. Signal Processing, Vol. 61, no.10, pp. 2429-2411, May 2013.

[2] A. J. Raymond, W. J. Gross, "A Scalable Successive-Cancellation Decoder for Polar Codes," IEEE Trans. Signal Processing, Vol. 62, no.20, pp. 5339-5347, Oct. 2014.

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FPGA implementation of a barrel and vignetting distortion correction processor for wide-angle cameras

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광각 카메라는 넓은 화각을 갖지만 촬영된 영상에서 배럴 왜곡 및 비네팅 왜곡 현상이 발생하여 영상 품질이 열화 된다. 따라서, 왜곡된 영상을 신호 처리 과정을 통해 보정하는 과정이 필요하다. 하지만 이러한 보정 과정이 높은 연산 복잡도를 가지는 고차 다항식의 계산을 포함하기 때문에, 하드웨어 구현에 있어서 어려움이 있다. 이에 기존의 연구들은 고차 다항식의 계산을 수학적으로 변형하여 연산 복잡도를 줄였다 [1][2]. 본 논문은 위의 왜곡 현상들을 보정하는 과정에서 공통적으로 쓰이는 고차 다항식의 계산을 스플라인 (spline) 보간을 적용하여 근사화하고, 이를 기반으로 제안하는 배럴 및 비네팅 왜곡 보정 프로세서의 하드웨어 복잡도를 낮추는 방법을 제안한다. 그림 1은 제안하는 프로세서의 전체 하드웨어 구조를 보여준다. 동작 검증을 위해 그림 2의 FPGA 기반의 데모 시스템을 제작하였고, 이를 통해서 제안된 방법의 유효성을 입증하였다. 제안하는 프로세서는 10,983개의 논리 소자로 합성되었고, 43 Mpixels/s의 속도를 달성하였다.

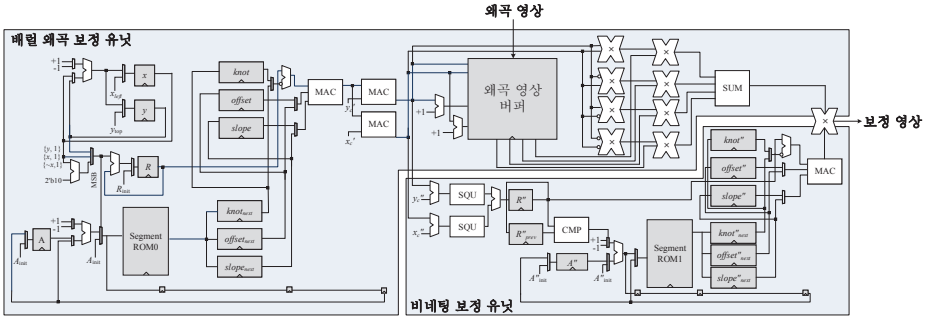

그림 1. 제안하는 배럴 및 비네팅 왜곡 보정 프로세서의 구조.

그림 2. FPGA 기반의 데모 시스템 및 보정 결과.

[1] P. Y. Chen, C. C. Huang, Y. H. Shiau, and Y. T. Chen, "A VLSI implementation of barrel distortion correction for wide-angle camera images," *IEEE Trans. Circuits & Sys. II: Express Briefs*, vol. 56, no. 1, pp. 51–55, Jan. 2009.

[2] C. Doutre and P. Nasiopoulos, "Fast vignetting correction and color matching for panoramic image stitching," in *Proc. IEEE Int. Conf. Image Process.*, pp. 79–712, Oct. 2009.

본 연구는 경기도의 경기도지역협력연구센터(GRRC) 사업[GRRC항공-2014-B04, 차세대 N-스크린서비스를 위한 스크린 협업 기술 및 스마트 카메라 기술연구]의 일환으로 수행하였음.

멀티스레드 효율을 개선한 Multi-banked Cache 설계

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최근 모바일 기기에서 지원하는 어플리케이션은 사용자를 만족시키기 위해 더욱 현실감 있는 3 차원 그래픽 효과와 다양한 고사양의 기능들을 제공하고 있다. 이러한 고사양의 기능을 지원하기 위해 최신 모바일 기기들은 AP(Application Processor)를 탑재하는 추세이다. 모바일 AP 에 탑재되는 GP-GPU 는 CPU 에서 처리하기 부담스러운 대량의 연산을 병렬처리를 통하여 가속할 수 있는 코프로세서로써 그 활용성이 더욱 더 증대되고 있다. 본 논문에서는 GP-GPU 의 성능을 향상시키기 위한 방안으로 메인 메모리에 접근하는 메모리 명령어를 효율적으로 처리하기 위한 Memory Operation System 의 구조를 제안한다. 설계한 Memory Operation System 은 그림 1 과 같이 SIMT (Single Instruction Multiple Threads)구조의 GP-GPU 의 각 코어마다 탑재되어 있는 Load/Store Unit 과 코어 외부에 존재하는 L1 데이터 캐시를 통합한 구조를 가진다. 캐시 미스 손해를 줄이기 위해 Non-blocking 캐시 구조를 적용하였으며 SIMT 구조의 특성을 고려하여 멀티 뱅크 메모리를 사용하였다.[1] 다양한 병렬처리 어플리케이션의 처리 시간을 측정하고 이를 기존의 Memory Operation System 에서의 처리시간과 비교하여 향상된 성능을 검증하였다.

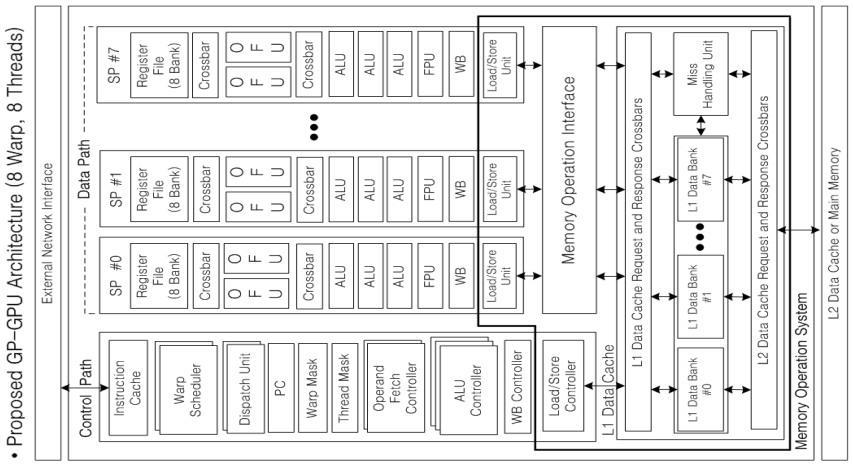

Fig 1. 제안하는 Memory Operation System 이 탑재된 GP-GPU 의 구조

[1] Ji Kim, "Microarchitectural Mechanisms to Exploit Value Structure in SIMT Architectures", School of Electrical and Conputer Engineering, Cornell University, NY, isca2013, (2013)

An Area Efficient Scaling-Free CORDIC Algorithm Using Global Shifting Sum (GSS) Method

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The Coordinate Rotation Digital Computer (CORDIC), which is a well-known iterative algorithm that can be implemented using simple shift-add operations with constant factor scaling, is widely used for hyperbolic and trigonometric functions in many digital signal processing (DSP) applications [1]. In previous works [2], constant factor scaling unit has been designed based on canonical signed digit (CSD) and common sub-expression (CSE) techniques. For the specific case of small elementary angles, "approximation" technique can be applied using $\sin 2^{-i} \approx 2^{-i}$ although the technique has a problem such as "range of angles" [3]. In this work, the scaling part is substituted by using Global Shifting Sum (GSS) method with only 1x adder and 1x barrel shifter which operate constantly at each step. According to the implementation results with Samsung 65nm process, the area of GSS CORDIC is reduced about 16% for 15 iterations, and 9% for 7 iterations with minor degradation in performance.

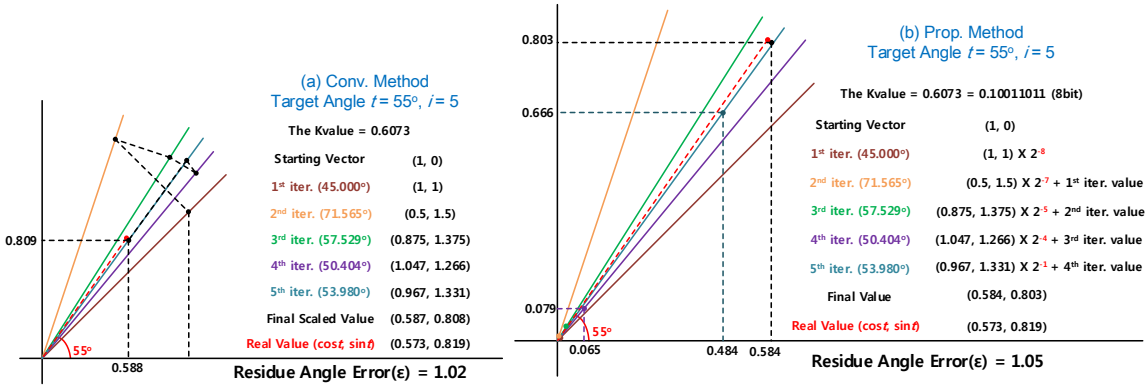

Fig. 1. Basic Principles of (a) Conventional CORDIC Algorithm and (b) Proposed GSS CORDIC Algorithm

# of iterations	Conventional (CSD+CSE)	Proposed (GSS)
8 iterations	2040	1864
16 iterations	3400	2870

Table. 1. Comparison of Gate Counts between Conv. CORDIC and GSS CORDIC in 65nm Sim.

[1] P. K. Meher, J. Valls, T. B. Juang, K. Sridharan, K. Maharatna, "50 years of CORDIC: Algorithms, Architectures, and Applications," *IEEE Trans. Circuits Syst. I,* vol. 56, pp. 1893-1907, June 2009.

[2] G. Gilbert, D. Al-Khalili, and C. Rozon, "Optimized distributed processing of scaling factor in CORDIC," *in 3rd Int. IEEE-NEWCAS Conf.,* pp. 35-38, June 2005.

[3] S. Aggarwal, P. K. Meher, and K. Khare, "Area-Time Efficient Scaling-Free CORDIC Using Generalized Micro-Rotation Selection," *IEEE Trans. Very Large Scale Integr. Syst.,* vol. 20, no. 8, August 2012.

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A MP-based BCH encoder for reducing the latency of SC based on re-encoding architecture

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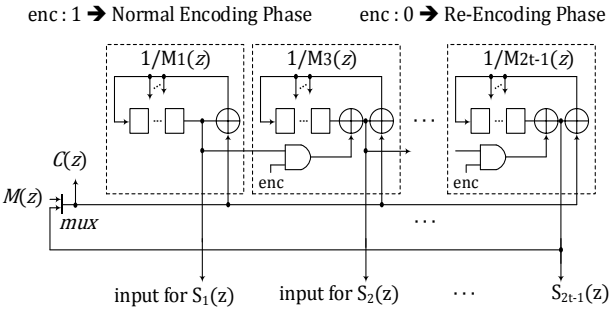
This paper presents a MP(minimal polynomial)-based Bose Chaudhuri Hocquenghem (BCH) encoder for achieving the minimum input length of Syndrome calculation (SC) through re-encoding approach. In the previous re-encodings[1][2], a remainder operation divided by long generator polynomials is implemented using linear shift feedback register (LSFR) in order to reduce the input length of SC. Considering the theoretical minimum input length for SC, MP-based BCH encoder is proposed for re-encoding by utilizing minimal polynomials as the denominators, as shown in the Fig.1. The implementation results of the proposed encoder are analyzed considering the gate counts of primitive cells provided by Samsung 65nm technology library. In the standard cell library, gate count of XOR gate is approximately 3 and that of register is 8.5 and that of AND gate is 2. As a result, latency reduction are achieved in SC module with a little HW complexity overheads on the BCH encoder. In case of BCH (8640, 8192, 32) codes of GF(2^{14}), the total latency of SC modules are reduced by 96.5% compared to the previous re-encoding approach with 3% hardware overhead on encoder architecture.



Gate count(GC)s are based on 65nm tech.		Previous re-encoding architecture	Proposed MP based re-encoding architecture
HW complexity of BCH encoder	XOR (GC:3)	448 (= mt)	479 (= mt + (t-1))
	Register (GC:8.5)	448 (= mt)	448 (= mt)
	AND (GC:2)	0	31 (= t-1)
	Total	5152	5307
Input length for SC value		448 bits	14 bits
Cycles for SC module (p_s = 16)		28	1

Fig 1. Proposed MP-based BCH encoder and implementation results based on 65nm cell library (error correcting capability t : 32, degree of Galois field extension m :14,)

[1] W. Liu, J. Rho, and W. Sung, IEEE Workshop on SIPS ’06, pp. 303–308.B. (2006).
[2] Y. Lee, H. Yoo, I. Yoo, and I.-C. Park, IEEE Trans. VLSI Syst., vol. 22, no. 5, pp. 1183–1187 (2014).

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Implementation and Analysis of Avalanche Photodiode for Single-Photon Detection

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정보화시대 이후, 정보의 중요성과 보안이 매우 중요해지면서 원천적으로 도청이 불가능한 통신방식을 사용하는 양자암호통신에 대한 연구가 많은 주목을 받고 있다 [1]. 이러한 양자암호통신은 단일광자에 암호키 정보를 실어서 전달하는 방식이기 때문에, 단일광자 수준의 약한 광신호를 검출할 수 있는 디텍터가 필수이다. 약한 광신호를 검출할 수 있는 디텍터로는 광신호를 증폭할 수 있는 디텍터인 avalanche photodiode(APD)가 많이 쓰이고 있으나, 일반 광통신에 쓰이는 APD 는 신호의 증폭률과 암전류(dark current)특성이 단일광자검출기로 사용하기에는 부적합하다. 본 연구에서는 APD 의 구조적 분석을 통하여 그림 1 과 같은 단일광자검출에 적합한 APD 를 설계하였고, 실제 소자를 metal-organic chemical vapor deposition(MOCVD)를 사용하여 제작하였다. 제작된 소자는 그림 2 와 같이 일반적인 APD[2]보다 높은 85V 에서 광신호의 증폭률이 무한대에 근접하는 geiger mode 특성을 보였으나, geiger mode 이전의 암전류가 0.1nA 수준으로 상용 APD 보다 낮았으며, 0.8A/W 의 우수한 반응도(Responsivity)를 보였다.

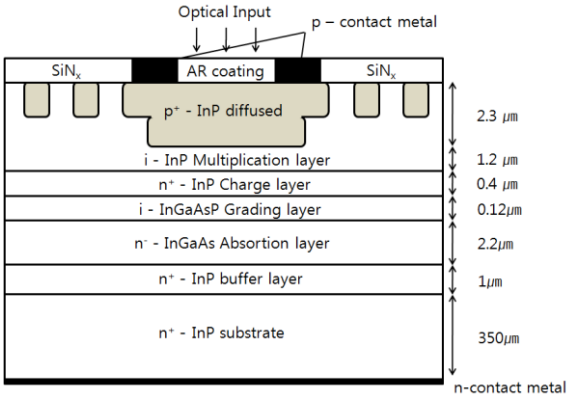

그림 1. APD 구조

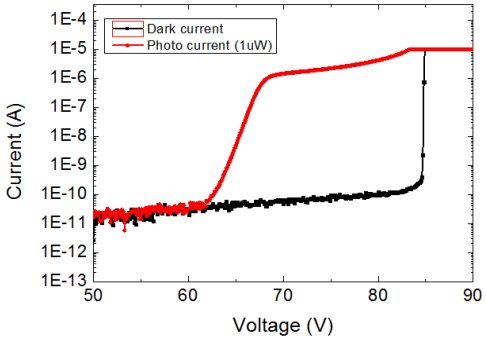

그림 2. 제작한 소자의 I-V 특성

[1] C. Gobby, Z. L. Yuan, and A. J. Shields. Appl. Phys. Lett. **84**, 3762 (2004)
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P&P QKD system using single photon detectors with dual path method

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InGaAs/InP avalanche photodiode (APD) is widely used as single photon detectors in plug and play quantum key distribution (P&P QKD) [1]. The APD uses a Geiger-mode operation with gated quenching for increase of single photon detection efficiency [2]. Altough Geiger-mode operation with gated quenching brings high detection efficiency, a background signal noise occurs simultaneously [3]. The noise degrades the performance of single photon detection, therefore it is important to suppress the noise. We have developed dual path method to reduce background signal noise. As a result, we can reduce after pulse noise that is one of the main noise sources. As shown in Fig 1, the after pulse probability using convention method was sharply increased form 1.10 % to 34.19 % at 5 % and 20% quantum efficiency. In contrast, the after pulse probabilty of dual path method is increased to 0.13 % to 12.84 % in the same quantum efficiency. We also have simulated secure rate key in QKD system. Fig 2 explains that the proposed dual path method can transmit over 100 km.

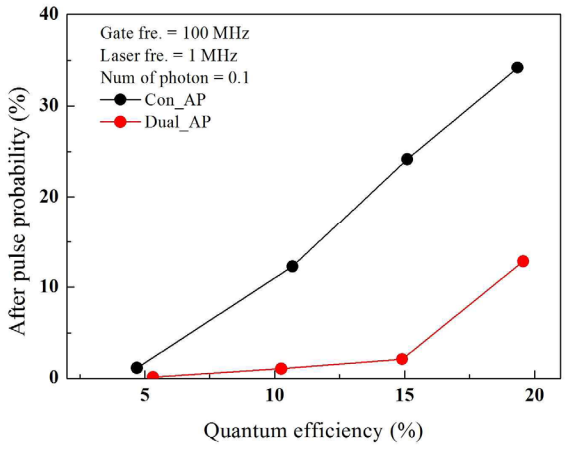

Fig 1. After pulse probability vs quantum efficiency

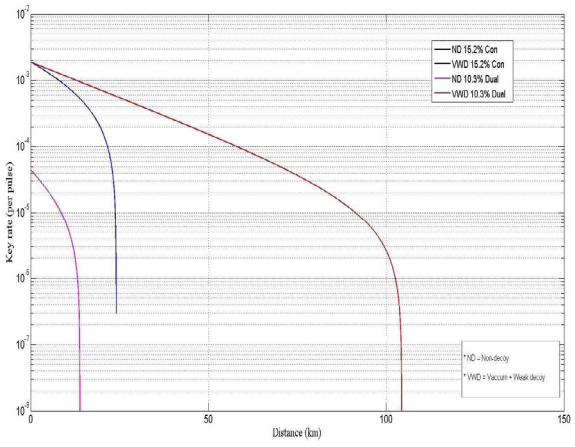

Fig 2. Quantum key rate versus distance in QKD system

[1] D. Stucki, N. Gisin, O. Guinnard, G. Ribordy, and H. Zbinden, Quantum key distribution over

67 km with a plug and play system, New. J. Phys., vol. 4, no. 41, Jul., pp. 41.1 – 41.8(2002).
[2] N. Namekata, G. Fujii , T. Honjo , H. Takesue, and S. Inoue, Differential phase shift quantum key distribution using single-photon detectors based on a sinusoidally gated InGaAs/InP avalanche photodiode, Appl. Phys. Lett., vol. 91, Jul., pp. 011112-1 – 011112-4 (2007).
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Theoretical and experimental investigation of two-photon interference with classical pulses

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Interference is one of the most interesting phenomena in nature for many physicists. In many experimental demonstrations with optical pulses, classical and quantum interference are usually measured when pulses have temporal overlap at a BS [1]. It often leads to a common misconception that classical and/or quantum interference requires the optical pulses to be temporally overlapping. However, it has been shown that quantum interference can be occurred without temporal overlapping between optical pulses [2].

In classical physics, however, the superposition of probability amplitudes and Feynman diagrams are not applicable. Instead, the classical electromagnetic waves superposition theory should be employed to describe the interference. It is easy to think that there would be no interference between two temporally non-overlapping optical pulses because it seems that the electromagnetic waves do not exist without an optical pulse. Counter-intuitively, however, the classical interference does not require the temporal overlap of optical pulses [3].

In this presentation, I will explore the two-photon interference between temporally non-overlapping classical pulses.

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[3] L. de Broglie, and J.A.E. Silva, Phys. Rev. **172**, 1284 (1968).

Electrical Characteristics of Electrolyte-Oxide-Silicon (EOS) capacitor with the gold nanoparticle (AuNPs) attachments

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The charge amplification method is newly proposed in order to enhance the sensitivity of ISFET (ion-sensitive field-effect transistor) in biosensing application. The eletrolyte-oxide-silicon (EOS) capacitor is used to analyze the properties of dielectric membrane on biologically sensitive field effect transistors (bioFETs) [1]. The charge of gold nanoparticles (AuNPs) on EOS capacitor was analyzed using C-V (capacitacne-voltage) measurements. The AuNP was attached to the oxide surface with the linker molecule of (3-Mercaptopropyl)trimethoxysilane (MPTMS). Using the reduction agent (mixture of 0.01% $HAuCl_4$ and 0.4 mM $NH_2OH \cdot HCl$), the precursors were reduced on the AuNP surface to increase the size of AuNPs [2]. The C-V characteristics were measured after the reduction. When the AuNPs were attached on the oxide surface, the negative charges of $-OH_2^-$ on the surface were partially neutralized as the MPTMS reacted with it and it cause the C-V curve shift to the left direction. As the reduction reaction continues, the C-V curve shifts to the right consecutively due to increase of the amount of negative charges of the AuNPs attached on the surface, which can be used to amplify the shift of threshold voltage and/or the drain current in ISFETs with various biodetection. Therefore the proposed method is very promising to improve the sensitivity of bioFETs.

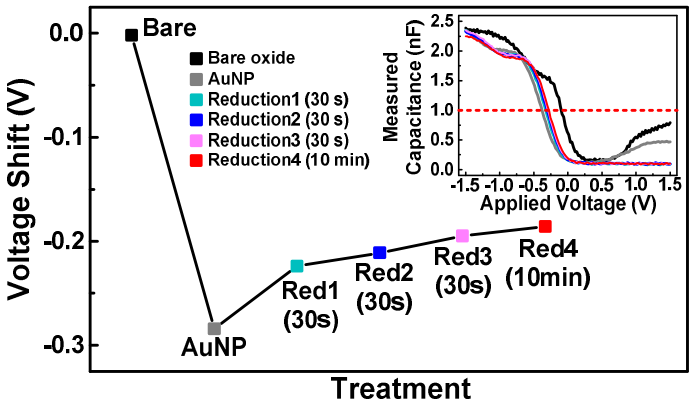

Fig 1. C-V curve of EOS capacitor with the attachment of AuNPs using the reduction treatment

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Analysis and Experiment of Interface Delamination Based BCB Cap Transfer Packaging of RF-MEMS Switch on MMIC

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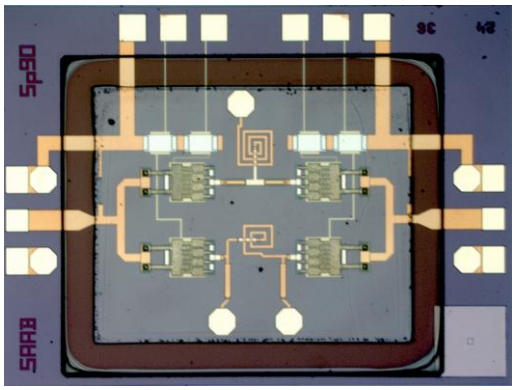
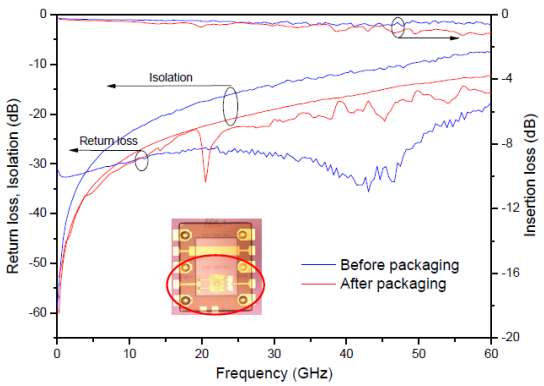
Wafer-level packaging is one of the critical technology for RF MEMS switches, especially for high frequency devices [1-2]. Capping material should have mininmal effect to the packaged devices. This paper presents a BCB cap transfer packaging of MEMS switches integrated with MMIC. To overcome a existing process compatibility issues between MMIC process and packaging process, a BCB cap transfer technique having maximum process temperature of 250 °C has been developed. A FEM modelling is also established to analyze the behavior oft he transfer process. A conventional 100 μm-thick MMIC wafer having RF-MEMS swithces is successfully packaged with help of temporary support wafer of 680 μm-thick GaAs support. The achieved success rate of BCB caps transfer is approximately 80 %. The implemented BCB caps have the height of 28 μm and the cavity of 13 μm for the housing of MEMS switches. The BCB cap packaging effect to microstrip line has been investigated through the S-parameters measurement before and after the packaging. Also, the packaged MEMS switch shows the insertion loss of 0.7 dB, the return loss of 25 dB and the isolation of 18 dB at 30 GHz.



(a) BCB capped RF-MEMS switches on MMIC



(b) S-parameter measurement of RF-MEMS switch before and after packaging

Fig 1. Packaging results and its characterization

[1] S. Seok, N. Rolland and P. A. Rolland,"Packaging methodology for RF devices using a BCB membrane transfer technique", Journal of Micromechanics and Microengineering, vol. 16, No.11, Nov. 2006, pp.2384-2388.

[2] S. Seok, N. Rolland and P. -A. Rolland, "Design, Fabrication and Measurement of BCB Polymer Zero-Level Packaging for Millimeter-Wave Applications", IEEE Transaction on Microwave Theory and Techniques, May 2007, pp.1040-1045.

Silicon bulk micromachined piezoelectric energy harvester using Interdigital shaped cantilevers

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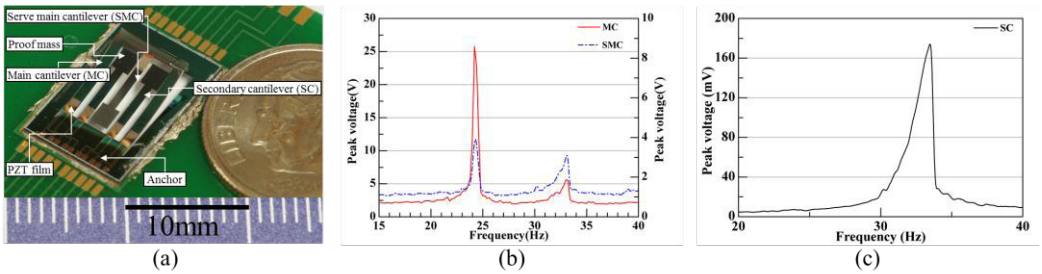
Recently, in order to generate electric energy from vibration with wideband frequency, several methods such as comprising an array of the cantilevers with different dimension and employing 2-degree-of-freedom (2DOF) systems are presented [1-2]. In this work, silicon bulk micromachined piezoelectric energy harvester was devloped by using interdigital shaped cantilevers to have multi degree-of-freedom (m-DOF) as shown in Fig 1 (a).

The fabrication process was started with low temperature oxide and SiNx on SOI (10μm/1μm/560μm) wafer. A Ti/Pt/Pb(Zr0.52Ti0.48)O3 (PZT)/Pt layer was deposited to form the bottom electrode, piezoelectric layer and top electrode. The Pt and Ti/Pt electrodes were patterned by dry etching technique, and the PZT thin film was wet etched. In order to form the cantilever and the proof mass, the KOH etchant was used to etch silicon (handle layer), and to release the membrane, the RIE etching was used to remove buried oxide in SOI wafer.

Fig 1 (a) shows the photograph of the fabricated device. The fabricated device was characterized by applying periodic sinusoids of different frequencies at 0.3g of low acceleration using vibration exciter. Fig 1 (b) shows the peak output voltage of the fabricated MC and SMC. 25.7mV and 5.5mV were generated at 24.2Hz and 33Hz by MC, and 4mV, 3.3mV obtained at 24.2Hz and 33.2Hz by SMC, respectively. Fig 1 (c) shows the output peak voltage of the fabricated SC. 182mV was generated at 33.6Hz of resonance frequency by SC.



(a) (b) (c)

Fig 1. Fabricated device and its output voltages: (a) photograph of the proposed energy harvester, (b) output voltages of the MC and SMC, (c) output voltage of the SC

[1] M. Ferrari, V. Ferrari, M. Guizzetti, D. Marioli and A. Taroni, Sensors and Actuators A: Physical. 142, 1 (2008)

[2] H. Wu, L. Tang, Y. Yang and C. K. Soh, Japanese Journal of Applied Physics, 51, 4R (2012)

Self-Powered Flexible Electronic Systems

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This seminar introduces three recent progresses that can extend the application of self-powered flexible inorganic electronics. The first part will introduce self-powered flexible piezoelectric energy harvesting technology. Energy harvesting technologies converting external sources (such as vibration and bio-mechanical energy) into electrical energy is recently a highly demanding issue. The high performance flexible thin film nanogenerator was fabricated by transferring the BaTiO3 thin film from bulk substrates. Second, we report the nanocomposite generator (NCG) for achieving a simple, low-cost, and large area fabrication based on BaTiO3 (or PZT) nanoparticles and graphitic carbons (CNT or RGO). The second part will introduce flexible electronics including memory and large scale integration (LSI). Flexible memory is an essential part of electronics for data processing, storage, and radio frequency (RF) communication. To fabricate a fully functional flexible memory, we integrated flexible single crystal silicon transistors with an amorphous titanium oxide (a-TiO2) based memristor to control the logic state of memory. The third part will discuss the flexible GaN LED for implantable biomedical applications. Inorganic III-V light emitting diodes (LEDs) have superior characteristics, such as long-term stability, high efficiency, and strong brightness. Our flexible GaN thin film LED enable the dramatic extension of not only consumer electronic applications but also the biosensing scale. A water-resist and a biocompatible PTFE-coated flexible LED biosensor can detect PSA at a detection limit of 1 ng/mL. Finally, we will discuss laser material interaction for flexible applications. Laser technology is extremely important for future flexible electronics since it can adopt high temperature process on plastics, which is essential for high performance electronics, due to ultra-short pulse duration. (e.g. LTPS process over 1000 °C) We will explore our new exciting results of this field from both material and device perspective.

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On-glass and flexible GaN light emitting diodes

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Recently, achieving large sized and flexible light-emitting elements is the most noticeable demand for lighting or displays. Here, we demonstrate on-glass and flexible GaN light emitting diodes (LEDs, Figure 1) [1, 2]. The former yielded improved luminance of > 10000 cd/m^2 at the peak wavelength of 494 nm via control of GaN crystallinity and p-GaN formation. The latter had luminance of 595 cd/m^2 at a bending radius of ~ 2 mm by accurately weakening the LT-GaN/Ti hetero-interface in the on-glass LEDs and embedding the GaN stack arrays into ultrathin, flexible substrates. Furthermore, we show that the proposed LED structure is favourable for a high stretchability that is potentially applicable to large sizes.

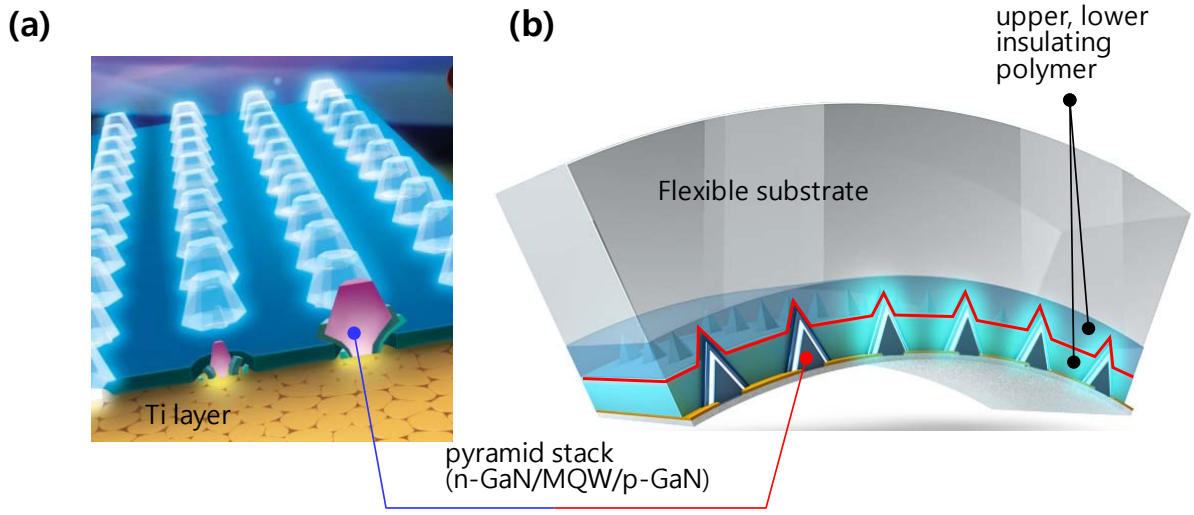

Fig 1. Schematic diagram of (a) on-glass and (b) flexible GaN-based LEDs

[1] J. H. Choi, A. Zoulkarneev, S. I. Kim, C. W. Baik, M. H. Yang, S. S. Park, H. Suh, U. J. Kim, H. B. Son, J. S. Lee, M. Kim, J. M. Kim, K. Kim, Nat. Photonics 5, 763 (2011).
[2] J. H. Choi, E. H. Cho, Y. S. Lee, M.-B. Shim, H. Y. Ahn, C.-W. Baik, E. H. Lee, K. Kim, T.-H. Kim, S. Kim, K.-S. Cho, J. Yoon, M. Kim, and S. Hwang, Adv. Opt. Mater. 2, 267 (2014).

Asymmetric sodium-ion pseudocapacitors based on ultra-thin hollow carbon nanospheres

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Recently, Na ion batteries (NIBs) have been considered as the promising alternative of LIBs in that the underlying electrochemical reaction is similar to that of LIBs but is based on the unlimited resources of Na. Nevertheless, the use of bigger and heavier Na ion as a charge carrier in NIBs inevitably led to the low energy and low power compared to LIBs, which have been a major obstacle to the widespread usages of NIBs. In this study, ultra-thin hollow carbon nanospheres (UTH-CNs) were fabricated for a use as anodes of asymmetric sodium-ion pseudocapacitors. The extremely high aspect ratio of hollow carbon (sphere radius vs. wall thickness; 300 nm/3 nm) shows that the pseudocapacitive sodium-ion storage is as fast as lithium-ion storages in spite of the relatively larger size of the sodium-ion. The asymmetric pseudocapacitors using the UTH-CNs as an anode demonstrated their superior electrochemical performances with high energy, power and stable cycles over repetitive 1,000 charge/discharge. The results of a specific energy of 43 Wh kg^{-1} with a power density of 10 kW kg^{-1} are the highest value reported thus far for asymmetric sodium-ion storage.

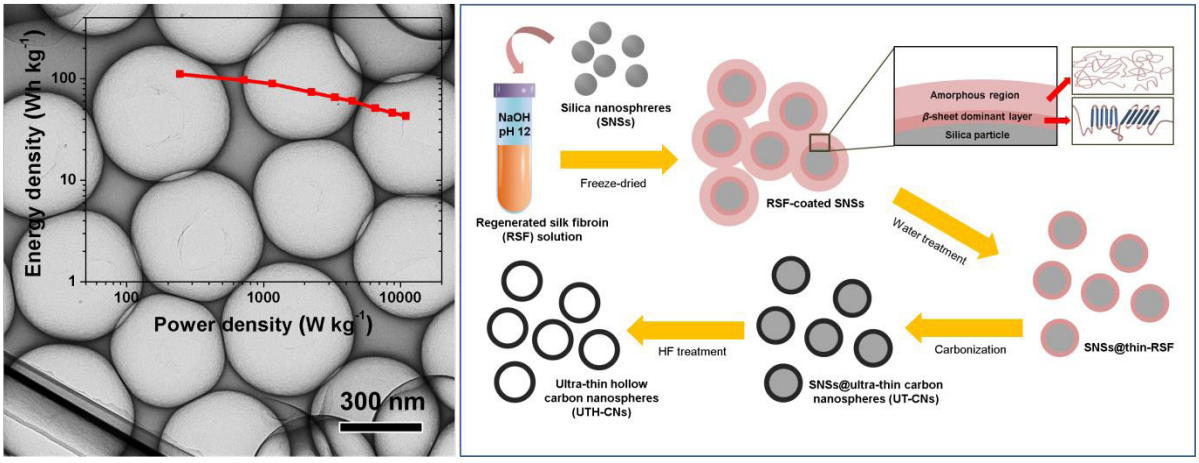

Fig 1. (left) TEM image of UTH-CNs and inset of Ragone plot. (right) Schematic diagram showing the fabrication process for the UTH-CNs.

Defect formation in Cu(In,Ga)Se_2 solar cells by proton irradiation

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Cu(In,Ga)Se_2 (CIGS) solar cells have been shown to have a higher radiation resistance than other types of solar cells such as Si and III-V compound, making them suitable for space application. Here we study the effects of proton irradiation on the build-up and decay of sub-bandgap defects. We employed 10 MeV proton beam—which is much higher than the typical range of energies used in the previous irradiation studies reported in the literature—with varying doses, from 10^9 to 10^{12} cm^{-2}. Photoluminescence (PL) analysis revealed three major peaks at 1.02, 1.13, and 1.19 eV from the CIGS. After the irradiation, the 1.02 eV and 1.13 eV peaks intensity decrease while the 1.19 eV peak intensifies. The fact that 1.19 eV peak is already present, although weak, before the irradiation suggests that the proton irradiation does not create a new type of defects but instead multiplies the number of the already-exisiting defects. The origin of these peaks and their implication on electrical properties will be discussed.

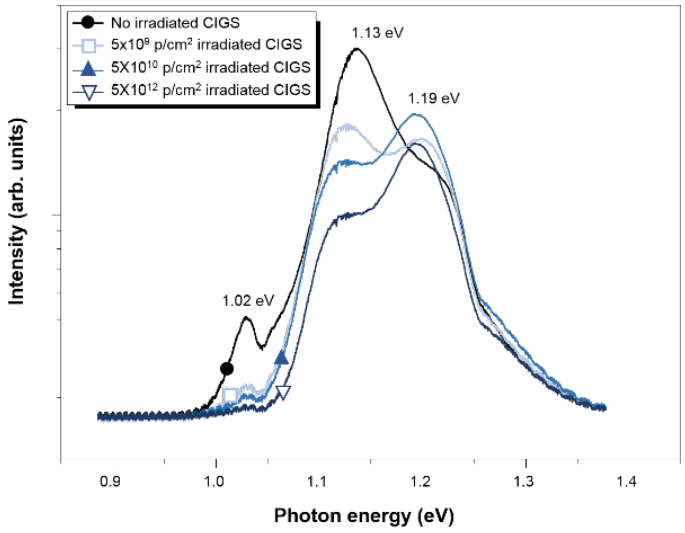

Fig 1. PL spectra (293 K) of proton irradiated CIGS thin film on Mo-covered glass substrate

Ni Barrier Effect on Electromigration Reliability of Cu/Sn-Ag Microbump

Young-Bae Park[1*], Gyu-Tae Park[1], Byeong-Rok Lee[1], Ho-Young Son[2], Min-Suk Suh[2], Nam-Seog Kim[2]

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[2]*SK Hynix Inc., Icheon, 467-701, Korea*
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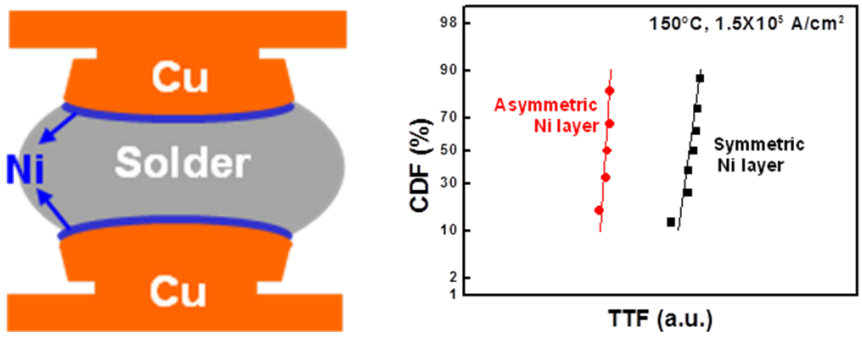
Recently, three-dimensional (3D) stacked multi-chip package technology has been developed for use in the through silicon via (TSV) process[1]. TSV integration is stacked using micro-bumps and through Si via. Micro-bump is one of the key enabling technologies for 3D integration where high I/O count devices and interposers are interconnected with hundreds of thousands of micro-bumps[2]. There are several important issues such as current crowding, joule heating, and electromigration(EM). And excessive intermetallic compound (IMC) growth and Kirkendall void formation in micro-bump can degrade the mechanical reliability of solder joints. Therefore, it is essential to understand the fundamental growth mechanisms of IMC and Kirkendall void. In this study, the electrical reliability of Cu/Sn-Ag microbumps under current stressing conditions according to Ni barrier were investigated using in-situ scanning electron microscopy chamber at 150°C with current density of $1.5x10^5 A/cm^2$.



(a) **(b)**

Fig 1. (a) Schematic diagram of Cu/Ni/Sn-Ag microbump and (b) Ni barrier effect on lognormal plots of TTF of microbump at 150°C with $1.5x10^5 A/cm^2$.

[1] E. J. Jang, J. W. Kim, B. Kim, T. Matthias, and Y. B. Park: Met. Mater. Int. 17, 105 (2011).
[2] Hsiao-Yun Chen, Da-Yuan Shih, Cheng-Chang Wei, Chih-Hang Tung, Yi-Li Hsiao, Douglas Cheng-Hua Yu, Yu-Chun Liang and Chih Chen, Proc. 63th Electronic Components and Technology Conference 2013, 49 (2013).

EMI issues in pseudo-differential signaling for SDRAM interface

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최근 스마트폰 등에서 여러 개의 전자소자를 매우 작은 면적 안에 위치시킴에 따라, 전자기파간섭(EMI)이 심각한 문제로 대두되었다. 예를 들어, USB3.0 커넥터에 의한 EMI 가 와이파이 무선 마우스 동작을 방해하는 경우가 발생하였다. 또한, 스마트폰에 내장되는 SDRAM 에 의한 EMI 를 감소시키기 위해 은박지(알루미늄 포일)등으로 SDRAM 을 감싸는 경우도 있다. 현재 SDRAM 과 메모리 컨트롤러 사이의 고속 데이터 인터페이스는 데이터 전송속도가 1.6Gbps 인 single-ended DDR4 표준이 쓰이기 시작하였다. Single-ended 신호전송방식은 차동(differential) 신호전송방식에 비해 EMI 를 크게 발생시킨다. 이를 줄이기 위해 최근에 SDRAM 인터페이스에서 balanced code 를 사용하는 pseudo-differential 신호전송방식이 제안되었다[1]. 본 논문에서는 pseudo-differential 신호전송방식의 EMI 를 측정하고, 이를 single-ended 와 차동 신호전송방식의 EMI 와 비교하였다. 이를 위해, 두 개의 평행한 3 인치 FR4 마이크로스트립 라인을 통하여 3GHz 클락신호를 전송하고(그림 1), H 필드를 측정하였다(그림 2). Pseudo-differential 신호전송방식에서는 두 개의 마이크로스트립 라인에 차동 클락신호를 인가하고(time delay = 0), 두 클락신호의 지연시간(time delay)를 -0.5 T_{period} 에서 +0.5T_{period} 까지 변화시켰다. 지연시간차이가 0 일 때는 차동 신호전송방식과 EMI 가 동일하고, 지연시간차이가 0.5T_{period} 일 때는 single-ended 전송방식보다 EMI 가 2 배가 되었다.

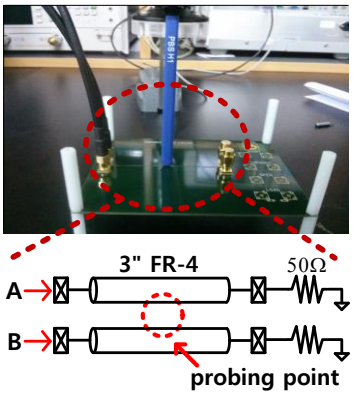

그림1. 측정 셋업

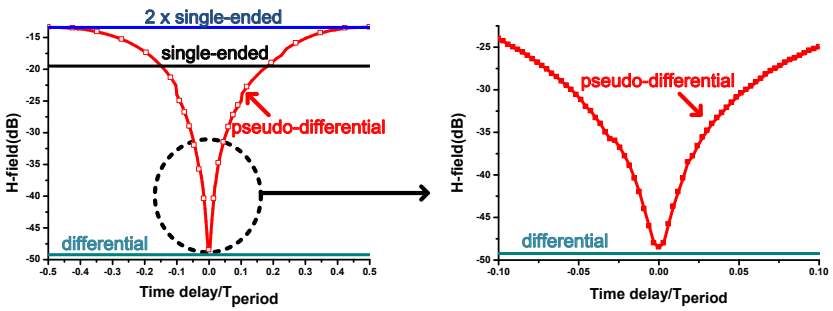

그림2. 측정 결과

[1] A. Singh, D. Carnelli, and A. Falay *et al.*, "A Pin- and Power-Efficient Low-Latency 8-to-12Gb/s/wire 8b8w-Coded SerDes Link for High-Loss Channels in 40nm Technology Anant," *in Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2014, pp. 442-443.

Pre-applied underfill film solution for the productivity of micro-bump interconnection

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Low-k dielectric devices are becoming more prominent in semiconductor packages. These fragile layers require next generation material solutions to provide support and improve reliability. Pre-applied underfill films are used in electronic packages to provide support of fragile, thin, fine pitch TSV and Cu pillar devices. There are two primary functions of the material: complete filling of the gap between two surfaces (die to die or die to substrate) and provide bump support during joint formation. In order to compete with existing liquid underfills, films should provide robust processing in as short a time as possible. Films also ease handling and processing to improve fillet, flow, and bondline control.

In this paper, a novel fast-curing film is presented. Henkel pre-applied underfill films feature a fast cure chemistry that enables a fast bonding profile of 0.9sec from contact to release while forming a reliable interconnect.

단결정 및 다결정 태양광 모듈 Package 의 Bypass Diode 동작 Point 에 관한 연구

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태양광 발전은 태양전지를 보호하기 위해 유리와 EVA, 외부의 습기 침투를 막기 위한 Back sheet로 구성하여 Package된 형태로 발전하게 된다. 이것을 태양광 모듈 Package 라고 하며, 태양전지를 온도, 습기, 바람 등에서 부식 및 파손을 방지하여 원활히 발전 할 수 있도록 보호하기 위함에 목적이 있다.

이렇게 Package된 태양광 발전은 PN 구조를 응용하여 빛을 받으면 전기를 발생하게 된다. 하지만 태양전지는 낮은 전압의 한계로 인해 수십 장을 직렬 연결된 태양전지 모듈 Package의 형태로 사용하게 되는데, 태양광 발전은 직렬 구조로 구성되어 Micro Crack, 태양전지 간의 Miss Match, Shading와 같은 상황에 발전 성능 저하와 내구성능에 영향을 받게 된다.[1,2] 이러한 경우에 한 개의 태양전지의 출력저하 뿐만 아니라 전체 String의 발전이 저하되게 되고, 이때 Bypass Diode가 동작하게 되는 것이다.[3,4]

최근 태양광 발전의 Package는 출력을 높이기 위한 연구와 함께 shading에 의한 Bypass Diode turn on에 대한 연구가 활발히 이루어지고 있다. [4,5,6] 하지만 대부분의 연구는 Shading 정도에 의한 출력저하를 시뮬레이션 하는 연구를 주로 하고 있으며, Shading과 저항의 관계, Bypass Diode의 유무에 대한 출력을 연구 하고 있는 실정이다. [5,7,8]

바이패스 다이오드는 태양광 모듈 Package의 직렬 연결된 String에 병렬로 연결되어 이상적으로는 −0.6[V]일 때 동작하게 되는데, 바이패스 다이오드의 동작은 태양전지의 역전압 특성과도 상관이 있다. 최근 태양전지가 고효율화 되어 감에 따라 직렬저항(Rs)과 병렬저항(Rsh)의 특성이 향상되었으며, 이와 함께 역전압 특성도 달라졌다.

본 논문에서는 결정질 태양전지에 따른 바이패스 다이오드의 동작 시점에 대한 연구를 진행하였으며, 고효율 단결정 태양전지와 다결정 태양전지의 역전압 특성을 비교 하였고, 실험에 필요한 특수 모듈을 제작하여 실험을 진행하였다.

실험은 특수 제작된 태양광 모듈Package의 태양전지 한 장에 음영 비율을 5[%]씩 증가 시키면서 바이패스 다이오드의 동작시점을 확인 하였다. 또한 바이패스 다이오드의 동

작은 역 바이어스뿐만 아니라 순 바이어스에 영향을 받기 때문에 String의 개수를 늘려가면서 경향성을 확인 하였다.

현재 태양광 업계에서 태양전지를 Package 공정으로 진행 할 때, 단결정과 다결정 태양전지의 Sorting기준은 같다. 하지만 태양전지의 효율이 좋아지면서 다결정 태양전지에 비해 단결정 태양전지는 약간의 음영에도 바이패스 다이오드는 동작하므로 태양전지간의 Miss match가 발생할 경우 단결정 태양광 모듈 Package의 바이패스 다이오드는 동작 할 것이다. 이에 따라 본 논문에서는 태양전지의 종류에 따라 각각의 Isc를 기준으로 한 Sorting이 필요함을 실험을 통하여 제시하는 바이다.

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[2] 김승태, 박지홍, 강기환, 화이티루, 안형근, 유권종, 한득영 "태양전지 모듈의 바이패스 다이오드 동작 특성 분석" Journal of the Korean Institute of Electrical and Electronic Material Engineers, Vol 21, No. 1, pp. 12-27, January 2008.
[3] M.C. Alonso-Garcia, J.M. Ruiz, F. Chenlo "Experimental study of mismatch and shading effects in the I-V characteristic of a photovoltaic module. Solar Energy Materials & Solar Cells 90 (2006) pp. 329-340
[4] S. Silvestre, A. Boronat, A.Chouder "Study of bypass diodes configuration on PV modules" Applied Energy 86 (2006) pp. 1632-1640.
[5] M.C. Alonso-Garcia, J.M. Ruiz, W. Herrmann "Computer Simulation of shading effects in photovoltaic arrays." Renewable Energy 31 (2006) pp. 1986-1993
[6] F. Martinez-Moreno, J. Munoz, E. Lorenzo "Experimental model to estimate shading losses on PV arrays" Solar Energy Mateials & Solar Cells 94 (2010) pp. 2298-2303
[7] W.Herrmann, W. Wiesner, W. Vaaben "Hot spot investigations on PV module - New concepts for a test standard and consequences for module design with respect to bypass diode" 26th PVSC; Sept. 30_Oct.3, 1997; Anaheim, CA
[8] I. Caluianu, G. Notton, Iolanda Colda, S. Caluianu and A. Damian "Photovoltaic Energy Generation under Partially Shading Conditions" Electromotion 2009-EPE chapter 'electric drives joint symposium, 1-3 July 2009, Lille, France. pp.1-6.

The Patterned Metal Plate(PMP) for Effective High Power LED Package

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High-power LED(고전력 발광소자)의 효율적인 열전달을 위해 COB(Chip on Board)형태의 구조들이 개발되었으며[1]-[2], 최근 매우 높은 열전도도를 가지는 알루미늄 (aluminum)과 구리(Copper) 소재의 요철금속판(Patterned Metal Plate, PMP)이 각각 개발되었다. <그림-1>은 현재 널리 사용되는 Metal PCB의 단면구조도로, 열전도도가 낮은 에폭시(epoxy) 성분의 절연층으로 인해 솔더(SnPb)로 SMT(Surface Mount Technology)된 High-power LED에서 발산(發散)되는 열이 금속기판(Metal Plate)으로 잘 전달하지 못하는 반면, <그림-2>와 같이 절연층 일부분을 열전도도가 높은 금속기판(Metal Plate)으로 대치함으로써 열흐름(Heat-flow)을 개선할 수 있다. <그림-3>은 개발된 구리(Copper) 소재의 PMP 단면사진이며, <그림-4>는 High-power LED가 SMT된 구리소재의 PMP 정면사진이다. <표-1>은 Metal PCB 및 알루미늄과 구리소재 PMP에 대해 측정된 열전도도 및 Lumens(주)의 High-power LED 3종(Eragon C, M, L)의 열전달면적 및 기판두께, 소모전력(P)로 부터 추출된 기판 열저항(Rth)과 상하부 온도차(⊿T)를 도시한 것으로, 기존의 Metal PCB에 비해 월등히 우수한 높은 열전도도 및 낮은 열저항과 낮은 기판 온도차 특성을 보이고 있어, 향후 고전력(High Power) LED 조명제품의 Package에 많이 활용될 것으로 기대한다.

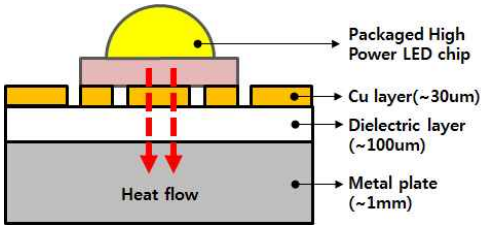

그림 1. 기존 Metal PCB 단면구조도

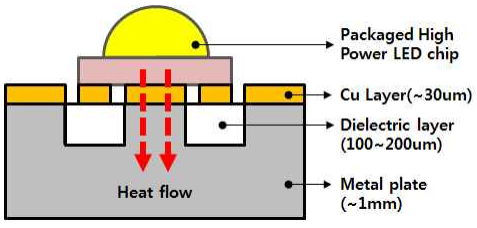

그림 2. 제안된 PMP(Patterened Metal Plate) 단면구조도

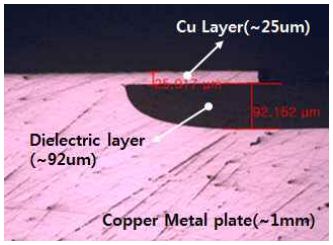

그림 3. 구리소재의 PMP 단면사진

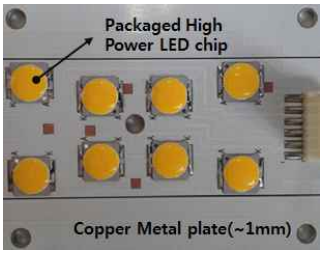

그림 4. High-power LED가 SMT된 구리소재의 PMP 사진

표 1. Metal PCB 및 알루미늄 PMP와 구리소재 PMP의 열전도도 및 High-power LED에 따른 열저항(Rth)과 기판의 상하부온도차(ΔT) 특성표

Type of Plate			Metal PCB	Aluminum PMP	Copper PMP
Conductivity [W/m-K]			40.9	112.9	298.8
High-power LEDs	Eragon C	Rth [K/W]	10.853	3.953	1.494
	(P=3[W])	ΔT [K]	32.6	11.9	4.5
	Eragon M	Rth [K/W]	3.527	1.277	0.483
	(P=8[W])	ΔT [K]	28.2	10.2	3.9
	Eragon L	Rth [K/W]	4.811	1.742	0.658
	(P=13[W])	ΔT [K]	62.5	22.6	8.5

[1] Mi-Hee Jee, Choong-Mo Nam, High Power LED Packaging by MOAMP(Multichip On Aluminum Metal Plate) Technology, The 17th Korean Conference on Semiconductors, 106 (2010).
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박막 태양전지 package의 warpage 현상에 대한 연구

Warpage behavior of thin solder cell package

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최근 태양광 발전은 비용절감을 위하여 태양전지 package를 박형화 하고 있는 추세이며, 현재 사용되고 있는 200um에서 보다 얇은 Wafer를 사용한 태양전지 제작을 연구 진행 중에 있다. 생산원가 절감은 Grid parity를 달성하기 위해서 필수적인 과정으로 박형 태양전지는 중요한 요소로 주목 받게 되었다.

열적 스트레스가 인가되는 제조 공정에서 warpage가 특히 심하게 발생되는 데, 이러한 warpage는 결국 태양광 모듈 packaging화 하는 과정에서 Crack으로 연결 되어 실제 장기간 발전 상황에서 출력 저하를 가지고 오게 된다. [1]

태양전지 package의 warpage는 다양한 재료의 적용으로 인해, 제작 공정에서 CTE mismatch에 의해 발생된다. 큰 warpage는 공정 또는 제품의 불량을 야기 시키는 주요 원인 중에 하나이다. 현재까지 태양전지 package의 warpage에 대한 연구는 Analytical and FE(finite element) 방법을 이용하여 다양하게 진행되고 있다. [2]

본 연구에서는 태양전지 package의 구조 및 공정 간 온도 변화에 기인한 태양전지 package의 warpage현상에 대하여 FEM을 활용한 예측과 실험 검증을 통해, 구조 및 제작 공정 동안 발생하는 Stress 이력과 이에 따른, Warpage현상에 대하여 고찰하고자 한다.

[1] 정태희, 김태범, 신준오, 윤나리, 우성철, 강기환, 안형근, 한득영, Tabbing 시 결정질 태양전지의 Bowing 현상에 관한 연구. 한국태양에너지학회 Vol. 30, No.2 2011 추계학술발표대회

[2] Chi-ming Lai, Chi-Hung Su, Keh-moh Lin, Analysis of the thermal stress and warpage induced by soldering in monocrystalline silicon cells, Applied Thermal Engineering 55 2013 7-16

Synchronized dual pulse etching effect of SiO_2 in capacitive coupled $C_4F_8/Ar/O_2$ plasmas

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Recently, the etching process of the nano-size contact hole using pulsed plasma technique has attracted a lot of attention due to its difficulty to etch the ultra-high aspect ratio contanct (UHARC) profile without twisting, sidewall bowing, etch stop, charging damages in conventional nanoscale etching [1]. Especially, SiO_2 etch process using dual-frquency capacitive coupled plasmas (DF-CCPs) which composed of a pulsed 60MHz as a source power and a pulsed 2MHz as a bias power have been widely investigaed to control the plasama density and ion bombardment energy, seperately. The 60MHz/2MHz combined dual-frequency capacitive coupled $C_4F_8/Ar/O_2$ plasmas are able to etch effectively because the gas dissociation is more effective than other frequency combinations. In this study, to increase etch charcteristics during SiO_2 etching by DF-CCP, a dual synchronized pulsing are simultaneously applied in the highly selective etching of SiO_2. As shown in this figure, the pulse phase lag of the bias power to the source power was varied from 0^o to 180^o. The results showed that the use of dual synchronized pulsing are improved the etch profile of SiO_2 masked with ACL. The etch mechanism by the dual synchronized pulsing will be presented.

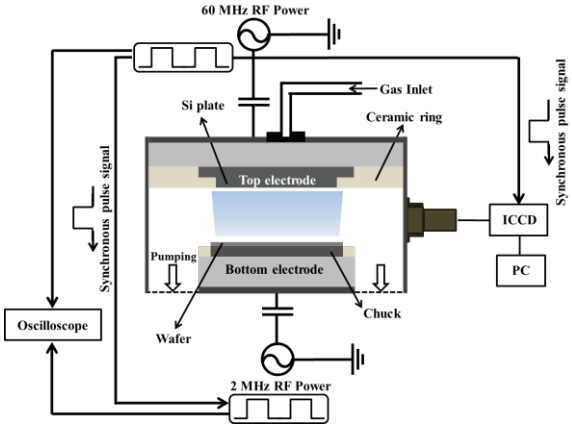

Fig 1. The schematic diagram of the dual-frequency capacitive coupled plasma.

[1] K. Tokashiki, et al., Jpn. J. Appl. Phys. 48, 08HD01 (2009)

그래핀 접촉저항 감소를 위한 플라즈마기술

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접촉저항은 그래핀 소자에 있어서 해결해야 할 과제이다. Parrish 와 Akinwande 연구그룹은 접촉 저항이 1.5Ω 에서 1.5KΩ 으로 증가함에 따른 그래핀 FET 소자의 current density, Trans-conductance, self gain, transit frequency 등의 중요 특성에 큰 영향을 준다는 시뮬레이션 연구를 보고 하였다.[1]

본 연구에서는 그래핀소자의 접촉저항을 감소시키기 위해서 Ar 6W ccp 를 처리방법을 이용하고자 하였다. 그래핀 표면에 Ar 6w ccp 를 처리하게 되면, 표면에 vacancy 와 sp3 bonding 을 형성시킬수가 있고,[2,3] 또한 소수성 성질의 그래핀을 친수성으로 변화시킬수 있게 된다.[3] 이는 그래핀과 금속과의 접합성을 증가시키는 요인으로 적용한다. 전극밑의 그래핀에만 Ar 6w ccp 를 처리한 결과, Vg=0V 조건에서 Ar 20s 에서 sheet resistance 가 391 ± 34 Ω/□에서 433 ± 24 Ω/□ 로 10% 정도 증가한 결과를 얻었고, 접촉저항은 3.0 ± 0.46 k Ωμm 에서 1.16 ± 0.39 k Ωμm 로 2.5 배 가까이 향상된 결과를 얻을 수 있었다. 이 Ar ccp 처리방법은 플라즈마를 이용하기 때문에 어떤 소자에도 손쉽게 적용할 수 있을 뿐만 아니라, 대면적에도 쉽게 적용할 수 있는 유용한 방법으로 생각된다

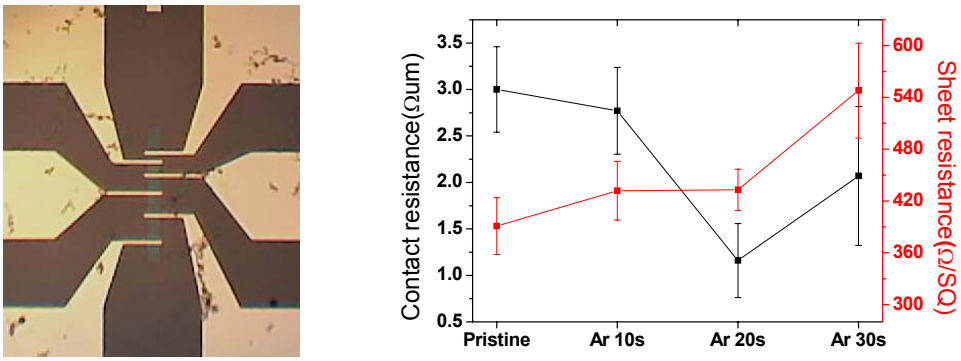

Fig 1. 그래핀 TLE 패턴 소자와, 플라즈마 처리에 따른 접촉저항

[1] K. N. Parrish and D. Akinwande,, Appled Physice Letters 98, 183505 (2011)
[2] J. Chen, T. Shi, T. Cai, T. Xu, L. Sun, X. Wu, D. Yu, Applied Physics Letters 102 103107 (2013)
[3] M. S. Choi, S. H. Lee, and W. J. Yoo, JOURNAL OF APPLIED PHYSICS 110, 073305 (2011)

Inductively Coupled Plasma Type Etcher의 ESC Edge Ring 소재 적합성 분석

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일반적인 inductively coupled plasma(ICP) type etcher 는 electrostatic chuck (ESC)을 보호하고 부품 소모에 따른 진행성 공정 변화를 최소화하기 위해, ESC 주위를 둘러싸는 edge ring(or focus ring)을 포함한다. Edge ring 은 소재, 단차, 가공단면 등 여러 가지 변수에 따라 공정능력 등에 변화를 야기할 수 있다 [1]. 본 연구에서는 edge ring 의 수명과 공정 및 설비 영향성, 공정 재현성 유지 등의 측면에서, C_xF_y gas 기반의 dry etching 공정에서 널리 이용되는 종래의 edge ring 소재인 Y_2O_3(yttria), Al_2O_3(alumina), quartz, silicon carbide 의 특징에 대해 고찰하고 한계점을 분석하였다. 그리고 실제 평가를 통해 문제를 정의하고 개선방향을 제시한다.

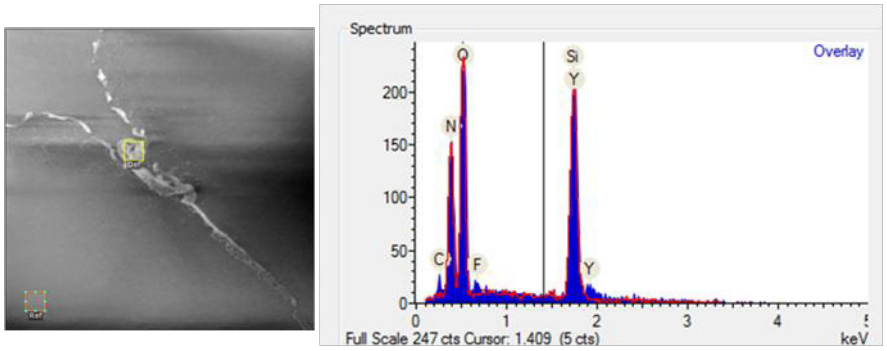

그림 1. Yttria edge ring 에 의한 defect 의 SEM 이미지 및 EDAX 분석

[1] Rex Anderson, Guenther Ruhl, Pavel Nesladek, Gerhard Prechtl, Winfried Sabisch, Alfred Kersch, Melisa J. Buie. Proc. of SPIE Vol. 5130 (2003).

RF Plasma SiN_x Etching Fault Detection Using Optical Emission Spectra with modified K-means Cluster Analysis and Principal Component Analysis

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Fault detection using optical emission spectra with modified K-means cluster analysis and principal component analysis are demonstrated for small area SiN_x inductive coupled plasma etching processes. The optical emission spectra from optical emission spectroscopy (OES) are used for detection. Furthermore, K-means cluster analysis algorithm is modified and applied to real-time detection and sensitivity enhancement for small area dielectric etching processes. For comparison, principal component analysis (PCA) is applied. The proposed techniques show clear improvement of sensitivity and significant noise reduction when they are compared with single wavelength signals measured by OES. These techniques are expected to be applied to various plasma monitoring applications including fault detections as well as endpoint detection.

Plasma-assisted preparation of metal nanoparticles on the branched nanowires to enhance the gas sensing properties

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[1]*Division of Materials Science and Engineering, Hanyang University, Seoul 133-791, Republic of Korea*
[2]*Department of Materials Science and Engineering, Inha University, Incheon 409-751, Republic of Korea*
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In order to enhance the gas sensing properties, it is essential to increase the surface-to-volume ratio. One important approach to increase the ratio will be to use the one-dimensional (1D) nanowires as a gas sensor. In order to further enhance the sensing capabilities, we prepared the 1D branches on the nanowires. This will facilitate the transport, adhesion, and reaction of the gas molecules. A variety of metals can be employed as a catalytic agent, we deposited metal nanoparticles to the branched nanowires. We explained the possible mechanisms for improvement of the sensing properties by the functionalization.

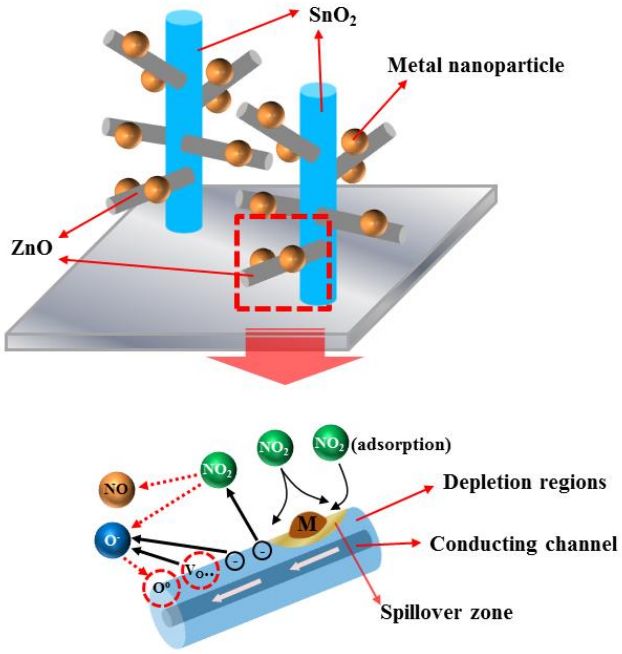

Fig 1. Schematic of a metal nanoparticles-decorated branched nanowire sensor.

Comparison of Electrical Characteristics between NanoPlate FET and Nanowire FET for 5 nm node Technology

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In this paper, we investigated the electrical characteristics of the NanoPlate FET for sub-5 nm node technology by comparing with Nanowire FET. For accurate comparison, we simulated single NanoPlate FET and three Nanowire FETs with the same total width. Device specifications of FETs follow the ITRS 2013 and we used TCAD (Sentaurus) simulation. Figure 1 shows the structure of NanoPlate FET and Nanowire FET. Figure 2 shows the electrical characteristics of both FETs. NanoPlate FET shows larger on-current, smaller subthreshold swing, and DIBL (Drain Induced Barrier Lowering) than Nanowire FET because of better gate controllability. Figure 3 shows the C-V characteristics of NanoPlate FET and Nanowire FET. Total capacitance includes parasitic capacitance [1] and total parasitic capacitance (C_{para}) consists of overlap capacitance (C_{ov}), outer fringe capacitance (C_{of}), and inner fringe capacitance (C_{if}). We extracted each parasitic component [2]. The all parasitic capacitnaces of Nanowire FET are larger than that of NanoPlate FET. Nanowire FET also has larger value of C_{para}/C_g at operating voltage. Since Nanowire FET has more parasitic capacitance, NanoPlate FET exhibits lower gate capacitance compared with Nanowire FET. At threshold voltage region, NanoPlate FET shows more steep gradient of C-V curve than Nanowire FET because of better gate controllability. From these results, NanoPlate FET is more competitive than Nanowire FET for the 5 nm node.

Acknowledgement

This work is supported by Samsung Electronics.

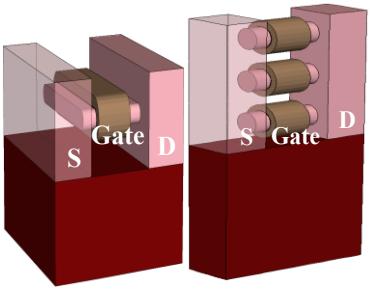

Figure 1. The structures of Nano -Plate and Nanowire FET

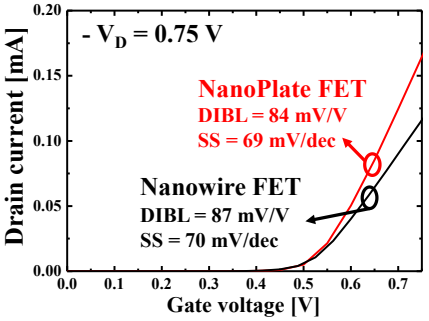

Figure 2. Electrical characteristics of both FETs

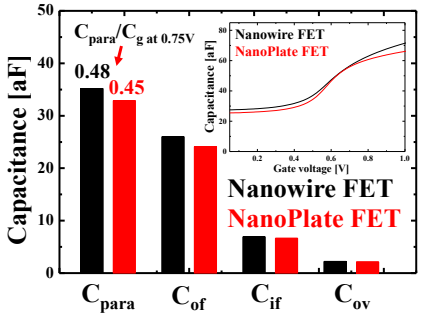

Figure 3. Comparison of the C-V characteristics

[1] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, IEEE EDL, Vol. 25, No. 8 (2004)
[2] Jae-Rok Kahng, Jang-Won Moon, and Jin-Hyoung Kim, IEEE ICMTS, Vol. 14, March (2001)

Investigation of the asymmetrical degradation behaviors under various gate and drain bias stresses in a-InGaZnO thin-film transistors

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Recently, amorphous indium-gallium-zinc oxide (a-IGZO) thin-film transistors (TFTs) are attracting much attention due to their excellent electrical performances [1]. In this work, we discuss the asymmetrical degradation behaviors of a-IGZO TFTs under various gate and drain bias stresses. The transfer curve exhibits an apparent negative shift after simultaneous gate and drain bias stresses, but different degradation behaviors are observed depending on the magnitude of applied gate and drain bias stresses. After an application of the gate-to-source (V_{GS}) and drain-to-source (V_{DS}) bias stresses of (V_{GS} = 16 V, V_{DS} = 16 V) and (V_{GS} = 22, V_{DS} = 10 V), the forward mode transfer curve exhibits a more negative shift compared to the reverse mode one. However, different types of asymmetrical degradation is observed after bias stress of (V_{GS} = 10 V, V_{DS} = 25 V). From two-dimensional simulation results and the separately extracted subgap density of states (DOS) in the source and drain sides of the TFTs before and after the application of various bias stresses, the non uniform generation of subgap states near the conduction band edge due to the local high electric field is considered as the dominant mechanism causing the asymmetrical degradation behaviors under various gate and drain bias stresses in a-IGZO TFTs.

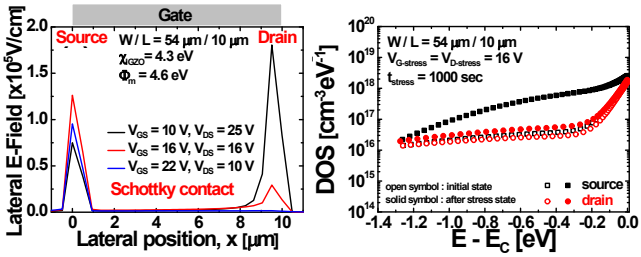

Fig 1. Lateral electric field distribution and separately extracted subgap DOS before and after the application of bias stress of (V_{GS} = 16 V, V_{DS} = 16 V) in a-IGZO TFTs

[1] K. Nomura et al, Nature (London) 432, 488 (2004).

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIP) (No. 2014-005368).

Various Heterojunction Single Gate Tunneling FETs with Graded Channel Doping in Sub-40 nm Channels

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Nowadays, nanoscale MOSFETs have been faced with short channel effects (SCEs) such as poor subthreshold swing (S/S), off current. Tunneling FET (TFET) with p-i-n diode operationg under reverse bias, which shows the excellent S/S is a promising candidate [1]. In addition, heterojunction and graded channel doping TFETs have been suggested to enhance the TFET performances and suppress SCEs [2].

In this work, we simulated single gate TFETs with various heterojunctions and graded channel doping (N_a) in sub-40 nm. The Si-$Si_{0.7}Ge_{0.3}$-Ge TFET show the largest on current levels below L_g = 40 nm, even though the off current of the Si-$Si_{0.7}Ge_{0.3}$-Ge TFET aggressively increases below sub-20 nm. This is because the $Si_{0.7}Ge_{0.3}$ Channel TFET has a lower potential barrier height, compared with other heterojunctions TFETs. On the other hand, the Si-Si-Si TFET show the excellent on/off current ratio (~10^7) and S/S (~30mV/dec) at L_g = 20 nm. This is because the Si has a larger band gap relative to $Si_{0.7}Ge_{0.3}$ and enhanced E-field with graded doping of channel. The small band gap of Ge at drain is vulnerable to reduce a leakage current at off-state.

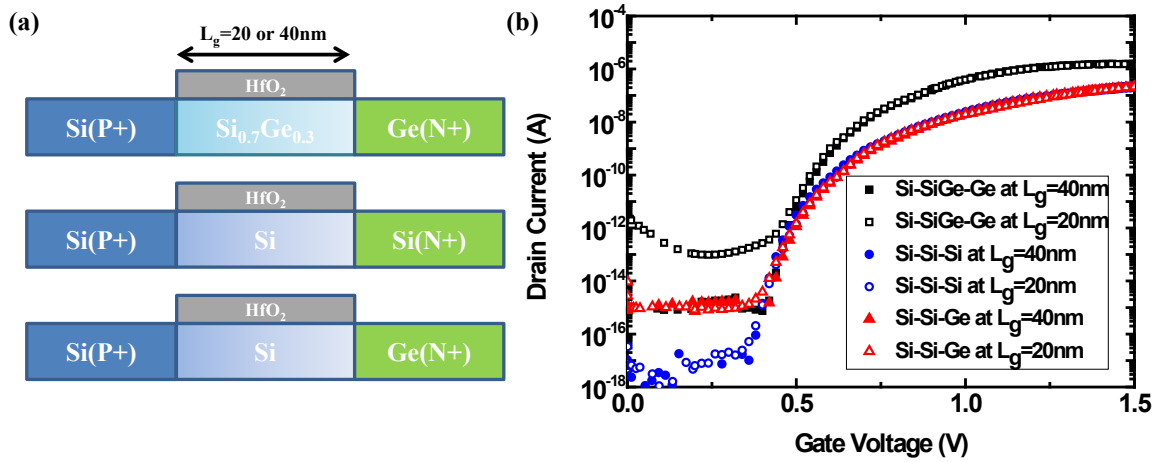

Fig 1. (a) The schematic and (b) I_d-V_g characteristics of various heterojunction TFETs.

[1] W.-Y. Choi, et al, IEEE Electron Device Letters, Vol. 28, No.8, (2007).
[2] Tejas Krishnamohan, et al, IEEE Electron Device Meeting (IEDM), (2008).

Analysis of structural dependences on the electrical performance of vertical organic field-effect transistor (VOFET)

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Organic semiconductors have attracted extensive interest in electronic device applications because of their homogeneity, low cost, and flexibility. However due to their low mobility, organic field-effect transistors (OFETs) require large working voltage to drive necessary current. Thus, the channel length defined as the gap between the source and drain electrodes should be as short as possible to address the aforementioned issues. For these purposes, the vertically stacked OFET (VOFET) has been proposed [1] and by extension, the carbon nanotube enabled VOFET has recently been demonstrated to facilitate the electrical performance of the VOFET [2]. However, an in-depth analysis of structural dependence on the electrostatics of the VOFETs has not been sufficiently performed yet.

Our study explores the structural dependence of electrical performance in VOFET by using TCAD. We first calibrated the P3HT (Poly(3-hexylthiophene-2,5-diyl)) organic semiconducting material with experimental data for a vertical channel in the simulation of VOFET. After that, by using the WKB-based tunneling model and incorporating the subgap density-of-states of the P3HT in the simulation, the structural dependences, i.e., channel length (film thickness), size of source electrode, etc., on the electrical performance of VOFET are comprehensively elaborated in this work.

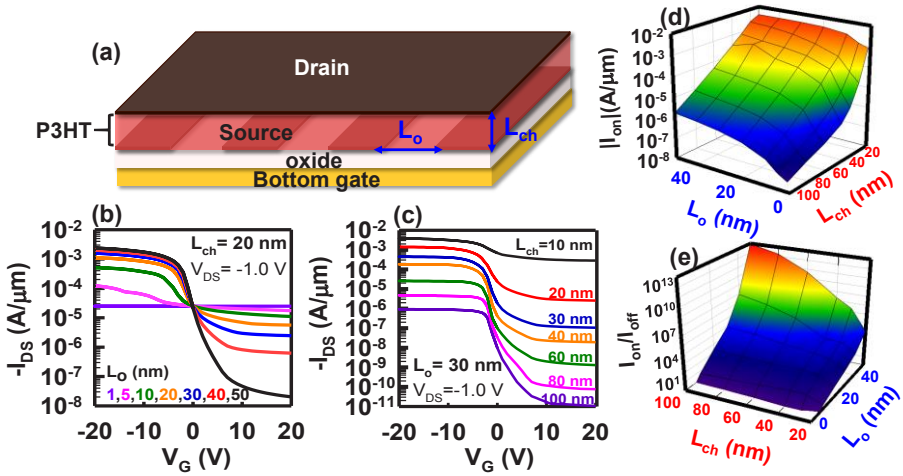

Fig 1. (a) A schematic illustration of the simulated VOFET. (b), (c) Transfer characteristics of VOFETs with various channel lengths (L_{ch}) and opening sizes (L_o). (d), (e) 3D plot of on-state current and on-off ratio.

[1] L. Ma and Y. Yang, Appl. Phys. Lett. 85, 21 (2004)

[2] M. A. McCarthy, B. Liu, and A. G. Rinzler, Nano Lett. 10, 9 (2010)

Acknowledgement: National research foundation of Korea (Grant 2013057870)

The High-κ/Metal Gate Structure to Suppress GIDL and FIBL in MOSFET

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Recently, sub-100nm CMOS Technology has adopted the high-k/metal gate (HKMG) structure to reduce the gate direct tunneling currents, however, there has been reported the unintended effect of fringing field induced barrier lowering (FIBL) which is caused by a potential penetration through the high-k gate oxide [1]. On the other hand, our previous work had verified a more supprssed gate-induced drain leakage (GIDL) on single high-κ dielectric structure in our previous works [2]. In this work, we suggest the optimum HKMG design method based on the analysis between GIDL and FIBL by using *Synopsis Sentaurus*^{TM} device simulation. Figure 1 shows the 2-D cross-sectional view of HKMG MOSFET having separated dielectrics between the gate and spacer with ε_{ox1} and ε_{ox2} respectively. In the energy band diagram on the inset of Fig. 1, the red line with low ε_{ox1} and high ε_{ox2} has more endurable FIBL and GIDL compared with the blue line of high ε_{ox1} and low ε_{ox2} owing to reduced field distribtuion from dain to channel and increased tunneing width. Figure 2(a) and (b) represent the GIDL currents at V_G=1V, V_D=1V and the drain induced barrier lowering (DIBL= $(V_{th,lin}-V_{th,sat})/(V_{DS,lin}-V_{DS,sat})$) with various combination of ε_{ox1} and ε_{ox2}, where FIBL can be represented in terms of DIBL based on barrier lowing phenomenon. Therefore, off leakage can be diminished by designing HKMG with seperated oxide region.

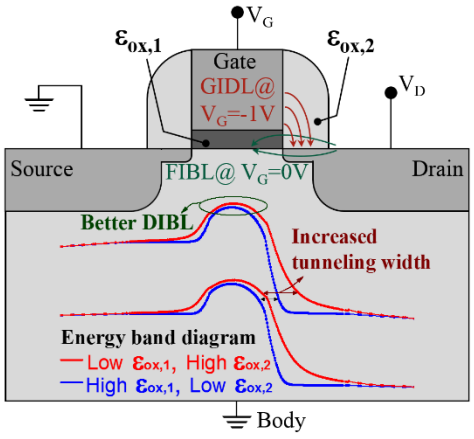

Fig 1. The 2D MOSFET schemeatic with fringing field distribution.

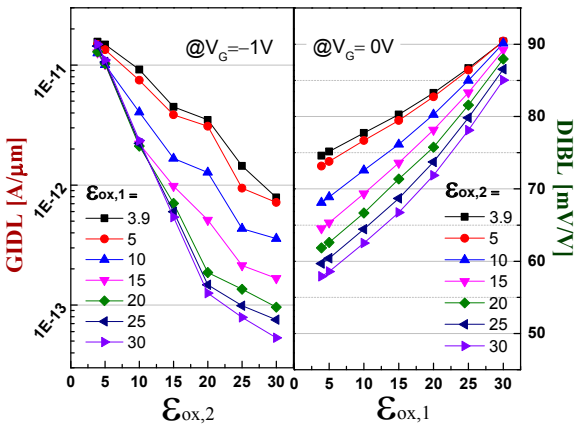

Fig 2. GIDL and FIBL on various ε_{ox1} and ε_{ox2}

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[2] E. S. Jang, J. W. J ung, S.H. Shin, and K.R. Kim, MNC 7P-11-48 2014.

2T SONOS Cell with a low voltage select gate for random access operation

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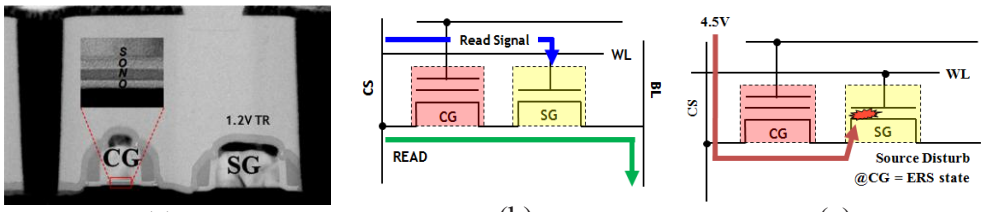
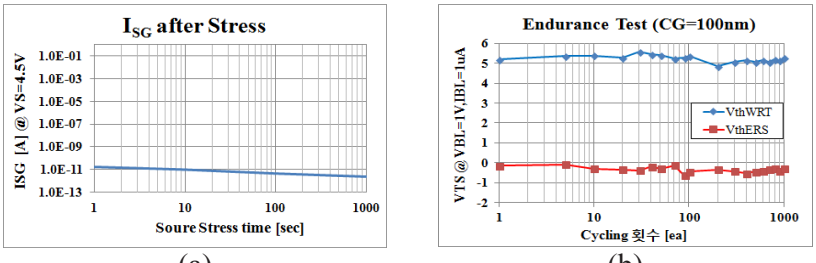
In this paper, we propose a high-read-speed 2T-SONOS(Silicon-Oxide-Nitride-Oxide-Silicon) device in 90nm LOGIC CMOS process with a 1.2 LV(Low voltage) SG(Select gate) and a CG(Control gate) shown in Fig. 1(a). Normally, in the 2T structure, a SG uses MV(Medium voltage) oxide to assure operating in variety of condition and retain the reliability. But recently many groups try to use LV oxide at SG to satisfy high read access time and low power consumption[1]. The proposed cell have around 6V PGM/ERS window and 1.2V read operation as Fig. 1(b). Worst case in the program operation is happened source disturb mode in Fig. 1(c). In this mode that cell is erase state, source bias passes through a CG channel and cause a SG gate oxide breakdown due to high electrical field. To confirm this oxide reliability, we measured SG current after disturb stress up to 1000s and concluded that no oxide breakdown problem, described in Fig. 2 (a). In the Fig. 2(b), the cell satisfy 1K cycling without Vt window decrease. From these result, we confirmed that there is no problem to use 1.2 LV oxide in 2T-SONOS cell.



(a) (b) (c)

WL (Word line), BL (Bit line), CS (Common Source), HV Tr → Slow, LV Tr → Fast

Figure.1. (a) TEM IMAGE, (b) Read operation scheme, and (c) Worst case in the cell



(a) (b)

Figure.2. (a) SG Current after stress, (b) 1K Endurance test of Cell

[1] T. Kono, et. Al ISSC, VOL. 49, NO. 1. JAN(2014)

Managing Power Consumption and Clock Skew Using Mesh Clock Network with Multiple Subtrees

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Clock mesh [1]는 clock skew 를 줄이기 위해 사용되지만, wire 의 증가에 따른 전력 소모가 크다. 한 보고에 의하면, 같은 chip 에 clock tree 를 적용하였을 때와 비교해서 mesh clock network 가 33.4%의 전력을 더 소모한다고 한다 [2]. 본 논문에서는 이러한 전력 소모를 줄이기 위해, mesh grid 아래에 subtree 를 갖는 그림 1 (a)의 구조를 채택한다. 이 구조는 mesh 의 fanout 을 줄여서 grid 에 사용되는 wire 를 줄이고, 따라서 전력소모를 줄일 수 있다.

본 논문의 mesh clock network 는 subtree 의 그룹핑을 잘 하는 것이 중요하다. 그림 1(b) 상단처럼, 단순히 subtree 를 균등하게 배치하여 가까운 clock sink 들끼리 그룹핑을 하면, subtree 들의 latency 차이가 커지고 clock skew 가 나빠진다. 본 논문에서는 그림 1(b) 하단과 같이 subtree 들의 latency 를 비슷하게 하는 그룹핑 알고리즘을 제안한다. 한편, launching-capturing pair 를 이루는 플립플랍을 같은 그룹에 배치할 경우, 그들 간의 clock skew 가 더욱 줄어들어 slack 이 향상된다. 이를 위한 그룹핑 조정 알고리즘 또한 본 논문에서 제안한다.

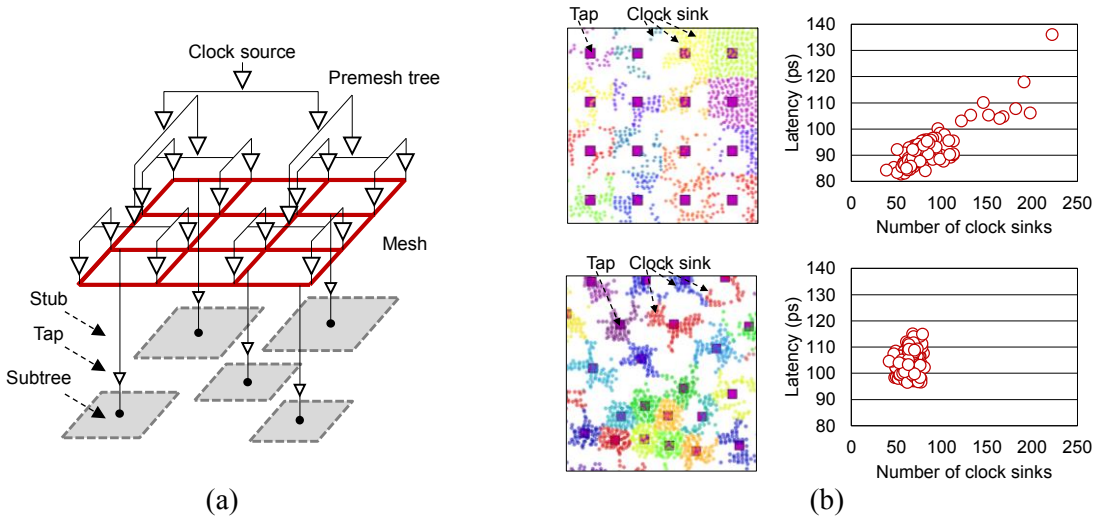

그림 1. 여러 개의 subtree 를 갖는 mesh clock network: (a) mesh clock network 의 구조, (b) clustering 을 통한 subtree 그룹핑 결과 비교.

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Efficient Configuration-Data Assignment Algorithm for CGRA-based Multi-Core Architecture

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Coarse-grained reconfigurable architecture (CGRA) has emerged as a suitable solution for the embedded applications like audio, video and graphics processing. However, single CGRA is sequentially optimized for the parallelized computations in a kernel at a time whereas the overall speedup of the entire application can be achieved by kernel-level parallelism (KLP) [1]. Therefore, such a limitation of single CGRA has resulted in the appearance of CGRA-based multi-core architectures [2]-[3] to support diverse KLPs. However, the existing architectures suffer from much energy and performance bottleneck because of poor resource utilization caused by insufficient flexibility. For this reason, ring-based sharing fabric (RSF) and intra/inter-CGRA co-reconfiguration was proposed to boost their flexibility level for the efficient resource utilization focusing on the kernel-stream type of the KLP as [4]. It can be achieved by the series of shifting configuration of kernel-stream on the multiple CGRAs - the more resources are utilized in the RSF, the more shifting configurations are performed. It means that each configuration memory (CM) should include multiple data-set for several reconfiguration of each processing element array (PA). Therefore, it is necessary to make the optimal pipeline-scheduling without exceeding a CM capacity. For this reason, we propose an algorithm for efficient configuration-data assignment as shown in Fig. 1. Experimental results show that the RSF based on the proposed algorithm improve performance by up to 88.8% and reduce energy by up to 48.2% when compared with the conventional CGRA-based multi-core architectures.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2014R1A1A2056604) and by IC Design Education Center (IDEC).

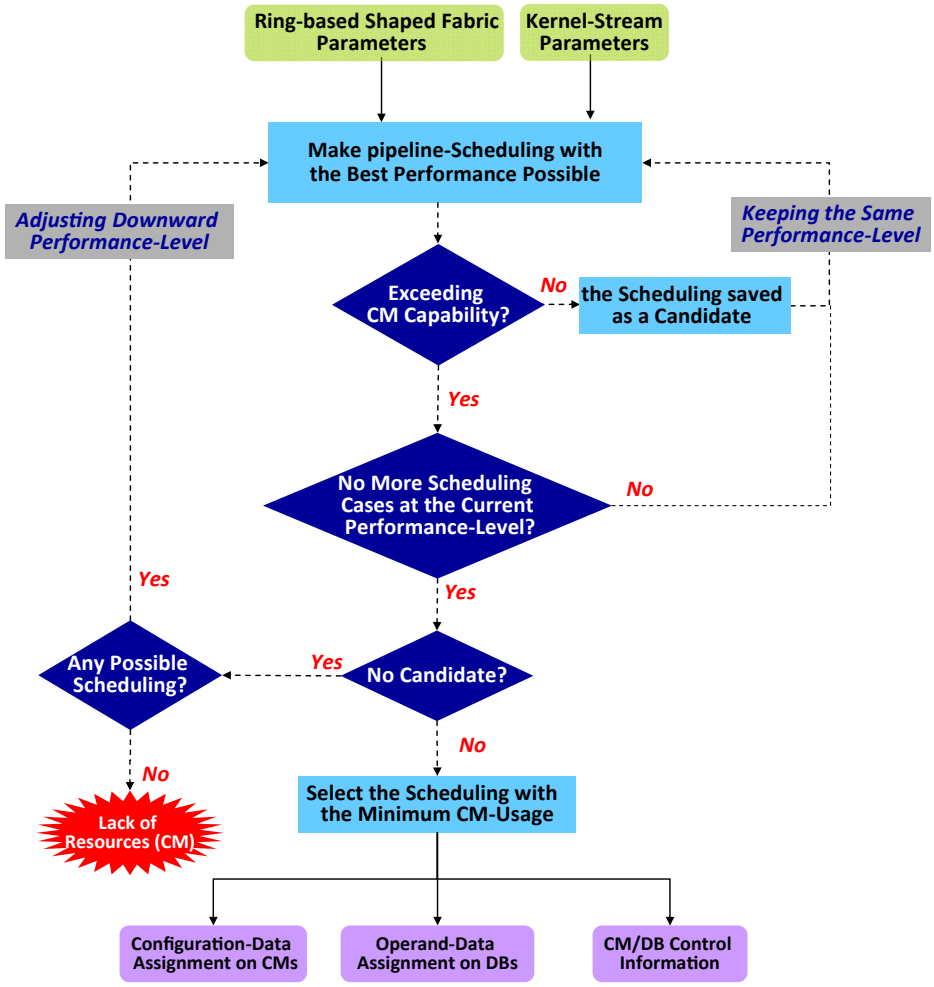

Fig 1. Configuration-data assignment algorithm.

[1] Nishihara, K., Hatabu, A., Moriyoshi, T.: 'Parallelization of H.264 video decoder for embedded multicore processor', *IEEE Int. Conf. on Multimedia and Expo*, Hannover, Germany, Apr. 2008, pp. 329-332.

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Pipelining Nested Loops with Triangular Iteration Space for High-Level Synthesis*

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A key transformation feature of HLS (High Level Synthesis) tool is single loop pipelining. State of the art tools like VIVADO HLS also support nested loop pipelining. However, the HLS transformation of nested loop pipelining uses more hardware resources and degrade throughput than the counterpart manually designed hardware. In addition, though state of the art HLS tools can pipeline rectangular nested loops, it is unable to pipeline efficiently nested loops that forms triangular iteration space. Thus, optimization in higher level code can be done such that the HLS tool can efficiently produce RTL code. To address the problem, efficient finite state machine (FSM) based control of nested loop pipelining that can be used for any affine bound loops is proposed in [1]. In [1], the higher level code is first optimized as per the proposed optimization technique and afterwards is fed to HLS tool. The derived FSM from the proposed technique [1] better utilizes hardware but it occupies significant amount of hardware resources due to inclusion of several control logics. Other novel techniques are required to reduce the hardware resources for nested loop pipelining specially of the form triangular iteration space without sacrificing on maximum operating frequency and overall throughput. In [2], optimization on high level language has been done specifically for input of polyhedral code generator, CLooG. The output of CLooG is then fed to HLS tool. By contrast, our proposed technique is directly for HLS tool.

We propose mirroring technique to transform triangular iteration space into a rectangular iteration space. The area of the converted rectangular iteration space is equal to that of the triangular space. The optimization is performed on the higher level language (i.e., C) such that the triangular nested loops are first converted to rectangular nested loops and then fed as input to HLS tool. The synthesis result in Xilinx Virtex 7 FPGA of our technique shows that in case of 2D triangular nested loop pipelining, the usage of hardware resources in terms of LUTs significantly reduces by 70.32 percent than that of [1] and by 19.24% than the default code without optimization, as summarized in Table 1.

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†Jongeun Lee is the corresponding author of this paper (e-mail: jlee@unist.ac.kr).

Table 1: Comparison of synthesis results of the proposed technique vs [1] vs default code

Iteration Space	Technique	Minimum clock period (ns)	Frequency (MHz)	Total Latency (Clock cycles)	FF count	ALUT count	LUT count	FPGA	HLS tool
Triangle 2D	[1] by Yuki	2.41	414.94	32	510	N/A	1075	Xilinx Virtex 7 XQ7VX 980TRF 1930-2L FPGA	VIVADO
	Default code without optimization	2.49	401.61	36	78	N/A	395		
	Proposed Mirroring technique	2.41	414.94	33	127	N/A	319		
	[1] by Yuki	3.23	308.83	322	1166	854	N/A	Arria II GX	Legup
	Default code without optimization	3.82	261.71	329	900	895	N/A		
	Proposed Mirroring technique	5.29	189.11	300	1082	1120	N/A		

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APPENDIX

```
for(int i=0; i<M; i++)
{
   for (int j = 0; j <=i; j++)
   {
    if(j<=i)
    {
     sum ^= a[i][j] ^ b[i][j];
    }
   }
}
```

(a)

```
int done=0; int done_1=0; int i=0; int j=0;
int i_n1=0; int i_n2=0; int j_n1=0; int j_n2=0;
if(N>=1)
{ i=0; j=0; i_n1=1; j_n1=0; }
else done=1;
while(!done)
{
 int ctrl_a0=(i<N-2);
 int ctrl_a1=(!(ctrl_a0))&&(!((i==(N-1))&&(j==(N-2))));
 int ctrl_a2=!(ctrl_a0||ctrl_a1);
 done = done_1;
 sum ^= a[i][j] ^ b[i][j];
 if(ctrl_a0){i_n2=i+2; j_n2=j;}
 if(ctrl_a1){i_n2=j+i-1; j_n2=j+1;}
 if(ctrl_a2) done_1=1;
 i=i_n1; j=j_n1;
 i_n1=i_n2; j_n1=j_n2;
}
```

(b)

```
for( i=0; i<=(M-1)/2; i++)
{
 for (int j = 0; j < M+1; j++)
 {
   int x, y;
   if(i>=j)
   {
     x = i; y = j;
   }
   else if(j<4)
   {
     x = M-1-i; y=M-1-j;
   }
   else if(1)
   {
     x = M-1-i; y=M-1-i;
   }
   sum ^= a[x][y] ^ b[x][y];
 }
}
```

(c)

Figure 1. Example codes of Triangle 2D loop (a) Original code (b) [1] by Yuki (c) proposed mirroring technique.

Fast Verification Flow with High-Level Synthesis - Case Study

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Design productivity is one of the most important challenges in multi-processor system on chip (MPSoC) design. High-level synthesis (HLS) to automatically create the RTL design provides productivity benefits in both design and verification through the controllability enhancement. In this paper, we present an electronic system level design flow with SystemC verification (SCV) library[1] for coverage measurement. Figure 1 shows the proposed verification flow with HLS that the coverage measurement is moved to the transaction level. Proposed design flow gives fast behavioral simulation and easy functional debugging to guarantee the higher quality of result (QoR) and shorten turn-around time (ToT). We use the transactor implementation and constrained random generation in SCV library that we can speed-up the simulation time on average 4.6 times faster and it reduces the verification and debugging to 1/3 still meeting the coverage goal. Experiment also shows the higher QoR that by using HLS technique, design time is reduced 40%~60% on same area compared to the traditional RTL design. In conclusion, our electronic system level (ESL) design using HLS technique reduced the design cycle by 30%.

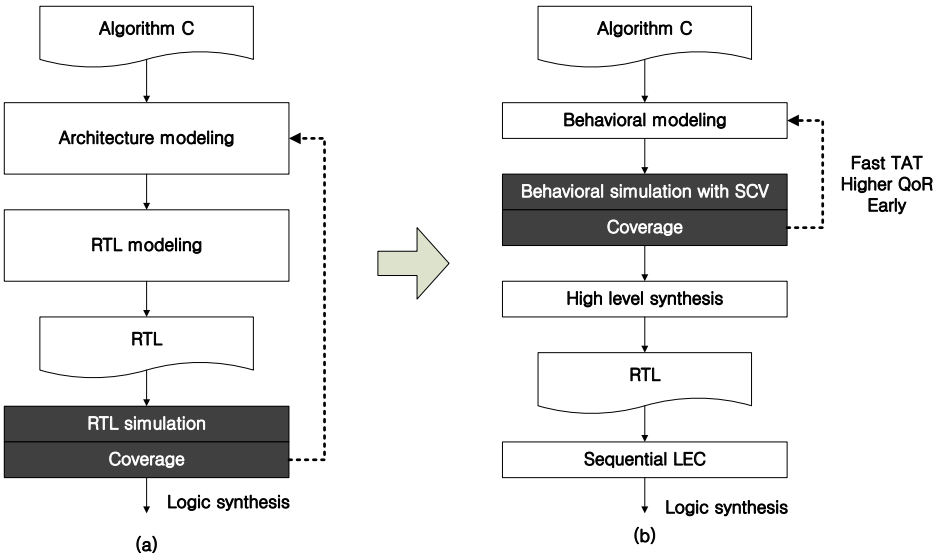

Figure 1. (a) Traditional RTL design flow (b) Electronic system level design flow

[1] SystemC Verification Library, http://accellera.org/activities/committees/systemc-verification/

UVM based Register Test Automation Flow

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In today's SoC design, the number of registers has been increased along with complexity of hardware blocks. Register validation is a time-consuming and error-pron task. Therefore, we need an efficient way to perform verification with less effort in shorter time. In this work, we suggest register test automation flow based UVM (Universal Verification Methodology). UVM provides a standard methodology, called a register model, to facilate stimulus generation and functional checking of registers [1]. However, it is not easy for designers to create register models for their functional blocks or integrate models in test-bench environment because it requires knowledge of SystemVerilog and UVM libraries. For the creation of register models, many commercial tools support a register model generation from register specification described in IP-XACT [2], but it is time-consuming to describe register specification in IP-XACT format. For easy creation of register model, we propose spreadsheet-based register template which is tranlslated to IP-XACT descrption, from which register models can be easily generated using commercial tools. On the other hand, we also automate all the steps involved integrating test-bench and generating test-cases, so that designers may use register model without detailed knowledge of UVM or SystemVerilog. This automation flow involves generating and connecting test-bench components (e.g. driver, checker, bus adaptor, etc.) and writing test sequence for each type of register test-case. With the proposed flow, designers can save considerable amount of time to verify functionality of registers.

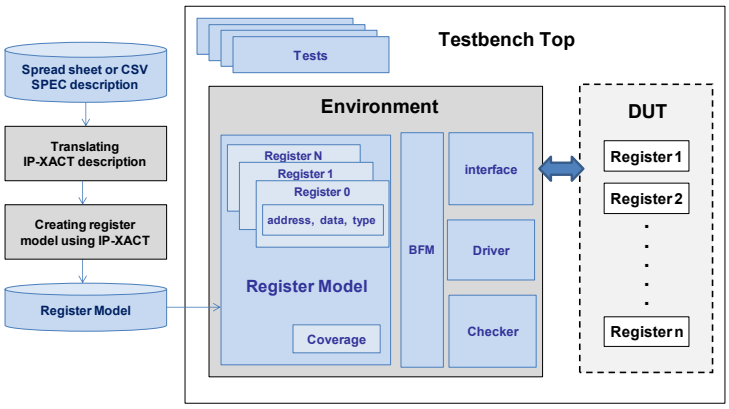

Fig 1. Register test test-bench top architecture

[1] Mark Litterick, Marcus Harnisch "Advanced UVM Register Modeling", DVCon 2014.
[2] David Murray, "Leveraging IP-XACT Standardized IP Interfaces for Rapid IP Integration", DVCon 2014.

Fault-Recoverability Evaluation of CGRA-based Multi-Core Architecture

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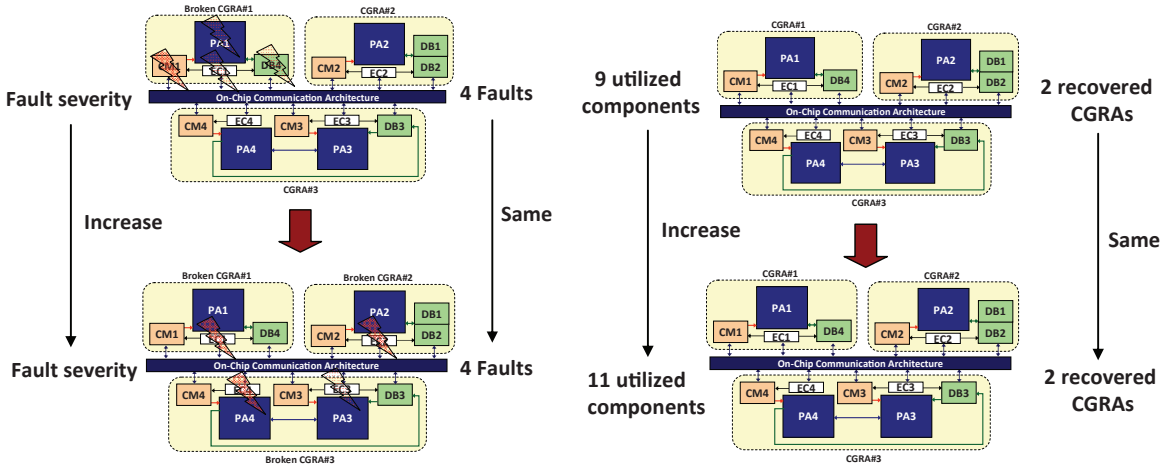
CGRA (Coarse-Grained Reconfigurable Architecture) based multi-core architecture can be considered as a suitable solution for the fault-tolerant computing engine because of its inherent redundancy and reconfigurability. However, there have been a few research projects [1][2] based on fault-tolerant CGRA without exploiting such strengths of CGRA as well as their works are limited to single CGRA. Therefore, in [3], we proposed two approaches enable exploiting the inherent redundancy and reconfigurability of the multi-CGRA for fault-recovery. One is a resilient inter-CGRA fabric that is ring-based sharing fabric (RSF) for the efficient replacement of the modules driving malfunction with minimal interconnection overhead. Another is a novel intra/inter-CGRA co-reconfiguration technique on RSF for maximizing resource utilization of the resources when faults occur. However, [3] only showed area/delay/power efficiency of the RSF without demonstrating the effectivenenss of the proposed approaches in terms of fault-recoverability. Therefore, in this paper, we evaluate the fault-recoverability of the RSF and the co-reconfiguration technique with various fault-occurrence cases.

First of all, we suggest a quantitative evaluation method of fault re-coverability of a multi-CGRA based on two criterions. First criterion is fault severity that does not mean only number of faults - even though some cases may show the same number of faults, the fault severity of the cases may be different. For example, Fig. 1 (a) shows such a case that the severity of the bottom multi-CGRA is more serious than the upper case despite of the same number of faults – the bottom case with 4 dysfunctional ECs (Execution Controllers) means that all of the CGRAs are broken and they are never recovered. Therefore, fault severity should reflect the seriousness degree of the fault-occurrence with considering recovery potential. The second criterion is the number of utilized components that are working after fault-recovery - it means the recovery degree. It is much more accurate than the number of recovered CGRAs because heterogeneous multi-CGRA can show different number of utilized components despite of the same number of the recovered CGRAs. Fig. 1 (b) shows such a case that the recovery degree of the bottom multi-CGRA is better than the upper case – both cases show the same number of the recovered CGRAs but the utilized components of the bottom case are more than the components of the upper case.

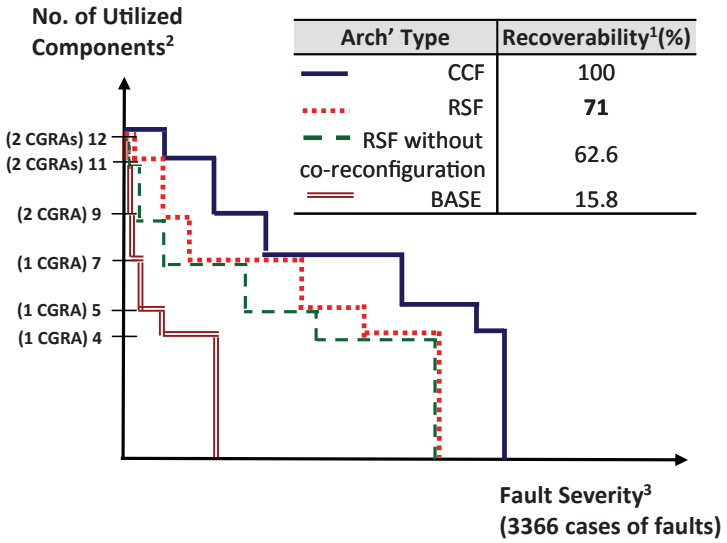
This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2014R1A1A2056604) and by IC Design Education Center (IDEC).



(a) Concept of fault severity (b) Concept of number of utilized components

Fig 1. Two criterions for evaluating fault recoverability.

If we consider two such criterions together, we can see an inverse relationship between them – if the fault severity increases, the number of utilized components decreases. For example, we can plot the relationship on the graph according to 4 types of multi-CGRA as Fig. 2 – CCF (Completely Connected Fabric), RSF, RSF without co-reconfiguration and BASE that is heterogeneous 3 CGRAs shown in Fig. 1. The fault recoverability of 4 types of multi-CGRA can be quantitatively represented as the rate of the area of the region in the horizontal/vertical-plane bounded by the



Arch' Type	Recoverability¹(%)
CCF	100
RSF	71
RSF without co-reconfiguration	62.6
BASE	15.8

Recoverability¹: 100 X area of graph RSF (or BASE) / area of graph CCF
No. of Utilized Components² : (No. of ECs) + (No. of PAs) + (No. of DBs) + (No. of CMs) on the recovered CGRAs
Fault Severity³: Increasing severity means decreasing recoverable CGRAs with more faults.
3366 cases of fault-occurrences are listed in the severity order on the horizontal axis.

Fig 2. Fault recoverability evaluation : BASE type - heterogeneous 3 CGRAs as shown in Fig 1.

graph – it is relative rate to CCF (100%) and shown in the right upper table on the graph. We have implemented such a fault recoverability evaluator with C language. The evaluator automatically increases fault severity and estimates corresponding number of utilized components according to 4 types of multi-CGRA. A BASE type is used for an input of the evaluator and the 4 cases of recoverability presented in the rate of the area are generated as outputs. In the graph, the RSFs show 71% of the fault recoverability. In addition, we can see the effectiveness of the co-reconfiguration technique – it enhances 7.5% of the recoverability of the RSFs compared with the RSFs without it.

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Dual-Gate p-GaN gate HEMTs for Steep Subthreshold Slope

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Recently, the AlGaN/GaN high electron mobility transistor (HEMT) has been widely investigated for high-power switching applications [1]. We investigated the sudden increase of the gate (I_G) and drain current (I_D) observed in p-GaN gate HEMT. Since the metal/p-GaN/AlGaN/GaN forms a n-p-n heterojunction bipolar transistor, when the gate bias (V_G) increases to a value larger than 4 V, breakdown of floating base BJT occurs [2]. By adapting dual-gate structure with floating gate formed between gate and source, turn-on voltage (V_{on}) ~ 4 V and we achieved extremely steep subthreshold slope less than ~0.1 mV/dec. Threshold voltage (V_T) of a single gate device on the same wafer is ~ 2 V. In the dual-gate device, I_D is controlled by V_G and potential of the floating gate (V_{FG}). When a V_G is less than 4 V, V_{FG} is smaller than V_T since floating gate is output node of a kind of voltage divider consist of two resistances, one is an equivalent resistance consisting of BJT and 2-DEG from the gate to the floating gate and the other is 2-DEG resitance from the floating gate to the source. Because a resistance from the source to the floating gate is smaller than the equivalent resistance, V_{FG} should be a value close to V_S. Therefore V_{FG} is less than V_T and GaN channel under the floating gate still remains as depleted although V_G is larger than V_T. As a result, the dual-gate device is off. At a V_G larger than 4 V, impact ionization occurs in the p-GaN depletion region. Therefore a lot of generated holes are injected in the channel layer. Because V_{FG} is smaller than V_G, holes easily move into the floating gate and the channel under the floating gate. As a result, the floating gate is charged with holes and the GaN channel under the floating gate turns on. Fig. 1 shows measured I_D-V_G curves of three different dual-gate p-GaN gate HEMTs. The curves show similar V_{on} and I_D. Obtained subthreshold slope is ~0.1 mV/dec, as plotting in inset of the Fig. 1.

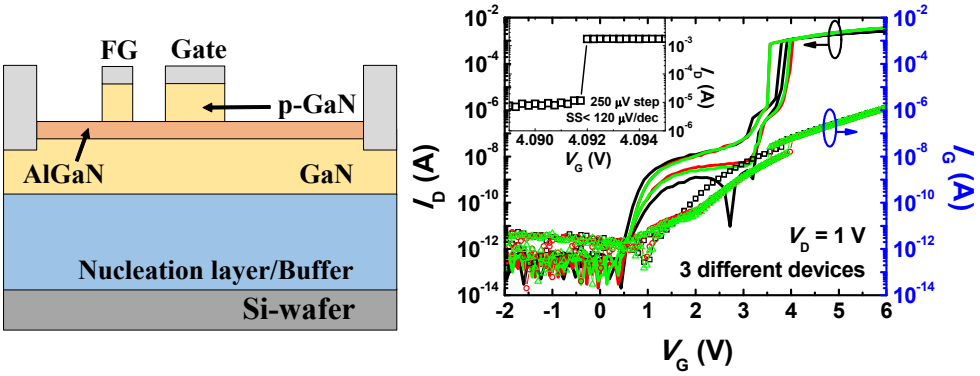

Fig 1. Dual-gate p-GaN gate HEMTs and *I-V* characteristics

[1] M. Meneghini, et al., *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 375-377, Mar. 2012.
[2] J.-H. Bae, et al., *IEDM,* pp. 31.6.1–4, 2013

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First Demonstration of Omega-shaped-gate AlGaN/GaN Nanowire FinFETs

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Recently, excellent device performances have been demonstrated in AlGaN/GaN-based nanowire FinFETs. The reason for the high performances is due to the 3-D gate configuration which greatly improves the gate controllability when the dimensions are nanosized. In this work, we have fabricated and characterized the omega-shaped-gate AlGaN/GaN nanowire FinFETs. For device isolation, the nanowire-shaped active region was patterned by E-beam lithography and defined by TCP-RIE using a BCl_3/Cl_2 gas mixture. The sidewall spacer of nanowire AlGaN/GaN fins was formed by using the 20 nm ALD HfO_2 deposition and blank etching. The combination of additional dry etching and lateral wet etching (TMAH - 20 % solution at 90 °C during 10 hr) were used to form the omega-shaped fin structure. After removing the HfO_2 sidewall spacer, a 20-nm-thick Al_2O_3 gate insulator and 50 nm TiN gate metal layer were then formed by ALD as shown Fig. 1(a). After contact hole opening for the S/D, Ti/Al/Ni/Au was deposited using an E-beam evaporator, followed by RTP at 850 °C for 30 s in nitrogen ambient. The device performances are shown in Fig. 1(b)~(c) with channel width from 30 nm to 250 nm. The V_{th} negatively increases as the width of the nanowire increases, which requires more negative gate voltage to deplete the channel (Fig. 1(b)). All devices except for fin width of 30 nm exhibit very low off-state leakage current as low as ~10^{-11} mA, the theoretical SS value of ~60 mV/dec, and high I_{ON}/I_{OFF} ratio (~ 10^9) from the I_{ds}-V_{gs} curve at V_{ds} = 0.1 V. The I_{ds}-V_{ds} curve shows that this device has very small amount of current collapse as increasing the drain voltage (Fig. 1(c)). The excellent off-state performances are due to the reduced GaN buffer layer in the omega shaped gate structure, which results in the low buffer leakage current. In addition, the gate can fully deplete the channel of this device due to the nano-sized bottom of fin.

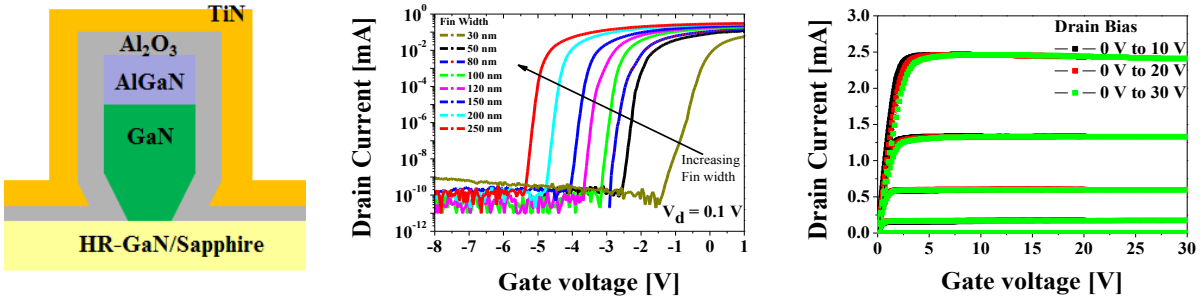

Fig. 1. (a) Schematic illustration of the proposed GaN nanochannel FinFET, (b) Logarithmic scale of drain current as a function of fin widths, and (c) I_{ds} - V_{ds} characteristics with different drain voltage.

낮은 온저항을 갖는 AlGaN/GaN 더블 쇼트키 다이오드에 대한 연구

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AlGaN/GaN 기반 전력반도체 소자는 AlGaN/GaN 사이에 형성된 이차원 전자가스(Two-Dimensional Electron Gas, 2DEG)와 높은 항복전압에 의해 고효율/고속 스위칭의 특성을 가지는 차세대 전력소자로 주목 받고 있다 [1]. 쇼트키 다이오드의 효율을 높이기 위해서는 낮은 온저항과 작은 전압에서 빨리 turn-on 할 수 있도록 만드는 것이 중요하다 [2]. 하지만, AlGaN/GaN 쇼트키 다이오드의 경우, turn-on 전압을 개선한 연구 결과들에 비해 낮은 온저항을 위한 연구 발표는 상대적으로 적을 뿐만 아니라, 특별히 패키지 제품 상용화를 위해서는 온저항을 더 낮추는 방법이 필요하다. 본 연구에서는 두 개의 다이오드를 병렬로 연결한 더블 쇼트키 다이오드를 패키지 제작하여 온저항이 반으로 낮아짐을 확인하였다. 기존의 단일 다이오드가 순방향 전류 12.4A 에서 온저항은 0.15Ω이었으나, 더블 다이오드에서는 0.08Ω을 나타내었다. 또한, 순방향 전압 5V 에서, 대전류 50A 가 흐르는 우수한 특성을 달성하였다. ETRI 가 개발한 더블 다이오드의 소자 제작 과정과 패키지 방법 및 특성에 대하여 설명하고자 한다.

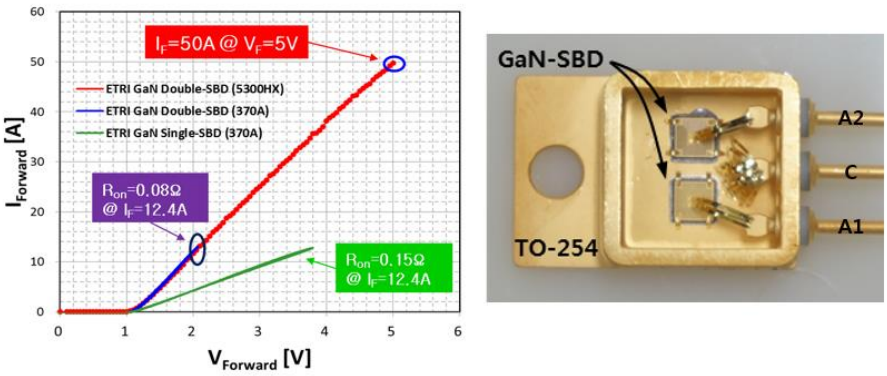

그림 1. ETRI GaN 더블 쇼트키 다이오드의 전류-전압 특성 및 패키지된 모습

[1] S. L. Selvaraj, T. Suzue, and T. Egawa, IEEE Electron Device Lett., 30, 587 (2009).
[2] E. Bahat-Treidel, O. Hilt, R. Zhytnytska, A. Wentzel, C. Meliani, J. Wurfl, and G. Trankle, IEEE Electron Device Lett., 33, 357 (2012).

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Normally-off Operation of AlGaN/GaN-on-Si MISHFET Integrated with Clamping Circuit

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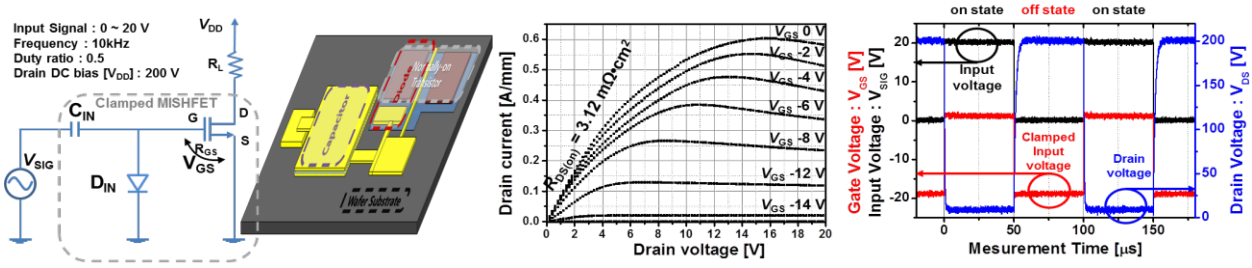
AlGaN/GaN heterojunction field-effect transistors (HFETs) are an outstanding candidate for next generation power switching applications owing to their fast switching speed, high carrier density and extremely large breakdown voltage. An important technical challenge for AlGaN/GaN power switching application is how to implement the normally-off operation. Though several different approaches have been reported for enabling the normally-off operation of AlGaN/GaN HFETs, the low threshold voltage and limited current density due to strong polarization effects limit the capability as a high efficient power switching device. In this work, we have developed an AlGaN/GaN MISHFET with an integrated clamping circuit. The integrated clamping circuit that was composed of a Schottky barrier diode and a capacitor was connected to the gate electrode of a normally-on AlGaN/GaN MISHFET. The integrated clamping circuit shifted the input driving signal from (0, 20 V) to (-20, 0 V), allowing the normally-on AlGaN/GaN MISHFET with a pinch-off voltage of -15 V to be operated as a normally-off device. The device exhibited a high drain current density of ~600 mA/mm with a breakdown voltage of > 800 V. In comparison with other normally-off GaN based FETs, much higher current (i.e. low on-resistance) and threshold voltage can be achieved with easy processing; no need for gate recess or complicated epitaxy growth.



(a) (b) (c)

Fig 1. (a) Schematic of AlGaN/GaN MISHFET with an integrated clamping circuit, (b) I-V characteristics of Normally-on AlGaN/GaN MISHFET, and (c) normally-off, switching oscillation waveforms measured at 10 kHz operation.

다이오드 브릿지 내장형 AlGaN/GaN 양방향성 전력소자

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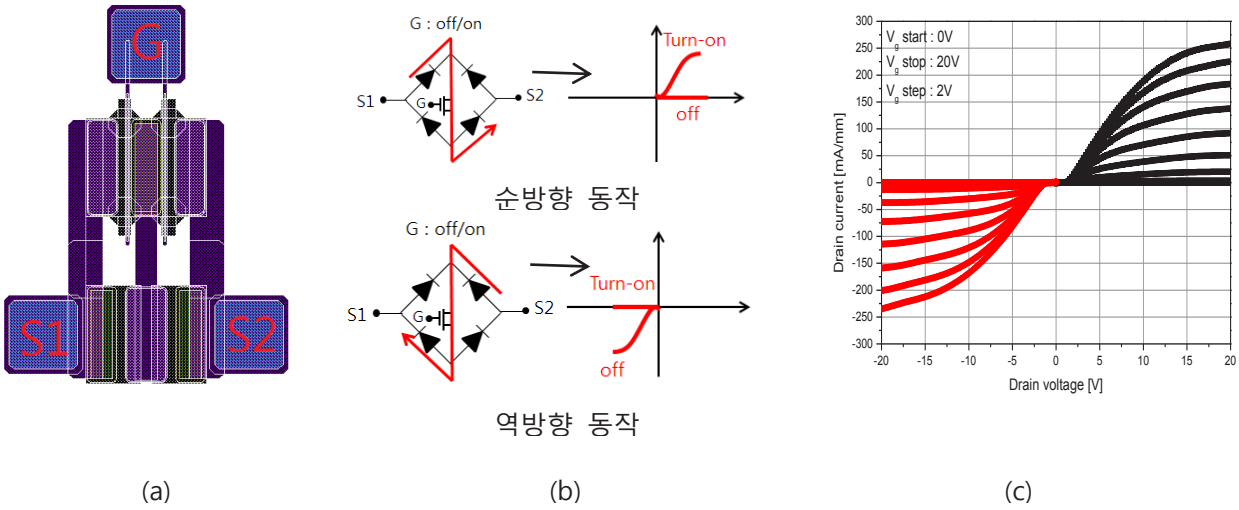
질화갈륨 이종접합소자는 높은 임계전기장, 전자이동도, 전하밀도를 가지고 있어서 차세대 전력반도체 소자로 주목을 받고 있다. 본 연구에서는 가전기기나 산업용 기기에서 사용되는 전력시스템의 전력변환 효율을 높이기 위한 양방향 스위치를 구현하기 위하여 AlGaN/GaN-on-Si 기반 FET 에 다이오드 브릿지를 내장시킨 형태의 전력소자를 제안하였다. 제작된 AlGaN/GaN FET 는 SiO_2 기반의 MOS 게이트와 채널 식각 방식을 활용하여 normally-off 특성을 구현하였으며, 이 때 순방향과 역병향 동작 모두에서 ~6V 정도의 문턱전압을 보였고 게이트 전압이 +20V 일 때 최대 드레인 전류밀도는 순방향과 역방향 모두 ~250mA/mm 수준이다. 본 연구에서 제안된 양방향 특성을 갖는 다이오드 브릿지 내장형 AlGaN/GaN FET 는 matrix converter 등에 유용하게 활용될 수 있으며, 하나의 게이트 드라이버 만을 이용함과 동시에 다이오드 내장형 형태를 취하고 있어서 궁극적으로 칩 크기를 줄이고 기생성분을 최소화 할 수 있는 장점을 가지고 있다.



(a) (b) (c)

그림 1. (a) 제작된 다이오드 브릿지 내장형 AlGaN/GaN 양방향 스위치 소자 레이아웃, (b) 다이오드 브릿지 내장형 AlGaN/GaN 양방향 스위치 동작 원리 (c) 제작된 양방향 스위치 전류-전압 특성

고효율 및 고속 스위칭용 GaN 기반 부스트 컨버터

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[1] 한국전자통신연구원, 정보통신 부품소재연구소, GaN 전력소자연구실
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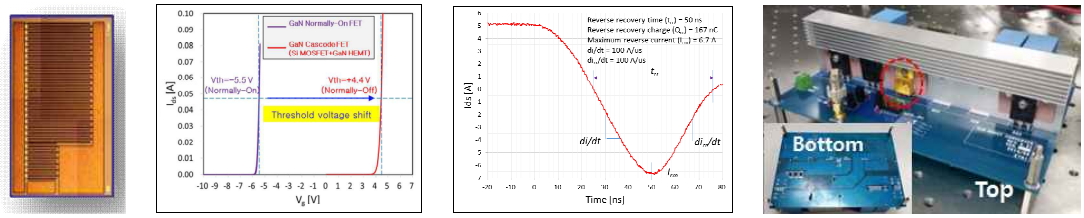
최근 에너지 효율에 대한 관심이 커짐에 따라 고효율 전력반도체에 대한 연구가 활발히 이루어지고 있다[1-2]. 본 논문에서는 고효율, 친환경 화합물 반도체인 GaN 전력반도체 소자 및 이를 적용한 부스트 컨버터에 대해 소개하고자 한다. 그림 1 은 실리콘 기판 위에 제작된 GaN HEMT 의 칩 사진과 측정된 Static/Dynamic 특성, 그리고 TO-254 로 패키지된 GaN HEMT 소자를 적용한 DC-DC 부스트 컨버터의 사진을 보여준다. GaN HEMT 소자의 게이트 폭은 46 mm 이며, 소자의 전체 사이즈는 3.2 x 1.8 mm^2 이다. GaN HEMT 는 기본적으로 Normally-on 특성을 보이므로, Gate recess 공정을 사용한 Normally-off 소자 연구와 동시에 Si-MOSFET 과 Normally-on GaN HEMT 를 집적한 캐스코드 GaN FET 를 연구하고 있다. GaN 소자의 측정된 V_{th} 는 4.4 V 이며, t_{rr}, Q_{rr}, 그리고 I_{rm} 은 각각 50 ns, 167 nC, and 6.7 A 이다. 이를 적용한 부스트 컨버터는 스위칭 속도와 Duty cycle 제어가 가능하도록 제작되었으며, 출력 전력, 스위칭 주파수 및 Duty cycle 에 대한 컨버터 효율 등의 상세한 측정결과는 최종 논문과 발표에서 소개될 예정이다. 이 결과는 GaN 기반 전력소자의 설계, 공정부터 Discrete 패키지 및 컨버터 시스템까지 일련의 모든 과정을 수행한 국내 최초의 성과라는 점에서 큰 의미가 있으며, 이는 IT 기기, 가전제품 및 자동차 등 산업 전반에 걸쳐 적용이 가능하다.



(가) (나) (다) (라)

그림 1. (가) GaN HEMT 소자 (나) V_{th} 및 (다) Dynamic 측정 결과 (라) 부스트 컨버터

[1] J. Popovic, J. Ferreira, J. Wyk, and F. Pansier, CIPS (2014)
[2] R. Mitova, et al., IEEE Trans. Power Electron. Vol 29, No. 5, pp. 2441-2452, May 2014

감사의 글: 본 연구는 미래창조과학부에서 지원하는 '스마트 데이터 센터용 차세대 광-전 모듈 기술' 사업(no. 10038766)으로 수행되었음.

Antireflective Subwavelength Structures for High Efficient III-V Photovoltaics

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Antireflective layers fabricated with subwavelength structures (SWSs) dramatically improve the performance of solar cells by gradually changing the refractive index at broad wavelengths [1]. Conventional SWSs are fabricated by dry etching nano-scale patterns after complicated electronic beam or nano-imprint lithography. In this work, we used a wet-based metal-assisted chemical etching to fabricate the SWSs for high efficient GaAs solar cells, which have optimum band gap energy according to the Shockley-Queisser theoretical efficiency limit. Nano-scale patterns were formed after agglomerating gold nanoparticles. Metal-assisted chemical etching followed by metal agglomeration is a new cost-effective anisotropic etch processes [2]. We optimized the feature size of SWSs by controlling agglomeration temperature and etching time. A significant reduction in the reflectance was acquired for 1.1μm height of SWSs. The specular reflectance, which is important for high quantum efficiency of solar cells in a wide angle of incidence, exhibited a strong dependency on the angle of incidence. Results showed that extremely low total reflectance of 4.5% and average reflectance of below 5% up to angle of incident of 50 degrees in the wavelength range of 200-850nm. GaAs SWSs fabricated with metal-assisted chemical etching combined with metal agglomeration have dramatically improved the reflectance characteristics of antireflective layer with simple and low-cost processes.

[1] H. K. Raut, V. A. Ganesh, A. S. Nair, and S. Ramakrishna, Energ. Environ. Sci. 4, 3779 (2011).
[2] Z. Huang, N. Geyer, P. Werner, J. de Boor and U. Gösele, Adv. Mater. 23, 285 (2011).

Anti-reflective and Electrical Characteristics of Al-doped ZnO Nanorods for Chalcogenide Thin-Film Solar Cell

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Transparent metal-doped ZnO having a high conductivity has been considered as an alternative to indium-tin-oxide (ITO), a typical transparent conductive oxide (TCO), which is used as an window electrode for solar cells and displays. Besides both transparency and electrical conductivity, anti-reflectivity is required in the window electrode for solar cell application. In our previous work, the simplest strategy to get an omnidirectional anti-reflective layer for chalcogenide thin film solar cell in which the metal-doped ZnO film has been used as a top transparent electrode is to directly grow ZnO nanorods (NRs) on it using a low temperature hydrothermal process [1]. However, the electrical contact type of ZnO NRs normally showing the n-type semiconducting property, with the screen printed silver commercially used for current collecting top electrodes, is Schottky. This high contact resistance originates from the electrical Schottky barrier between the n-type ZnO NRs and the silver. In this work, this serious problem was solved by doping aluminum in the ZnO NRs to change the electrical contact type from Schottky to Ohmic for various Al-doping concentrations while maintaining the excellent omnidirectional anti-reflecting performance.

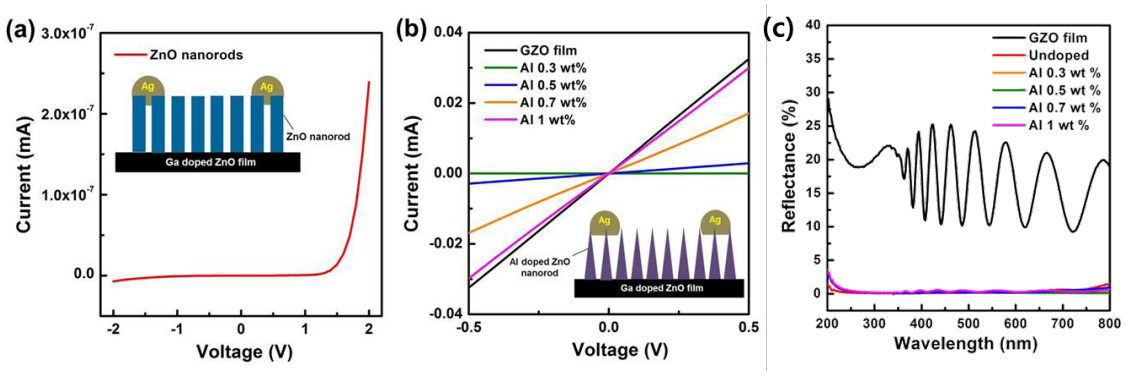

Fig 1. I-V characteristics of (a) Ag/ZnO NRs/Ag configuration with 0 wt% (b) with different Al-doping concentrations from 0.3 to 1 wt%. (c) Total reflectance of GZO film, undoped ZnO NRs and Al-doped ZnO NRs

[1] B.-K. Shin, T.-I. Lee, J. Xiong, C. Hwang, G. Noh, J.-H. Cho and J.-M. Myoung, Sol. Energ. Mat. Sol. 95, 2650 (2011).

Realistic Circuit Model of an Impact-Based Energy Harvester

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Energy harvesters and conversion circuits have been presented recently [1]. Because characteristics of harvesters depends on conversion methods, structures and so on, a specific model for the harvester is needed to design optimized interface circuits. We have previously proposed an equivalent circuit model of an impact-based piezoelectric energy harvester [2]. In this work, we present an improved circuit model that reflects realistic operating conditions, i.e. non-periodic movements with varying strength. The harvester consists of a movable ball within a case and a cantilever-type beam covered with piezoelectric material. When the harvester is shaken, the ball repeatedly hits each sidewall of the case until kinetic energy of the ball dissipates. When the ball strikes a sidewall, electrical signal is generated and attenuated exponentially. The model was composed a R_{d1}-L_m-C_k branch, a R_{d2}-C_p branch, a transformer and a voltage source. In contrast to previous modeling methods with a sinusoidal voltage source, the voltage source in our model generates pulses at irregular interval. Pulses are modeled as an exponentially decaying sine wave with varying amplitudes. The voltage source was modeled in Verilog-A and the other parts are modeled in Spice. This model was verified with test results with a resistive load. Simulation results show good agreement with measured data both in single-pulse response and long-time responses at irregular movements.

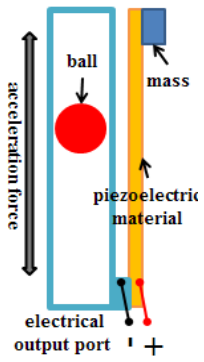

Fig 1. A schematic of the harvester.

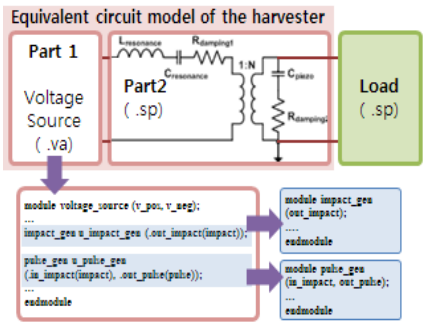

Fig 2. A circuit model using Verilog-A and Spice

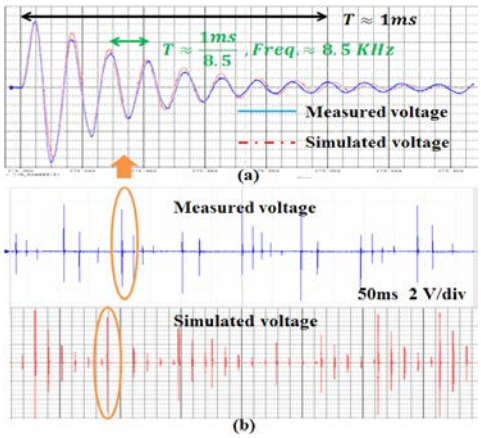

Fig.3 Measured vs. simulated signals in (a) single-pulse and (b) long-time responses.

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[2] S. H. Kim, S. Ju, C. H. Ji, and S. J. Lee, PowerMEMS2014 (2014)

Graphene as interfacial layer for improving cycle performance of Si nanowires in lithium ion battery

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Abstract

One of major issues that still challenges the commercial application of silicon (Si)-based anode materials for next generation lithium-ion batteries (LIBs) is pulverization during Li ion cycling, which leads to fast performance degradation. The anode based on Si nanowires (SiNWs) directly grown on current collector has been proven to allow lateral relaxation and thereby reduce pulverization. However, even with the improved designs, SiNWs based structures still exhibit limited cycling stability for extended numbers of cycles, because of underlying thin Si films formed simultaneously during the NW growth which delaminated and were disconnected from current collector even in the early stages of cycling. Here we propose a facile method to sharply reduce the formation of Si thin film by introducing graphene interfacial layer between SiNWs and current collector. In this situation, formation of the parasitic Si thin film has been almost avoided except some isolated Si islands formed around the defects and grain boundary of graphene. Consequently, we demonstrate significantly enhanced cycling stability for SiNW-based LIB anodes, with retentions of more than 70% and discharge capacity over 100 cycles. We believe this approach can be used in other anode materials and expedite its commercial application of Si in the near future.

Key words: Silicon, graphene, interface, lithium ion batteries

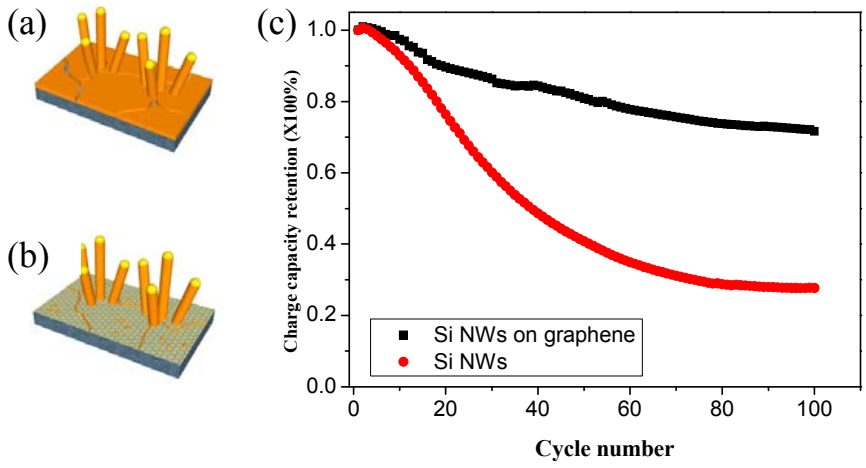

Figure 1: Schematic diagrams of Si NWs electrode morphology after battery test on (a) bare and (b) graphene covered stainless steel substrate with (c) charge capacity retentions.

Thin $Hf_xZr_{1-x}O_2$ Films (x=0.1-0.4) for a Monolithic Device for Various Energy-related Applications

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In this presentation, antiferroelectric (AFE) $Hf_xZr_{1-x}O_2$ (HZO, x=0.1-0.4) thin films are reported as new Si-compatible materials for a monolithic device for pyroelectric energy harvesting, electrocaloric cooling, electrostatic energy storage, and infrared sensing. $Hf_{0.2}Zr_{0.8}O_2$ and $Hf_{0.3}Zr_{0.7}O_2$ films could work as pyroelectric energy harvesters using the Olsen cycle with the harvested energy densities (HEDs) of 11.5 and 5.7 J/cm^3 cycle[1], which are ~7.6 and ~3.7 times larger than the largest value to date.[1] The electrocaloric effect (ECE) of HZO films was also firstly examined, and the maximum ΔT values of the $Hf_{0.2}Zr_{0.8}O_2$ and $Hf_{0.3}Zr_{0.7}O_2$ films were 13.4 (at 307K) and 9.8 K (at 448 K), respectively.[1] The wide temperature range for the large ECE of the HZO films are expected to be promising for the actual cooling cycle with large magnitude of the reversible work. Moreover, the large capacitance of the HZO films due to the field-induced transition between the ferroelectric and AFE phase can be used for electrostatic energy storage and high-charge capacitors. They showed the large energy storage density (ESD) up to ~46 J/cm^3, and the ESD value did not decrease with increasing temperature up to 175 ^{o}C, which was in fact limit of our measurement system.[2] Furthermore, the k^2 and F_v values, which are the figures of merit for conventional pyroelectric energy conversion and infrared detection for thermal imaging, of the $Hf_{0.2}Zr_{0.8}O_2$ film were 24.4x10^{-3} and 32.0x10^{-2} m^2/C, respectively, which prove that $Hf_{0.2}Zr_{0.8}O_2$ is also a promising material for these applications.[1] Moreover, they could be deposited conformally and uniformly using ALD which is appropriate for the nanostructured template. From these results, thin HZO films are believed to be a promising candidate for the new material for a monolithic device for various energy-related applications.

[1] M. H. Park, H. J. Kim, Y. J. Kim, T. Moon, K. D. Kim, and C. S. Hwang, Nano Energy, accepted (2014).
[2] M. H. Park, H. J. Kim, Y. J. Kim, T. Moon, K. D. Kim, and C. S. Hwang, Adv. Energy Mater. Early view article, DOI: 100.1002/aenm.201400610 (2014).

Proton irradiation effects on Normally-off AlGaN/GaN MISHFETs

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GaN-based transistors are excellent candidate for high voltage and high frequency applications thanks to GaN's superior material properties such as wide bandgap and high saturation velocity. They are also suitable for space communication systems which require radiation hardness for robust reliability [1]. Recently, many researches are in progress to realize normally-off operation of AlGaN/GaN HFETs for high power switching application [2, 3]. Normally-off AlGaN/GaN MISHFETs and conventional HEMTs fabricated on the same commercial wafer were irradiated with 5 MeV protons. After irradiation, both devices indicate the positive shift of the threshold voltage (V_{th}). V_{th} shift was increased as the irradiation doses were increased. No degradation on gate leakage characteristics was observed. TLM measurement shows the increase of sheet resistance. The increase of density of states was detected by DIF (Differential subthreshold Ideality Factor) technique. The positive shift of V_{th} is the result from the influence of acceptor-like traps generated by proton irradiation.

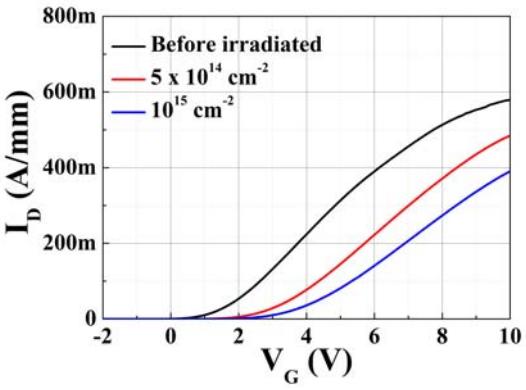

Fig. 1. The transfer characteristics as the irradiation doses were increased.

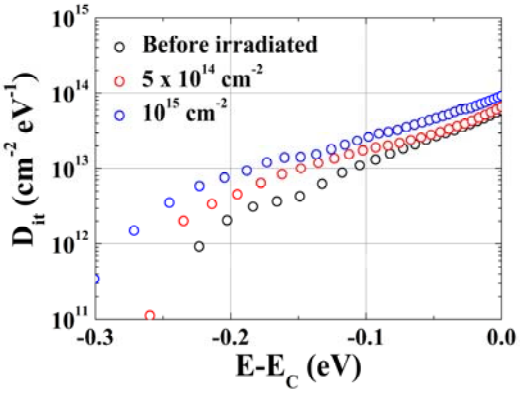

Fig. 2. Extracted D_{it} as the irradiation doses were increased.

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Probabilistic detection sensitivity of localized surface plasmon resonance biosensing

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A localized surface plasmon resoance (SPR) biosensor has been widely used to detect biointeractions of interest. The characteristics of detection sensitivity has been studied for ultimate moleculare detection *label-free* [1]. We studied the detection sensivity in a localized SPR biosensor based on the probablisitic behavior of target molecules using poisson distribution. Defined as an overlap energy integral between near-field intensity and permittivity, optical signature was calculated in three detection models of non-specific, non-colocalized and colocalized detection shown in Fig. 1(a-c). The near-field was obtained from randomly subcontinuous silver medium by rigorous coupled wave analysis. The perimittivity of general biomolecules (refractive index = 1.366) or buffer solution (refractive index = 1.33) was used. The signature was proportional to target size and concentration as shown in Fig. 1(d), which was common to the three models, among which colocalized detection showed the largest optical signature. The relative confidence interval related the certainty of the signature and colocalized detection was the smallest (see Fig. 1(d)), which suggested that the limit of detection can be improved by more than four orders of magnitude by colocalized detection.

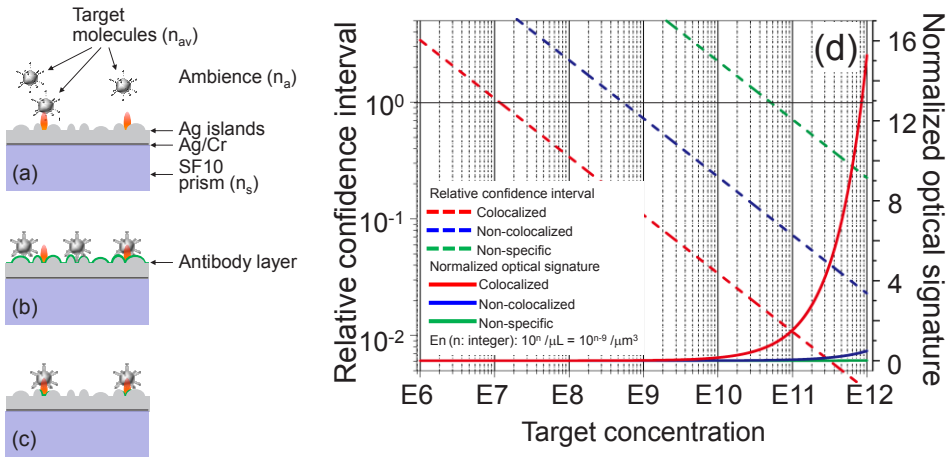

Fig 1. (a) Schematic of non-specific detection (b) non-colocalized (c) colocalized (d) relative confidence interval and normalized optical signature in three models

[1] Y. Oh, W. Lee, Y. Kim, and D. Kim, Biosens. Bioelectron, 51, 401-407 (2014)

Ultrasensitive protein detection using biologically-sensitive field-effect transistors (BioFETs) with multiple Si-nanowires

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Silicon nanowire (Si-NW) BioFETs have emerged as a versatile sensor platform for ultrasensitive and label-free detection of various ions and proteins [1]. The chance of binding events between antigen and antibody could increase by enlarging the sensing area. In this presentation, we fabricated 20 parallel-connected straight nanowires and measured the biosensing characteristics. The multiple nanowires (MN) BioFETs were fabricated using top-down approach and have been demonstrated superior sensing properties in detection of cardiac troponin I (cTnI) biomarker. After immobilization of antibodies (Abs) on the multiple nanowire surfaces, the attachment of Abs was analyzed through atomic force microscope (AFM). Non-specific binding test was conducted through detection of C-reactive protein (CRP) to demonstrate selectivity of devices. The MN BioFETs showed excellent characteristics in terms of selectivity and sensitivity. The limit of detection (LOD) of the device is calculated as low as ~10 pg/mL level which is 20 times lower compared to current clinical methods [2]. Analysis of low frequency noise (1/f) at various stages of biosensing was also conducted.

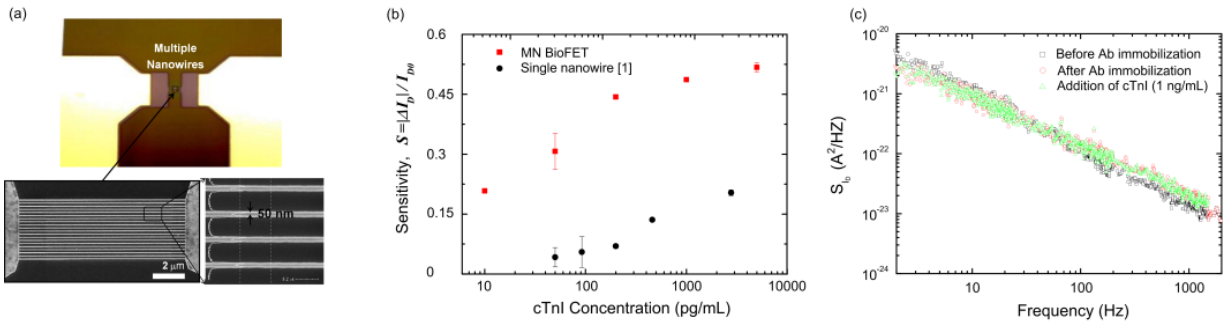

Fig 1. (a) the MN BioFET device, (b) Sensitivity vs. cTnI concentration, (c) 1/f noise characteristics

[1] T. Kong, R. Su, B. Zhang, et al., Biosensors and Bioelectronics, 34, 267 (2012).
[2] V. S. Mahajan and P. Jarolim, Circulation, 124, 2350 (2011).

Design and fabrication of vertical nanoslit fluid channel array for high volume flow application

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Thesedays, nanofluidic devices have been studied for various biological application including DNA streching, ion concentration, and nanoparticle based protein detection [1, 2]. Generally, the volume flow of the nanofluidic device is very low because the small dimension of the nanochannel dramatically increase hydraulic resistance. Therefore, nanofluidic device for high volume flow application such as nanoparticles filtration is required. In this paper, we developed noble nanofluidic device which has large numbers of nanoslit (300 nm) pattern on a silicon oxide (SiO_2) membrane for high volume flow application. We studied the relation between the number of nanoslits and the volume flow rate using FEM simulation and numerical calculation. And then, the volume flow of the proposed nanofluidic device was measured by using pressure-driven pump system and compared to the theoretical values. This study will be helpful to design a nanofluidic device for high volume flow application and understand the relation between the number of nanochannels and hydraulic resistance.

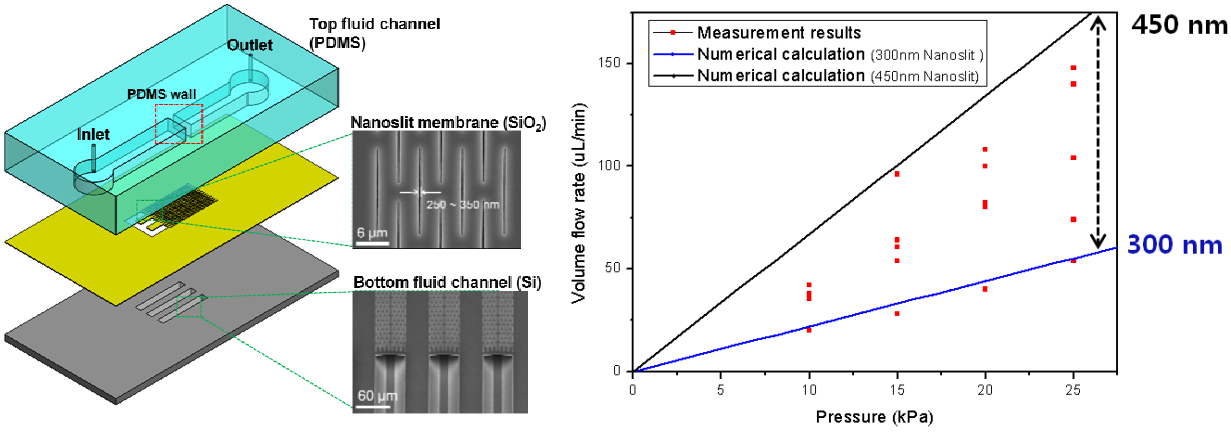

Fig 1. Schematics of the nanoslit fluidic device and the volume flow rate measurement

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Influence of Buffer Dilution on the Sensing Performances of the Silicon Nanowire Field-Effect Transistor Sensors

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Silicon nanowire FETs (Si-NW FETs) are widely used as sensors due to their high sensitivity, high selectivity and good compatibility to integrated CMOS technology [1]. For the liquid-based operation of the Si-NW FET, the change in buffer concentrations can affect the sensing performances. In this presentation, we have experimentally investigated the influence of buffer-dilution on the characteristics of the Si-NW FETs. Phosphate-buffered saline (PBS) with various buffer concentrations was prepared for detecting the pH and bio-molecules. The result showed that the sensitivity increases as the buffer concentration decreases for bio-molecule detection, while the pH sensitivity of the Si-NW FETs is insensitive to the buffer solutions. The Debye length (λ_D) of the buffer solution can be a crucial factor to detect biomolecules using FET sensors. For the buffer solution with high ionic strength, λ_D becomes shorter than the distance between the sensing membrane and the target-molecules so that the charges of target-molecules are screened out [2]. For the pH sensing, however, small hydrogen ions are bound close to the membrane surface and are detected at even higher buffer concentration. Those results indicate that the concentration of buffer solution should be carefully provided depending on the target molecules in liquid-based FET-sensor applications.

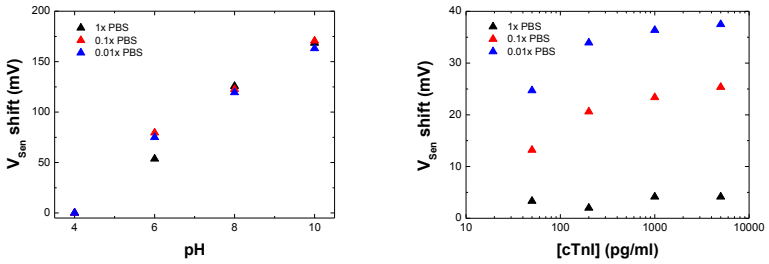

Fig 1. V_{Sen} shift of Si-NW FET as the pH and [cTnI] varies for various buffer concentrations

[1] M. J. Schöning and A. Poghossianb, *Analyst*, 127, 1137–1151 (2002).

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Biosensing comparison between dry and wet environment in silicon nanowire transistor

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In this paper, we report sensitivity difference between dry and wet environment in biosensing experiment. Since the dielectric constant of water is higher than that of the air, the biosensing sensitivity varies in accordancd with surrounding conditions of SiNW [1]. Through the charged polymer reaction experiment in SiNW, we were able to obtain the result elucidating that the threshold voltage (V_T) shift in water is smaller than that of the air. Furthermore, we have analyzed the sensitivity by changing the electrolyte concentration in the wet condition, and confirmed that the V_T shift increases in low-concentration condition due to the Debye length [2]. Our study led us to anticipate that the results would be contributing to advanced biosensing experiment in the future.

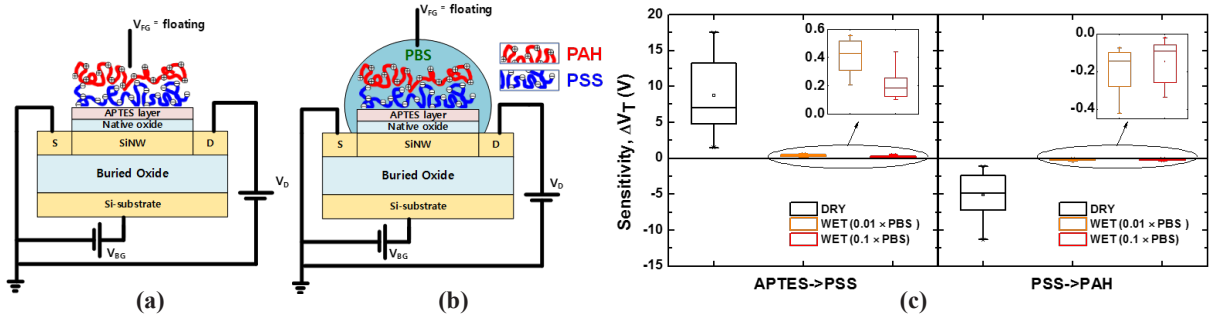

Fig 1. The measurement schematic in (a) dry, and (b) wet (0.1 × PBS) environments after reacting to PAH polymer. (c) The measured V_T shift depending on the environment surrounding SiNW before and after the reaction to charged polymer PSS and PAH.

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Acknowledgements

This work was supported by BK21+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No. 22A20130000042) and National Research Foundation of Korea through the Ministry of Education, Science and Technology under (Grant No. 2014063597).

Sensing Property of FET-type Gas Sensor Having a Sensing Material of ZnO Film Prepared by ALD

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Recently, there has been a growing interest in gas sensors to detect noxious gases causing lung diseases. A promising FET type gas sensor based on *Si* MOSFET (Metal Oxide Semiconductor Field Effect Transistor) having a horizontal floating gate (*FG*) has been proposed to achieve low cost, low power, high reliability, and small size [1]. In this work, we investigate sensing property of *Si* MOSFET-type gas sensor having a horizontal *FG* and a 10 nm thick n-type *ZnO* (Zinc oxide) prepared by atomic layer deposition (*ALD*) as a sensing layer. The sensing layer is formed between the control gate (*CG*) and the *FG*. Fig. 1 (a) and (b) show schematic top and 2-D cross sectional views of the fabricated gas sensor, respectively. The device reads out work-function (*WF*) change in the sensing layer butted to the control gate, when the device is exposed to a target gas. Fig. 2 shows transfer (I_D-V_{GS}) curve for the fabricated gas sensor exposed to N_2 (Nitrogen) gas ambient as a reference and 1 ppm NO_2 (Nitrogen dioxide). The I_D of the gas sensor based on p-type MOSFET increases when the device is exposed to NO_2. The NO_2 is an acceptor-type gas on the *ZnO* [2]. When the gas sensor is exposed to NO_2 gas, the gas molecules are absorbed on the surface of *ZnO* film and extract electrons from the *ZnO* and become negatively charged at the surface. It creates a positive space-charge (depletion) region in the *ZnO* and increases *WF* of the *ZnO*. The increased *WF* shifts threshold voltage of the device into the positive bias direction and increases sensing current [2], [3].

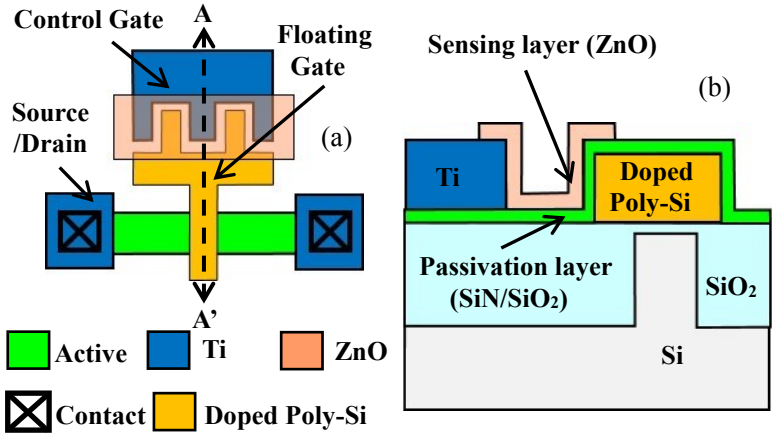

Fig.1. Schematic (a) top view of the fabricated gas sensor and (b) its 2-D cross sectional view cut along A–A'.

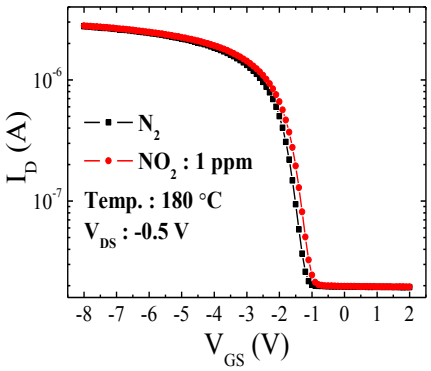

Fig.2. Transfer (I_D-V_{GS}) curve for the fabricated gas sensor exposed to N_2 and NO_2 gases at 180 °C.

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Acknowledgement

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Inkjet-Printed Stretchable Electrodes Based on Nano-Particle Materials

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One of the strategies that has been widely explored to implement stretchable electronic system is based on a platform containing rigid and soft areas, where active devices are located on the rigid area and they are connected by the stretchable interconnect electrodes. Conductive nano materials can be easily formed into inks so that they can be printed on flexible or stretchable platform, being used as stretchable interconnection electrodes. My group is focusing on inkjet printing process of such materials and has focused on building "Printed System on a Stretchable Platform." In this talk, our efforts on the inkjet-printed interconnection electrodes will be presented. We are currently using silver (Ag) nano particle ink, conductive single walled carbon nano tube (SWCNT) ink, and nickel nano particle composite. For stretchable electrode development, three key parameters of conductivity, stretchability, and cycling stability must be considered. The printed Ag electrodes showed high initial conductivity but a limited stretching performance issue, which can be potentially solved by introducing vertically wavy structure. The printed SWCNT electrodes showed relatively high resistance but showed little resistance changes during the cycling test even with 100% tensile strain. For composite electrodes, they showed negatively strain-dependenct resistance, which was used for extremely stretchable electrodes combined with the inkjet-printed Ag electrode and for resolution-sustainable lighting devices. Based on our experience, Ag electrode is good for applications where relatively low (<15%) stretchability but high conductivity are required while SWCNT and composite electrodes are good for stretchable systems requiring very high stretchability.

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Resistive memory and switch device for stackable scalable 3D nanoscale memory

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The era of fast-moving information and computer technologies has been driven by silicon CMOS technology. Currently, the two basic components of random access memory devices are the select switch and storage node. It is required to improve the performance of both of these elements in order to achieve extreme high density memory. Furthermore both components will be required to be compatible with technologies such as three-dimensional cell stacking, multi-level cell, endurance and scaling down below 10 nm node. Oxide based devices have been kept in focus because of its possibility of emulating organic brain functions and reconfigurable functions on Si circuits. Resistive random access memory (RRAM) combined with stackable select devices has been considered to be one of the most promising candidates to overcome scaling limits of the conventional memory due to its scalability. In this presentation, the RRAM materials, a new switch devices and its architecture will be discussed.

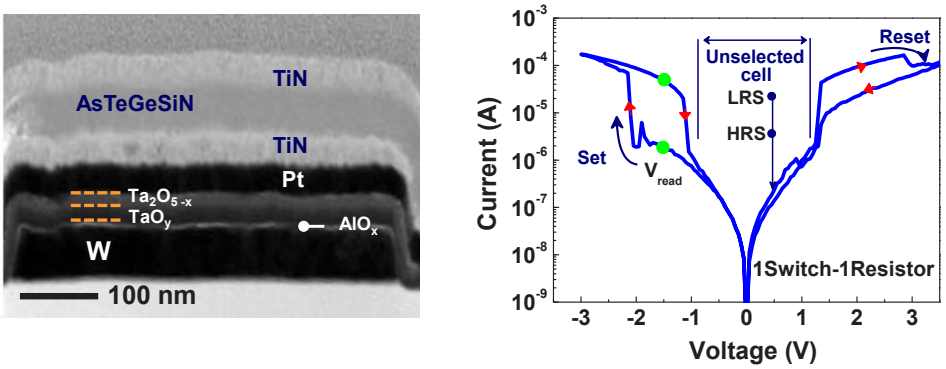

Figure 1. A cross-sectional TEM image of the combined switch and memory device structure and its I-V characteristics.

[1]M.-J. Lee et al., Nature Communications 4, 2629 (2013)

Conductive Filaments Control of Resistive Memories Employing Self-Assembled Silica-Nanodots for Switching Stability Improvement

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Resistive random access memory (ReRAM) has been a promising candidate for the future nonvolatile memories (NVM). Resistive switching (RS) in metal-insulator-metal (MIM) structure is generally assumed to be caused by the formation/rupture of nanoscale conductive filaments (CFs) under the electric potentials. However, its critical issue for a core memory application is the insufficient repeatability of operating voltage and resistance ratio. Here, we present an innovative methodology based on the self-assembly of a block copolymer (BCP), uniformly forming an insulating SiO_x nanostructure, to control the CF growth in the unipolar NiO resistive memory for the uniformity improvement. In this way, the standard deviation (SD) of set and reset voltages was markedly reduced by 76.9% and 59.4%, respectively. The SD of high resistance state (HRS) also decreased significantly, from 6.3 x 10^7 Ω to 5.4 x 10^4 Ω. In addition, we report direct transmission electron microscopy (TEM) analyses, which are metallic Ni filament observations in NiO active material and controllable CF growth by the SiO_x nanodots (SiO_x-NDs). The simulation results theoretically support the filament control mechanism by the locally blocked SiO_x-NDs.

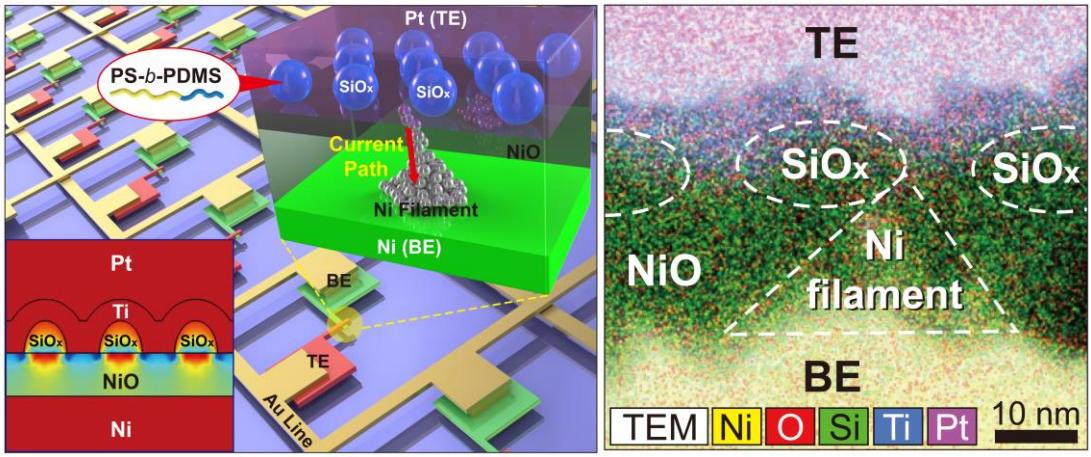

Fig 1. Structure and simulation of NiO resistive memories inserting SiO_x-NDs and its TEM/EDS analysis for the Ni filament observation.

Transferred partially-grown patterned graphene layer for charge-floating gate in organic non-volatile memory transistors

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Graphene has attracted much attention from many researchers because of its unique electrical properties and potential use for electrical applications. Among many applications, graphene charge storage element in memory device is being studied for its low dimensionality [1].

In this work, we investegated memory aplication for graphene as charge floating gate. For graphene charge floating gate, we demonstrate a simple synthesis method producing a graphene layer with discrete patterns, where the growth time was controlled during the conventional CVD growing process. We fabricated organic nonvolatile memory transistors with bottom-gate/top-contact structure using pentacene and polystyrene as active and charge tunneling dielectric layer as shown in Fig. 1(a). For charge floating gate, we transferred the partially grown graphene layer from the copper film onto the silicon dioxide gate dielectric layer. The fabricated organic memory transistor showed anti-clockwise hysteresis in transfer curves, which means that the positive charges are effectively trapped onto the graphene floating gate during the negative direction sweep and they induce early turn-off during the following positive direction sweep. Our devices exhibited a large threshold voltage shift (~ 28 V), a reasonable program/erase cycles endurance of >10^2 times, and an estimated long data retention time of >1 year. Details of the device performance and fabrication process will be further discussed at conference.

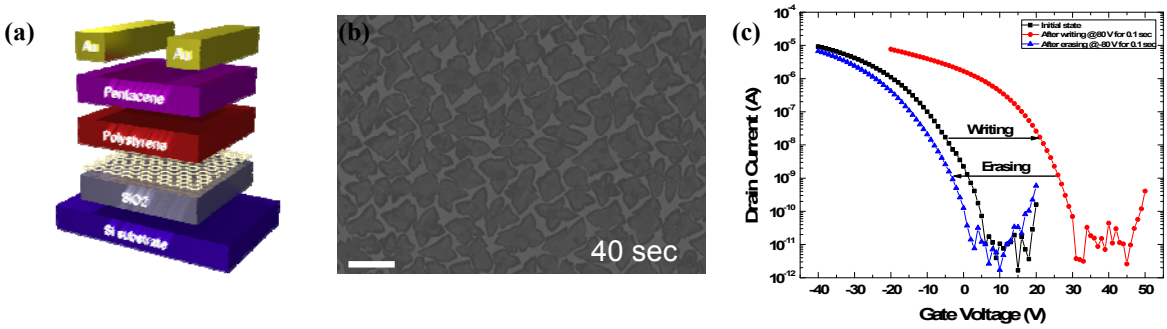

Fig 1. (a) Schematic of organic non-volatile memory transistor (b) SEM image of partially grown

graphene for floating gate (c) Memory properties of organic non-volatile memory transistor

[1] J. C. Scott and L. D. Bozano, Advanced Materials, 19, (2007)

Packaging Completed Ultrathin Si-based Flexible NAND-type Flash Memory

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Flexible devices have been studied widely owing to its thin, light-weight, foldable and non-breaking properties and broad research on flexible device fabrication has been conducted. In contrast, further investigation on flexible packaging compatible with the bending condition has to be conducted since the thin flexible device is vulnerable to external force and requires special equipment for measurement. In this study, we fabricated packaging completed ultra-thin Si based flexible device utilizing flip-chip (FC) bonding technology using anisotropic conductive film (ACF). By flip-chip bonding the device on the flexible substrate followed by thinning process or by the opposite order, we demonstrated ultra-thin silicon based flexible NAND flash memory array with packaging process completed for the first time. The demonstrated flexible NAND flash memory array showed mechanical stability even in 5mm bending radius, and also showed fine electrical characteristics such as read/write/erase operation and endurance/retention properties as is the rigid device, showing the easiness and the usefulness of the method. Furthermore, we are also investigating the roll-packaging process applicable to this method for continuous mass production.

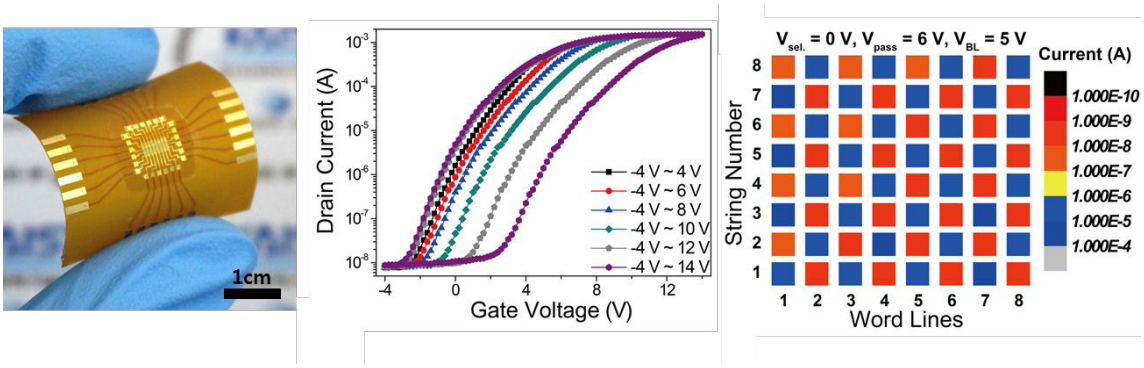

Fig 1. Ultrathin Si-based flexible NAND flash memory and its electrical data

Liquid cooling system with TSV for high power 3D packages

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3D 기술은 성능 향상, 소형화, 배선 길이 감소, 전력 손실 감소, 이종 접합 가능 등 많은 이점을 제공하지만, 전력 전달, 전기적 테스트, 열관리는 아직 해결해야 할 과제로 남아 있다 [1]. 특히, 고성능 소자의 전력밀도가 100W/cm^2 이상으로 증가함에 따라 열관리는 주요 핵심 기술로 부각되었다 [2]. 3D 소자의 경우 면적당 전력 밀도가 크고, 열 유속이 높기 때문에 기존의 heat sink 나 TIM 으로는 소자의 열 문제를 해결하는데 한계가 있다. 이에 최근에는 액체 냉각과 같은 능동 냉각시스템에 관한 연구가 활발히 진행되고 있다 [3][4]. 본 연구에서는 TSV 와 microchannel 을 이용하여 액체 냉각 테스트 시편을 제작한 후 pressure drop, water flow rate 과 flowing 형상을 분석하였다. TSV 와 microchannel 은 Si 웨이퍼에 DRIE 공정을 이용하여 제작되었으며, microchannel 크기는 100μm(W)x50μm(D)x200μm(S)이고, TSV 크기는 50~100μm(dia)x100~200μm(D)로 하였다. 제작된 TSV 와 microchannel, 그리고 테스트 시편의 단면사진을 Figure 1 에 나타내었다. 냉각 효율 산출을 위해 heater 를 이용하여 실온에서 300ºC 까지 시편을 가열한 후 적외선 현미경을 통해 측정 분석하였다.

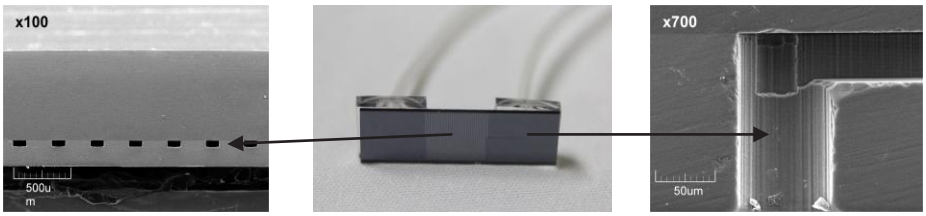

Figure 1. Fabrication of TSV and microchannel for liquid cooling

[1] E. Kim, “Overview of High Performance 3D-WLP”, Kor. J. Mater. Res. V17(7), 371-375 (2007)
[2] S. F. Al-Sarawi, D. Abbott, and P. D. Franzen, “A review of 3-D packaging technology,” IEEE Trans. Compon. Packag. Manuf. Technol. Pat B, vol.21 (1), 2-14 (1998)
[3] G. Y. Tang, S. P. Tan, N. Khan, D. Pinjala, J. H. Lau, A. B. Yu, K. Vaidyanathan, and K. C. Toh, “Integrated Liquid cooling Systems for 3-D Stacked TSV Modules”, IEEE Trans. Coomp. Packag. Tech, 33(1), 184-195 (2010)
[4] S. C. Mohapatra and D. Loikits, "Advances in liquid coolant technologies for electronics cooling", IEEE STMMS, 354–-360 (2005)

3D IC thermal management using Cu filled TSVs

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3D IC 디바이스에서 안정되고 정확한 전력전달은 디바이스 scaling 에 매우 중요한 체린지 중 하나이다. 디바이스가 scaling-down 됨에 따라 on-chip 전력 방출은 점점 심각해지고, 이는 디바이스의 열 신뢰성 문제를 일으키기 때문이다 [1]. 특히, 디바이스의 두께가 얇아지면서 hot spot 부분의 열관리 문제는 반드시 해결해야 할 핵심 기술로 부각되고 있다. ITRS 에 의하면 로직 디바이스 hot spot 의 경우 전력밀도가 500W/cm^2, 적층 메모리의 경우 300W/cm^2 으로 예측하고 있다 [2]. 디바이스의 열 관리 방법으로는 thermal interface material, thermoelectric, heat sink, liquid cooling, heat pipe, thermal via 등 많은 연구가 진행되고 있고, 본 실험에서는 구리(Cu)로 채워진 TSV 를 3D IC 의 열 관리 방법으로 연구하였다. TSV 사이즈는 8μm(dia)x40μm(D)이고, DRIE 공정, SiO_2/Ti/Cu barrier layer 증착, 그리고 Cu 전기도금을 통해 제작하였다. TSV 웨이퍼와 Si 기판 웨이퍼는 열 압착으로 본딩되었고, 열 방출은 point heating 방법으로 시편을 50°C, 100°C, 150°C, 200°C 로 가열한 후 적외선현미경으로 측정 분석하였다. Figure 1 은 적외선현미경으로 측정한 IR image 를 보여주고 있고, TSV 가 열 방출에 효과적임을 확인할 수 있다. 또한, 본 연구에서는 Si 두께와 적층 수가 열 방출에 미치는 영향도 분석하였다.

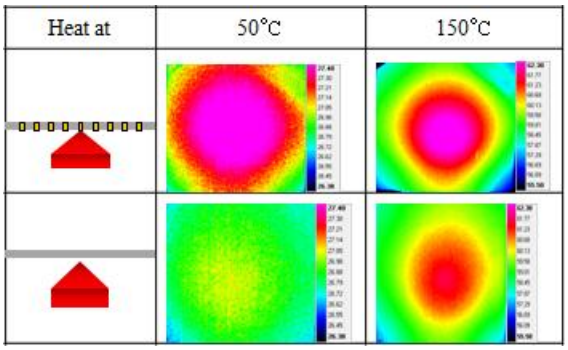

Figure 1. IR measurement of Si wafer with and without TSVs

[1] K. Oh, J. Ma, S. Kim, S. E. Kim, Interconnect Process Technology for High Power Delivery and Distribution, J. the Microelectron. & Packag. Soc., 19(3), 9-14 (2012)
[2] ITRS: http://www.itrs.net

The roughness reduction methods using Layer-by-Layer laminar structures on TSV sidewall

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The through silicon via (TSV) with 3D-IC stacked structure is continuously developed for high density at the same area, high performance by its shorter signal line, lower power consumption, chipper fabrication cost, and so on. DRIE (Deep Reactive Ion Etching) by Bosch process is the main method to mak high aspect ratio pattern easily and reduces process time. But this process can make scallop and porous surface which have the rough morphology on TSV sidewall. They can effect to post process of sidewall deposition and via filling. [1]

To solve this problem, layer-by-layer (LbL) flexible layers are deposited on TSV sidewall to make flat sidewall. The stack structure of LbL layers has been made by using PAH (polyallylamine hydrochloride) and PSS (polystyrene sulfonate), which are used with solution dipping method. [2, 3] Multilayers of LbL between TSV and Si pattern can enhance the various properties such like morphology reduction, mechanical flexibility and so on. As thicknesses of LbL is increased, sidewall morphology is decreased. Young`s modulus is continuously decreased because of flexible property of LbL multilayers

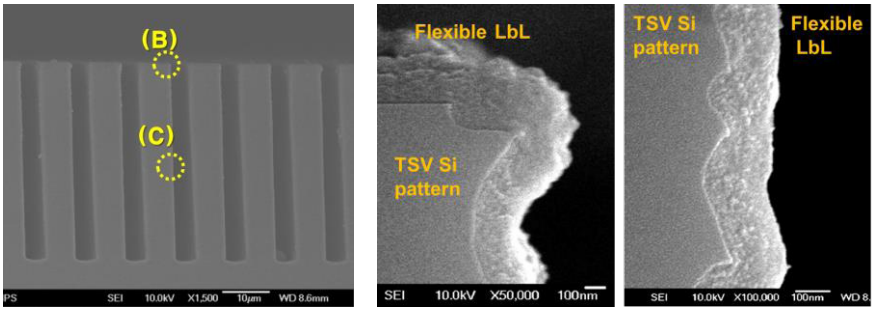

Fig1. FE-SEM images of TSV morphologies after LbL treatment
(a) LbL treated TSV pattern (b) Top edge part (c) Sidewall part morphology

[1] S-H. Seo, J-S. Hwang, J-M. Yang, W-J. Hwang, J-Y. Song and W-J. Lee, Thin Solid Films, 546, 14 (2013).
[2] J. Cho and K. Char, Langmuir, 20, 4011 (2004).
[3] S. S. Shiratori and M. F. Rubner, Macromolecules, 33, 4213 (2000).

Micro Solder Bump 에서의 Ag Contents 에 따른 영향성 검증

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High performance 및 low power consumption 제품에 대한 요구는 WIO (wide I/O) 또는 HBM (high bandwidth memory) device 와 같이 다수의 I/O 를 통하여 전체 signal transfer speed 를 향상 시키는 기술에 대한 관심을 증가시키고 있다. WIO, HBM 과 같이 제한된 Si 면적에 다수의 I/O 를 구현하기 위해서는 지름 20um 이하의 u-bump 를 통한 F/C (flip-chip) bonding 기술이 필요한데, 기존 F/C bump 대비 u-bump 기술의 특징은 상대적으로 적은 solder volume 에 의한 solder microstructure 변화에 있다. 따라서 본 논문에서는 지름 20um 의 u-bump 를 사용하여 Sn-Ag solder 조성 내 Ag 함량에 따른 u-bump microstructure 변화를 연구하였다. 연구 결과 solder 내 Ag 함량이 1.3wt.% 이하인 경우 groove 현상에 의한 abnormal bump 가[1], Ag 3.2wt.% 이상인 경우에는 needle-like Ag3Sn 상이 석출하는 것을 관찰하였다. 이러한 결과를 바탕으로 본 논문에서는 최적 Ag Composition Spec. Range 를 제안하였다.

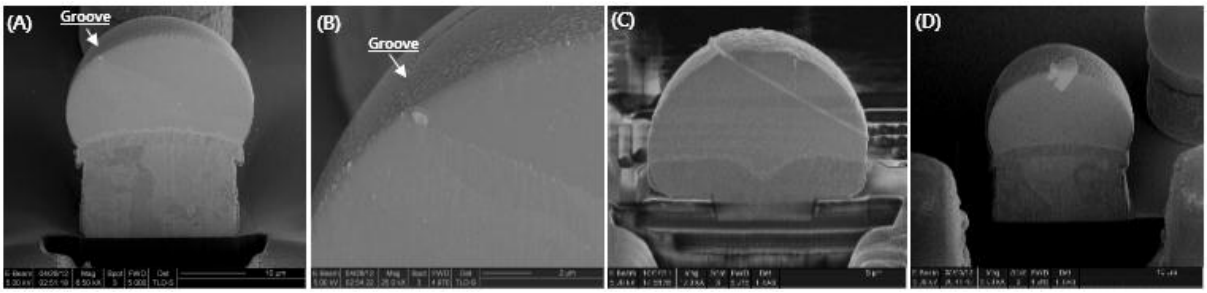

Fig.1 Groove Bump (A),(B)와 Ag3Sn 석출 (C),(D) Bump FIB SEM Image.

[1] Study on Sn-2.3Ag Electroplated Solder Bump Properties Fabricated by Different Plating and Reflow Conditions. C. K. Hsiung, C. A. Chang, Z. H. Tzeng, C. S. Ho, and F. L. Chien R&D Department of Wafer Bumping Technology. 2007

새로운 구조의 Ground를 이용한 Crosstalk 저감 연구

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최근 반도체 패키지의 고속화, 소형화, 다기능화로 인해 반도체 패키지 기판의 배선 집적도가 높아지고 있다. 데이터 전송을 위해 사용되는 신호의 성분이 높은 주파수 대역으로 점점 올라감에 따라 PCB 설계 시 누화(crosstalk)문제가 크게 대두되고 있다[1]. 발생되는 누화 잡음은 신호를 지연시키거나 시스템의 오작동을 유발하여 신호 무결성(signal integrity)에 큰 영향을 미치게 된다[2]. 본 논문에서는 누화를 줄이는 방법으로 전자기장을 격리시켰다. 격리 방법은 Ground(GND) Plane에 선로와 같은 방향으로 삼각뿔 모양의 패턴을 삽입하여 전자기장을 격리시키는 방법을 제안한다. ANSYS 사의 HFSS를 이용하여 시뮬레이션을 수행한 결과, 추가적인 GND 패턴의 효과로 누화는 크게 감소되었다. 누화가 감소되는 이유는 GND Plane에 추가한 삼각돌기로 인해 전자기장이 GND 방향으로 집중되고 집중된 전자기장만큼 다른 한쪽 신호선에 영향을 주는 전자기장은 감소하기 때문이다. 본 논문은 새로운 구조의 GND Plane을 제안하며 패키지 기판에서 배선의 고집적으로 인한 누화 문제를 저감 할 수 있음을 증명하였다.

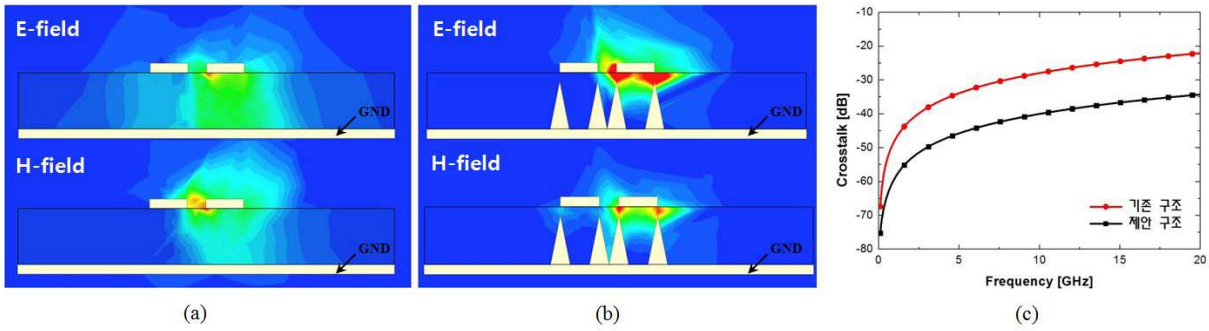

그림 1. (a)기존구조 (b)제안구조 (c)누화 특성 비교

[1] Jae-Kwon Han and Dong-Chul Park, KIEES, vol.18, no. 8, pp. 23-29 (2007)
[2] Jangteak Oh and Ikmo Park, KIEES, vol. 23, no. 7, pp. 774-783 (2012)

A Study of RDL Reliability Improvement with Developing New UBM Etchant

Min Ki Son, Sung Won Yoon, Jae Yong An, Il Hwan Cho, Jae Myun Kim, Nam Seok Kim
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습식 식각(Wet Etching)은 반도체 소자 제조 공정에서 Non Patterning 영역의 하부 Metal 을 제거하는 가장 보편화된 기술로써 특히 RDL(Re-Distributed Layer)과 CPB(Copper Pillar Bump)와 같은 WLP(Wafer Level Package) 시장의 급속한 발전과 다양한 미세 선폭 Device 의 개발에 의해 그 기술의 중요성은 증대되고 있다. 본 논문은 등방성(Isotropic) & 타이타늄(Ti) 식각의 특징을 가지는 Ti Etchant 특성 연구를 통해 WLP 에 적용되는 제품 군(RDL & CPB) 의 신뢰성을 만족 시키는 다 기능 UBM(Under Barrier Metal) Etchant 개발 측면으로 연구를 진행하였다.

현재 전 세계적으로 RDL 형성 시 금 배선을 형성하기 위해 채택하는 방식으로는 물리적 증기 증착법(PVD)을 이용한 Ti/Au UBM 박막 증착 후 포토 레지스트 Open 영역에 금 배선을 형성하고 Au/Ti Etchant 를 이용하여 습식 식각 방식으로 RDL Au Trace 를 형성한다. 식각 성능에 따라 절연층(Dielectric) 상부에 잔존 Metal 로 인하여 Package & Test 를 진행 시 Current leakage, DC Fail 등과 같은 품질 불량을 야기 시킬 수 있다. 따라서 이를 개선 하기 위해 Ti 식각 기술력을 확보하는 것이 핵심 이라고 할 수 있다.

본 논문에서는 Etchant Performance 향상을 위해 Etchant Base 별 특성 파악, 첨가제 구성(Al Damage Free 특성 구현: Chelating Agent, Galvanic Corrosion Inhibitor)를 통해 특성을 향상 시켰다. 개선 방식으로는 A-Type Base Ti Etchant 의 문제점(Etching After Ti ion peak, Ti/Al Selectivity, Etching Ti Dusting) 개선을 위해 Etchant Base 물성 변경(B-Type) & Chelating Agent 첨가(Ti Ion 간 척력 작용으로 Metal Dusting 방지 & Al Surface 에 Minus Ion 으로 대전되어 Barrier 역할로 Al Damage 방지)를 통해 해결 하였으며 Ti/Al Metal Galvanic Corrosion 에 의한 Damage 개선을 위해 Inorganic 계열 Alkali 혼합물 첨가(K + Alkali 혼합물 첨가로 Ionization Tendency 가 높은 특성을 기반으로 Corrosion 방지)로 문제점을 개선하였다.

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Al Metal Damage

Investigation of the Effect of Plasma Treatment on Electrical Contacts of Graphene

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It is well known that its electronic performance is limited by the contact resistance of the metal-graphene interface. For usual surface contact at the metal-graphene (M-G) interface, carrier injection takes place from the metal into the underlying graphene, followed by carrier transport into the channel region. However, it is understood that, the contact resistance (R_c) is mainly determined by chemical bonds and electronic structures at the M-G interface. Therefore, a process needs to be developed to facilitate efficient charge transport at the M-G interface so as to minimize R_c, and this requires the understanding on the difference in surface and edge contacts at the M-G interface. In this study, we demonstrate the use of a controlled plasma processing technique for edge-contacted graphene in which bonding between the edge of the graphene and the contact metal is changed by controlling the edge structure, enabling the significant reduction of the contact resistance. Mechanisms of pre-plasma process leading to low R_c was revealed by using SEM, Raman spectroscopy, with the help of the understanding on the difference in surface and edge contacts at the M-G interface. We found that the contact resistance was significantly reduced by using the pre-plasma processing.

Thickness control of MoS_2 by using O_2 plasma

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2차원 소재 중에서 현재 연구가 활발이 진행되고 있는 MoS_2는 소자 분야 외에도 광센서, 촉매 등 다양한 분야에 적용이 가능하다. MoS_2가 가지고 있는 특성을 활용하기 위해서는 특히 MoS_2의 두께를 조절하는 것이 중요하다. 왜냐하면, MoS_2는 두께에 따라 다른 밴드구조를 가지기 때문인데, 단층 MoS_2는 약 1.9eV 정도의 direct bandgap을 가지는 반면, bulk MoS_2는 약 1.2eV 정도의 indirect bandgap을 가진다. 이러한 Indirect-to-direct gap transition을 이용하면 광효율을 최대화할 수 있으며, 200-500cm^2/Vs의 높은 mobility를 얻을 수 있다고 보고된다 [1]. 이를 위해 CVD방법을 이용한 단층 MoS_2 합성 [2], Laser thinning [3], gaseous reactant인 XeF_2를 이용한 etching [4] 등의 다양한 방법이 연구되고 있는데, 본 연구에서는 O_2 플라즈마를 이용하여 대면적 MoS_2를 만들기 위한 연구를 수행하였다. 또한 AFM 및 Raman spectroscopy를 통해 MoS_2와 O_2 플라즈마가 반응하는 매커니즘을 분석하고자 한다.

본 연구에서는 O_2 플라즈마 처리를 통해 평균 0.10 nm/s의 etching rate으로 4층의 MoS_2에서 단층의 MoS_2를 얻는데 성공하였다. 그리고 Laser thinning할 때 roughness가 pristine의 3배까지 증가한다는 연구결과와는 달리, 플라즈마를 이용하면 roughness가 pristine 상태 (0.5nm)와 비슷하거나 더 향상된 결과를 얻을 수 있었다. 한편 반응성이 높은 O_2 플라즈마를 처리하면 절연체의 성질을 가지는 MoO_3가 형성될 가능성이 높은데, MoO_3는 melting point가 795℃라서 제거하기가 힘든 물질이다. MoO_3의 형성유무를 밝히기 위해 Raman spectroscopy를 이용해 분석하였고, MoO_3 peak인 820cm^{-1}과 Mo-O bonding peak인 225cm^{-1}이 나타나지 않는다는 것을 확인할 수 있었다. 이를 통해 O_2 플라즈마가 MoO_3 형성 화학반응 없이 etching을 일으키는 것을 확인하였다. 본 연구결과는 transition metal dichalcogenides 등의 다른 2차원 극박막 물질의 플라즈마 에칭에 응용되어, 2차원 반도체 소자개발을 가속화시킬 것으로 예측된다.

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Wet etching process 를 통한 free-standing EUV pellicle membrane 제작

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극자외선 리소그래피(EUV lithography)는 13.5nm 단파장의 광원을 사용함으로써, 기존 193nm 광원을 사용하는 ArF 리소그래피에 비하여 반도체 패턴의 한계 해상력을 향상시키는 기술이다. 그러나 극자외선 광원은 그 짧은 파장으로 인해 상대적으로 더 큰 atomic scattering 을 하며, particle 및 defect 가 발생할 시 이미징에 미치는 악영향이 매우 크다. 따라서 포토마스크 표면을 대기 중 분자나 다른 형태의 오염으로부터 보호해주는 pellicle 의 필요성이 크게 대두되었으며 현재 개발 중에 있다. 하지만 거의 대부분의 물질은 극자외선 광에 대하여 높은 소광 계수(extinction coefficient, k)를 가지기 때문에 EUV pellicle 용 membrane 제작에 난항을 겪고 있는 실정이다. 본 연구에서는 높은 투과도와 안정적인 기계적 특성을 가지는 free-standing EUV pellicle membrane 제작을 목표로 하였다. Free-standing pellicle 은 mesh 로 인한 이미징 특성 저하가 발생하지 않는다는 점에서 mesh wire pellicle 보다 이점을 갖고 있지만, mesh wire pellicle 보다 낮은 기계적 강도로 인하여 제조에 어려움을 겪고 있다. 본 연구에서는 wet etching process 를 중심으로 극자외선 광에서 보다 낮은 소광 계수를 가지는 Si 기반의 물질들을 사용하여 free-standing pellicle membrane 제작에 성공하였으며, 제작된 membrane 의 투과도 측정 결과 등을 통하여 해당 process 의 feasibility 를 확인하였다.

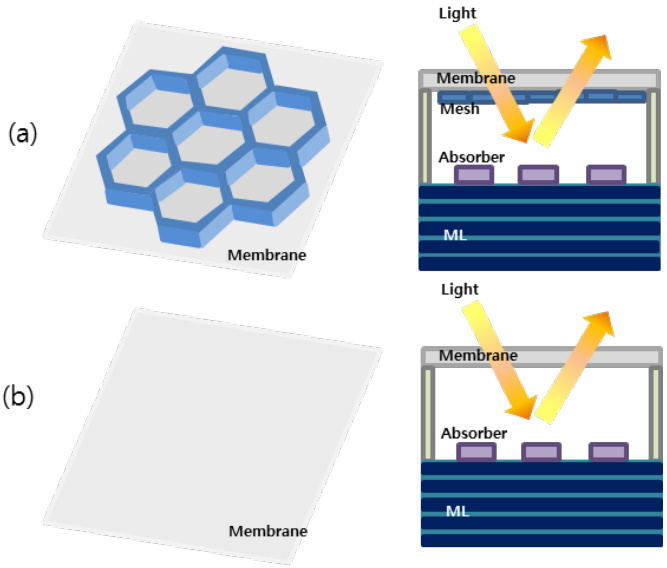

그림 1. (a) Mesh wire pellicle 과 (b) free-standing pellicle 간 비교

Hybrid Input-output (HIO) 알고리즘을 사용한 마스크 패턴의 이미지 재구성 연구

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최근 양산을 앞두고 있는 극자외선 리소그래피 (extreme ultraviolet lithography, EUVL) 기술에서 중요하게 다루어지고 있는 분야는 검사 및 평가기술이다. 극자외선 리소그래피 기술은 기존의 원자외선 (deep UV) 리소그래피와는 다르게 반사광학 원리를 사용하기 때문에, 마스크 및 광학계가 다층박막 거울을 사용한 반사광학계로 제작된다. 수십 층 이상의 다층박막 거울을 기반으로 제작된 극자외선 마스크를 검사하기 위해서는 다층박막 내부까지 깊숙이 침투할 수 있는 극자외선 광원을 사용한 actinic 검사기술이 반드시 필요하며, 본 연구 그룹에서 연구중인 coherent scattering microscopy (CSM) 기술은 이러한 actinic 검사기술의 하나이다. CSM 은 마스크 패턴으로부터의 회절광을 획득하고, 이를 hybrid input-output (HIO) 알고리즘을 사용해 위상 정보를 복원하여 원래의 이미지를 재구성한다. 본 연구에서는 HIO 알고리즘의 내부 인자 β 및 반복 횟수를 변화시키며 웨이퍼 기준 14~32nm 크기의 line and space (L/S), contact hole (C/H), dot 형태의 패턴을 가진 마스크의 이미지를 재구성하여 복원된 위상과 광량을 확인하였다. 알고리즘 인자 변화를 통해 위상과 광량 복원 능력이 가장 뛰어난 알고리즘 수행 조건을 결정하였고, 이를 바탕으로 NA 및 sigma 의 조명조건을 변화시키며 웨이퍼에 전사되는 aerial image 를 재구성하였다. NA 는 현재 양산을 위한 시험 가동 중인 HVM 조건과 같은 0.33 과 이보다 더 큰 (higher NA) 0.45 를 적용하였고, conventional illumination 의 sigma 값은 0.2~0.9 의 값을 적용하여 마스크의 특성을 확인하였다.

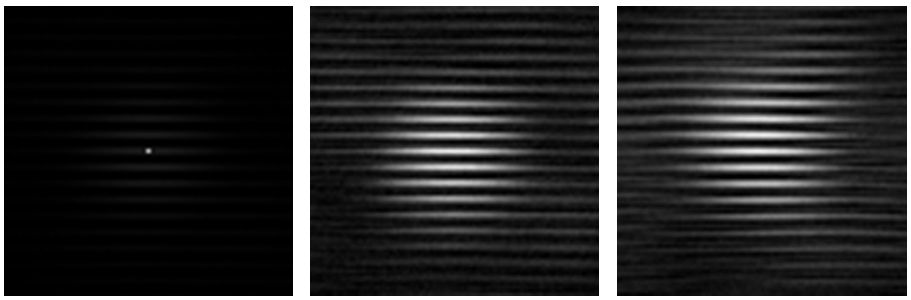

그림 1. 0.9 β 조건에서 HIO 알고리즘을 (왼쪽 그림부터) 각각 1 회, 15 회, 30 회 반복 수행했을 때 32nm L/S 패턴의 이미지 재구성 결과

Plasma Etching to forming One-Dimensional Electrical Contact to Molybdenum Disulfide

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Through stacking of molybdenum disulfide and hexagonal boron nitride (h-BN), we fabricate h-BN-MoS2 –h-BN heterostructure devices. It is well known that, in the devices using 2-dimensional materials the possibility to get good electrical properties depends on the ability to make high-quality electrical contact. Now we are introducing a geometry in which we metalize 1D edge of monolayer MoS2, in which the fabricaiton is based on plasma etching technology. In addition, this structure could lower contact resistance through letting electrode metal atoms form new bonds with MoS2 dangling bonds on the edge of 2 dimensional structure. Figures 1 and 2 show the output characteristics (I_d-V_d) and MoS2 field-effect mobility of one dimensional contact device under the atmospheric pressure condition. In contrast, Figures 3 and 4 show the output characteristics (Id-Vd) and MoS2 field-effect mobility of one dimensional contact device in vaccum (6.9 mtorr). In MoS2 heterostructures, all of these enable high electronic performance, eg. high room-temperature mobility. Moreover, this geometry also provides possibilities to fabricate new designs of two dimensional device.

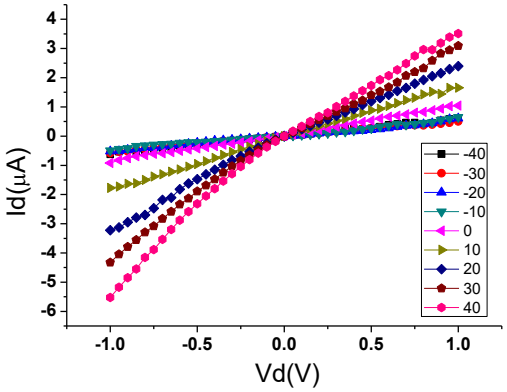

Figure 1. Drain voltage is 0.1 V.

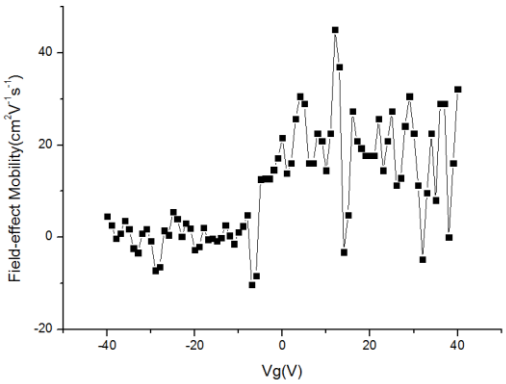

Figure 2. Field-effect mobility. Drain voltage is 0.1 V.

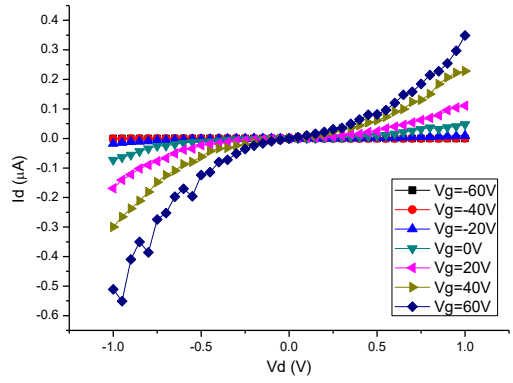

Figure 3. Drain voltage is 0.1 V.

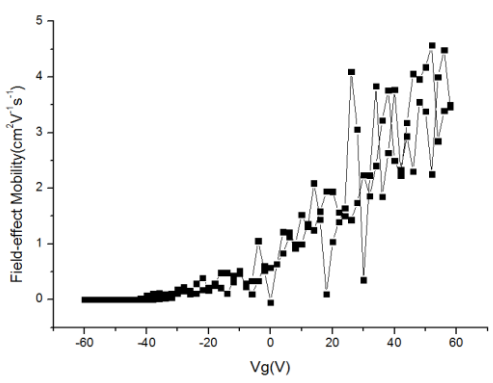

Figure 4. Field-effect mobility. Drain voltage is 1 V.

Etch Characteristics of Magnetic Tunnel Junction Materials using Substrate Heating in Pulse-biased Inductively Coupled Plasma

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The spin transfer torque magnetic random access memory (STT-MRAM) is considered as a next generation semiconductor memory device because of the high density storage, fast access time, infinite rewrite, low operating voltage, etc [1]. In the STT-MRAM device, the multi-layer of the magnetic tunnel junction (MTJ) which consisted of CoFeB/MgO/CoFeB is the most important structure due to the main data that are recorded in this stack. To improve the charictaristics of the MTJ materials, it is necessary to completely remove the etch residue on the MTJ feature sidewall and decrease the roughness of the profile. Therefore, precise and sophisticated nano-scale etching techniques of this MTJ materials must be developed. Previously, many research have been investigated about improving the etch charictaristics such as using non-corrosive gas mixture to prevent the corrosion of the magnetic materials. But non-corrosive etch gas mixtures do not form stable and volatile compounds result in low etch selectivity and sloped etch profile. To overcome this problem, pulse-biased inductively coupled plasma (ICP) technique was investigated by applying the pulsed rf power to the substrate with the continuous ICP source power, the etch selectivity could be improved owing to the formation of more volatile and stable etch compounds during the pulse-off time [2]. Furthermore, increase the substrate temperature can more increase the etch rates and etch selectivities of MTJ materials. In this study, we investigated the effect of substrate heating on the etching of MTJ materials using CO/NH_3 gas mixtures in the pulse-biased ICP system. The etch characteristics of MTJ materials and etch mechanism have been investigated to improve the etch profile and etch selectivities of MTJ materials over hard mask.

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RF Plasma Dielectric Etching Endpoint Detection using Optical Emission Spectroscopy with Real-time Density Based Cluster Analysis

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Dielectric layer etching endpoint detection (EPD) was demonstrated using optical emission spectroscopy (OES) with real-time density based cluster analysis (RTDBCA) at inductively coupled plasma (ICP) chamber.

In etching processes, the layer materials can be unetched or overetched if proper process conditions are not satisfied. These can cause layer thickness difference or short circuit, and lead to severe device defects. Hence, the accurate etch endpoint detection is essential. This is known as EPD. For EPD, optical emission spectroscopy is commonly used; however, the sensitivity of OES signal is too low to detect endpoint. To enhance OES sensitivity, real-time density based cluster analysis (real-time DBCA) is applied.[1]

The real-time DBCA is one of the modified cluster analysis algorithm—a partitioning method of subsets and have been used for searching the boarder of cluster[2]—for real-time plasma process monitoring. The real-time DBCA algorithm needs the distance between newest data and previous data. Then, extract the longgest distance from calculated distances. The longgest distance is defined as maximum distance (MD). If new MD value is larger than the previous MD value, we can decide this data is different from the previous data. This time is considered as the endpoint.

For verifying this technique, small size sample SiN_x and SiO_2 wafers are used as etched materials. The size is shrinked down from 8.0 % to 0.5 % relative to 100 mm wafer. The ellipsomtry was used to measure the residual layer. The proposed algorithm shows the improved sensitivity compared to single wavelengths signal of OES. This method can be applied to the other diagnosis equiptments.

[1] Jang, H., Nam, J., Kim, C. K. and Chae, H., "Real-time endpoint detection of small exposed area SiO_2 films in plasma etching using plasma impedance monitoring with modified principal component analysis", Plasma Process., Polym., 10, 850-856(2013)

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Etch characteristic of Si_3N_4 layer by pulse-biased capacitively-coupled plasmas for nano-scale patterning of multi-level resist structures

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During plasma etching of ultra nano-scale patterns, several issues should be overcome such as plasma-induced damage, control of line-edge roughness, selectivity, aspect ratios, etch profiles and maintenance of critical dimensions [1]. In order to mitigate these issues, we investigated pulse-biased etching in capacitively-coupled plasma for nano-scale patterning of multi-level resist structures. Recently, for the etching of Si_3N_4 underlayer using fluorocarbon plasmas, dual-frequency, superimposed CCP (DFS-CCP) etcher widely used to control the plasma density and ion bombardment energy, separately [2]. The system is equipped with LF power of 2MHz, which has the ability of CW- and pulse-biasing and an HF power of 27.12 MHz. The Si wafers with line and space patterns of KrF PR were prepared on a stack of bottom anti-reflected arc (BARC)(~50nm)/SiO_2(~50nm)/ACL(~50nm)/Si_3N_4(~600nm) on an 8-inch wafer. $CH_2F_2/CF_4/O_2$/Ar mixture gas chemistry was used for the etching process of the Si_3N_4 layer. The differences in critical dimension and line-edge roughness of Si_3N_4 under CW-mode and pulsing mode using the DFS-CCP system were studied as functions of pulse duty ratio (100-25%) and pulse frequency (1~5kHz)of 2MHz LF bias power.

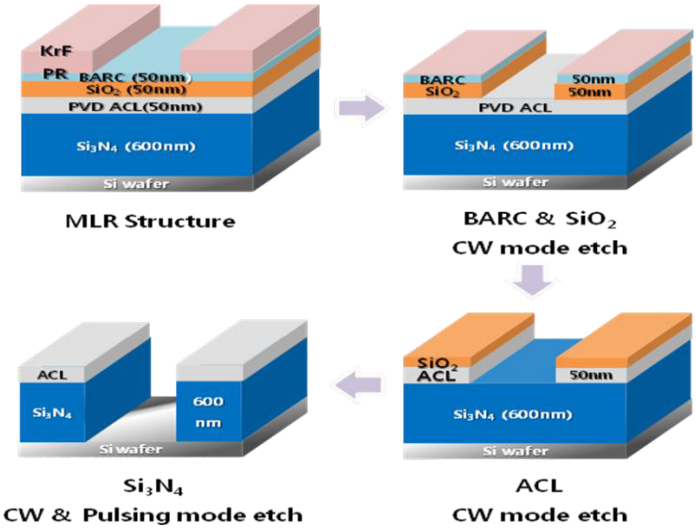

Fig 1.The diagrams of each process for patterning of the MLR structure.

[1] Hyelim Lee, Sechan Kim, Gyuhyun choi, and Nae-Eung Lee, J. Nanosci. Nano-technol. 14, 1-7 (2014)

[2] B.S. Kwon, J.H. Lee, N. −E. Lee, Thin Solid Films 519, 6741-6745 (2011)

Pulse-biased etching of SiO_2 layer in capacitively-coupled plasmas for nano-scale patterning of multi-level resist structures

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As the pattern size of semiconductor devices is shrinking down to ultra nano-scale range of 10-nm, many issues must be overcome including reduced plasma-induced damage, control of line-edge roughness, etch profiles, aspect ratios, selectivity and tighter critical dimension control [1]. Due to the difficulties in immediately etching the underlayer using an ArF PR mask, new schemes have been developed for nano-scale patterning using multilayer resist (MLR) structures [2]. Recently, we have investigated nano-scale etching process of SiO_2 underlayer with the purpose of comparing CW(continuous wave) mode with pulsing mode in MLR structure. The system is equipped with LF power of 2MHz that has the ability of CW- and pulse-biasing and an HF power of 27.12MHz. The Si wafers with line and space patterns of ArF PR were prepared on a stack of bottom anti-reflected arc (BARC)(~50nm)/SiO_2(~50nm)/ACL(~50nm)/SiO_2(~600nm) on an 8-inch wafer. $CH_2F_2/C_4F_8/O_2$/Ar mixture gas chemistry was used for the etching process of the SiO_2 layer. The differences in the etch rates of SiO_2 and ACL and their etch selectivities under CW-mode and pulsing mode using the DFS-CCP system were studied as functions of pulse duty ratio (100-25%) and pulse frequency (1~5kHz) of 2MHz LF bias power.

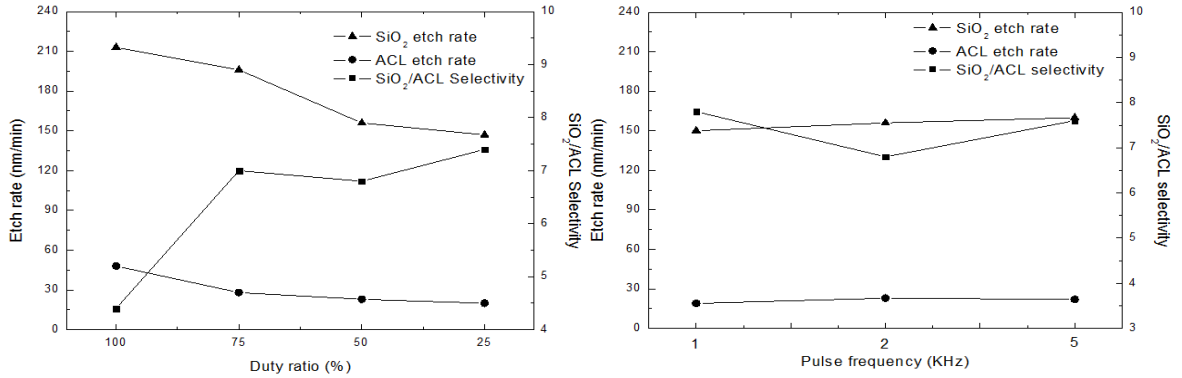

Fig 1.Etch rates and selectivities of the SiO_2 etched under pulse-biasing conditions

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[2] B. S. Kwon J. S. Kim, N. -E. Lee, and J. W. Shon, J. Electrochem. Soc. 157 (3) D135-D141 (2010)

Pt nanoparticles generated from plasma-sputtered Pt films and their use in enhancement of sensing characteristics in SnO_2 nanowires

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We have prepared SnO_2-cored heteronanowires by sputtering technique with the platinum (Pt) target, subsequently investigating the effects of thermal annealing. The surface of SnO_2-Pt core-shell nanowires became rougher by the thermal annealing, being attributed to the agglomeration of the shell layers into the nanoparticles. The gas sensing test demonstrated the ability of the Pt functionalization to attain the higher sensitivity and faster response than bare SnO_2 nanowires. The possible mechanisms for improvement of the sensing properties by Pt-functionalization are discussed [H. G. Na, J. C. Yang, D. S. Kwak, Y. J. Kwon, C. Lee, S. S. Kim, H. W. Kim, J. Nanosci. Nanotech. 13 (2013) 6216-6221].

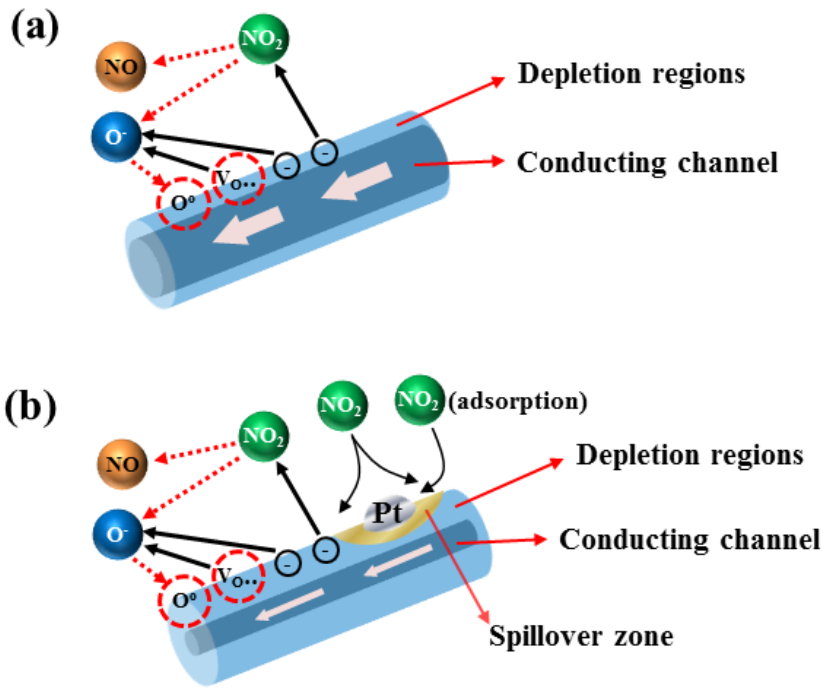

Fig 1. (a) Schematic of a bare nanowire sensor. (b) Schematic explaining the suppression of conducting channel by Pt functionalization

Inductively Coupled Plasma Reactive Ion Etching of Ru Thin Films Using $CH_4/O_2/Ar$ Gas Mixture

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New kind of memory devices which combine the advantages of current major memory devices have been required for the next generation. The new memory devices ought to have the features containing fast process rate, high density, non-volatility and good endurance. Among many possible candidates, magnetic random access memory (MRAM) has a great attention for the next generation memory device.

MRAM is composed of magnetic tunnel junction (MTJ) stack and complementary metal-oxide semiconductors (CMOS). MTJ stack is a key parts in MRAM devices and they consist of various magnetic materials, metals, and a tunneling barrier layer. Recently, Ru has been used as a coupling layer and electrode because of its high thermal stability and low resistivity [2]. For the realization of MRAM devices, the etching of Ru films should be developed. Currently the CH_3OH/Ar, CH_4/Ar and $CH_4/O_2/Ar$ chemistry have been known to be good etch gases for the etching of MRAM devices [3,4]. Therefore, the etching of Ru films also needs to be developed using CH_3OH/Ar, CH_4/Ar and $CH_4/O_2/Ar$ gas mixture. However there are few studies about Ru thin films etching using non-corrosive gas mixtures such as CH_3OH/Ar, CH_4/Ar and $CH_4/O_2/Ar$.

In this study, the etch characteristics of Ru thin films have been investigated by using CH_4/Ar and $CH_4/O_2/Ar$ gas mixtures using inductively coupled plasma reactive ion etching (ICPRIE). The effect of the ratio of gas mixture on the etch rate, etch selectivity, and etch profile were studied. In addition, the influence of etch parameters including, ICP rf power, dc-bias voltage to the substrate, and process pressure in the chamber was investigated. Optical emission spectroscopy (OES) was utilized to identify the species in plasma.

[1] R. C. Sousa, I. L. Prejbeanu, C. R. Physique, vol. 6, pp. 1013–1021, 2005.
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[3] E. H. Kim, T. Y. Lee, C. W. Chung, Journal of The Electrochemical Society, vol. 159, no. 3, pp. H230-H234, 2012
[4] T. Y. Lee, E. H. Kim, B. C. Min, C. W. Chung, Thin Solid Films, vol. 521, pp. 216–221, 2012

Inductively coupled plasma reactive ion etching of nanometer-size patterned magnetic tunnel junction stacks using C, H, O containing gases

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Semiconductor memory devices are used in almost every electronic gadget such as computers, tablets, digital cameras etc. Roughly, the actual semiconductor memory market is dominated by traditional flash memories and random access memories (static and dynamic); however this generation edge technologies are pushing through, making more and more difficult for these devices to comply with design specifications, thus increasing manufacturing complexity [1]. In order to address these difficulties, spin transfer torque magnetic random access memory (STT-MRAM) have been proposed as the next generation semiconductor memory device owing to its non-volatility, high storage capacity, fast read/write, low power consumption, low operating voltages, and more importantly compatibility with CMOS processes [2].

Etching of the MTJ stacks is one of the key process in the fabrication of MRAM devices, however problems such as formation of non-volatile compounds, redeposition of etched materials, post-etch corrosion and more importantly damage of the magnetic layers complicate its fabrication; therefore the selection of a proper etching gas and optimization of the etch parameters are necessary [3]. Inductively couple plasma reactive ion etching (ICPRIE) of MTJ stacks using halogen containing gases such as Cl_2 and HBr has been done; however due to the nature of the etching gases, corrosion and degradation of the magnetic properties of the films after the etching process occurred [4]. As an effort to reduce the use of toxic halogen containing gases, several investigations reported the etching of MTJ using C, H, O (CH_4, CH_3OH, CO, H_2O) containing gases or vapors. Among those, the etching of MTJ stacks using CH_3OH vapor has produced exceptionally good results compared to traditional ion milling and other halogen gases [6]; therefore the etching of MTJ stacks using vapor (or gases) that contain the C, H and O compounds need to be further developed.

In this study the reactive ion etching of MTJ stacks using C, H, O containing vapor/gas mixture was used to etch nanometer scale MTJ stacks. The etching of MTJ stacks was investigated by varying the concentration of C, H, O containing solutions and by varying its ratio in an Ar gas mixture. Additionally, the effect of rf power, dc bias and pressure on the etch profile was investigated. The etch rates were obtained using a surface profilometer and etch profiles were obtained by a field emission scanning electron microscopy. The surface chemistry and etch mechanism were analyzed by optical emission spectroscopy and transmission electron microscopy.

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3. Tomonori Mukai, Butsurin Jinnai, Seiji Samukawa, Plasma irradiation damages to magnetic tunneling junction devices, J. Appl. Phys. 102 (2007), 073303 1-4.
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5. Tea Young Lee, Il Hoon Lee, Chee Won Chung, Inductively coupled plasma reactive ion etching of magnetic tunnel junction stacks using H_2O/CH_4 mixture, Thin Solid Films 547 (2013) 146−150.
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The Transition from Ion Flux Limited to Neutral Flux Limited Process Regime in High Aspect Ratio Contact Etching

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As device dimensions decrease to under tens of nanometers, the requirements for high aspect ratio contact (HARC) etch processes such as vertical profile and uniformity are getting more stringent. Therefore, controlling of loading effect and aspect ratio dependent etching (ARDE) are becoming core technologies in HARC etch process development. Increasing ion flux and directivity is one of well known ways to reduce depth loading (lower etch rate in deeper contact hole). In these circumstances, development of HARC etching processes and equipments are moving toward higher low-frequency (LF) power, consequently higher plasma potential (Vpp), and larger electrode gap. But in our experiments with ~20 nm of top critical dimension (CD), no improvement of depth loading (inverse of the slope) was observed when Vpp applied to wafers is larger than 1.18 (normalized Vpp) (Fig. 1). It looks that the etching process is getting into neutral flux limitation regime from ion flux limitation regime [1]. This implies an unbounded increase of LF power does not always guarantee higher etch rate at deep contact; and optimization of other process parameters should be also combined with such as higher process temperature and longer residence time for achieving higher neutral flux and reducing depth loading.

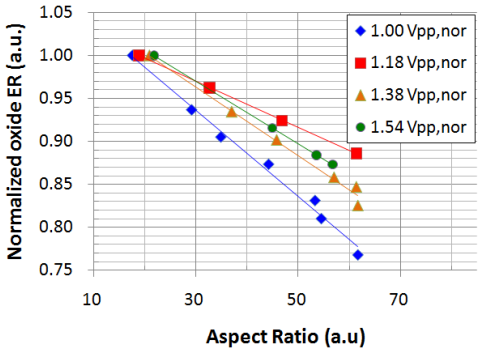

Fig 1. Normalized oxide etch rate as a function of aspect ratio (etch depth/top CD) and plasma potential

[1] R. A. Gottscho and C. W. Jurgensen, and D. J. Vitkavage, *J. Vac. Sci. Technol. B* **10(5)**, 2133 (1992)

Variation of bottom critical dimension induced by reactive ion etching lag in high aspect ratio contact etching process

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In recent semiconductor devices, the high aspect ratio contact (HARC) is one of the most challenging processes. The devices require deeper and smaller contact holes for design rule shrinkage. The most critical index of HARC process is usually bottom critical dimension (CD) which tends to be smaller with higher aspect ratio [1]. Figure 1 shows the 2-D shape of a hole and the etching rate (E/R; depth/etching time) changes with mask top CD. In our experiment, the variation of bottom CD was investigated according to the photolithography after development inspection (ADI) CD size. With 4.5% decrease in the ADI CD, the variation of ADI CD increased 6.5% and the variation of bottom CD increased 8.8% in standard deviation. The increase of CD variation was originally induced from the photolithography and seemed to be amplified by each dry etching process. The root cause of the deterioration was analyzed with the previous studies on reactive ion etching (RIE) lag. The etching amount after hole bottom touching (overetch) of each hole differed with the mask top CD size due to the RIE lag. The practical solutions for reducing the bottom CD variation were discussed.

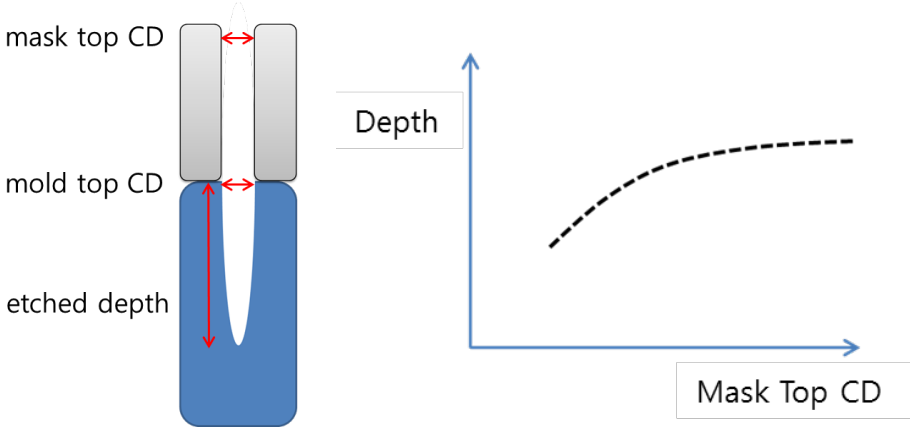

Figure 1. (a) 2-D schematic diagram of HARC etching process (b) Etched depth according to the mask top CD.

[1] O. Joubert, G. Oehrlein and M. Surendra, J. Vac. Sci. Technol. A 12, 665(1994).

Low afterpulse noise single-photon detector with detrap schemeors

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단일 광자 측정기는 매우 중요하다. 각종 양자물리학적 실험 및 양자암호키 분배 시스템에서 사용되고 있다. 그 중에서도 광통신용도로 사용되는 1550nm 파장에서 단일광자를 측정하기위해선 현재 가장 앞선기술을 가진 실리콘 기반 반도체에서는 사용이 불가능 하다. 이에 InGaAs 기반 단일광자측정기가 만들어지고 있다. 그러나 이는 실리콘에비해 노이즈, Dark Count 및 Afterpulse 가 발생하여 검출기의 신뢰도를 떨어뜨린다. 특히 Afterpulse 는 MHz 이상 동작시 그 영향이 급속도로 증가하기 때문에 고속동작으로 사용하기 매우 어렵다. 이를 해결하기 위해 Detrap 기술을 제안한다.

[1] P KRAINAK, Michael A. Photoionization of trapped carriers in avalanche photodiodes to reduce afterpulsing during Geiger-mode photon counting. In:*Conference on Lasers and Electro-Optics*. Optical Society of America, 2005. p. CMGG4.

민감도 향상을 위한 NDIR CO_2 Sensor 연구

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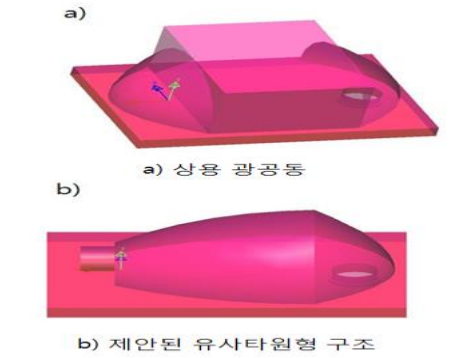
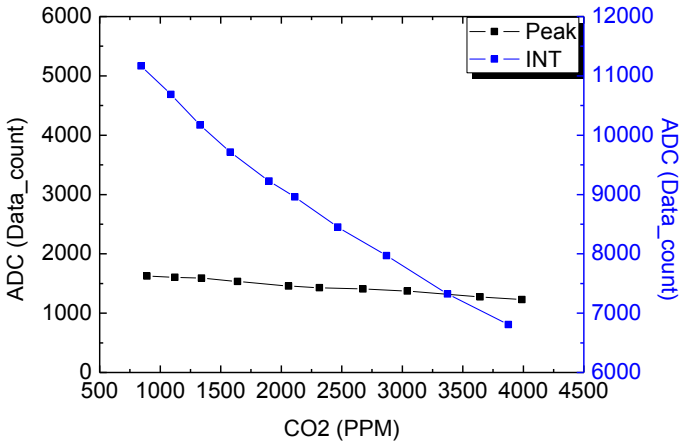
이 논문에서는 NDIR CO_2 센서의 민감도 향상을 위한 광공동 설계와 신호처리 방식을 제안한다. 이산화탄소가 4.2um 대역의 적외선을 흡수하는 성질을 이용한 NDIR CO_2 센서는 크게 발광부, 수광부, 광공동의 센서부와 신호를 제어 및 처리하는 제어부로 나누어진다.
센서부의 광공동은 광원에서 출발한 적외선이 이산화탄소화 만나 감쇠되어 수광부로 도착할 때 광이 이산화탄소를 많이 거쳐 감쇠율을 높여주는 역할을 한다. 이때 광공동 설계를 통하여 광경로를 조정해 줌으로서 집광률을 높여 센서의 민감도를 높일 수 있다. 이때 파라볼릭 반사경을 이용하여 직광을 만들어 주는 방법을 많이 사용하는데 이는 광원에서 산란되는 광은 무시하는 결과가 된다. 이에 우리 연구는 직광 뿐만 아니라 기존에 무시되던 산란광 또한 집광하는 설계를 통하여 센서의 민감도를 올렸다.
제어부에선 기존방식과 같이 센서의 안정도를 높이기 위해 광원의 On/off 제어를 사용하였으며 신호처리과정에서 수광부의 검출 신호를 데이터 수집 알고리즘을 통해 기존 P-t-P 측정방식보다 더 높은 민감도를 가진 센서를 만들었다.



	Simulation output	효율
상용	$143mW/mm^2$	26.5%
제안	$193mW/mm^2$	35.7%

< 광공동 타입에 따른 출력 신호 비교>



< CO_2 농도에 데이터 수집 알고리즘 비교>

[1] HAN, Ji-Hoon, et al. High Detection Performance of NDIR Sensor Using Stair-Tapered Reflector. *Sensors Journal, IEEE*, 2013, 13.8: 3090-3097.

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프렌슨 간섭계의 비대칭성을 이용한 두-광자 간섭 특성 분석

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일반적으로 HOM 간섭실험은 얽힘 상태 광자쌍이 빔 분할기(beamsplitter:BS)에 동시에 도달할 때, 빔 분할기의 한쪽 출구로만 뭉쳐서 지나가게 되므로, 양쪽 출구에서 동시계수를 측정을 통한 간섭무늬의 선명도가 고전적으로 설명이 불가능한 50%를 넘는다. 중요한 점은 빔 분할기에 동시에 도달하는 것이다. 하지만, 빔 분할기에 광자쌍이 동시에 도달하지 않아도, 빔 분할기 양쪽 출구에 놓인 두 단일광자 검출기에 도달하는 시간차가 같다면 우리는 양자간섭 무늬를 구할 수 있다.

본 논문에서는 빔 분할기에 도달하는 시간차에 따른 HOM 간섭무늬를 측정할 것이다. 또한 광원으로 사용한 cw 멀티모드 다이오드 레이저의 주기적인 반복성이 반영되는지도 확인할 것이다. 실험장치도는 그림1과 같다. 제 2형의 BBO 결정을 이용하여 $|\psi\rangle=\frac{1}{\sqrt{2}}\left(|H_1\rangle|V_2\rangle+|V_1\rangle|H_2\rangle\right)$ 와 같이 서로 다른 편광을 가지고 얽힘 상태가 발생시켰다. 여기서, H와 V는 수평과 수직 편광을 나타낸다. 발생된 광자쌍을 Franson 간섭계를 이용하여 빔 분할기에 도달하는 시간차를 조절할 수 있었다. 이 때, 빔 분할기에 도달하는 광자쌍의 상태는 $|\psi\rangle=\frac{1}{\sqrt{2}}\left(|S_1\rangle|L_2\rangle+|L_1\rangle|S_2\rangle\right)$ 와 같이 표현되고, 우리는 이때 빔 분할기에 도달하는 광자쌍의 짧은 경로와 긴 경로 사이의 상대적인 거리차이(τ_1, τ_2)에 따른 τ_3 값의 변화에 따른 HOM 간섭현상을 측정할 것이다.

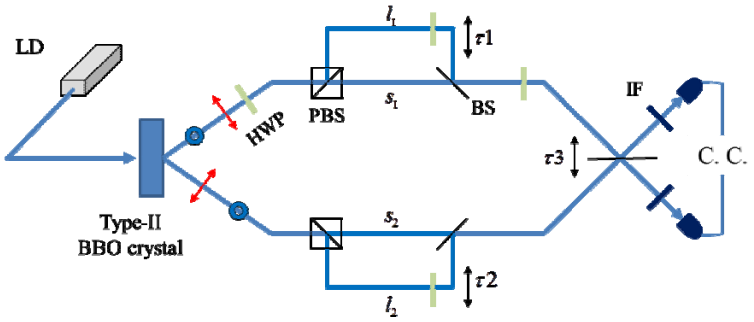

Fig 1. 실험장치도

[1] C. K. Hong, Z. Y. Ou, and L. Mandel, Phys. Rev. Lett. 59 2044 (1987)

Observation of two-photon interference with continuous-wave operating coherent light

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Since two-photon interference was first introduced by Hanbury Brown and Twiss, it has been widely utilized to investigate the quantum nature of light [1]. The rapidly developing quantum information science has boosted research on two-photon quantum interference. Note that two-photon quantum interference is essential for many quantum information protocols including linear optics quantum computation [2].

Recent research shows that the two-photon interference with classical light can sometimes imitate quantum interference and thus it can be useful for quantum information science. For example, ghost imaging or ghost interference, which was considered as a result of two-photon quantum interference, can be implemented with classical light sources. Since the implementation of classical light sources is much easier than that of quantum light sources, these results show the practical benefits of two-photon classical interference for quantum information science. Thus, the study of two-photon classical interference is not only important for a better understanding of the nature of interference but also for applications in quantum information science.

In this presentation, I will explore a Hong-Ou-Mandel (HOM) type two-photon interference with a multi-mode diode laser.

[1] L. Mandel, Rev. Mod. Phys. **71**, S274 (1999).
[2] E. Knill, R. Laflamme, and G.J. Milburn, Nature **409**, 46 (2001)

Characteristics of strained InGaAs quantum well infrared photodetector for gas sensor applications

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Solid state quantum well infrared photodetectors (QWIPs) using intersubband absorption have been extensively investigated for the use of gas sensors, thermal imaging systems etc. N-type doped QWIPs have exhibited higher responsivity and detectivity due to the higher electron mobility, optical absropton and photoconductive gain related with the smaller electron effective mass compared with p-type QWIPs. However, due to the quantum mechanical slection rules, n-type doped QWIPs having sysmetry quantum wells have difficulty to copule normal incidence light. To avoid the selection rules, special light coupling schemes such as gratings and beveled edges are required, which can accompany additional process and reduce effective area of the device. These effects can be overcomed by breaking the sysmetry of quantum wells through structural modification, and GaAs based QWIP was demonistrate for very long wavelength [1]. However, for gas sensor applications, smaller wavelength QWIP materials are required. In this paper, we report the results on the InP based-strained $In_{0.5x}Ga_{0.4x}As$/InAlAs QWIPs for short wavelength infrared absorption grown by metal-organic chemical vapor deposition. The performance and detailed epitaxial growth method of QWIPs will be introduced.

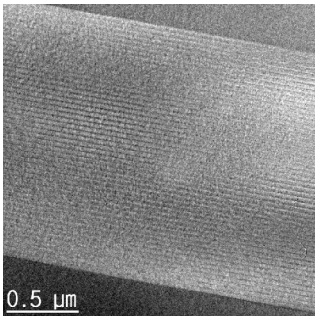

Fig 1. Cross sectional view of lattice mismatched InGaAs/InAlAs QWIP

[1] S. Y. Wang, and C. P. Lee, Appl. Phys. Lett. 71, 119 (1997).

Detection of hepatitis B surface antigen using dual-gate EGFET

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B 형 간염은 전세계적으로 빈번하게 발생하는 감염증으로서, B 형 간염 바이러스가 간세포를 공격함으로 인해 간기능 상실, 간경화, 심하게는 간암에까지 이르게 할 수 있는 질병이다. 현재 이용되고 있는 B 형 간염의 진단 방법으로는, B 형 간염 바이러스의 표면항원(HBsAg)과 항체의 반응을 유도한 후 이를 효소를 이용한 발색 반응이나 화학적 발광 반응으로 바이러스의 존재를 시각적으로 확인하는 방법이 있으나, 이러한 방법은 한 번의 검사를 시행하는데 걸리는 시간이 오래 걸리고 정기적인 진단을 위해서는 매번 병원에 가야 하는 불편함과 비용을 감수해야 한다는 단점이 있다. Extended-gate field-effect transistor (EGFET)는 화학 용액 속의 이온농도를 검출하는 바이오센서로, 빠른 검출 속도와 낮은 제조 비용, 휴대 가능 등의 많은 장점을 가지고 있는 바이오센서이다. 하지만, 기존의 EGFET 는 이론적으로 최대 감도의 한계를 가지고 있으며, 이로 인해 낮은 농도에서의 미소한 신호를 검출하는데 있어 어려움이 있다.

따라서, 본 연구에서는 이러한 문제를 해결하기 위해 Silicon-on-insulator (SOI) 기판을 이용하여 dual-gate (DG) 동작을 갖는 EGFET 를 제안하였다. DG 동작은 소자 내의 capacitive coupling 현상을 유발함으로써 추가적인 회로 구성 없이도 감도를 크게 증폭시킬 수 있는 시스템이다.[1] 결과적으로, 낮은 농도의 HBsAg 을 정확하게 검출할 수 있는 DG EGFET 바이오센서를 개발하였으며, B 형 간염 바이러스의 현장진단 tool 로서 응용 가능성을 보여주었다.

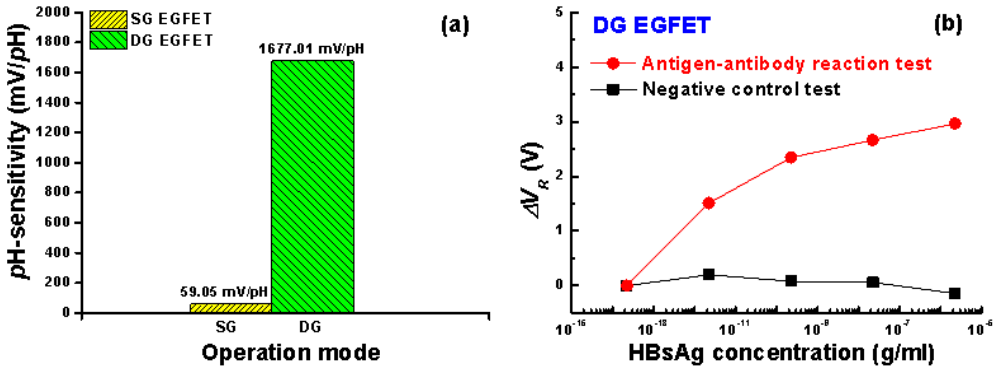

Fig 1. (a) Comparision of pH-sensitivity in SG and DG EGFETs. (b) Detection of HBsAg using DG EGFET.

[1] H. K. Lim, and J. G. Fossum, IEEE Trans. Electron Devices, 30, 1244, (1983).

Detection of HBs auto-antibody using extended-gate field-effect-transistors

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자가면역질환은 핵, 세포질 및 핵막의 특정 항원을 인지하는 자가항체의 존재를 특징으로 하는 질환이다. 일반적으로 자가면역질환을 진단하기 위해서는 자가항체를 검출하며 검출 방법으로는 간접면역형광법 (indirect immunofluresent assay, IFA)과 효소면역측정법 (enzyme linked immunosorbent assasy, ELISA)을 주로 이용한다 [1]. 그러나 이러한 항체검사 방법은 소요시간이 길고 검사를 위한 과정이 복잡하다는 단점이 있다.

따라서, 본 연구에서는 이러한 문제점을 해결하기 위해 간단하고 저렴한 방법으로 검출이 가능한 extended-gate ion-sensitive field-effect transistor (EG-FET) 소자를 이용하여 자가면역질환 진단에 적용하였다. 300 nm 의 SiO_2 가 성장된 p-type Si wafer 에 Ti 전극을 150 nm 두께로 형성한 다음, SnO_2 감지막을 45 nm 두께로 증착하고 polydimethylsiloxane (PDMS) reservoir 를 설치하여 extended-gate 를 제작하였고[그림 1(a)], SOI 기판 상에 제작한 n-type 의 MOSFET 에 연결하여 EG-FET 를 완성하였다. SnO_2 감지막을 O_2 플라즈마 표면처리 후에 150 nM 의 농도를 가지는 HBs (B 형 간염) 항원을 주입하여 감지막 표면에 부착시켰다. 그 후 BSA (Bovine serum albumin) 용액에 희석 시킨 항체를 1.5 aM 부터 15 pM 까지 반응 시켜준 뒤 1x PBS 용액을 사용하여 potential 변화를 확인하였다. 그 결과, 항원-항체의 농도에 따른 potential 변화가 확인되었으며[그림 1(b)], 매우 낮은 농도에서도 항체를 검출할 수 있는 FET 기반의 B 형 간염 센서를 개발할 수 있었다. 본 연구의 결과는 반도체 FET 소자를 이용해서 간단하고 저렴한 방법으로 자가면역 질환의 현장 진단 응용 가능성을 보여주었다.

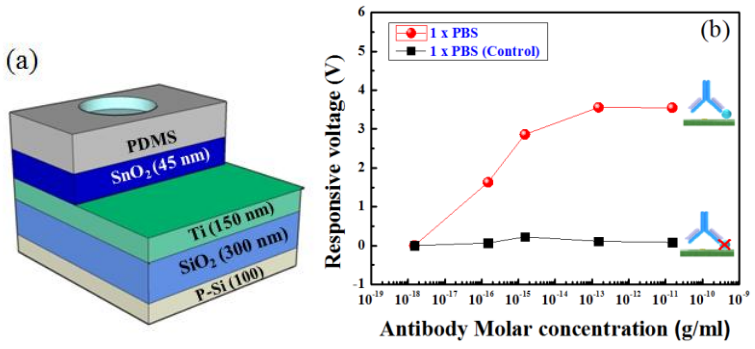

Fig 1. Schematic of EG-FET and changes in the threshold voltage as a function of concentration of antibodies.

[1] Dey. Ida Dzifa et al., "Autoimmune Disease: Diagnosis." *eLS*.

Sensitivity enhancement of Dual Gate EGFET by control of channel thickness of SOI transistor

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Extended-gate field-effect transistor (EGFET)는 화학 용액 속의 이온 농도를 감지할 수 있는 바이오센서로서, 측정부와 감지부가 분리되어 있는 구조를 가지고 있다. EGFET 는 고집적화, 낮은 단가, 높은 수율과 같은 많은 장점들을 가지고 있으며, CMOS 공정과의 호환이 가능하기 때문에 향후 센서의 상용화에 있어 큰 잠재력을 지닌다. 하지만, EGFET 는 바이오 물질들간의 반응으로부터 나오는 미소한 신호를 감지하는데 감도가 낮다는 단점을 가지고 있으며, 이를 극복하기 위해 SOI 기판을 이용하여 이중 게이트 (Dual gate, DG) 동작 모드를 갖는 DG EGFET 가 제안되었다. DG 동작은 SOI 기판의 구조적 특수성으로 인해 상부 FET 와 하부 FET 사이의 capacitive coupling 현상을 유도함으로써 감도를 크게 증폭시키는 동작 모드이다[1]. 본 연구에서 우리는 capacitive coupling ratio (감도 증폭율)에 영향을 주는 요소인 채널 두께를 조절함으로써, 감도가 더욱 향상된 SOI 기반의 DG EGFET 를 개발하였다. 이는 기존 센서의 낮은 반응 감도 한계를 극복함으로써 향후 고성능 바이오센서의 응용에 있어 유망한 소자가 될 것으로 기대된다.

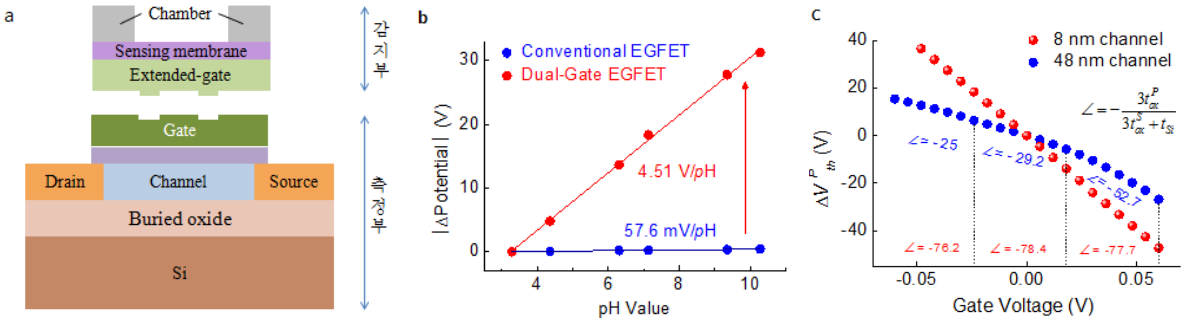

그림 1. (a) DG EGFET 의 모식도, (b) 기존 센서와 제안된 DG 센서의 pH 감도 비교
(c) DG 센서의 채널 두께에 따른 감도증폭율

[1] Ohata A, Pretet J, Cristoloveanu S, Zaslavsky A, Correct biasing rules for virtual DG mode operation in SOI-MOSFETs. IEEE Trans Electron Dev 2005;52(1):124-5

Development of Interdigitated Ring Electrode Array for Electric Cell Impedance Sensing

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A label-free and real-time monitoring of cells is often required for disease diagnostics and for drug screening assays at the cellular level. Electric cell impedance sensing (ECIS) is one of the label-free and real-time methods to monitor and analyze the cell behaviors e.g. adhesion, proliferation, differentiation and cellular responses to external stimuli such as pharmacological and toxic effects.[1] In the present work, we developed a unique interdigitated ring electrode (IRE) which provided better observability of the cell morphology around the electrodes compared to the traditional interdigitated electrodes. Further, the impedance spectra of IRE with cells during cell growth were measured and analyzed by using an equivalent circuit for the electrical characterization of the new sensor.

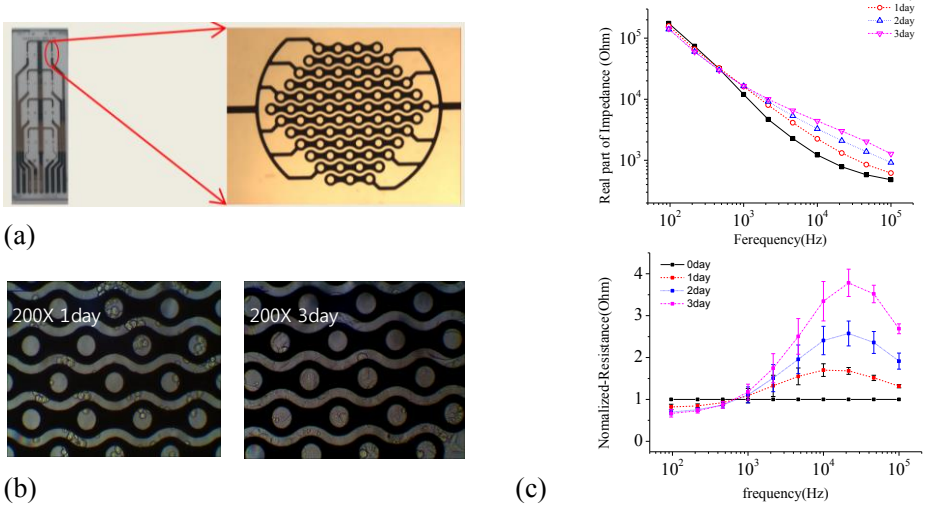

Fig 1. (a) Fabricated IRE array with both finger width and spacing of 20 μm, (b) Phase contrast micrograph of 293/GFP cells cultured on IRE for 1 day and 3 days, (c) Real part of impedance and normalized resistance with standard deviation (n = 4) measured during cell growth.

[1] H. Jun et al, Journal of Biomedical Nanotechnology 9,699 (**2013**).

Dependence of Hydrophilic Microchannel Length by O_2 Plasma Treatment on Microchannel Width and Entrance Hole Diameter of PDMS Mask

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Hydrophilic surface modification has been used to make hydrogen bonding for PDMS-based microfluidics, immobilization of DNA or antibody probes for biochemical sensors, or cell patterning for high throughput screening of drug candidates. Further, the hydrophilic surface patterning was utilized for neural network or spinal cord injury research [1]. The hydrophilic patterned surface can be fabricated by using microstamp with chemical solutions or O_2 plasma treatment with elastomeric masks [2]. In this article, it was reported whether the hydrophilic length can be affected by the hole size of the PDMS microchannel with O_2 plasma treatment.

For a master mold of PDMS microchannel, SU-8 (3050, Microchem, USA) was coated on a slide glass and patterned for a single channel with 240 μm width and 50 μm height by photolithography. A mixture of PDMS base monomer with curing agent (10:1) (Sylgard 184, Dow Corning, USA) was applied on the fabricated SU-8 mold and cured at 100 ˚C for 45 minutes. The PDMS microchannel released from the mold, and the both ends of a single channel were punched out with a 0.75, 1 or 1.5 mm circle punch. After the PDMS microchannel was positioned on a polystyrene (PS) dish, O_2 plasma was applied at 100 W, 0.5 Torr for 20 s (CUTE-RP/R, Femto Science, Korea). After taking out the PDMS structure, the 293/GFP cells with cell culture medium were applied on the PS dish, and incubated at 37 ˚C and 5 % CO_2 for 1 day.

The 293/GFP cells adhered only on the hydrophilic strip of PS surface treated by O_2 plasma but not on the hydrophobic PS surface masked by PDMS during O_2 plasma treatment. The strip length adhered with cells was dependent on the hole size of PDMS microchannel. The average length of the strip covered by cells was 4.80, 5.46 or 6.79 mm when the diameter of the opened hole was 0.75, 1 or 1.5 mm, respectively. Therefore, it was found that the degree of O_2 plasma treatment via PDMS microchannel is modulated by the hole size involving with the amount of O_2 plasma. Based on the result, it is expected to optimize the fabrication of the hydrophilic pattern using the O_2 plasma treatment with PDMS microchannel.

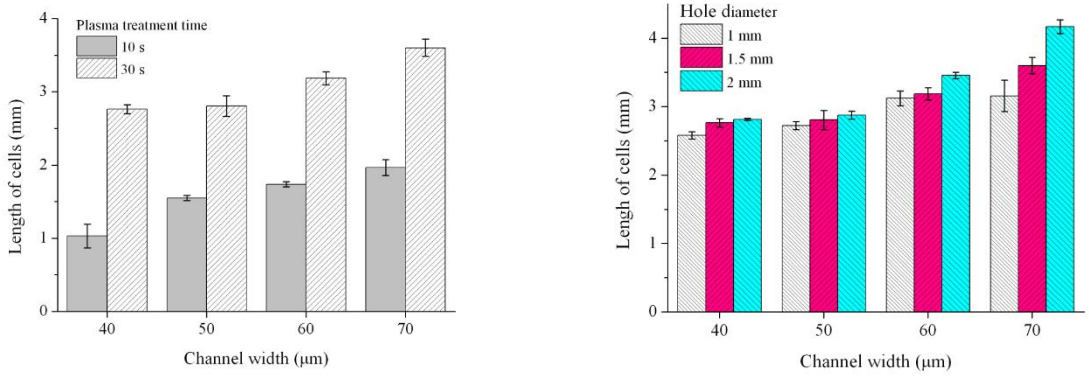

Fig 1. Averages and standard deviations of the length of cells patterned with respect to the channel width of PDMS mask and (a) O_2 plasma treatment time (hole diameter: 1.5 mm) or (b) the hole diameter of PDMS mask (plasma treatment time: 20 s), n = 4.

Reference

1. B. Vahidi et al, *Journal of Neuroscience Methods* 170, 188 **(2008)**.
2. A. Tourovskaia et al, *Langmuir* 19, 4754 **(2003)**.

Arbitrary vibration driven piezoelectric energy harvester using curled and elongated cantilever

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Most of cantilever based MEMS energy harvesters have generated several micro-watts of output power from induced single directional (vertical or longitudinal) vibration [1-2]. In this research, a curled and elongated cantilever ased piezoelectric energy harvester was newly developed to effectively scavenge three-dimensional ambient (or arbitrary) vibrations. In order to oscillate the cantilever with decent displacement under vertically induced, longitudinally and horizontally induced vibrations, the cantilever of the proposed energy harvester, called a hair-cell structure, is intentionally elongated and curled as shown in Fig 1 (a). The proposed energy harvester is comprised of the elongated and curled piezoelectric cantilever and a proof mass with high aspect ratio at the free end of the cantilever. Fig 1 (b) shows a SEM image of the fabricated energy harvester. The fabricated device generated the peak output voltage of 15 mV under vertically induced vibrations with an acceleration of 50 m/s^2 at its resonance frequency of 116 Hz. In addition, it also generated the peak output voltage of 33 mV and 10 mV under longitudinally and horizontally induced vibrations, respectively as shown in Fig 1 (c).

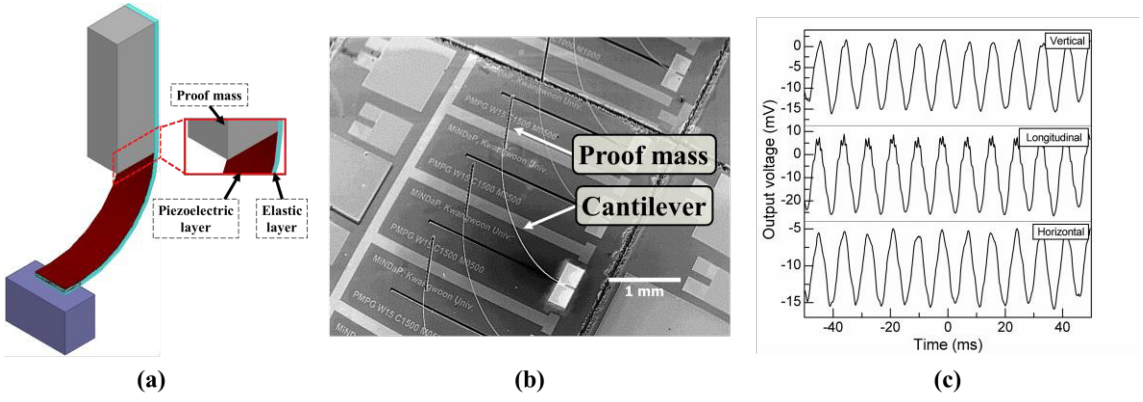

Fig 1. Proposed energy harvester and its frequency response: (a) proposed energy harvester, (b) SEM image of the fabricated energy harvester, (c) output voltage of the fabricated device

[1] Beeby S P, Tudor M J and White N M, Meas. Sci. Technol. 17 R175 (2006)
[2] Park J C, Park J Y and Lee Y, J. Microelectromech. Syst. 19 1215 (2010)

Dielectrophoretic On-Chip for Simultaneous Detection of Live Cell Responses to Small Molecule Drugs

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Quantitative detection of cellular responses of living cells is highly important in not only investigation of cell-to-cell signaling but also evaluation of novel drugs effect in nanomedicine. Although the microfluidic lab-on-chip is very useful in those studies to serve a variety of environment to living cells, it is restrictive for the quantitative detection of cellular dynamic responses to drugs that requires precise manipulation and enormous data collection. Here, we demonstrate that the microfluidic dielectrophoretic (DEP) chip enables simultaneous detection of cellular responses of live B16F10 human melanoma cells to small molecule drug such as N-ethylmaleimide (NEM). It is shown that the B16F10 cells are levitated by DEP force in the chip, which can allow quantitative characterization of three-dimensional (3D) cellular responses resulted from subtle variations in DEP properties of the cells as a function of NEM concentration. Using DEP modeling of a live cell, the changes of cellular biophysical dynamics attributed to activation of K^+/Cl^- cotransporter (KCC) channels distributed on the cell surface can be statistically analyzed by cellular responses to NEM which plays a specific role in inactivation of the ion channels.

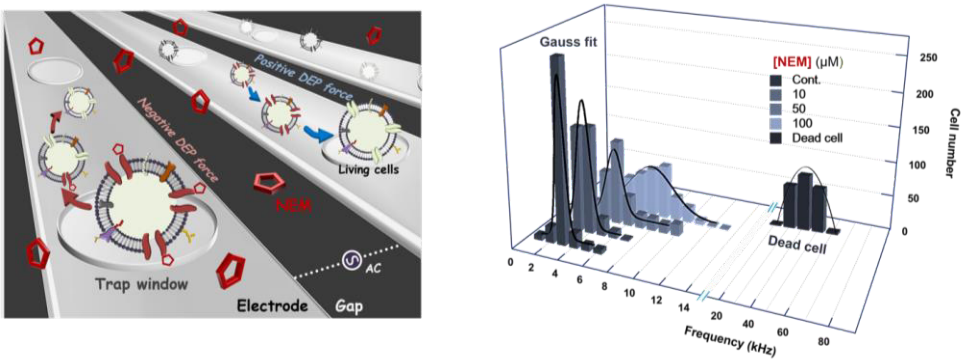

Fig 1. Quantitative detection methods and the result of cellular responses to small molecule drug.

[1] Cross, S. E., Jin, Y. S., Rao, J. and Gimzewski, J. K. *Nat. Nanotech* **2**, 780-783 (2007).

[2] Rotsch, C. and Radmacher, M. *Biophys* **78**, 520-535 (2000).

Direct measurement of frequency-dependent dielectrophoresis force in various medium condition

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Recently, movement of microsphere have been analyzed by various microelectrode design in dielectrophoresis(DEP) application for using medical and environmental science [1]. Mostly, knowledge of the quantitative DEP force is of primary importance in designing effective DEP devices that perform nondestructive separation and trapping, However, it is difficult to perform direct quantitative measurements of the frequency-dependent DEP force. In this study, we investigated the reliable DEP characteristics of non-functionalized and carboxyl-functionalized polystyrene microsphere in different concentration of electrolyte (NaCl) based on optical tweezers and a microfluidic chip. In case of carboxylated polystyrene particles, DEP characteristics was severely changed along the increase of electrolyte medium. It was affected by conductivity of medium solution. This phenomenon can be explained by a decrease in Debye length and the charge screening effect of an excessive NaCl concentration. When the NaCl concentration is increased, counter-ions collect near the bead surface, and the charge screening effect becomes predominant, resulting in a decrease in Debye length. This system can be used for the frequency dependent DEP manipulation and give insight into the design of practical application of DEP in microsystem.

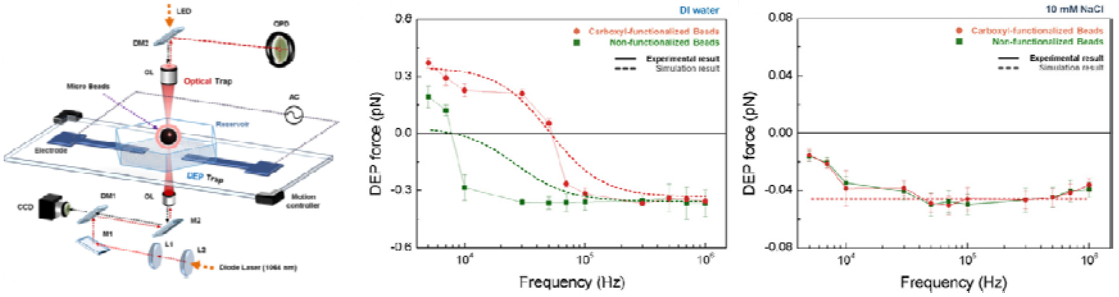

Fig 1. DEP force measurement device based on optical tweezers and its DEP force data

[1] Dash, S. and S. Mohanty, Electrophoresis, 35(18), 2656 (2014).

Fabrication of micro-probe sensor array using copper TGV(Through Glass Via)

Young-min Shin[1], Yong-Kweon Kim[1], Seung-Ki Lee[2], Jae-Hyoung Park[2,] *
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In the past decade, 3D Microelectrode arrays (3D MEAs) give a method for accessing numerous neurons simultaneously with spatial resolution [1]. With the growth of the 3D MEAs technology, the 3D MEAs need more high resolution accuracy about simultaneous and spatial sensing. For this reason, the 3D MEAs is required to new structure.

In this study, we explain a fabrication method about micro-probe sensor array using copper TGV. This electrode combined with micro-probe array and copper TGV. A copper TGV was fabricated by glass reflow and seedless electroplating process using low resistance Si substrate. This enables a vertical interconnection between the sensing pad and micro-probe sensor array through the glass substrate. A micro-probe array with high aspect ratio is achieved by the combination of anisotropic DRIE and isotropic RIE process of Silicon substrate, with one-step photolithography and single silicon oxide etch mask.

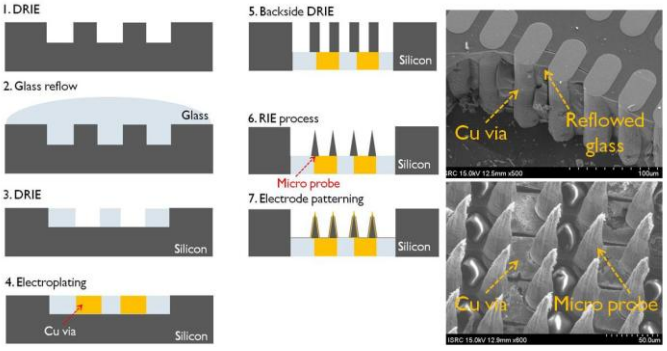

Fig 1. Fabrication process and fabrication result

[1] Y. Yao, M. N. Gulari, J. A. Wiler and K. D. Wise, *Journal of Microelectromechanical Systems*, 16, 977 (2007).

* Acknowledgement: This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education (2013R1A1A2008700).

Surface potential characterization of original and regrown amyloid fibrils

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Kelvin probe force microscopy (KPFM) which is known as a variant of atomic force microscopy (AFM) has been developed in 1991 [1] in order to measure the surface potential of nano/biomaterials such as nanoparticle, polymer, carbon nanotube, graphene and DNA.
In our previous study, we measured the surface potential of amyloid fibrils on silicon substrate by using KPFM.[2] Amyloid fibrils are critically contributed to degenerative diseases such as Alzheimer's, Parkinson's, and Creutzfeldt-Jakob diseases. For development of the therapeutic methods of such degenerative disases, ultrasonication has recently been used to break the amyloid fibrils. Although it is crucial to investigate the regrowth behavior of the broken fibrils formed by ultrasonication, the regrowth mechanism has not yet been fully elucidated.
In this work, we characterize the surface potential of original and regrown amyloid fibrils by AFM and KPFM, which is believed to help in understanding of the mechanism at the molecular level.

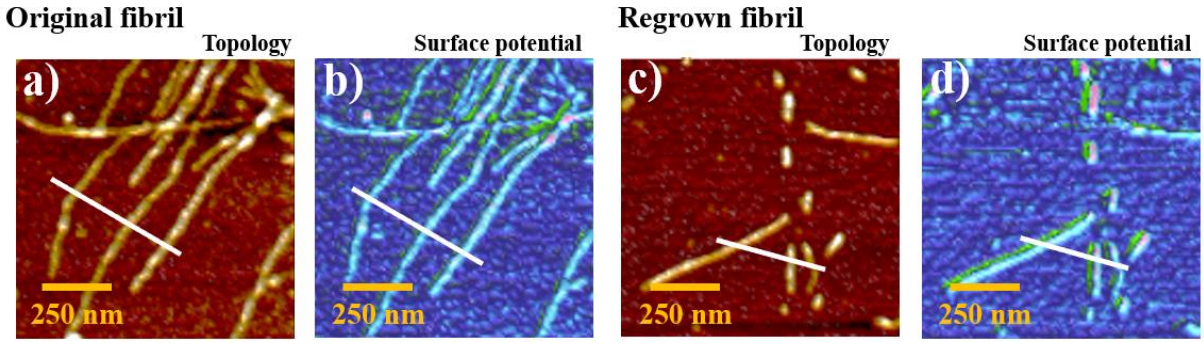

Fig. 1. KPFM image of original and regrown fibril. Topology image of original fibril a) and regrown fibril c). Surface potential image of original fibril b) and regrown fibril d).

[1] M. Nonnenmacher, M. P. O'Boyle, and H. K. Wickramasinghe, Appl. Phys. Lett. 58, 2921 (1911).
[2] G. Lee, W. Lee, H. Lee et al. Appl. Phys. Lett. 101, 043703-043704 (2012).

Characterization of DNA- gold nanoparticle conjugates surface potential with various substrates *via* Kelvin probe force microscopy

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Nanoparticle is a well used material for rapid, sensitive, reliable, and cost-effective genetic detection in clinical diagnostics [1]. DNA-gold nanoparticle has been applicable to an important part of molecular assemblies of genetic detection systems. Due to the negatively charged phosphate backbone of DNA, the surface charge of nanoparticle has a major impact on structural formation of molecular assemblies [2]. Here, by using Kelvin probe force microscopy (KPFM), we have chracterized the surface potential of DNA immobilized nanoparticle with various substrate (*i.e.*, Au, Si, SiO_2, and Fe). DNA-gold nanoparticles on various substrates are individually imaged, and their diameters and surface potentials are quantitatively measured by KPFM. It turns out that the difference in surface potential between nanoparticle immobilized P-C DNA and P-M_1 DNA on p-type Si substrate is larger than those on any other substrates. This leads to the suggestion that the Si substrate exhibits higher binding affinity to nanoparticle rather than others, and is a suitable substrate for nucleic acid assay using nanoparticle. Our approach enables not only characterization of the surface potential of DNA-gold nanoparticle, but also contribution to investigation of molecular interactions between nanoparticle and other molecules.

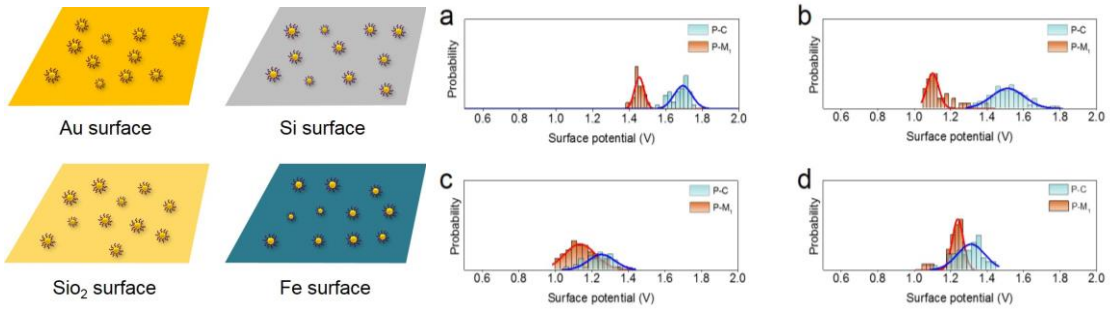

Fig 1. Schematic of experiment and surface potential distribution of DNA immobilized nanoparticle. (a) Gold substrate, (b) silicon substrate, (c) silicon dioxide substrate, and (d) iron substrate.

[1] J.-S. Lee, P. A. Ulmann, M. Han, and C. A. Mirkin, Nano letter. 8, 2 (2008).
[2] Y.-C. Lin. *et al.*, Journal of Colloid and Interface Science. 340, 126 (2009).

Influence of reduced graphene oxide-nanoparticle layers on indium tin oxide electrode in electrical cell-substrate impedance sensing

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Functionalized carbon based materials are popular due to their excellent electrical, mechanical and optical properties. Among many carbon based materials graphene, a two-dimensional (2-D) and one-atom-thick sheet, has been attracting much attention owing to its fascinating physical properties with wide range of applications [1]. Hence in this study, we fabricated a transparent indium tin oxide (ITO) disc electrode array electrodes through standard fabrication methods subsequntly the reduced graphen oxide-gold nanoparticle (rGO-NP) layer was electrodeposited by cyclic voltammetry (CV). The rGO-NP/ITO electrodes showed higher electrochemical conductivity compared to ITO electrodes and further with HEK 293 cells cultured directly on the electrode confirms the biocompatible nature of the modified electrode. Further to elucidate the influence of different layers of rGO-NP/ITO for HEK293 cells immbilization, the activity of cells on the electrode were investigated through the electrical cell substrate impedance (ECSI) sensing [2]. The observed cell proliferation, the impedance magnitude results revealed that HEK293 cells on rGO-NP/ITO electrodes has higher conductivity and biocompatibility comparred with rGO/ITO and NP/ITO electrodes. Thus, the developed rGO-NP/ITO electrode holds a great promise for electrochemial sensor and biosensor design.

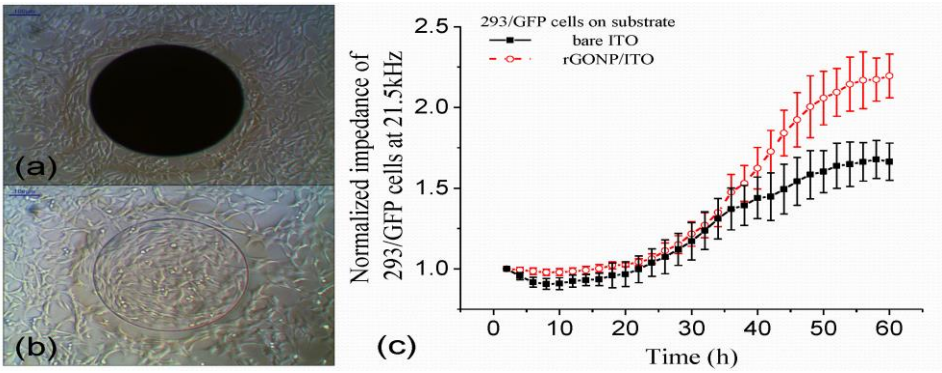

Fig 1. Optical phase contrast images obtained for a) HEK293 cells on rGO-NP/ITO and b) HEK 293 cells on ITO electrode. c) ECSI measurements on HEK cells on rGO-NP/ITO electrode.

[1] J. Yang, J. R. Strickler and S. Gunasekaran, Nanoscale. 4, 4594 (**2012**).

[2] F. Asphahani, M. Thein, O. Veiseh, D. Edmondson, R. Kosai, M. Veiseh, J. Xu and M. Zhang, Biosens. Bioelectron. 23, 1307 (**2008**).

A pressure driven flow control apparatus for microfluidic application

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In the field of microfluidics, the flow control systems such as syringe pump, peristaltic or piston pump have been used over the past decade. Existing setups typically rely on expensive syringe or peristaltic pumpss that exhibit poor temporal response and instability in fluid delivery, thus limiting theris utility in procedures that require precise muliport fluid injection and periodic flow stoppage[1]. In this paper, we present the simple and inexpensive pressure driven flow control apparatus. The pressure-driven flow control apparatus can have the pulseless flow due to no mechanical part and compose the multichannel flow easily unlike syringe pump. Throught digital control pressure-drive flow can accomplish the fast response time and scalable digital microflow. This appratus consist of pressure controller, control system and reservoir box. From the reservoir box, the controllable, precise and pulesless flow can supply to the microfludic chip. The pressure of reservoir box can be constantly maintained by the presuure controller. In order to evaluate the characteristics of the pressure-driven flow system, the flow rates have been measured with tygon tube(ID :0.25mm, OD :0.76mm). With 50kPa, the flow rate is 50~270 μl/min depedent on the length of the tube. With 10kPa, the flow rates have been controlled below 50 μl/min. The flow rate is inversely proportional to the length of the tube and proportional to the pressure. For microfluidic application, our proposed appratus is quite useful that many channels must be controlled at the same time and require the vairous flow rate.

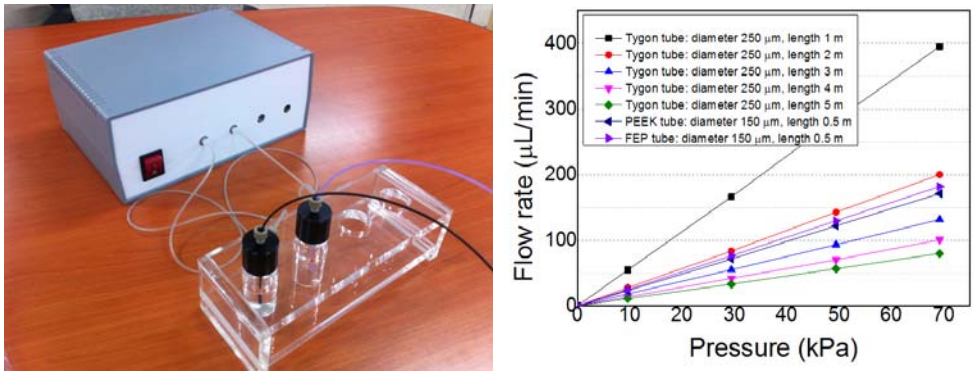

Fig 1. Flow control apparatus and its flow chracteristics

[1] K.W Bong, S C. Chapin, D C. Pregibon, D. Baah, T M. Floyd-Smith, P S.Doyle, Lab on a chip, 11., 743~747 (2011).

Structure optimization of THz modulator based on a uniform graphene

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E-mail : sangin@ajou.ac.kr

Graphene 은 단 원자 층으로 구성된 육각구조의 탄소물질로써 dirac cone 형태의 밴드구조로 인하여 나타나는 전자기적으로 특성에 대하여 많은 관심을 받고 있다. 특히 Terahertz 영역에서 전기적으로 graphene 의 optical condutivity 를 쉽게 조절이 가능하다는 점을 이용하여 광 변조기로 응용을 위한 연구가 진행되고 있다[1]. 이 논문에서는 Fig 1 과 같이 금속 반사체(Au)위에 일정한 거리에 위치한 graphene 에 대한 반사율 변화를 RCWA 방법을 이용한 시뮬레이션 하였다. 기존 논문의 결과와 다르게 graphene 의 도핑 농도가 높아지면서 반사율 변조를 최적화하기 위한 금속반사체와 graphene 의 거리가 변화함을 볼 수 있었다. 이는 graphene 이 단 원자 층으로 매우 얇은 두께를 가짐에도 optical condutivity 가 매우 커진다면 graphene 층에서 phase shift 가 발생하기 때문이다. 따라서 광변조기로써 성능을 최적화 하기 위해서는 graphene 과 금속 반사체의 광학적 거리를 0.284 λ 만큼 유지하고 0.181eV 까지 도핑하여 주었을 때 최대의 변조 폭을 가질 것으로 예상된다.

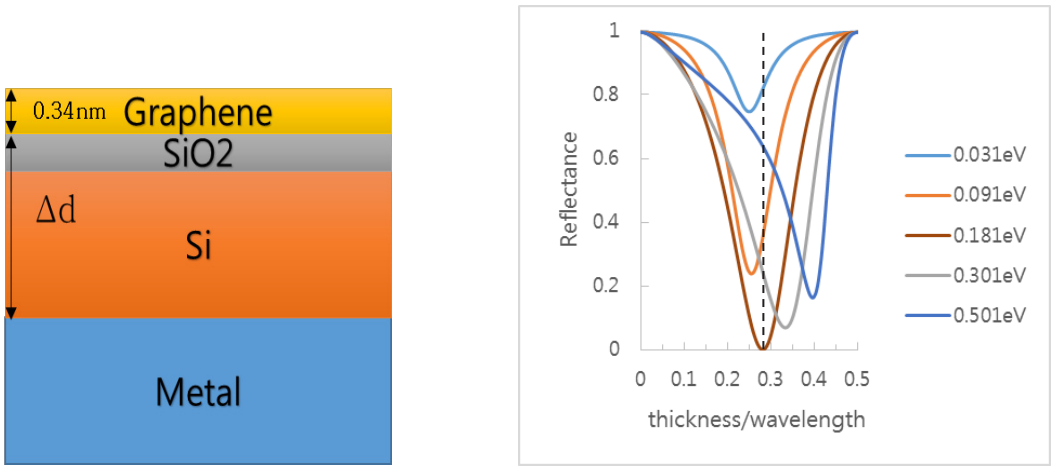

Fig 1. Graphene modulator structure and reflection spectrum.

[1] B. Sensale-Rodriguez, R. Yan, S. Rafique, M. Zhu, W. Li, X. Liang, D. Gundlach, V. Protasenko, M. M. Kelly, D. Jena, L. Liu, and H. G. Xing, Nano Lett. 12(9), 4518–4522 (2012)

plasmon-induced transparency in a graphene grating

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Plasmon-induced transparency (PIT)는 두 개의 플라즈닉 공진기의 상호작용에 의하여 특정 파장에서 투과가 커지는 현상을 의미하고, 강한 dispersion 에 의하여 빛의 군속도를 크게 낮출 수 있기 때문에 최근 PIT 에 관한 많은 연구가 진행되고 있다 [1]. 본 논문에서는 주기적으로 놓인 도핑된 그래핀 에 의하여 생성되는 그래핀 플라즈몬 공진모드와 금속과 유전체 사이에서 형성되는 표면 플라즈몬 공진 모드를 이용하여 PIT 현상과 유사한 흡수영역에서 반사가 급격히 커지는 현상을 발생시켰고 그 특성을 살펴보았다. 제안된 구조는 그림 1 에 나타내었다. 입사된 빛은 Au 에 의한 표면 플라즈몬을 여기 시키고, 생성된 플라즈몬 모드는 도핑된 그래핀에 의하여 생성되는 그래핀 플라즈몬 모드를 여기시킨다. 이 두 공진 모드간의 상쇄간섭에 의하여 그림 1 의 스펙트럼에서 볼 수 있듯이 흡수영역 특정 파장에서 급격히 반사가 커진다. Reflection peak 지점에서 계산된 delay time 은 3ps 이다.

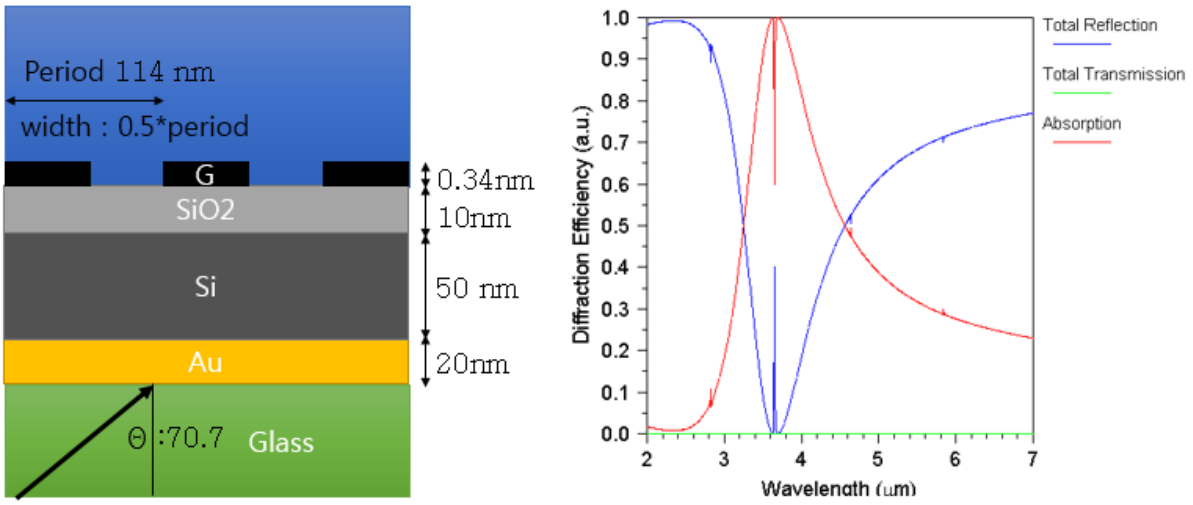

Fig 1. Proposed graphene based PIT structure and transmission spectrum.

[1] S. Zhang, D. A. Genov, Y. Wang, M Liu, and X. Zhang, Phys. Rev. Lett. 101, 047401 (2008).

Taste sensor based on cascoded compatible lateral bipolar transistor (C-CLBT) for detection of sweetness

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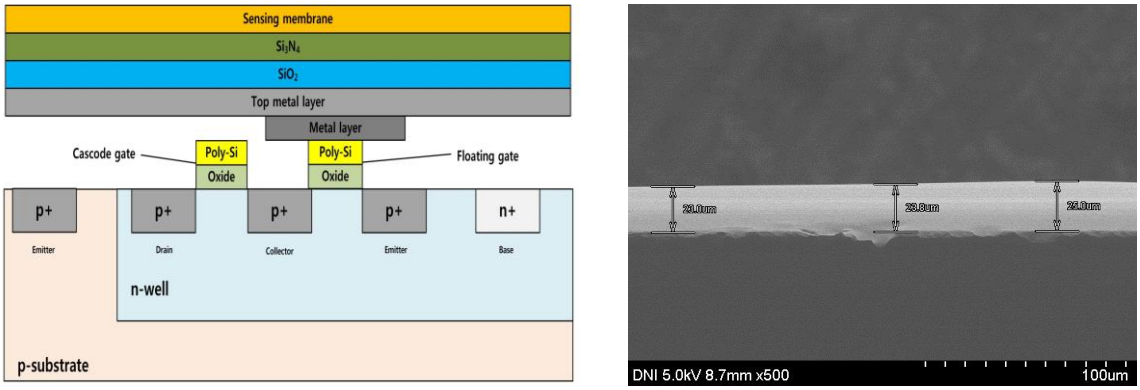
Food is one of the most important requisites for human's life. A global selectivity taste sensors are already developed by many researchers. However, taste sensors that have higher sensitivity are needed with improving the quality of life. We developed high sensitivity taste sensor using new device called Cascoded Compatible Lateral Bipolar Transistor (C-CLBT) [1]. The schematic is shown in Fig. 1 (a). This device was fabricated by Magnachip-SK Hynix Co. Ltd. Via the Integrated Circuit Design Education Center Multi-Project Wafer (IDEC - MPW) project using a standard 0.35 μm logic process. As shown in Fig. 1 (b), the sensing membranes consist of a conductive polymer and a lipid membrane on passivation layer. The Dioctyl phosphate (DOP) was used as lipid membrane for detecting sweetness taste substance [2]. According the results, the C-CLBT can be used taste sensor and the sensing limit was approximately 1 fmol/L.



(a) (b)

Fig 1. Schematic of taste sensor structure (a), FE-SEM image of conductive polymer (b).

[1] van Schaik, André, Eric Fragnière, and Eric Vittoz. "Improved silicon cochlea using compatible lateral bipolar transistors." *Advances in neural information processing systems* (1996): 671-677.

[2] Toko, Kiyoshi. "Taste sensor." Sensors and Actuators B: Chemical 64.1 (2000): 205-215.

This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea Government (MSIP) (No.2008-0062617) and in part by IDEC.

Fabrication of silicon microlens array on flexible substrates using a transfer printing

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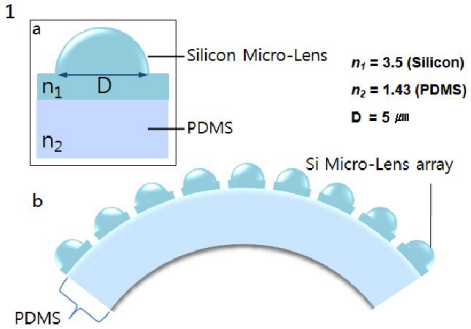
One of the appealing features of microlens arrays that gained popularity recently is their ability to be fabricated onto curved surfaces to increase their field of view (FOV)[1]. However, for most traditional fabrication processes, the fabrication of optical elements such as ommatidia or microlenses onto curved surfaces is a challenge. Polydimethylsiloxane (PDMS) is a promising polymer material for fabrication of microlens arrays on curved surfaces, since it has fascinating properties, such as low surface energy, thermal curing property, and it's soft nature. Unfortunately, it's relatively low refractive index (n = 1.41) is not desirable for practical applications. Microlens arrays in silicon are suitable for an important wavelength range within the IR spectrum, since silicon features relatively high refractive index and is transparent at the aimed wavelengths, leading to microlenses with a focal length short enough to allow compact systems. In this paper, we propose an alternative solution for the fabrication of silicon microlens arrays using conventional thermal reflow and dry etching processes on a SOI (Silicon On Insulator) wafer, followed by the transfer printing on a PDMS substrate combining the advantages of elasticity of PDMS and high refractive index of silicon. The performance and detailed fabrication processes will be introduced.

* This work was partly supported by the KBSI grant (D34500) and by Basic Science Research Program through the NRF of Korea funded by the Ministry of Science, ICT & Future Planning (2014R1A1A1005945).

1



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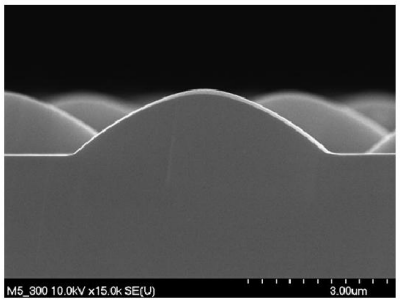

Fig1 | Schematic illustration of silicon microlens array on the PDMS substrate
Fig2 | Cross-sectional SEM image of the silicon microlens array.

[1] Y. M. Song, Y. Xie, V. Malyarchuk, J. Xiao, I. Jung, K.-J. Choi, Z. Liu, H. Park, C. Lu, R.-H. Kim, R. Li, K. B. Crozier, Y. Huang, J. A. Rogers, Nature 497, 95 (2013).

Electrical Determination of NT-proBNP utilizing the Competitive Assay Method for Biosensor Application

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[2]*Department of Biochemistry and Molecular Biology & Cancer Research Institute, Seoul National University College of Medicine*
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The properties of biomolecules, such as charge density and bio-affinity, are significantly influenced by the surrounding environment. Tight control of these properties guarantees stable biosensor performance. The screening effect means that ions against the target molecule in the solution neutralize the charge of the target molecules; hence, the sensitivity of the biosensors is degraded by the screening effect. This problem can be solved by using the small molecules such as peptide as the receptor rather than using the antibody which is usually a large molecule, so immune to the charge screening effect. In this work, we employed the competitive assay method in order to utilize the peptide as the receptor molecule.

In the present study, authors proposed the electrical detection of a N-terminal probrain natriuretic peptide (NT-proBNP) using competitive assay method in order to utilize the peptide as the receptor molecule. The receptor peptides were expressed and produced by Dr. Chung's group [1]. The designed peptide has been used as the receptor of the NT-proBNT for the biomarkers of heart failure disease. The peptide molecules were introduced to thiol group and attached to the CGi system by covalent bonding (a carbon nanotube network as the electrical channel decorated with the gold nano particles). Then, the antigen-antibody complexes solution was dropped on to the electrical channel. At this time, the concentration of the antigen was unidentified. Although, the amount of antigen (biomarker) is not clear, the antibody molecules which have not hybridized with the antigen molecules will be bonded to the peptide on the electrical channel, thereby causing the change in the current. It is possible to indirectly estimate the antigen by monitoring the current change (Fig1). If the concentration of NT-proBNP is more than 2ng/ml more in blood, the probability of heart failure increases to 95%. The peptide has an epitope, pep9-12, that matches the antigen. The antigen, the antibody, and the peptide are provided from Dr. Chung's group. The pulse-train (0.3V in amplitude, 1kHz) generated by the function generator has been applied to the electrical channels and four non-inverting operational amplifier circuits have been used to convert the output current to voltage signals. The Fig.2 and Fig.3 show the change in the normalized current of CNT channel as function of time after applying two samples; one with NT-proBNP antibody of 100ng/ml and the other with phosphate buffered saline(PBS) without antibody. Based on combined result, the selectivity of the antibody and peptide was confirmed.

In conclusion, the electrical detection of the antigen molecules was successfully confirmed by the receptor peptide in the electrical channel. This technique can be possible to alternative NT-proBNP detection biosensor in the near future.

This work was supported by the Brain Korea 21 Plus Project in 2015 and this research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (NRF-2012-0009555).

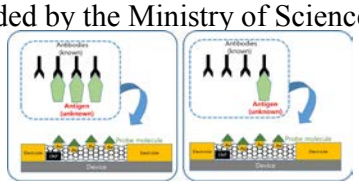

Fig.1 scheme of the competitive assay method

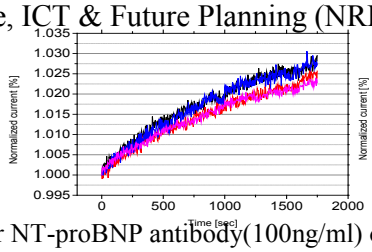

Fig.2 The normalized current characteristic for NT-proBNP antibody(100ng/ml) on pep9-12(1μg/ml)

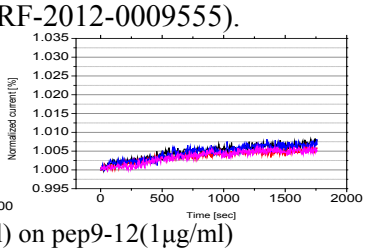

Fig.3 The normalized current characteristic for PBS on pep9-12(1μg/ml)

[1] Yujean Lee, Hyori Kim, and Junho Chung, Experimental & Molecular Medicines (2014)46,e114.

Detection of E-Coli in Solution by using Quartz Crystal Microbalance

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E-coli is one of the intestinal bacteria of warm-blooded organisms, however, pathogenic types may cause serious food poisoning and various diseases such as cystitis, pyelitis, peritonitis, sepsis or neonatal meningitis [1]. Therefore, the fast and accurate detection of E-coli is continuously and increasingly required for food and health protection. In this study, the direct detection of E-coli in solution was investigated by using Quartz crystal microbalance (QCM), real-time and quantitative detection of mass by measuring the change in frequency of a quartz crystal resonator [2].

For experiment, E-coli at different CFU/ml was prepared by dilution with LB medium and then each 50 μl of sample was applied to a QCM gold electrode (International Crystal Manufacturing co. (ICM), USA) by using a flow cell and peristaltic pump (KDS200, KS Scientific, USA). While injecting the E-coli cells, the resonant frequency of the QCM sensor was recorded by a frequency oscillator (35366, ICM, USA) and counter (53131A, Hewlett-Packard, USA). Fig. 1(a) shows the measured frequency of QCM during the application E-coli with a concentration from 1.77 x 10 to 1.77 x 10^8 CFU/ml. The frequency was immediately decreased as soon as the solution with E-coli was applied. Due to the mass of E-coli, the frequency was shifted according to the Sauerbrey equation: $\Delta f = -2\Delta m {f_0}^2 / A\sqrt{\rho_q \mu_q}$, where, Δf is frequency change, Δm mass change, f_0 resonant frequency, A is piezoelectrically active crystal area (= 408.4 cm^2), ρ_q density of quartz (= 2.643 g/cm^3), μ_q shear modulus of quartz for AT-cut crystal (= 2.947 x 10^{11} $g \cdot cm^{-1}s^{-2}$).

From the equation and measured frequency shift, the mas change caused by the different concentration of E-coli was drawn in Fig. 1(b). Symbols and bars in the figure represent the average and standard deviation (n = 4). The result proved that the E-coli in solution could be directly detected by QCM without any surface modification of the electrode for E-coli adhesion. Therefore, it is expected that QCM based sensing is feasible for real-time and quantitative detection of E-coli in solution, which is required for food and health protection.

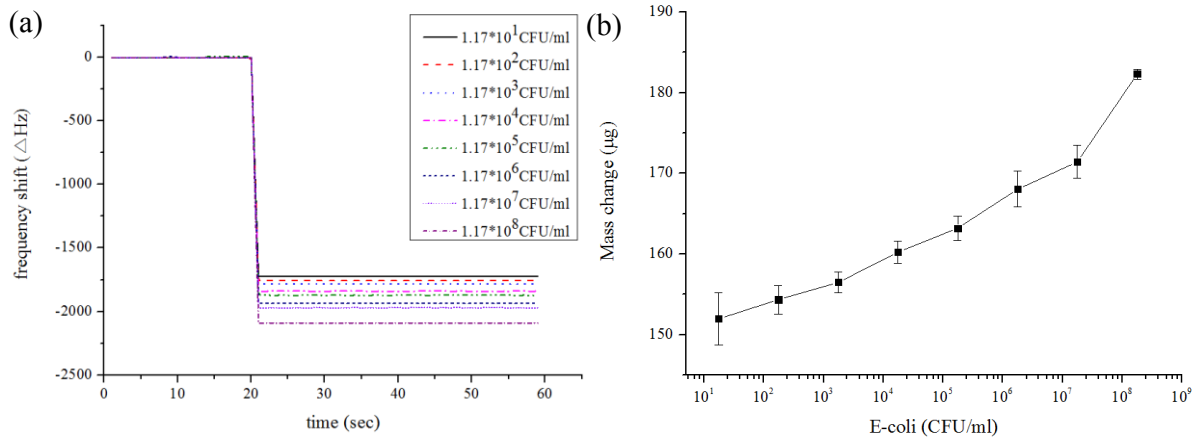

Fig 1. (a) Frequency change of QCM sensor during injecting 50 μl of LB media with different concentration of and (b) Mass change with respect to the E-coli concentration.

[1] Subramanian Krishnan et al, *The Journal of Infectious Diseases* 16.7 (2014)
[2] Shen, Zhihong, et al, *Analytical chemistry* 79.6 (2007)

Edge Contacts of Graphene Formed by Using Controlled Plasma Treatment

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Despite that the outstanding properties of graphene are well known, its electronic performance is limited by the contact resistance of the metal-graphene interface. In this study, we demonstrate the use of a controlled plasma processing technique for "edge-contacted" graphene in which bonding between the edge of the graphene and the contact metal is facilitated by controlling the edge structure and the significant reduction of the contact resistance. This simple approach requires no additional post-processes and has been proven to be very effective. The controlled pre-plasma processing was applied to produce CVD-graphene field effect transistors with enhanced adhesion and carrier mobility. The contact resistance attained by using the pre-plasma processing was 270 Ω·μm, which is a 77% decrease from that without it.

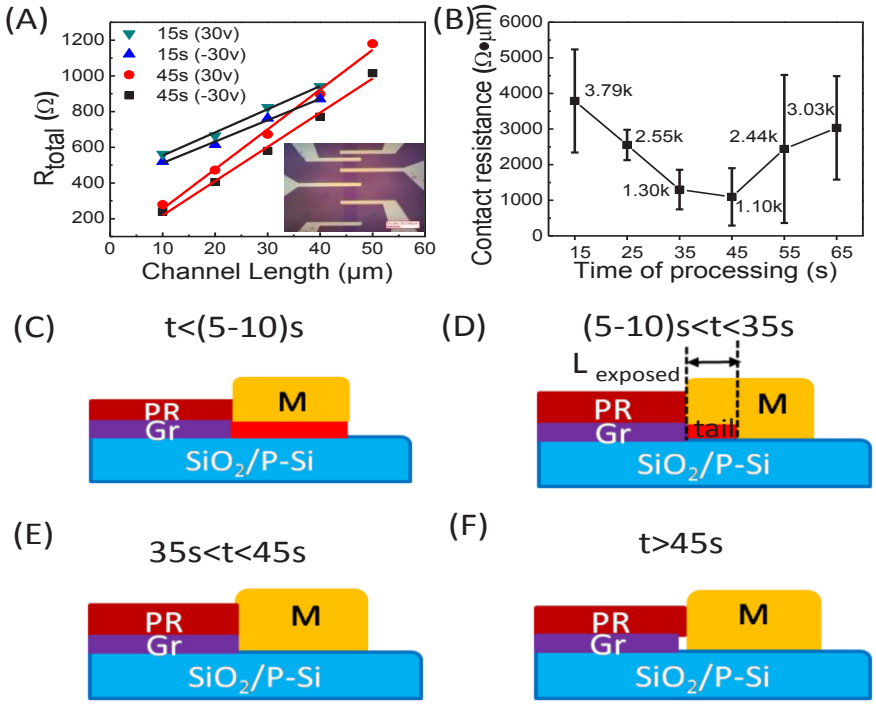

Figure 1 Establishment of Edge-contact and Reduction of R_c.

Synthesis of SnS Nanomaterials in Aqueous Solution and their Morphology Control

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Two-dimensional (2D) layered materials such as graphene and transition-metal chalcogenides have drawn widespread interest because of their uncommon electronic, physical and chemical properties associated with lateral anisotropy.[1-3] Here we report a surfactant free, low temperature, aqueous phase synthesis approach for highly crystalline two-dimensional (2D) SnS nanosheets having ~500 nm lateral dimension. The synthesis procedure involves two steps, first the formation of an intermediate tin oxide hydroxide and then its transformation into the nanosheets in presence of sulfur precursor. Interestingly, we have found that in presence of a small amount of polyvinylpyrrolidone (PVP) as surfactant during the synthesis, the final product is well defined nanocubes instead of nanosheets. Based on theoretical surface energy calculation, we anticipate that the stabilization of surface energy in presence of PVP might be the driving force for the formation of nanocubes, under similar experimental condition. Finally, the optical property of synthesized SnS nanosheets and cubes are investigated and we have found an wide UV-vis-NIR absorption pattern with a maximum at around 570 nm.

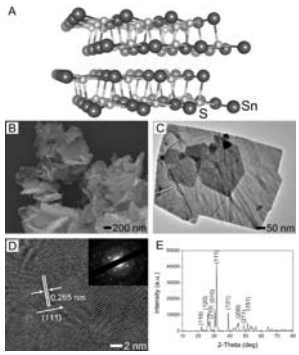

Fig 1. Structural analysis of SnS nanosheets

1. Geim, A. K.; Novoselov, K. S., Nat Mater 2007, 6, (3), 183-191.
2. Huang, X.; Yin, Z.; Wu, S.; Qi, X.; He, Q.; Zhang, Q.; Yan, Q.; Boey, F.; Zhang, H., Small 2011, 7, (14), 1876-1902.
3. Min, Y.; Moon, G. D.; Kim, C.-E.; Lee, J.-H.; Yang, H.; Soon, A.; Jeong, U., J. Mater. Chem. C 2014, 2, (31), 6222.

Highly effective piezoelectric nanogenerator and self-powered pressure sensor using micro-patterned film

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Understanding in optimizaing surface morphology of piezoelectric film is quite critical for improvement of power performance of nanogenerator (NG). In this report, we fabricated line and pyramid-like micropatterned flexible piezoelectric P (VDF-TrFE) polymer films based nanogenerator for effectively converting mechanical energy into electrical energy under vertical compression and for highly sensitive self-powered pressure sensor. The output voltage and current reached up to high value of 3.8 V, 2.4μA and 4.4 V, 3.3μA for line and pyramid-like micropatterned P (VDF-TrFE) based NGs, respectively, while non-patterned P (VDF-TrFE) based NG exhibited low output power under same vertical compressive force. The micro patterning process made P (VDF-TrFE) polymer ultra-sensitive in response of mechanical deformation, and we successfully demonstrated their application as self-powered pressure sensor in which mechanical energy came from water droplet and wind. The mechanism of the high performance was intensively discussed and illustrated in terms of strain developed in flat and micropatterned films. The impact derived from the pattering on the output performance was studied in term of effective pressure using COMSOL simulation.

Flexible One Diode-One Block Copolymer Incorporated Phase Change Memories Array on Plastic Substrates

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Keywords: Flexible electronics, Flexible memory, One diode-one resistor, Phase change memory, Block copolymers, Self-assembly

Currently, flexible electronics are at the high level of industrial and academic interest because of their potential for being very thin, light weight, less-breakable, and amenable to bio-implantable or wearable devices in comparison to devices built on the conventional rigid Si or glass substrates. Ease access to flexible electronics possibly extends their potential applications to flexible displays, batteries, and electrodes. Especially, flexible memory is the fundamental component for data processing, information storage, and radio frequency communication in the flexible electronics systems. Up to now, most studies on phase change random access memory (PRAM) have focused on the conventional bulk silicon technology except for a few elegant approaches (Cite the relevant references). Therefore, there is still a big challenge to improve performance efficiency of the flexible PRAM. In this paper, we developed flexible one-diode-one phase change memories array by spatially integrating a high-performance single crystal diode with a block copolymer (BCP) incorporated phase change memory (PCM), the chronic issue of power consumption and cell-to-cell interference between adjacent memory cells can

be effectively solved. This work can create a new chance of practical methodology to realize the nonvolatile memory for the flexible electronic applications.

A Study of Passivation affecting Power Output of Zinc Oxide Based Piezoelectric Nanogenerators

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Understanding power generation behaviors of a nano generator is essential to apply it as a sustainable power source for wireless sensors and microelectronics. Generally, piezoelectric nano generators based on semiconducting material zinc oxide (ZnO) can generate only a few volts intrinsic piezoelectric potential owing to free carriers screen some part of the piezoelectric potential. Lee et. al. reported p-type polymers could prevent the piezoelectric potential screening effect at the interface of ZnO, and by introducing a conducting polymer, 36 times increased output power was achieved. For further enhancement, we believe understanding and optimizing a relation between ZnO piezoelectric potential, purity, and crystallinity is essential. In the present study, c-axis oriented insulator-like sputtered ZnO thin films were grown in various temperatures to fabricate an optimized nano generator. The purity and crystallinity of ZnO were investigated with X-ray diffraction (XRD), and low temperature (10K) photoluminescence (PL). Insulating-type ZnO thin film-based NGs (IZ-NGs) generates output voltage around 1.5 V that is over ten times higher than that of an n-type ZnO thin film-based NG (around 0.1V). It was discussed how piezoelectric passivation effect works in ZnO thin films having different types of defects.

Development of real-time resynchronization system for plug and play quantum key distribution

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한국과학기술원 나노양자정보연구센터

양자암호시스템은 수학적 복잡성이 아닌 비가역적인 물리학적 자연현상에 기반 하여 비밀 키를 송신자(Alice)와 수신자(Bob)가 안전하게 나누어 가질 수 있는 암호시스템이다. 양자암호시스템의 송신자는 매우 감쇄된 단일광자 수준의 빛을 전송하고, 수신자는 단일광자검출기를 이용하여 신호를 측정한다. 전송하는 광자에 송신자는 정보를 인코딩하고 수신자는 디코딩 하는 과정에서 양자암호통신 프로토콜에 의해 송신자와 수신자는 안전하게 비밀 키를 나누어 가지게 된다. 단일광자검출기는 잡음에 취약하여 보통 저온에서 동작하며 게이트를 열어주어 열린 시간동안 광자가 오는 경우 측정이 된다. 그러므로 정확한 광자의 도착시간에 게이트를 단일광자검출기에 열어주어야 하기 때문에 단일광자를 측정하는데 있어서 송신자와 수신자간의 동기화는 양자암호시스템에서 매우 중요한 부분이다.

Plug and play 양자암호시스템은 수신자가 강한 빛을 송신자에게 전송하고 송신자는 강한 빛을 읽어서 동기를 유지하여 인코딩을 하고, 빛의 감쇄를 통해 단일광자수준의 빛을 다시 수신자에게 전송하는 Two way 시스템이다. 이러한 시스템 아키텍처는 수신자가 먼저 강한 빛을 전송하고, 수신자가 다시 단일광자검출기로 광자를 측정하므로, 광자의 송신 시점을 정확하게 알 수 있어 동기 시스템을 구축하는데 다른 양자암호시스템에 비해 매우 편리하다. 또한 중요한 특징으로 Plug and play 양자암호시스템은 빛 신호가 동일하게 두 번 환경적인 잡음이 반영되므로 편광의 변화 등이 자동적으로 보상된다. 따라서 실시간 Plug and play 양자암호시스템 구동에서 Quantum bit error rate(QBER)의 증가와 Key rate의 감소는 주로 온도변화에 따른 광자전송채널의 길이변화에 의한 광자도착시간과 게이트 시간이 달라져 생기게 된다. 그러므로 Plug and play 양자암호시스템에서 QBER 및 Key rate 자동보정은 Key rate의 실시간 모니터링을 하여 광자의 도착시간 변화에 맞춘 게이트 시간의 Tracing만으로 이루어질 수 있다.

QBER 및 Key rate 자동보정을 실험하기 위해 실시간으로 Plug and play 양자암호시스템을 1시간 동안 구동하였고, 임의로 온도변화를 주었다. 실험에서 게이트 시간의 폭은 4ns, Tracing step은 600ps로 하였다. 그림 1은 동기화 자동 보정 흐름도이고, 그림 2는 실험결과를 나타내고 있다. 그림 2에서 실시간 모니터링 알고리즘에 의해 50분 동안 3번 Key rate가 자동보정 되었다.

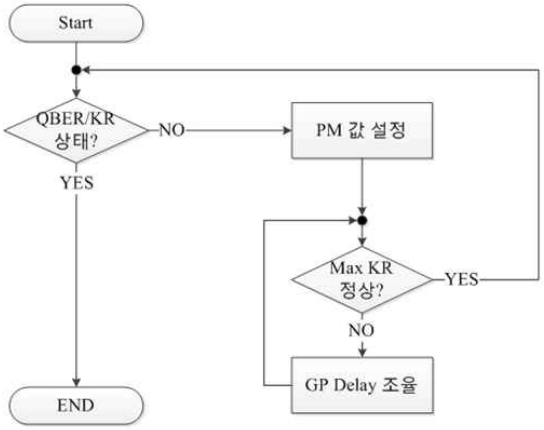

그림 1. 동기화 자동 보정 흐름도

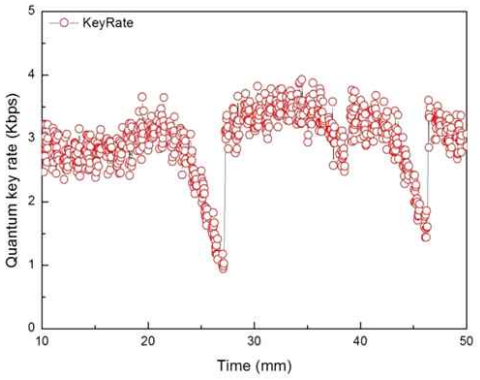

그림 2. 자동 보정에 따른 Key rate 회복

플러그 앤 플레이 측정 장비 무관 양자키분배 실험

김용수 [1], 최유준 [1,2], 권오성 [1], 한상욱 [1], 문성욱 [1]
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양자키분배는 BB84 프로토콜이 처음 제안된 이후 양자정보과학의 가장 실용적인 기술로 평가되고 있다 [1]. 양자역학의 법칙들에 근간을 둔 양자키분배는 이론적으로 해킹(도청)이 불가능하지만, 실제 장비로 구성한 시스템에서는 장비의 불완전성으로 인해 다양한 해킹 방법들이 이미 제시된 상태다. 측정 장비 무관 양자키분배는 이러한 이론과 실제의 차이를 줄이기 위해 제안되었다 [2]. 측정 장비 무관 양자키분배는 검출기의 불완전성을 이용한 모든 해킹 방법을 막을 수 있어서 보안을 대폭 향상시킬 수 있다. 하지만 벨 상태 측정을 위해 빛의 파장, 편광, 타이밍을 일치시켜야 하기 때문에 비싸고 복잡한 능동 조절 유닛이 필요하고, 따라서 실용성이 떨어지는 측면이 있다. 본 논문에서는 플러그 앤 플레이 방식을 측정 장비 무관 양자키분배에 적용하였다. 플러그 앤 플레이 방식을 쓰면 능동 조절 유닛 없이 파장이 일치되고 환경 변화에 따른 위상과 편광 변화가 보상되는 장점이 있다. 결과적으로, 플러그 앤 플레이 측정 장비 무관 양자키분배는 더 안전하고 실용적인 양자키분배를 가능케 할 교두보가 될 것이다.

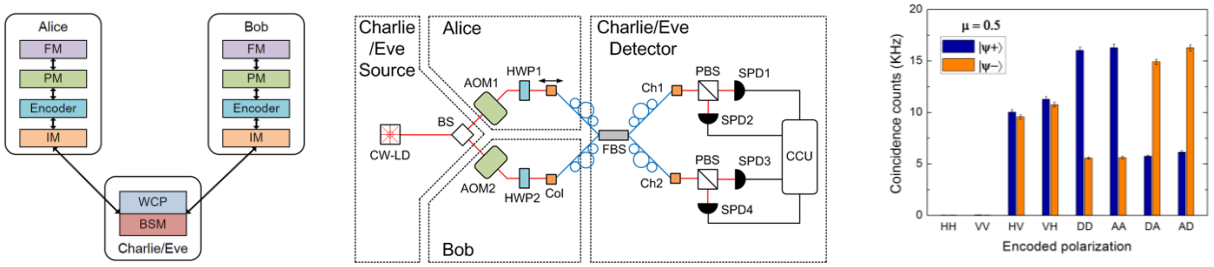

그림 1. 개념도와 실험셋업과 결과 데이터

[1] Bennett, C. H. & Brassard, G. Quantum cryptography: public key distribution and coin tossing. *Proceedings of the IEEE International Conference on Computers, Systems and Signal Processing*, Bangalore, India 175-179 (1984).
[2] Lo, H.-K., Curty, M. & Qi, B. Measurement-device-independent quantum key distribution. *Phys. Rev. Lett.* 108, 130503 (2012).

Quick chemical synthesis of molybdenum disulphide nanosheets, microplates and thin films

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Two-dimensional layered metal sulphide materials such as MoS_2 and WS_2 exhibit many unique properties, and are thus attractive materials for numerous applications. However, the high-yield, large-scale synthesis of well-defined metal sulphide nano/micro structures by a facile wet-chemical method is yet to be realized. Here we demonstrate a surfactant-free, quick, scalable, microwave-stimulated wet-chemical method for the synthesis of well-defined ultrathin MoS_2 nanosheets (~100 nm) and microplates (~1-2 μm). Electron microscopic results reveal that the synthesized MoS_2 nanosheets and microplates are highly crystalline. Moreover, following the same procedure we successfully synthesize large area thin MoS_2 films on Si substrate, where the thin film can reach an area scaling up to mm^2. Finally this synthetic protocol is extended to synthesize other metal sulfides such as WS_2, SnS and PbS nanocrystals.

Graphene/Hexagonal Boron Nitride Heterostructure-Based Transparent Flexible Microheater

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Herein, we demonstrate graphene/hexagonal boron nitride (h-BN) heterostructure-based transparent flexible (TF) microheaters that are very useful in novel applications such as flexible gas sensors, micro-fluidic lab-on-chip devices, micro-reactors, and electronic skins. For the fabrication of TF microheaters, large-scale graphene synthesized in a chemical vapor deposition (CVD) process is transferred on a polyethylene naphthalate substrate, patterned and then protected by a CVD-grown h-BN nanosheet. Our microheaters achieved a heating temperature in excess of 200 °C in circular active regions of diameter ~146 μm with no hot spots, and maximum temperature difference of ~21 °C. Bending tests confirmed that the proposed microheaters are mechanically robust and flexible. The basic building block of the demonstrated graphene/h-BN heterostructure-based microheaters can be easily embedded into more complex structures and devices.

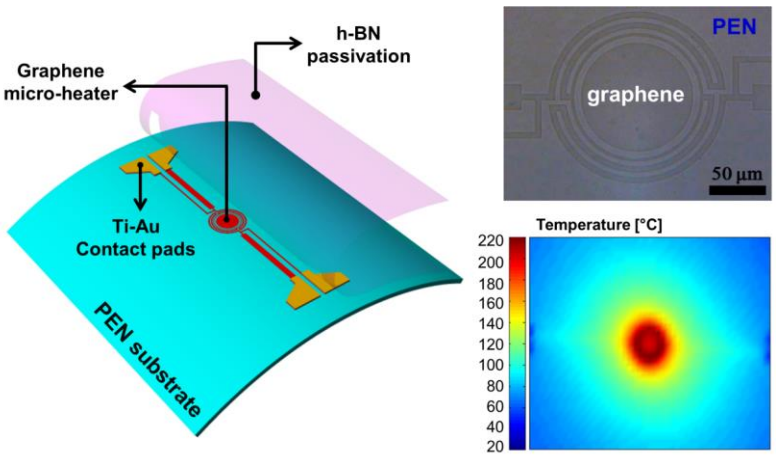

Fig 1. Graphene microheater structure, highly contrasted optical microscopy image and uniform temperature distribution image obtained by thermal camera.

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Photoresponse characteristics of MoS_2 field effect transistors under gate-bias stress conditions

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Recently, molybdenum disulfide (MoS_2) has attracted great attention due to its intriguing electrical properties. We have previously investigated the gate-bias stress-induced electrical instabilities of MoS_2 field effect transistor (FET) devices [1]. For example, we observed that when a positive (negative) gate bias stress was applied to the device, the current decreased (increased) and the threshold shifted in the positive (negative) gate bias direction. These phenomena can be explained by the charge trapping due to the adsorption or desorption of oxygen and/or water on the MoS_2 surface with a positive or negative gate bias, respectively [1]. We also investigated photoresponse characteristics of MoS_2 FET under various gate-bias stress conditions. We varied oxygen pressure of the measurement environment and applied different gate bias stress when we measured the photoresponse characteristics of the device [2]. More recently, we are investigating the effect of alkylthiol molecules deposition on the MoS_2 FET. When we deposit thiol molecules on MoS_2, the thiol molecules tends to be chemically absorbed at the sulfur vacancy site of the MoS_2 channel and influence the electrical properties of MoS_2 FET. Our studies will be helpful in understanding the electrical properties of the MoS_2-based electronic devices.

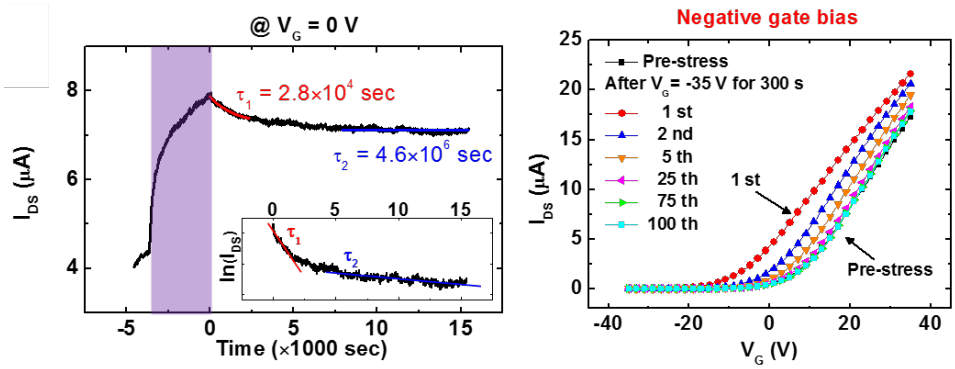

Fig 1. (left) Photoresponse characteristics and (right) electrical data of MoS_2 FETs

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Modulating the Energy-Band Structure of Hybrid Heterojunctions with Self-Organized P(VDF-TrFE) Nanomatrices

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Recently, organic and inorganic components have attracted much attention in hybrid optoelectronic devices due to combined advantages of the two material classes.
We investigated ferroelectric coupling effects on the energyband structure of the hybrid heterojunction of poly(3-hexylthiophene- 2,5-diyl) (P3HT)/zinc oxide (ZnO) in a self-organized P(VDF-TrFE) nanomatrix. We designed a novel architecture for the self-organized photoactive polymer layer, consisting of a P3HT domain in a P(VDF-TrFE) matrix, without any additional processes for incorporating ferroelectric material. P3HT with p-type conductivity and ZnO with n-type conductivity were used to show a well-defined bilayer p.n junction interface. We analyze The effects of ferroelectric polarization on the energy-band structure of P3HT/ZnO systematically basis of photovoltaic characteristics and numerical calculation. By using the artificial control of the electric polarization in the ferroelectric materials, The energy band of the p.n junction was significantly tuned, resulting in tuning the V_{OC}.

Neutralization effect of acceptor dopants on the enhanced piezoelectric potential of ZnO nanowires

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Due to their unique structural, biocompatible, and piezoelectric semiconducting properties, ZnO nanowires are considered to be one of the most promissing energy-harvesting nanomaterials for potential use in self-powered nanosystems and nanosensors [1]. The piezoelectric potential of ZnO can be enhanced by acceptor dopants to neutralize the donor concentration. In this study, unitentionally doped n-type dopant is assessed through modeling ZnO nanowires where the activation process of donors (N_d^+) is given with a Fermi level (E_F) close to the conduction band and followed by the introduction of an acceptor dopant (N_a^-) in order to allow E_F to be within the optimum range of $1 \leq E_F \leq 3.2$ eV, which corresponds to the maximum piezoelectric potential calculated. The finite element method simulation reveals that the maximal range of ZnO piezoelectric potential can be obtained due to the intrinsic characteristics of the ZnO nanowire transformed using acceptor dopants, which implies that the limitations on the free-charge carriers could reduce the screening effects on the piezoelectric potential. Furthermore, the difference [N_d^+ - N_a^-] is calculated to approach zero near the mid-gap and the energy band structure, which deviates from the normal flat line within the optimal range of $1 \leq E_F \leq 3.2$ eV under the external stress imposed.

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Transparent Flexible Graphene Triboelectric Nanogenerators

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Graphene, a two-dimensional (2D) "aromatic" monolayer of carbon atoms arranged in a hexagonal and honeycomb lattice with an sp^2 atomic configuration, has demonstrated exceptional physical properties, including ultra-high electron mobility (as high as 26 000 cm^2 V^{-1} s^{-1}), an excellent optical transparency of approximately 97%, mechanical flexibility, high mechanical elasticity (with an elastic modulus of approximately 1 TPa), high thermal stability, chemical inertness, and ballistic charge-carrier transport.[1–3] Owing to its unique and exceptional properties, graphene is considered to have high potential for technological applications in many areas. The multifunctional properties of graphene, such as its high transparency, conductivity, elasticity, and impermeability, enable it to be used in flexible electronics, transparent protective coatings, and barrier films.[4–7] These fascinating properties make graphene an ideal material for transparent, flexible electrodes in solar cells, photodetectors, nanogenerators, and light-emitting diodes (LEDs).[8–13] Although the attention focused on graphene in recent years has been accompanied by an increasing interest in 2D next-generation electronics, its application has been limited to transparent electrodes and catalysts.[13–16] To the best of our knowledge, graphene has not been used as an active material in energy-harvesting devices and systems.

Recently, a new type of power-generating device that converts mechanical energy into electricity using triboelectricity was intensively studied.[17–20] Further, nanogenerators based on the triboelectric effect have been proven to be a cost-effective, powerful, and robust tool for harvesting mechanical energy and their application as various self-powered nanosensors including for pressure, magnetic, vibration, and mercury-ion detection has been recently demonstrated.[19,21–24] The triboelectric effect depends on various factors, such as the electron affinity, work function, friction, chemical structure, pressure, surface roughness, and humidity.[25–28] A number of theoretical studies on the electrostatic behavior of graphene have been reported, and it has been concluded that graphene can store an electric charge for a period of time, which adds to its suitability for triboelectric nanogenerators (TNGs).[29–32] In addition, although graphene is assumed to be flat its natural shape exhibits many ripples because of inhomogeneous interactions with the substrate, which causes stress-induced deformations in the form of ripples along the stiff directions of the graphene lattice, enhancing its roughness and friction.[33,34] Therefore, large surface charges can be created through contact electrification/triboelectric effect for highly efficient power generation.[17,18]

In this study, we demonstrate electrical energy harvesting from graphene by mechanical stressing. We fabricated graphene-based TNGs (GTNGs) using large-scale graphene grown by chemical vapor deposition (CVD) on copper (Cu) and nickel (Ni) foils. We designed and fabricated flexible transparent GTNGs by using monolayer (1L), bilayer (2L), trilayer (3L), and quad-layer (4L) graphene using a layer-by-layer transfer technique of 1L graphene grown on Cu foils. Additionally, few-layer graphene samples with Bernal stacking (rhombohedral stacking) grown on Ni foils were also utilized to fabricate GTNGs. The dependence of the power output performance of the GTNGs on the number of graphene layers is also discussed in detail in terms of the work function and friction, which arises due to different electronic relations between randomly and regularly stacked graphene layers. This study provides a simple and cost-effective means of harvesting electrical energy from various types of mechanical energy sources in nature using GTNGs.

A polyethylene terephthalate (PET) polymer[35] was selected for the development of a transparent flexible 1L-GTNG because of its high strength, high transparency, and light weight. To achieve a high triboelectric effect, the TNGs should be fabricated using two materials that have distinctly different triboelectric characteristics; one must readily lose electrons, whereas the other must readily gain electrons.[17,27] Furthermore, to fully utilize the other well-known properties of graphene, a 1L of graphene was transferred onto the PET polymer, thus serving

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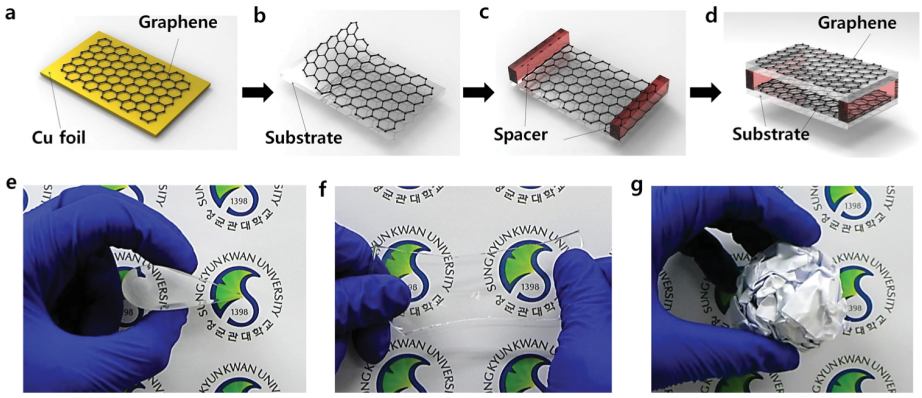

Figure 1. Schematic diagrams of device fabrication and compatibility of graphene with an arbitrary substrate. a) Cu-foil 1L graphene grown by the CVD method is used. b) The 1L graphene is transferred to the PET substrate. c) A plastic spacer is connected to create an air gap. d) The spacer-incorporated 1L graphene is integrated with the PET/graphene (top electrode) to fabricate the GTNG. e–g) The flexibility, stretchability, and adjustability of graphene with the crumpled substrate are shown.

as the top electrode for the GTNG. In the present case, graphene plays a dual role for the GTNG; it functions as the top electrode as well as the triboelectric layer at the bottom of the GTNG. Before assembling the device, the graphene samples grown on the Cu and Ni foils were characterized using Raman spectroscopy (Details of the growth procedure of graphene and the Raman spectra (Figures S1, S2) are given in the Supporting Information (Part 1 and 2)). The CVD-grown graphene samples have wrinkles and ripples, which make these graphene structures more suitable for high-output voltage applications because of the significant amounts of friction and surface charge created by the triboelectric effect.

Figure 1a-d provides a schematic illustration of the experimental procedures used to fabricate the transparent flexible 1L-GTNG. At first, large-scale 1L graphene was grown on a Cu foil using CVD (Figure 1a). Next, the 1L graphene was transferred onto a flexible PET substrate using the well-known wet transfer method (Figure 1b). The two substrates, i.e., the PET/1L graphene (bottom side) substrate and the PET/graphene (top electrode) substrate, were then connected using a plastic spacer, leaving a narrow 0.8 mm space between the 1L graphene and top PET layers (Figure 1c-d). The use of a spacer in the GTNG significantly improves the capacitance of the system in the deformation process because of the presence of air voids between the PET polymer and the graphene, which increases the strength of the dipole moments formed during mechanical deformation. A schematic of the final structure of the GTNG device is shown in Figure 1d. The entire device fabrication process is quite simple and novel, which leads to an easy understanding of the charge-generation mechanism and allows for a low-cost device fabrication process that is needed for possible future commercialization. The well-known features of graphene, such as its flexibility, stretchability, and compatibility with arbitrary substrates, are also shown in Figure 1e-g.

To investigate the performance of the GTNGs, we carried out a detailed electrical characterization of the device. This unique structure allowed for the generation of an output voltage and output current density from 1L-GTNG of 5 V and 0.5 μA cm^{-2}, respectively, when a vertical compressive force of 1 kgf (1 kgf = 9.880665 N) was applied, as shown in **Figures 2**a and 2b. The 1L-GTNG exhibited a very stable output voltage and current under a cyclic compressive force. 'Switching polarity' tests were also carried out to confirm that the measured output signals were generated from the GTNG rather than from the measuring system. As we reverse the polarity of the voltage and current meters, the output signals are reversed, as shown in Figures S3 and S4 in the Supporting Information.

To further examine the effect of the number of graphene layers on the output performance, we fabricated 2L-GTNGs, 3L-GTNGs, and 4L-GTNGs (*non*-AA/AB/ABC/AAA, stacking, i.e., random turbostratic stacking). We obtained 2L-, 3L-, and 4L-graphene samples by stacking 1L graphenes on PET substrates by using a wet transfer technique that was subsequently integrated with the PET/graphene for the fabrication of the TNG. The electrical power output signals were measured under identical compressive forces for the 2L-, 3L-, and 4L-GTNGs, and their corresponding data are shown in Figure 2a,b. The output voltage and output current were found to decrease with an increasing number of graphene layers. Average output voltage values of 3.0, 2.0, and 1.2 V and average output current density values of 250, 160, and 100 nA cm^{-2} were observed for the 2L-, 3L-, and 4L-GTNGs, respectively. These studies confirmed that 1L graphene is a good candidate for high-performance GTNGs and that randomly stacked graphene layers exhibit a decreased output performance.

Because multiple graphene layers were prepared on the PET substrate using a wet transfer method, there are weak interlayer interactions and random turbostratic stacking between the graphene layers. Thus, regularly stacked (such as AA/AB, ABC, and ABA) multilayer graphene grown on Ni foils by a CVD method was also utilized for the fabrication of GTNGs. The electrical power outputs of few-layer-based GTNGs were measured under identical mechanical stress, and the output data are shown in Figure 2c,d. Interestingly, the output voltage and output current density dramatically increased to 9 V and 1.2 μA cm^{-2}, respectively, under a vertical mechanical force of 1 kgf. The observed output voltage is nearly 1.8 times larger than that of the 1L-GTNG and nearly 7.5 times larger than the randomly

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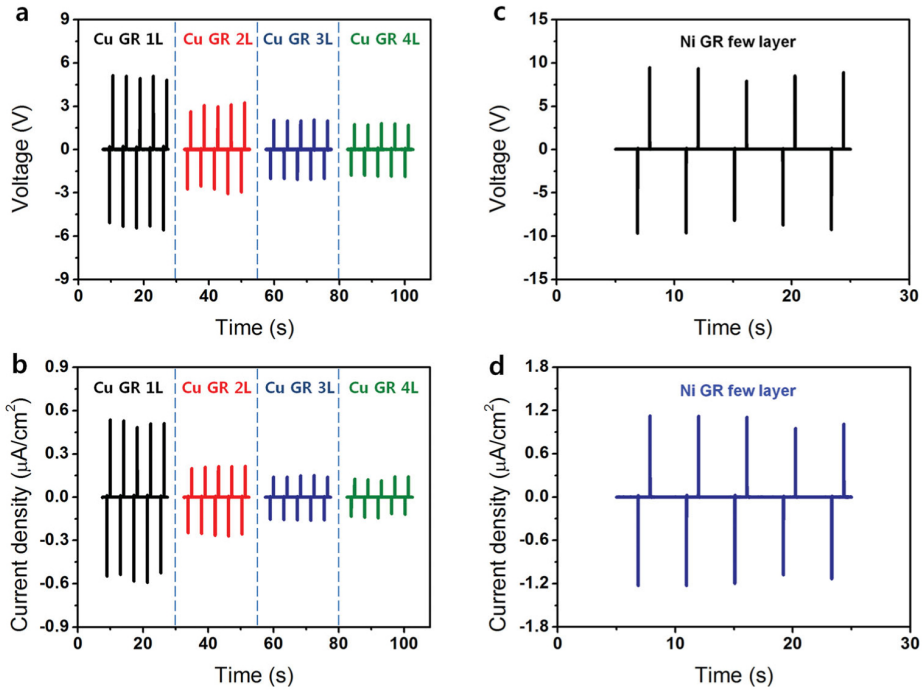

Figure 2. Output performance of 1L, randomly stacked, and regularly stacked GTNGs. a,b) Output voltage and current density from a Cu foil-grown 1L GTNG and randomly stacked 2L-, 3L-, and 4L-GTNGs under a vertical compressive force of 1 kgf. c,d) Output voltage and current density from regularly stacked, few-layer GTNGs under a vertical compressive force of 1 kgf.

stacked 4L-GTNG. A similar trend was also observed in the output current, which was nearly twelve times larger than that of the 4L-GTNG (Figure 2b,d). Further, to investigate the effective electric power of GTNG, the output performance of the 1L-GTNG was systematically studied at different loads. As shown in Figure S5a in the Supporting Information the maximum current decreases with increasing resistance, whereas the output voltage shows the opposite trend. The power density of 1L-GTNG was also plotted as a function of external resistance and is shown in Figure S5b (Supporting Information). The output power density increases at a low resistance region and then decreases at a higher resistance region. The maximum value of the power density of around 2.5 μW cm^{-2} occurs at about 10 MΩ. In addition, a durability test (over ~1000 cycles) was also conducted to confirm the mechanical durability of the GTNG (Figure S6, Supporting Information).

The operating principle of the GTNG can be described using the coupling of contact charging and the electrostatic effect under a cycled compressive force. A COMSOL simulation was also carried out to understand the working process of the GTNG (Supporting Information, Part 3). The corresponding surface-charge distribution and electric potential are shown in **Figure 3**. According to the work function values of the PET (Figure S7, Supporting Information) and graphene, electrons are injected from the PET to the graphene, resulting in the build-up of a net negative charge on the graphene surface and a net positive charge on the PET surface. Furthermore, because of the spacer placed between the graphene and the PET surface, air voids are created, which result in the formation of dipole moments. Therefore, an electric potential difference is developed between the two electrodes, that is, between the bottom graphene (the active triboelectric material as well as the electrode) and the top graphene (electrode), which results in an electric signal generated across the electrode.

Figure 3 demonstrates the working mechanism of the GTNGs at each stage of the cyclic deformation. Initially, the device is neutral in the absence of any pressure/force, and no charge is generated on the surface of the PET and graphene; therefore, no electric potential difference is established between the two electrodes (Figure 3a), and no output signal is observed. On the contrary, when a vertical compressive force is applied to the top surface of the device, the PET and 1L graphene layer are rubbed together. Thus, triboelectric charges with opposite signs are generated because of electron injection in the graphene by induced thermal energy during the contact between the PET and graphene. These charges are distributed on the contact surfaces of PET and graphene. As we discussed in the above section, because of the differences in the work function of the PET and graphene, the electrons are injected from PET to graphene, resulting in the generation of negative charges on the graphene surface and positive charges on the PET surface. At this stage, the generated surface charges with opposite signs nearly coincide on the same plane, generating an insignificant electrostatic potential difference between PET and graphene (Figure 3b). Therefore, no electrical signal was detected at this stage.

When the pressure is released again, the PET film reverts back to its original position because of its own elasticity and flexibility. Once the PET and graphene surfaces are separated from each other, the dipole moment becomes stronger, and a very strong electric potential difference is created between the

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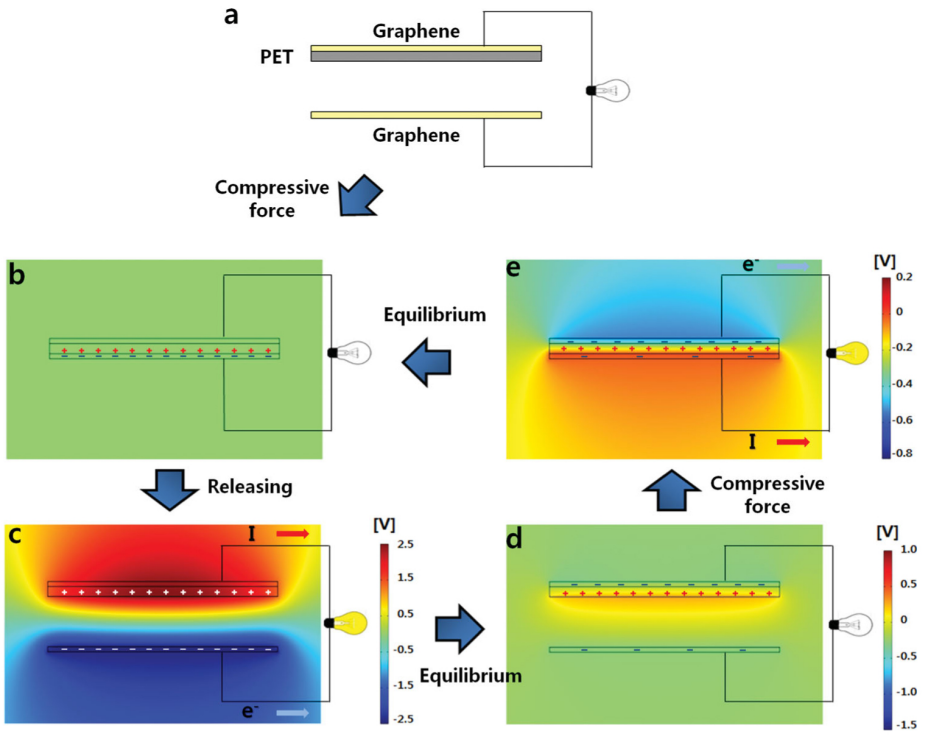

Figure 3. Power generation mechanism of GTNGs. a) Schematic diagram for the initial state of the GTNG; the device was neutral when no force was applied. b–e) Potential distribution of the GTNG simulated by the COMSOL multi-physics software.

two graphene electrodes. Therefore, to achieve equilibrium, electrons start to flow from the negative potential side (bottom graphene) to the positive potential side (top graphene), leading to an accumulation of electrostatically induced charges on the electrodes, resulting in a positive electrical signal (Figure 3c). No electrical signal is observed at equilibrium (Figure 3d). Furthermore, when an instantaneous vertical compression is applied to the GTNG, the PET and graphene come into contact and short each other out. The dipole moment subsequently disappears or decreases in magnitude, and the electrostatic potential difference starts to diminish. Therefore, the reduced electric potential difference generates a flow of electrons from the top electrode side to the bottom electrode side that causes the accumulated charges to vanish, resulting in a negative electrical potential across the electrodes (Figure 3e). This negative electrical potential causes electrons to be pumped back and forth between the two electrodes because of contact charging. Therefore, the continuous application and removal of a vertical compression on the GTNG drives a flow of electrons between the top and bottom electrodes across the external load via the triboelectric charge, which provides an alternating current signal from the GTNG. To further confirm our mechanism, we fabricated a 1L-GTNG without a spacer and measured the electrical output signal (Figure S8, Supporting Information). No significant output voltage was produced using any vertical mechanical strain. These results demonstrate that our model is fairly valid in explaining the working principle behind the GNTGs. The COMSOL simulation results also confirm the proposed mechanism.

The above study revealed that 1L graphene and regularly stacked few-layer graphene are the best candidates for high-performance GTNGs. We observed that the output performance decreases with an increasing number of randomly stacked graphene layers, and the performance increases when regularly stacked few-layer graphene is used. Such enhancements in the output voltage and current observed in regularly stacked few-layer graphene-based TNG over 1L- and randomly stacked 2L-, 3L-, and 4L-based GTNGs are attributed to the increased work function of few-layer graphene with Bernal stacking and a strong electronic relation between regularly stacked graphene layers. Raman spectra of the graphenes grown on the Cu and Ni foils were taken to examine their stacking order (Figures S1 and S2, Supporting Information).

Many researchers have proposed that the work function of graphene varies with the number of graphene layers following an increasing trend with the number of regularly stacked graphene layers (i.e., graphene work function = 4.3, 4.4, 4.5, and 4.6 eV for n = 1, 2, 3, and ∞, respectively, where n is the number of graphene layers).[29,30,36] Therefore, the difference in work-function values can significantly change the surface-charge density on few-layer graphene due to the triboelectric effect when rubbed with PET, which further increases the output voltage and current in few-layer-based GTNGs relative to 1L graphene. Mathematically, the contact potential difference (V) is given as

$$V \sim -(\varphi_p - \varphi_g)/e, \quad (1)$$

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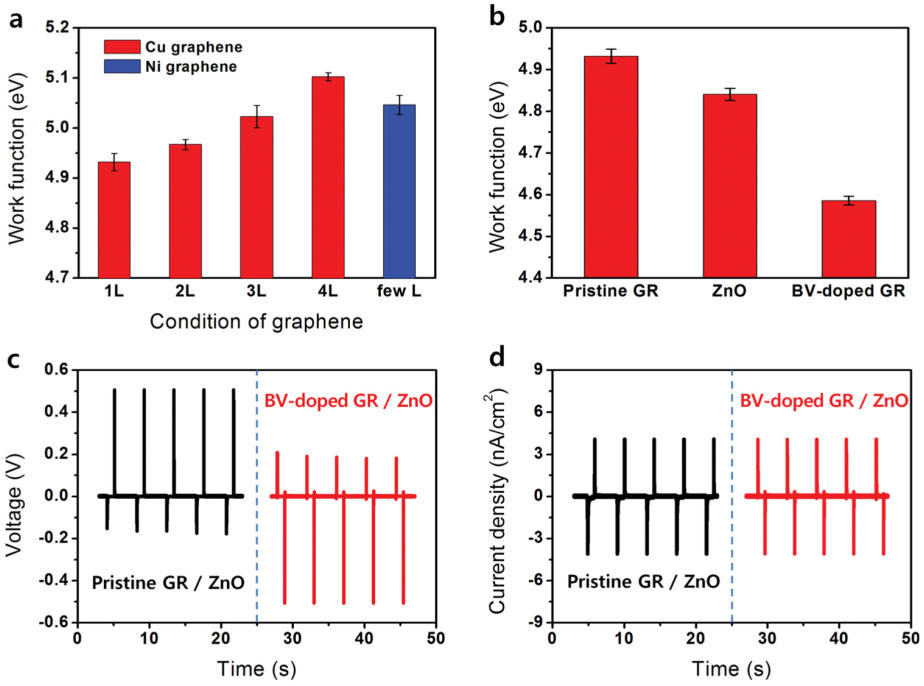

Figure 4. Work-function measurement and electric outputs. a) Measured work function of 1L graphene and randomly and regularly stacked 2L, 3L, and 4L graphene. b) Work function of pristine and BV-doped graphene, and ZnO thin film. c,d) Output voltage and current density measured from the 1L pristine graphene-ZnO TNG and the BV-doped graphene-ZnO TNG under a vertical compressive force of 1 kgf.

where φ_p is the effective work function of the PET polymer, φ_g is the work function of the graphene, and e is the elementary charge.[26,27,31] Therefore, an increasing work-function difference leads to an enhanced GTNG output power.

To calculate the precise value of the work function for 1L-, 2L-, 3L-, 4L graphene (Cu foil-grown), and few-layer graphene (Ni foil-grown), a Kelvin probe force microscopy (KPFM) technique was used, as shown in Figure S7 in the Supporting Information. The output results are shown in **Figure 4**a; the work functions of graphene were determined to be 4.92, 4.96, 5.04, 5.11, and 5.08 eV for the Cu foil-grown 1L, 2L, 3L, 4L graphene samples and the Ni foil-grown, few-layer graphene samples, respectively. These results coincide with previous reports.[36,37] The above results confirm that the work function plays an important role in the output performance of GTNGs. However, the observed discrepancy in the variation of the output voltage/current density between 1L-GTNGs and randomly oriented 2L-, 3L-, and 4L-GTNGs is discussed below.

The linear reduction of the output power from randomly stacked graphene-based TNGs caused by increasing the number of graphene layers can be explained by the friction depending on the number of graphene layers used, which arises because of the puckering effect and electron–phonon coupling effect.[38,39] The surface charge and output potential is strongly related to the friction generated between rubbed materials (i.e., graphene and PET in the present case). When 1L graphene grown on a Cu foil using CVD is transferred onto a certain template, it preserves its corrugated surface leading to the appearance/enhancement of friction when rubbed against other materials. Furthermore, the friction in graphene is decreased with an increasing number of graphene layers (i.e., the 1L graphene reveals an approximately 20% higher amount of friction than 2L graphene due to the puckering effect in graphene).[40] The puckering is less prominent with an increasing number of graphene layers because of the larger bending stiffness of the graphene sheet, and therefore, the friction decreases for the 2L, 3L, and 4L graphene compared to 1L graphene.[38–40]

Further, such variations in the amount of friction between 1L graphene and 2L, 3L, and 4L graphene can also be attributed to the strong electron–phonon coupling in the single-layer epitaxial graphene and to the susceptibility of the graphene to out-of-plane elastic deformation.[38–43] Therefore, the amount of friction in 1L graphene is larger than that in 2L, 3L, and 4L graphene, which results in a larger electrical power output from 1L-GTNGs. This variation in the amount of friction in the graphene is also observed in regularly stacked graphene layers[44] but to a lesser extent. Therefore, the large output voltage and output current density from the regularly stacked Ni-catalyzed, few-layer GTNG are mainly related to its large work function.

Regardless, we still carefully investigated the output variation of the randomly stacked 4L-GTNG to visualize the surface features of the PET to understand their effect on the output performance. We assumed that in the case of randomly stacked GTNG, a portion of the graphene is attached to the opposite PET surface because of the weak adhesion/interaction between randomly stacked graphene layers, which results in a low output voltage/current density. Therefore, to observe the surface morphology/features of the rubbed PET for the 4L-GTNG, we obtained optical images and Raman spectra of the PET polymer before and after the application

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of the mechanical stress on the randomly stacked 4L-GTNGs (Figure S9a,b, Supporting Information). Raman peaks corresponding to graphene are also observed along with Raman peaks corresponding to the PET in the case of the randomly stacked 4L-graphene. Moreover, we have also taken friction force microscope (FFM) images of pristine and rubbed PET (Figure S9c,d, Supporting Information). The analysis revealed that because of weak interlayer interactions between the randomly stacked graphene layers, the mechanically transferred graphene is easily attached to the opposite PET surface, which results in a significantly decreased output potential because of the reduced work-function difference between the rubbed PET and the 4L graphene.

In addition, two controlled experiments were also carried out to further confirm the effect of the work function of the two rubbed materials on the polarity of the induced charge and total triboelectric output voltage/current. We fabricated two additional TNGs based on pristine and 1,1′-dibenzyl-4,4′-bipyridinium dichloride doped (BV-doped) 1L graphenes, and we utilized a ZnO thin film instead of PET because of the high work function of ZnO relative to PET. The work function of pristine graphene decreases significantly after doping it with BV.[45] Hall measurement data for pristine and BV-doped 1L graphenes are given in Table S1 in the Supporting Information. The work function values of pristine graphene (4.92 eV), BV-doped graphene (4.59 eV), and the ZnO thin film (4.85 eV) were also measured by using KPFM measurements, as shown in Figure 4b. The output voltage and output current density from pristine graphene/BV-doped graphene-ZnO-based TNGs are significantly lower than those of the graphene-PET-based TNG when identical vertical compressive forces are applied (Figure 4c,d). The signal polarity is reversed for the BV-doped graphene-ZnO-based TNG relative to the pristine graphene-ZnO-based TNG because of the lower work function of BV-doped graphene relative to the ZnO thin film. These results further prove the importance of the work function of graphene for high-performance GTNGs. Again, 'switching polarity' tests were also conducted to confirm that the measured output signals were generated from the graphene-ZnO-based TNG rather than from the measuring system. The output signals were reversed when we reversed the polarity of the voltage and current meters. This result, along with the device structure, is shown in Figure S10 in the Supporting Information.

To study a practical application of the GTNG, we drove small electronic devices, such as a liquid crystal display (LCD), LED, and electroluminescence (EL) display unit, using solely the output power from a flexible, few-layer graphene-based TNG. Initially, an LCD screen with the Sungkyunkwan University logo was used for the test, and it was directly connected to the output of the GTNGs without any capacitor. A rectification circuit was used to convert the AC signal into a DC signal to power the LCD. **Figure 5** presents the images of the photos taken before and after the GTNGs were activated (Figure 5a). The LCD screen was activated when the output power generated by the GTNG exceeded the threshold voltage of the LCD screen. The LCD screen turned on when the GTNG was stressed vertically. We also manage to power white, blue, and green LEDs by the GTNG equipped with a rectification

Figure 5. Driving a commercial LCD, LED, and EL displays using the GTNG. The left panel presents the OFF state, and the right panel presents the ON state of the LCD, LED, and EL display units. a) A snapshot of the LCD, which was lit up and displaying "Sungkyunkwan University" and the university's logo using the GTNG under a periodic vertical compressive force. b) A captured image showing the three LED arrays simultaneously lit up by the power output generated from the GTNG. c) Commercial EL display unit containing "Sungkyunkwan University" and the university's logo was activated using the GTNG under a periodic vertical force.

circuit and capacitor (2.2 μF). Commercial LEDs with white, blue, and green emissions were used, as shown in Figure 5b. When a periodic mechanical force was applied vertically to the GTNG, the total rectified output power generated from the GTNG was sufficient to simultaneously activate all three LEDs. These results were recorded, and their corresponding videos are shown in the Supporting Videos 1 and 2 in the Supporting Information. Moreover, we directly operated an EL display unit using the power generated by the GTNG using a rectification circuit, capacitor (22 μF), and inverter. Figure 5c illustrates that the EL display activates when a vertical compressive stress is applied to the GTNG. This is the first demonstration of a novel energy-harvesting application of graphene using the triboelectric effect (See Supporting Video 3, Supporting Information). The schematic circuit diagrams used for operating the LCD, LED, and EL displays are shown in the Supporting Information (Figure S11).

In conclusion, we have successfully demonstrated the application of CVD-grown graphene as a transparent, flexible TNG. GTNGs based on 1L, 2L, 3L, 4L, and few-layer graphene grown on Cu and Ni foils using CVD have been fabricated, and their output voltage and output current density were measured under mechanical strains. The 1L-GTNG exhibited a high

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output voltage and output current density of 5 V and 500 nA cm^{-2}, respectively. Additionally, the output voltage and output current density increased to 9 V and 1.2 μA cm^{-2}, respectively, for the regularly stacked few-layer GTNG. The variations in the electrical power output of randomly stacked 1L-, 2L-, 3L-, and 4L-GTNGs and regularly stacked few-layer GTNGs were explained in terms of their work function and friction. We were able to power an LCD, LEDs, and an EL display using the electrical power output of the GTNG without any other external energy source. This study provides a simple and novel method for harvesting mechanical energy using transparent and flexible GTNGs for powering low-power portable devices and self-powered electronic systems.

Experimental Section

Fabrication of GTNGs based on 1L graphene, randomly and regularly stacked graphene: For the device fabrication, 1L graphene was coated with poly(methyl methacrylate) (PMMA) and immersed in an etchant (Transene, type 1) to etch away the Cu foil. When the Cu was completely etched away, the 1L graphene with PMMA was rinsed in deionized water three times to wash away the etchant residues. The large-scale monolayer graphene grown on the Cu film by the thermal CVD method was transferred onto the hard-coated PET (Higashiyama Film Co., Ltd) substrate using the well-known wet transfer method. Furthermore, to fabricate randomly stacked double, triple, and quadruple layers of graphene, one, two and three monolayers of graphene, each synthesized in an identical manner, were placed onto the 1L graphene/PET substrate by the wet transfer method, respectively. Next, the other PET/graphene (electrode) substrate was connected by a thin plastic spacer to the PET/graphene (active triboelectric material), leaving a narrow spacing between the graphene surface and the top PET surface. The spacer was made of an insulating polymer film with double-sided adhesive with a thickness of 0.8 mm and the area of each spacer was 2 mm × 2 cm. Graphene plays a dual role in the device: it works as the top electrode and as the triboelectric material on the bottom and top sides of the device. Regularly stacked GTNG fabrication was conducted in an identical fashion.

Characterization and Measurements: Raman spectra and optical images of the Cu-grown 1L graphene and Ni foil-grown, few-layer graphene were examined using Raman spectroscopy (Renishaw, RM-1000 Invia, 514 nm, Ar+ ion laser). The friction force image between the PET and graphene layers were measured using the friction force microscopy mode (Park system, XE-100). The KPFMs were performed to precisely determine the work function of the 1L and randomly and regularly stacked few-layer graphene (Park system, XE-100). A picoammeter (Keithley 6485) and oscilloscope (Tektronix DPO 3052) were used to measure the low-noise output currents and voltages generated by the device using a force stimulator (Z–TEC ZPS 100).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Air 및 Argon 분위기에 따른 2차원 물질 *n*-type 도핑

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본 연구에서는 가장 높은 환원전위를 가지는 Benzyl Viologen (BV) 을 이용하여 molybdenum disulfide (MoS2) 표면에 air와 argon (Ar) ambient (glove box 안에서 실험 진행)에 따른 두 환경에서 도핑 후 전류 밀도 차이 및 시간에 따른 전류 밀도 변화에 대해 연구하였다. 최근까지의 연구 결과에 따르면, 2차원 물질의 도핑분석 결과들은 많지만, 현재 논문에서는 대기 중에서 BV용액을 만들어 도핑을 하는 것 보다 glove box에서 Ar 분위기로 BV용액을 만들어 도핑하는 논문이 없고, 본 실험 결과에 따르면 Ar분위기에서 도핑을 할 경우 전류 특성이 향상되기 때문에 응용분야에 더욱 더 도움이 될 것으로 예상된다. MoS2는 mechanical exfoliation을 이용하여 285 nm silicon oxide wafer위에 얹혀졌고 전자빔 리소그래피를 사용하여 소자 제작이 이루어졌다. Glove box를 이용하여 도핑 할 경우, air 환경에서 만든 것에 비해 Id-Vd 그래프는 약 4.5배, Id-Vg 그래프는 4배 Current 차이가 있는 결과를 얻었다. 두 환경에서 만든 같은 농도의 BV 색을 보면 확연히 다른데, 이는 분자구조 변화 또는 산화에 의한 영향이라고 생각한다. 이와 관련하여 더욱 정확한 데이터를 위하여 nuclear magnetic resonance(NMR)를 통해 분석하였다. 그리고 시간에 따른 전류 밀도 변화는 1일, 2일 단위로 측정 결과 Glove Box에서 만든 BV도핑은 1일 후 Current가 약 1.6배 떨어지고 2일 후는 약 1.1배 떨어진 것을 확인하였다. 결론적으로 Argon 분위기에서 만든 BV용액 도핑과 Air 분위기에서 만든 BV용액 도핑 결과 2일이 지나도 Current가 2.8배 차이를 확인하였다. N-type doping 용액인 BV를 MoS2에 도핑시킨 후 2일이 지나면 MoS2 BV 코팅 박막이 안정하다는 결과를 알 수 있었다. 그리고 측정과정 중에 BV가 산화되어 Current가 떨어졌다고 예상함으로, 산화되는 것을 방지하여 소자를 만들면 응용분야에 더욱 더 도움이 될 것으로 예상된다.

Vertical stacking methods for two-dimensional heterostructures

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Two-dimensional (2D) materials, including graphene, hexagonal boron nitride (hBN), and transition metal dichalcogenides (TMDCs), have been extensively studied for years. Recently, heterostructures of 2D materials, which are held with van der Waals forces, are rising as a promising candidate for advanced electronics[1]. For fabrication of the heterostructure, diverse stacking techniques have been developed. However, when sacrificing polymer films are used, it is known that contamination of heterointerfaces from trapped bubble and polymer residue deteriorates the performance of 2D heterostructure devices[2]. Here we report various vertical stacking methods for ultraclean 2D heterointerfaces. We combine polymer films and soft stamp so that we can utilize electrostatic force, absence of adhesive, and softness of these transfer substrates. The multi-stacked heterostructures through our proposed methods show the ultraclean and ultrasharp heterointerfaces, which can be suitable for high performance electronics[3]. Our stacking methods pave a new way toward fabrication of artificial van der Waals heterostructures of various 2D materials, allowing for fabrication of advanced electronic devices consisting entirely of 2D materials along with flexible and transparent form.

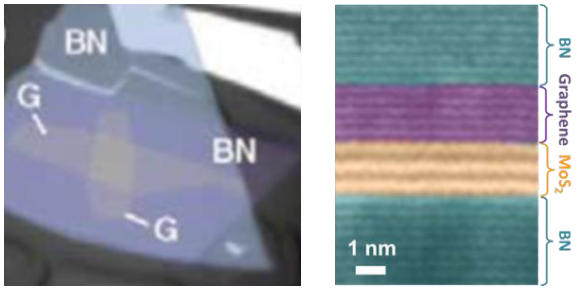

Figure 1. Optical image of vertically stacked 2D materials and cross-section TEM image of multi-stacked heterostructure

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Top gate graphene FET 의 Fermi level 과 계면결함 밀도의 상관관계 연구

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Graphene top gate FET 의 전자소자로 활용하기 위해서는 소자 안정성문제를 해결해야만 한다. 소자의 불안정성을 유발하는 요인인 그래핀과 유전체층 사이의 계면 또는 유전체층 내의 계면결함을 제어하는 것이 소자안정화에 결정적으로 중요한 요소로 알려져 있다. 이 때문에 열처리, 클리닝, passivation 등 다양한 공정을 최적화하여 소자 특성을 개선하려는 연구가 진행되고 있으며, 대부분의 경우, 전기적 측정, 예를 들어 I_d-V_g 를 통한 hysteresis, mobility 등을 통해서 상대적으로 특성을 분석하거나, Pulse I-V method 를 통하여 결함의 종류를 상대적인 비율을 이용하여 분석하는 방법으로 공정의 효과를 검증하고 있다. 하지만, 위와 같은 분석법들은 결함의 특정한 에너지 레벨과 같은 물리적인 분석보다는 총체적인 정량분석 결과만을 제시하기 때문에 문제의 원인 자체를 규명하는 데에는 한계가 있다. 최근에 개발된 discharge current analysis(DCA) method 는 정량적으로 소자 내의 결함을 분석할 수 있다고 보고하였다. [1]

본 연구에서는 DCA 측정법을 개선하여, 그래핀의 Fermi energy level 과 소자안정성의 척도가 되는 계면 전하 밀도 (interface charge trap density, D_{ct})의 상관관계를 분석하는 방법을 제시하고자 한다. D_{ct} 를 추출하기 위하여, DCA 측정과 capacitance measurement(C-V) 방법을 결합하여, graphene 의 Fermi level 을 추출했으며, D_{ct} 값이 Fermi level 이 -0.4~0.4eV 로 변할 때 10^{12}~10^{13} (#/cm^2· eV^{-1}) 사이에서 변화된다는 것을 알게 되었다. 이 결과는 그래핀 소자의 계면결함밀도가 Fermi level 과 어떤 관계를 가지는 지에 대한 최초의 실험적 분석이라는 데, 의의가 있다. [1] U. Jung et al., Sci. Rep., vol. 4, 4886 (2014)

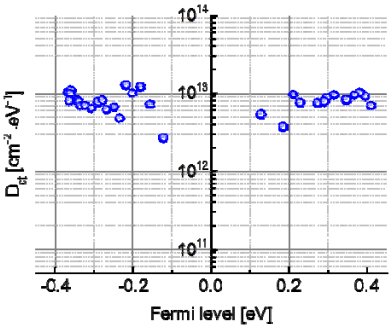

Figure 1 Representative interface charge trap density of top gate graphene FETs

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Influence of Surfactant-treated PEDOT:PSS on Graphene Electrode

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Graphene has been considered as highly suitable for the the transparent conductive electrode material in organic photovoltaic (OPVs) due to its novel and remarkable properties. The potential applications of graphene in OPVs are restricted because of the surface wettability. Especially, the hole transportation layer, aqueous solution poly(3,4-ethylenedi-oxythiophene):poly(styrene sulfonate) (PEDOT:PSS), is hard to be uniformly coated on the graphene[1]. In this study, we demonstrate high performance OPV by employing nonionic surfactant modified PEDOT:PSS as hole transport layer[2]. The surfactant can improve the wettability of the PEDOT:PSS on graphene by forming nanofibril structure of hydrophobic and conductive PEDOT. Moreover graphene can be effectively doped, decreasing 39% of sheet resistance and endured more during the stretching compared to the pristine graphene which supports this method as appropriate candidate for the flexible OPV. These kinds of influence of PEDOT:PSS on graphene are directly related to the improvement in the OPV performance with power conversion efficiency of 3.19% under AM1.5.

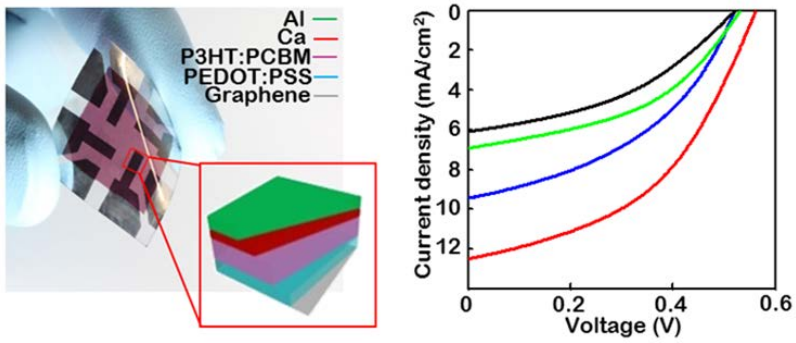

Fig 1. The flexible OPV image and output characteristic curves of pristine graphene and PEDOT:PSS (black), UV treated graphene (green), HNO_3 doping and UV treated graphene (blue), and Triton X-100 treated PEDOT:PSS (red).

[1] Hobeom Kim, Sang-Hoon Bae et al., Nanotechnology 15, 014012 (2014)
[2] Woon-Hyuk Baek, Mijung Choi, Tae-Sik Yoon et al., Appl. Phys. Letts. 96, 133506 (2010)

High-Speed Baseband Modem for 60 GHz Proximity Wireless Communications

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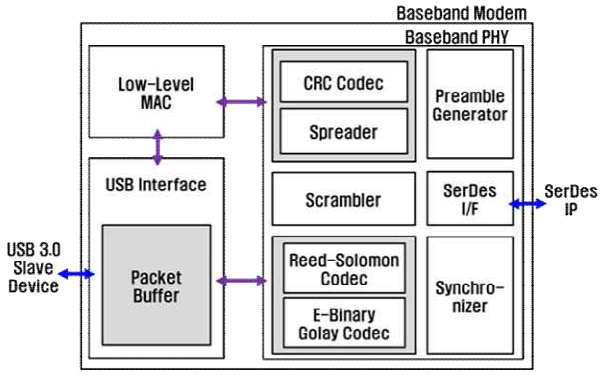
Recently, wireless technologies for near field communications, such as NFC [1] and TransferJet [2], are used to support the pre-paring process of high-speed wireless communications and low-speed data transmission. We present a simple and portable digital baseband modem that is developed for high-speed proximity data communications using 60 GHz RF band. As depicted in Fig. 1, the baseband modem consists of three major function units: a low-level MAC, a baseband PHY, and an USB interface. The baseband modem is suitable for point-to-point data transfer between two powered devices and performs hardware efficient tasks for the low-level MAC and baseband PHY, such as link management, bit-intensive and time-critical parts. Each unit implemented in the baseband is considered in terms of small size and fast data processing. The primary clock input of the baseband modem is 100MHz. The bus width of the internal data path is 32 bits. The maximum PHY rate for RF supports up to 3.2 Gbps. The proposed baseband modem is mapped in an FPGA and are verified for the point-to-point communication protocol between two FPGA test boards. Furthermore, the baseband modem ASIC is implemented in a 65nm CMOS technology that has 1,504,375 logic gates and occupies olny 2,500 × 1,500 um^2 area.



ASIC Characteristics

Item	Description
Technology	65nm 1P-9M
Total Gate Count	1,504,375 gates
Total Area	2,500 x 1,500 um^2
Core/IO Voltage	1.0V / 2.5V
Operation Clock	100 MHz

Fig. 1. Baseband modem overall architecture and ASIC characteristics

[1] NFC Forum, NFC Digital Protocol Technical Specification, Digital 1.0, November (2010).
[2] ECMA, Standard ECMA-398 Close Proximity Electric Induction Wireless Communications, June (2011).

This work was supported by the ICT R&D program of MSIP/IITP. [14-000-04-001, Development of 5G Mobile Communication Technologies for Hyper-connected Smart Services]

Hardware Implementation of a Real-time Central Point Detection for Motion Recognition System

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With the recent development of sensors that can measure and visualize depth, gesture research involving the analysis of human movements using 3D distance information is being vigorously carried out. an algorithm to track regions of interest such as mean shift or cam-shift is used in order to extract each joint [1]. On the software front, this algorithm offers such advantages as fast computing speed. but, a pre-processing algorithm block is needed to set the size and the location of the initial window. Also, if a size of search window is increased, the number of accesses to the frame memory increases, and more clocks are required for computation. A central point detector that works in real-time without requiring an additional pre-processing block was implemented. For real-time updating of the hardware design, we have divided label tables into read-only memory and write-only memory. Also, a large amount of memory was used to comprise a multi-tier structure suitable for the real-time hardware system. While the proposed algorithm is on average faster than the cam-shift, it can still find the center point with a single scan, and its wider scanning region allows accurate identification of the center point. As object complexity grows, that difference in performance increases. The proposed algorithm was developed in the Windows Program using the OpenCV and implemented by Verilog-HDL. Also, we verified the proposed system using a FPGA board.

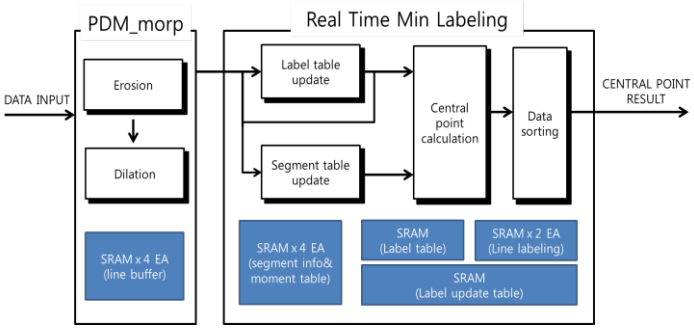

Fig 1. Block diagram of the proposed algorithm

[1] H. Chu, S. Ye, Q. Guo, and X. Liu, "Object Tracking Algorithm Based on Camshift Algorithm Combinating with Difference in Frame," *Proceeding of the IEEE International Conference on Automation and Logistics*, Jinan, China, pp. 51-55, AuG. 2007.

A Noise-Resilient and Ditherless Lock Detection Scheme for Bang-Bang Controlled Calibration Loops

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In modern mixed-signal systems, bang-bang-controlled loops are widely used for calibrating the properties of analog circuits such as clock timing errors, voltage/current offsets, filter coefficients, and even circuit nonlinearities. While bang-bang control is the simplest method to employ digital calibration algorithms without requiring linear analog-to-digital converters, one of its drawbacks is that the resulting output cannot settle to a steady point; it constantly dithers near the locking point, incurring additional noise which may degrade the system performance. While one way to avoid such dithering is to disable the bang-bang control once the loop reaches a lock [1], determining the correct lock point especially in presence of noise is difficult. This paper presents a novel lock detection scheme for bang-bang-controlled calibration loops which is both noise-resilient and ditherless. The proposed scheme determines the best locking point on the quantized grid as the one that yields the minimum distance to the ideal locking point in a statistical sense. In other words, the scheme observes a sufficiently large number N of the bang-bang detector outputs and selects the interval that encloses the ideal locking point with the highest probability. It will be demonstrated that by doing so, the loop can always find the correct locking point even in presence of noise and hence the loop can safely disable the bang-bang control to avoid dithering and residual error. The paper provides analysis on how to select large enough N as a function of the noise present in the system.

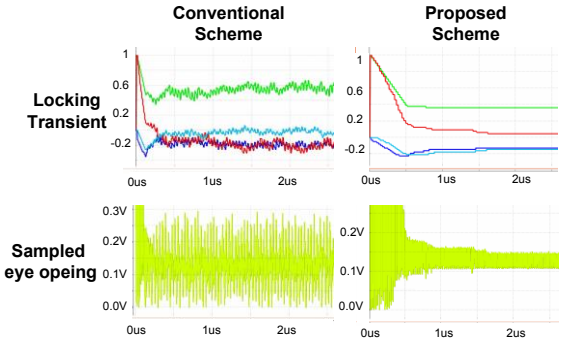

Fig 1. The bang-bang adaptation trajectories of FIR equalizer coefficients with and without the proposed lock detection scheme.

[1] M.-J. Park, et al., "A 5-Gbps, 1.7-pJ/bit Ditherless CDR with Optimal Phase Interval Detection," *in Proc. IEEE Custom Integrated Circuits Conf.*, pp. 1–4, Sep. 2012.

Adaptive Voltage Scaling in the Near-Threshold Voltage Regime Using Current Sensing Completion Detection

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In recent technology nodes, supply voltage scaling in the super-threshold voltage regime has been stalled, which incited engineers to design circuits operating in the near-threshold voltage regime to further improve power performance. But the power reduction accompanies lower clock frequencies as well as exponentially increased dependency on variations (process, voltage, temperature, aging etc.). Previous approaches to cover those variations may no longer work. *Razor* style techniques [1], for example, may not catch timing errors if the timing variations are large. *Critical path replica* style techniques [2] may not handle intra-die variations properly and a timing margin still need to be used. We propose a method based on a current sensing completion detector (CSCD) [3]. If the computation doesn't end within a clock cycle, we slightly increase the supply voltage to speed up the circuit. This is repeated until no error occurs. It allows us to avoid to add timing margins and detects errors regardless of the amount of delay variations. If the critical path is known, we can pre-adjust the voltage by using the test vectors that sensitize the path. If it isn't, the method is used to gradually reduce the error rate (most DSP applications allow rare errors). Experiments on a 32-bit adder show that we reduced power by 52% on average compared to a single voltage technique.

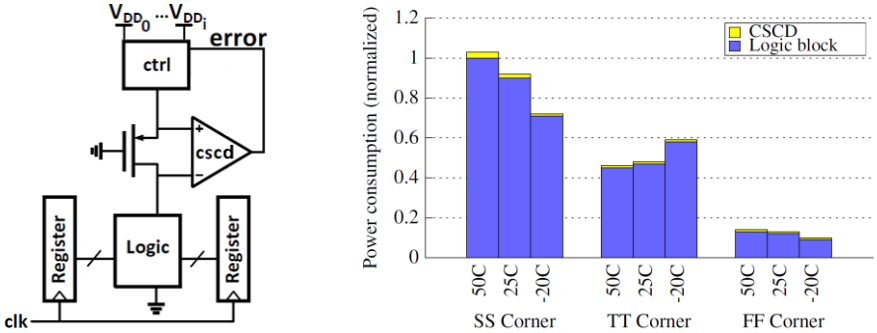

Fig 1. Architecture of our approach and normalized power reduction.

[1] D. Ernst, et al. "Razor: A low-power pipeline based on circuit-level timing speculation." Proceedings. 36th Annual IEEE/ACM International Symposium on. IEEE, 2003.
[2] S. Dhar, et al. "Closed-loop adaptive voltage scaling controller for standard-cell ASICs." *Proceedings of the 2002 international symposium on Low power electronics and design*. ACM, 2012
[3] J. Crop, et al. "Regaining throughput using completion detection for error-resilient, near-threshold logic." *Design Automation Conference* (DAC), 2012. IEEE, 2012.

Sensorless BLDC motor drive in methods of Sliding Mode Observer with Resistance Estimation in FPGA

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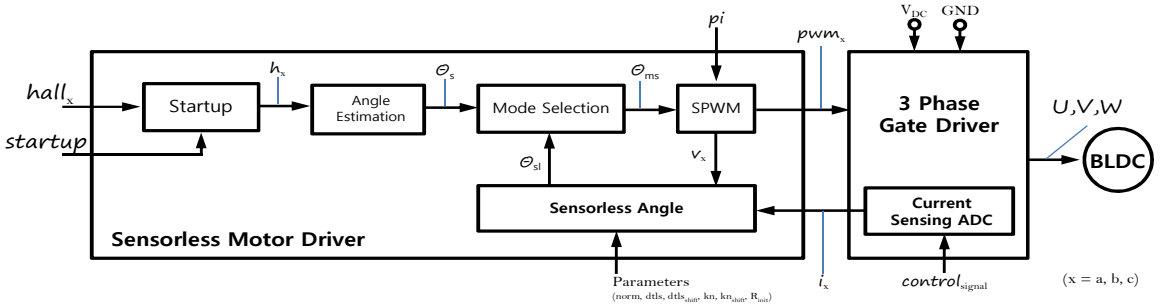
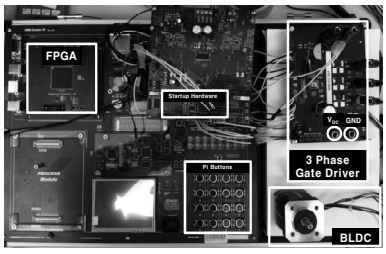
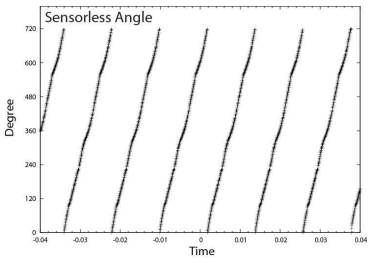
A request of sensorless control in motor drive fields such as home appliance and industry is continuing increasingly due to strengths of decreasing detection areas of motor position. Several sensorless control methods are introduced in [1,2] and the sliding mode observer method with resistance estimation scheme is utilized in 24W BLDC system in this paper. This paper shows the abilities that a stable driving in BLDC motor system could be realized and our sensorless method can drive the BLDC motor in a wide range of speed from 1286rpm to 3705rpm.



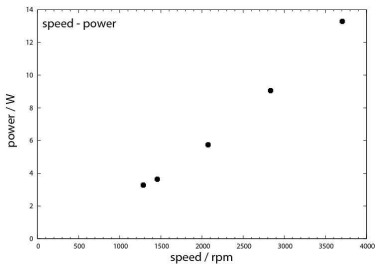
(a) Block diagram of Sensorless BLDC motor



(b) Experimental setup



(c) Sensorless angle



(d) Speed-power relations

Fig 1. Sensorless BLDC motor block diagram, experimental setup and its electrical data

[1] H. Kim, *et al.*, Trans. KIEE. Vol. 59, No. 1 (2010).
[2] K. Kan, *et al.*, IEEE 7th PEMC– ECCE Asis (2012).

High Performance memory controller processing multiple requests

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Frequent access to shared memory by multiple masters usually limits the performance of a system. In this paper, we propose a high performance memory controller architecture using an algorithm of arbitration and shuffling of requests which enables high bandwidth, low latency and low power consumption in systems with SoC network protocols that support outstanding address and out-of-order completion transactions. The memory access commands are stored in a queue, analyzed and shuffled in order to minimize activating new rows and to reduce the power consumption in the proposed architecture. It also adjusts the priority of processing commands if the network protocol supports QoS. We design a LPDDR2 SDRAM controller based on the proposed algorithm using Verilog-HDL. The memory controller consists of a request organizer, bank controllers and a command generator. The request organizer shuffles requests according to the propaosed algorithm and stores them. The bank controller stores requests for the corresponding bank and requests command generation. The command generator generates commands for memories according to the results of the request organizer and makes minor reordering of requests to improve the performance. The performance of the memory controller is compared with that of a previous work[1] and a normal memory controller, and it is improved by 10 – 47%.

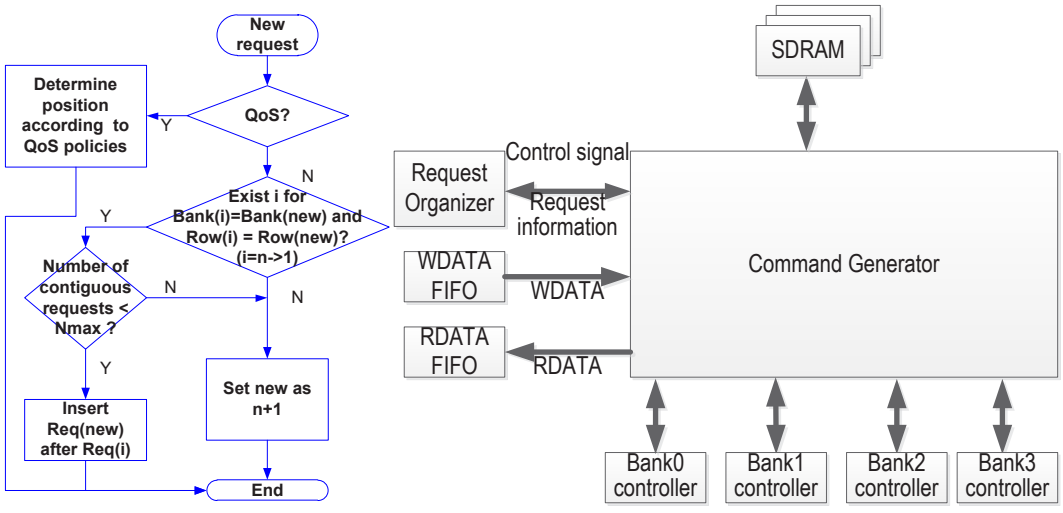

Fig 1. Arbitration and shuffling algorithm and memory controller architecture

[1] Behzad Boroujerdian, Ben Keller, Yunsup Lee "LPDDR2 memory controller design in a 28nm process", unpublished, UC Berkeley EECS, Dec, 2012

This work was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(2010-0021225) and sponsored by the Industrial Core Technology Development Program(10049192, Development of a smart automotive ADAS SW-Soc for a self-driving car) funded By the Ministry of Trade, industry & Energy. The EDA tools were supported by IDEC.

The fabrication of nanocrystal based metamaterial by nanoimprinting

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In this study, we present the nanoimprinting of colloidal nanocrystals for nanoscale metamaterial fabrication. The nanocrystal based metamaterials are demonstrated with Au, Ag and VO_2 colloidal nanocrystals by nanoimprint lithography [1,2]. The nanocrystals based nanostructures were fabricated by direct nanoimprint lithography. The nanocrystal dispersion was dropped on the substrate and quickly covered and pressed by PDMS template for filling the cavity between the substrate and the template. After evaporation of the solvent, the PDMS template was carefully detached from the substrate. It was fabricated over large areas of up to a few centimeters in scale with high resolution for various nanostructure geometries of nano-pillars, nano-rods, and nano-holes composed of nanocrystals. The direct nanoimprinting with room temperature process allows for the demonstration of these plasmonic nanoscale superstructures on the rigid substrates as well as, on the various flexible polymers substrates. Engineering the coupling between the nanocrystals within the nanostructures allows tailoring of the dielectric function of the nanostructures from that of a dielectric to that of a plasmonic metal by replacing the long, insulating ligands used in nanocrystal synthesis with the compact ligand. The optical plasmonic resonances of the nanostructures were tuned by the choice of nanocrystal building block, the dielectric function of the nanocrystal nanostructure, and the nanostructure geometry and periodicity. Tunable metamaterial nanostructures were also fabricated from nanocrystals of the reversible phase change-able material vanadium oxide (VO_2) nanocrystal. By tailoring their geometry and structural motif, and thermally annealing to control nanocrystal phase, we realized VO_2 nanostructures with a low-loss, plasmonic resonance that is reversibly, thermally on-off switchable with temperature.

[1] S-H Hong et al, “Chemically Tailored Dielectric-to-Metal Transition for the Design of Metamaterials from Nanoimprinted Colloidal Nanocrystals”, Nanolett. 13(2) 350-357 (2013)

[2] S-H Hong et al, “Solution-Processed Phase-Change VO_2 Metamaterials from Colloidal Vanadium Oxide (VOx) Nanocrystals”, ACS Nano 8(1) 797-806 (2014)

Electrical Characteristics of GaN Schottky Barrier Diode with Variety Buffer Thicknesses

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Gallium Nitride (GaN) Schottky Barrier Diodes (SBDs) and High-Electorn-Mobility-Transistors (HEMTs) have attracted much research interest in recent years [1, 2]. Because of their low power consumption, high voltage and high temperature operation for next-generation power electronic devices. In this study, GaN SBDs were grown on c-plane sapphire substrates using a metal-organic chemical vapor deposition (MOCVD) system. Fabricated SBDs has a different GaN buffer thickness (T_{GaN}) of 3.5 um, 5 um and 10 um, respectively. Ohmic junctions of Ti/Al/Ni/Au and Schottky junctions of Ni/Au are used in the fabrication. The on-state resistances (R_{on}) of T_{GaN} (3.5 um) is 5.42 mΩ-cm^2. The R_{on} of T_{GaN} (5 um), T_{GaN} (10 um) are 46.6 mΩ-cm^2, 20.9 mΩ-cm^2, respectively. The reverse breakdown voltage (V_B) increased with the spacing between Schottky and ohmic metal contacts, reaching 447 V for T_{GaN} of 5 um and 610 V for T_{GaN} of 10um, at reverse leakage current density of 500 mA/cm^2 for 120 um gap spacing. For gaps between 30 and 120 um, V_B is linearly dependent on the spacing, with slopes of 3.9E5 V-cm^{-1} for T_{GaN} of 5 um and 2.6E5 V-cm^{-1} for T_{GaN} of 10um, respectively. The figure of merit $(V_B)^2/R_{on}$ was in the range 0.55 – 1.78 V^2/Ω-cm^2 for all the devices.

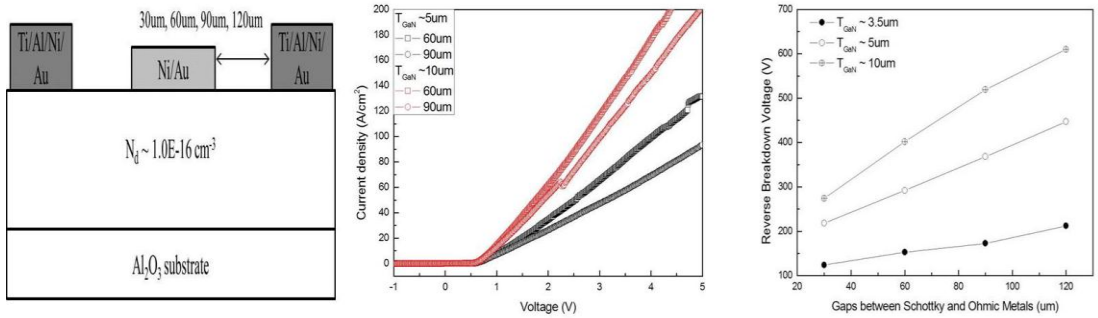

Fig 1. DC characteristics of GaN SBDs and its Breakdown characteristics.

[1] I. B. Rowena, S. L. Selvaraj, and T. Egawa, IEEE Electron Device Letters. Vol. 32, No. 11 (2011).
[2] Y. Chen,Y. Jiang, P.Q. XU, and H. Chen, Journal of Electronic Materials. Vol. 41, No. 3 (2012)

Fabrication of ambipolar transistors and inverters based on single-walled carbon nanotube-InGaZnO hybrid structure using microwave irradiation

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최근, mobile display system 에 이용되는 유연하고 가벼운 devices 의 재료로 산화물 반도체가 많은 주목을 받고 있다. 산화물 반도체는 비정질 상태에서 뛰어난 전기적 특성과 투명성을 가지고 있으나, 저온 열처리 방법 및 p-type 반도체 개발에 어려움이 있다[1]. 반면, 유기물 반도체는 p-type 전도특성을 쉽게 얻을 수 있지만, 온도에 민감하고 장기간 신뢰성에 문제점이 있다. 한편, carbon nano tube(CNT)는 뛰어난 화학적 안정성과 p-type 전도 특성을 가지기 때문에 산화물 반도체와 함께 CMOS 구조 형성에 유리하지만 고온의 열처리 공정에 취약하다는 단점이 있다. 본 연구에서는 dip-coating 방법에 의하여 mono-layer 의 SWCNT film 을 형성하고 그 위에 a-IGZO film 을 solution deposition 방법으로 적층하여, ambipolar 전도 특성을 가지는 SWCNT-IGZO hybrid thin film transistors(TFTs)구조를 제안하였다 [그림 1(a)]. 용액공정으로 형성된 a-IGZO 층은 TFT 소자에 적합한 전기적 특성을 얻기 위하여 높은 온도의 열처리 공정이 필요하지만, SWCNT film 은 이 열처리 과정에서 특성 열화가 발생되므로 기존의 열처리 방법으로는 SWCNT-IGZO hybrid TFTs 제작이 불가능하다. 따라서, 우리는 저온의 (< 100 °C) microwave 열처리 공정을 이용하여 용액공정 기반의 SWCNT-IGZO hybrid TFTs 제작의 핵심적인 열처리 공정의 문제점을 극복하였으며, 그 결과 게이트 전압의 극성에 따라서 N 형(a-IGZO film)과 P 형(SWCNTs film) 전도 특성을 가지는 ambipolar TFT 를 제작하였고, 이를 이용하여 CMOS inverter 구현이 가능하였다 [그림 1(b)]. 본 연구에서 구현한 소자 및 공정기술은 유연하고 투명한 기판 상에서 전자 회로의 구현이 가능하므로 차세대 디스플레이 및 플렉서블 소자에 유망한 기술로 기대된다.

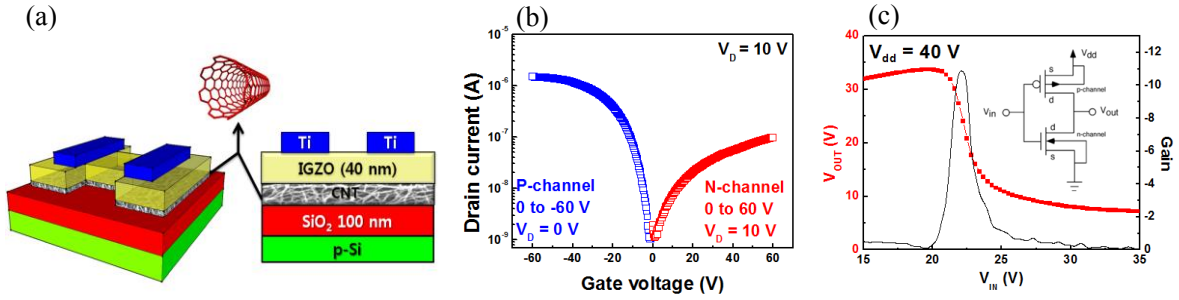

그림 1. (a) Schematic structure of hybrid CNT-IGZO TFT. (b) Ambipolar transfer characteristics. (c) Output characteristic and gain of inverter constructed.

Investigations of baking temperature on solution processed In-Ga-Zn-O thin film transistor.

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최근에 display system 의 구동소자로 oxide semiconductor 를 이용한 TFT(thin film transistor)가 큰 주목을 받고 있다[1]. 특히, TFT 의 채널을 형성하는 방법 중에서 용액공정은 대면적화,경제성 및 다양한 장점을 가지고 있다. 하지만, 용액공정으로 형성된 박막에는 수분,탄소 계열 불순물이 포함되어 소자의 전기적 특성 열화를 초래하기 때문에 이를 제거 하기 위한 baking 과정이 필수적이다[1]. 따라서, 본 연구에서는 용액 공정 중의 baking 조건이 용액 기반 IGZO TFT 의 전기적 특성에 미치는 영향에 대하여 연구 하였다. p type Si 위에 건식 산화방식으로 성장한 SiO_2(100 nm) 상부에 In:Ga:Zn 의 조성비를 2:1:1 의 비율로 만든 용액을 이용하여 IGZO 박막을 형성 하였다. 그리고, baking 과정으로 180~250 °C 의 범위에서 10 분 동안 열처리를 실시하였다. TFT 의 채널을 형성한 후, N_2 기체 분위기에서 600 °C 로 30 분 동안 후속 열처리를 실시하고 금속전극을 형성하여 전기적인 특성을 평가하였다. 그 결과, 600 °C 의 고온에서 동일한 후속 열처리를 거쳤음에도 불구하고 baking 과정에서의 온도 (160~250 °C)에 의해 소자의 mobility, hysteresis 등의 전기적 특성에 큰 차이를 발견 하였다. BOE 에 대한 etching rate 등 화학적 성질도 낮은 온도에서 크게 달라졌다. IGZO TFT 소자의 전기적 특성은 baking 온도가 낮을 수록 높은 구동 전류와 양호한 hystesis 특성을 보였다 이는 baking 에서 온도 별로 일어나는 반응과 그에 따른, 채널내의 산소 관련 결함 성분과 관련이 있는 것을 XPS (x-ray photospectroscopy)와 열 중량/시차 주사 열량 분석을 통하여 확인 하였다.

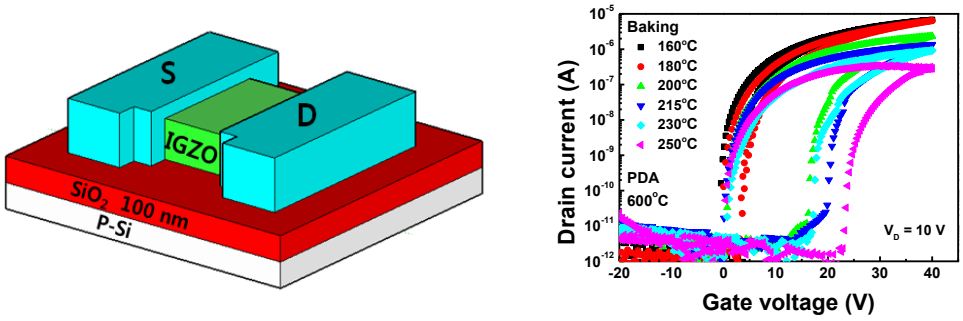

그림 1. 소자의 구조와 Baking 과정의 온도변화에 따른 IGZO TFT 의 전달특성.

[1] S. Jeong, Y. Jeong and J. Moon, J. Phys. Chem.Lett. 4, 11082(2008)

Improvement of Electrical Characteristics of Solution Processed In-Ga-ZnO TFTs by Double Side Irradiation

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최근 몇 년간 마이크로웨이브 열처리 기술을 이용한 많은 연구들이 활발하게 진행되고 있다. 마이크로웨이브 열처리 기술은 소자에 에너지를 직접적으로 전달하기 때문에 기존의 열처리 기술에 비해 에너지 전송 효율이 높고 공정 시간 및 비용 또한 적게 들며, 저온의 열처리 공정으로 인하여 flexible 기판 이나 glass 기판 기반으로의 확대 적용이 가능하다는 수 많은 장점들을 가지고 있다 [1]. 하지만 이러한 마이크로웨이브 열처리 방식에 따른 소자 특성의 개선에 대한 연구는 아직까지 많이 미흡하다. 따라서 본 연구에서는 전기적 특성 평가가 용이한 Junctionless 구조에서 용액공정을 이용한 InGaZnO TFTs 를 제작하여 각기 다른 두 가지 방식의 마이크로웨이브 열처리를 실시하여 전기적 특성을 평가해 보았다. 열처리는 각각 Single side irradiation(SDI), Double side irradiation(DSI) 방식으로 진행하였으며, 두 가지 방식 모두 1000 W 의 출력으로 15 분 동안 실시하였다. 그 결과, DSI 방식으로 열처리를 진행한 소자에서 subthreshold swing(SS), $I_{on/off}$ ratio, field-effect mobility 등이 개선 되는 것을 확인하였다. 본 연구에서 검증한 DSI 방법을 이용하여 마이크로웨이브 열처리 공정을 실시하게 되면 보다 균일한 가열 성능으로 인하여 소자의 특성 개선에 확실한 효과를 볼 수 있을 것으로 생각된다.

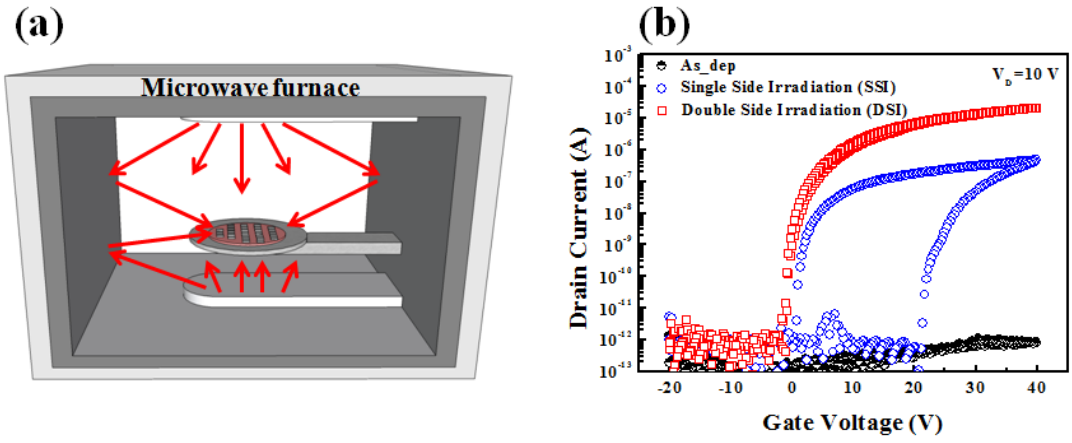

Fig 1. (a) Schematic of microwave irradiation method. (b) Transfer characteristic curve (I_D-V_G) of a-IGZO TFTs annealed by a microwave irradiation at SSI and DSI mode, respectively.

[1] L. F. Teng, P. T. Liu, Y. J. Lo, et al., Appl. Phys. Lett., vol. 101, no. 13, pp. 132901-1, Sep. (2012).

GaAs single junction solar cell on Si substrate with direct wafer bonding

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Integration of III-V solar cell (SC) on Si substrate is promising method to obtain both advantages of high energy conversion efficiency from GaAs cell and low cost, mechanical robustness, large thermal conductivity from Si substrate [1], [2]. However, due to the large difference of lattice constant between GaAs and Si, epitaxial growth of GaAs layer is not easy on Si substrate. To circumvent this issue, we have fabricated GaAs SC on Si substrate using direct wafer bonding.

Fig. 1 shows the final device structure of GaAs SC on Si substrate. Firstly, GaAs SC layer was grown on semi-insulating GaAs substrate with $Al_{0.8}Ga_{0.2}As$ etching sacrificial layer between GaAs cell and GaAs substrate. Then, III-V and Si wafers (p-type, resistivity of 0.001-0.005 Ω·cm) have been bonded each other by direct wafer bonding. Subsequently, GaAs donor substrates were etched by H_3PO_4 based solutions and citric acid to etch GaAs and stop on $Al_{0.8}Ga_{0.2}As$ layer. Then, $Al_{0.8}Ga_{0.2}As$ layer was etched by HF solutions. Using this GaAs/Si wafer, we have fabricated SC with top metal electrode for GaAs and bottom electrode for Si. Cross-sectional SEM image of GaAs SC on Si is shown in Fig. 2. GaAs SC on Si was confirmed by the images. It is shown that bonding interface seems to be very clean without any voids, indicating our bonding process provides clean GaAs/Si interface. Fig. 3 highlights typical current density (J) – voltage (V) characteristics of fabricated GaAs SC on Si. Even without anti-reflection coating, energy conversion efficiency (η) was high of 13.25 % at 1 sun, AM 1.5G measurement conditions.

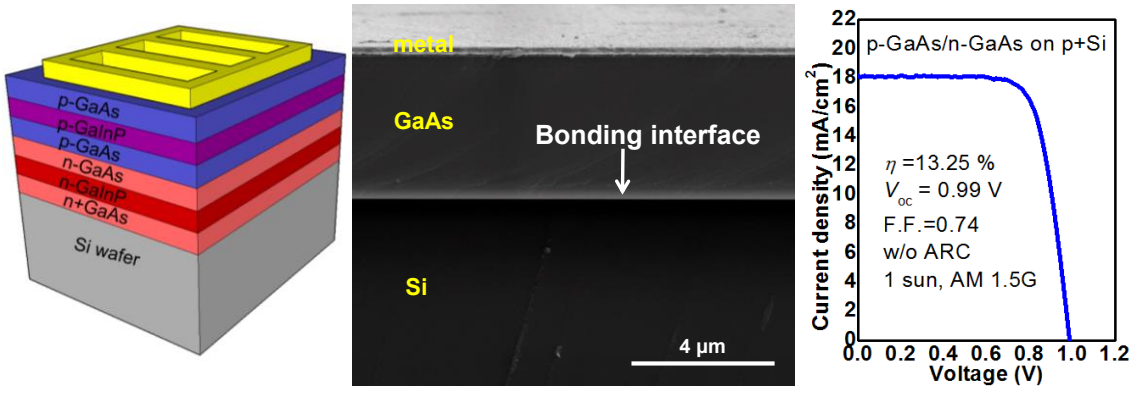

Fig. 1 Device structure of GaAs SC on Si (**left**) Fig. 2 Cross-sectional SEM image of GaAs on Si (**center**) Fig. 3 Typical *J-V* characteristics of GaAs SC on Si substrate (**right**)

[1] K. Tanabe *et al.*, *Sci. Rep.* **2**, 349 (2012) [2] K. Derendorf *et al.*, *IEEE J. Photovolt.* **3**, p.1423 (2013)

GaAs on Si substrate realized by wafer bonding and epitaxial lift-off

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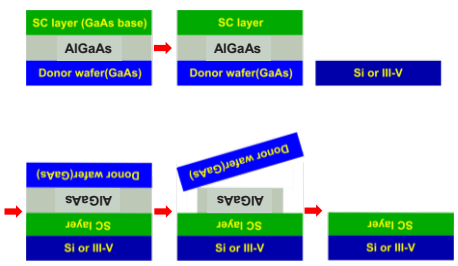
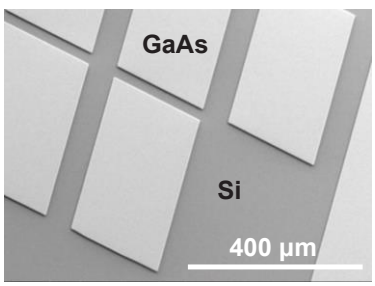
III-V on Si structure has been studied for many applicactions such as electronic and photonic devices to use strong optical properties of III-V semiconductor and good productability of Si-based materials. However, epitaxial growth of III-V layers on Si is not easy due to large lattice mismatch between III-V and Si. To circumvent this issue, we have fabricated GaAs on Si structure using wafer bonding (WB) and epitaxial lift off (ELO) technique as shown in Fig. 1.

Firstly, GaAs-based epitaxial layer was grown on bulk GaAs substrate with $Al_{0.8}Ga_{0.2}As$ etching sacrificial layer. Then, wafer was diced to 1.5×1.5 cm^2 chips and bonded to Si wafer by WB (direct or metal). Subsequently, samples were dipped in HF:DIW (1:5) solutions to selectively etch $Al_{0.8}Ga_{0.2}As$ layer, which is located between GaAs donor substrate and thin GaAs layer. Finally, substrate splitting was observed after around 30 hours from the dipping in HF:DIW (1:5) solutions.

To reduce long processing time for ELO, we have added pre-patterning and mesa etching process before WB. This pre-patterning can make extra possible etching area of AlGaAs layer, resulting in the reduction of ELO time. Fig. 2 shows a tilted SEM image of GaAs on Si fabricated by ELO with pre-patterning. The image clearly shows GaAs on Si structure can be fabricated by ELO with pre-patterning. Also, ELO time was significantly reduced to 6 hours. To further enhance ELO process, we have changed HF concentration and added hydrophilic substances of isopropanol (IPA), acetone (Ace). Fig. 3 shows ELO time as a function of various solutions. It was shown that pre-patterning and addition of hydrophilic substances significanlty reduce the processing time as short as 20 min. These results strongly suggest ELO process developed in this study can be promising technology for future III-V-based electronic and photonic applications on Si substrate.





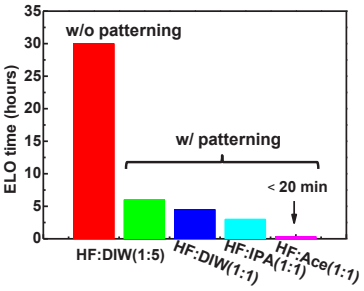


Fig. 1 Fabrication of GaAs on Si structure by WB and ELO (**left**) Fig. 2 Tilted SEM image of GaAs on Si substrate (**center**) Fig. 3 ELO time of GaAs/$Al_{0.8}Ga_{0.2}As$/GaAs/Si as a function of used structure and solutions (**right**)

Low-Noise Microwave Performance of AlGaN/GaN HEMTs on SiC with Wide Head T-Shaped Gate

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The GaN-based HEMTs have attracted a lot of attention because of high power, high frequency, low-noise performance[1]. To improve the noise performance of these devices, it is required to reduce the parasitic gate resistance(R_g) as well as the scaling of L_g and L_{sd} [2]. However, little work has been reported on the noise performance of GaN HEMTs with a wide head T-shaped gate to further reduce R_g. In this work, we present the low-noise microwave performance on 0.18 μm gate-length AlGaN/GaN HEMTs on SiC with a wide head T-shaped gate. The $Al_{0.25}Ga_{0.75}N$ /GaN HEMT epitaxial structure on SiC was used for fabricating these devices. Ohmic contacts were formed by Ti/Al/Ni/Au evaporation and RTA. The ion implantation was used for device isolation. Wide head T-shaped gate having 0.18 μm gate-length and 1.07 μm gate-head was fabricated by two-step e-beam lithography. The devices had a gate width of 150 μm and a source-drain spacing of 3.5 μm. The threshold voltage was – 3.5 V. The extrinsic transconductance was 270 mS/mm at a gate bias of – 2.8 V and a drain bias of 10 V. These devices have a f_T of 45 GHz and f_{MAX} of 136 GHz. For noise measurement bias condition of V_{ds} = 5 V and V_{gs} = – 2.75 V, the devices showed minimum noise figure (NF_{min}) of 0.81 dB and associated gain (G_a) of 12.1 dB at 10 GHz. At 18 GHz, NF_{min} and G_a were 1.41 dB and 9.6 dB, respectively. The noise data at 10 GHz is one of the best ever reported for GaN HEMTs with similar gate-length, which is attributed to the reduction of gate resistance resulting from the large cross-sectional area of the gate.

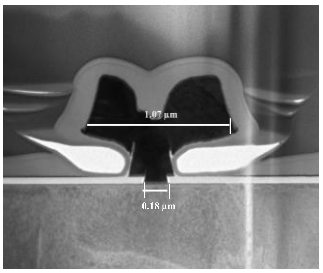

Fig.1. Wide head T-shaped gate.

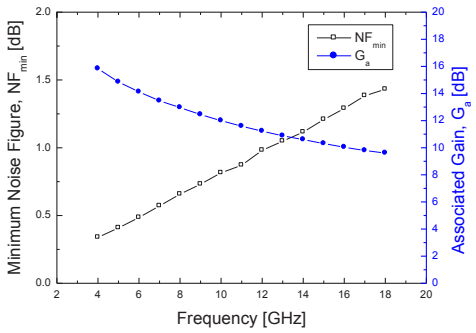

Fig.2. NF_{min} and G_a vs frequency for the device.

[1] J. S. Moon, *et al*,, IEEE Eletron Device Lett., vol. 32, no.3, pp.297-299(2011).

[2] C. H. Oxley, Solid State Electron., Vol.45, pp. 677-682(2001).

X-band 40W pulsed power amplifier using 0.2um AlGaN/GaN HEMT

강동민, 이종민, 민병규, 윤형섭, 안호균, 김성일, 주철원, 김해천, 임종원
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This paper describes the successful development and the performance of X-band 40 W pulsed power amplifier using a 40 W GaN-on-SiC High Electron Mobility Transistor(HEMT). The GaN HEMT with a gate length of 0.2 μm and a total gate width of 12 mm were fabricated. The GaN HEMT provide a linear gain of 6 dB with 42 W output power operated at 30 V drain voltage in pulse operation with a pulse width 100 us and 20 % duty cycle at X-band. It also shows a maximum output power density of 3.3 W/mm. The X-band pulsed power amplifier exhibited an output power of 42 W(46.2 dBm) with a power gain of 6 dB in a frequency range of 9.2 – 9.5 GHz.. This 40 W GaN HEMT and X-band 40 W pulsed power amplifier are suitable for the radar systems and related applications in X-band.

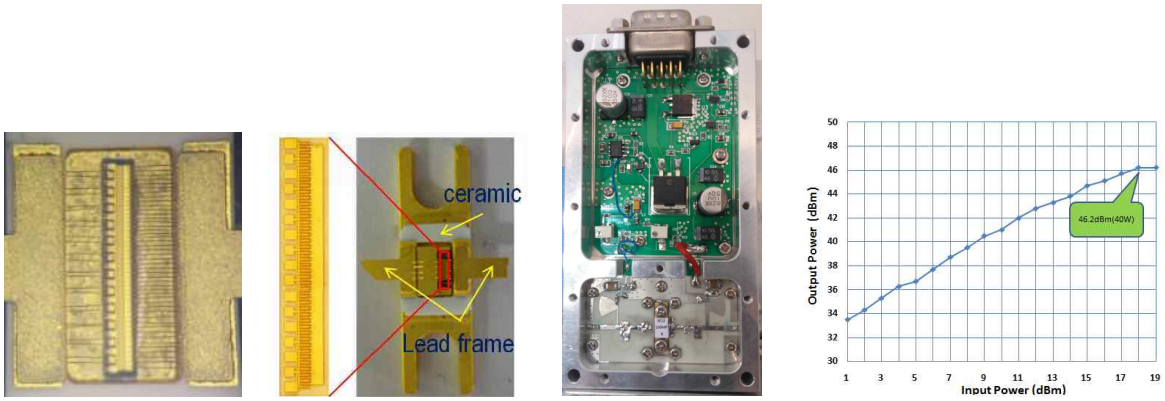

그림 1. 40W GaN HEMT 소자, 패키지 및 전력증폭기 사진

[1] M. Casto et al., “100W X-band GaN SSPA for medium power TWTA replacement,” Wireless and Microwave Technology Conference 2011 IEEE 12th Annual.

Surface passivation oxide study of 4H-SiC Bipolar Junction Transistors

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실리콘 카바이드(SiC)는 와이드 밴드갭 반도체로서 실리콘에 비해 높은 전계강도(~2.3×10^6 V/cm)와 높은 열전도율(3-4 W/cmK at 300K)을 가지고 있기 때문에 실리콘 전력용 반도체를 뛰어넘는 차세대 전력용 반도체 소재로서 주목을 받고 있다 []. 전력용 소자로서 SiC BJT(Bipolar Junction Transistor)는 FETs 소자에 비해 게이트 산화막 문제에 상대적으로 자유로운 점과 낮은 온 저항이라는 장점을 가지고 있다. 하지만, SiC BJT소자의 낮은 전류이득(Current gain)은 고성능의 전력용 스위칭 소자를 위해 해결해야 할 중요한 요소중의 하나이다. 본 연구에서는 SiC BJT소자의 passivation layer로서 Thermal oxide와 아산화질소 산화막(nitrous oxide)을 비교하였고, 표면 재결합 (surface recombination current)의 억제를 통해 ~2배정도의 전류 이득의 향상을 가져왔다.

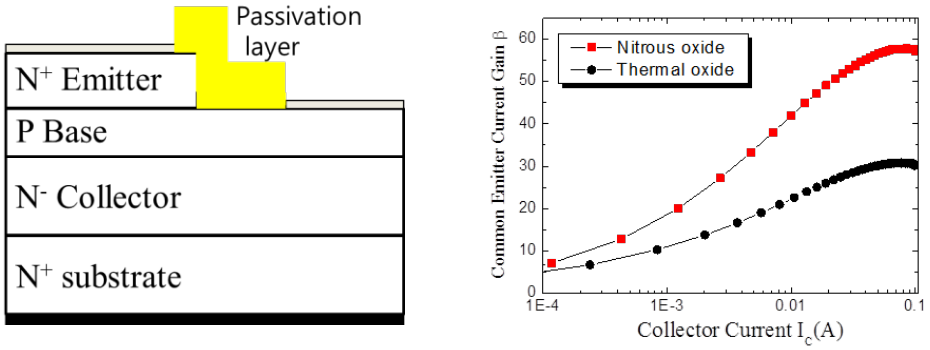

Fig 1. Cross-sectional view of SiC BJT (left) Measured current gain β as a function of collector current I_C for 4H-SiC BJTs with different passivation (right)

[1] C.-M Zetterling, “Process technology for silicon carbide devices,” in EMIS processing series, IEE, (2002)
[2] H.-S Lee, et al., IEEE Electron Device Lett. Vol 28, No. 11, pp. 1007-1009, 2007

Improvement in high mobility of indium zinc oxide transistor by metal capping method

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ZnO 기반의 박막트랜지스터(TFT)는 뛰어난 전기적 특성, 균일도 및 투명성을 갖고 있어, 고해상도 모바일 LCD 와 OLED TV 에 적용 가능하다[1]. 이러한 특성에도 불구하고 산화물 반도체 TFT 는 저온공정 폴리 실리콘(LTPS) TFT 와 경쟁하기 위하여 고이동도 특성을 필요로 한다. 본 연구소에서는 이 문제를 해결하기 위하여 기존의 Bottom 구조 TFT 소자에 메탈 캡핑 구조를 적용하는 연구를 진행하였다.

메탈 캡핑 구조는 Ca/Al 의 메탈층을 이용하여 InZnGaO TFT 소자의 고이동도 특성을 보인 연구 결과가 보고된 바 있다[2]. 이 메카니즘은 메탈이 반도체 채널층에 존재하는 loosely bonding oxygen 을 gathering 하여 산화되면서 이동도의 향상을 보여주는 것이다. 본 연구에서는 Titanium 을 캡핑 소재로 이용하여 InZnO TFT 에 적용시키는 연구를 진행하였으며, 열처리를 통해 캡핑 소자의 안정화를 알아 보고자 하였다. Titanium 은 현재 TFT 백플레인 생산라인에서 적용하기에 적합한 소재로, 본 연구에서 캡핑 소재로 선정한 이유이다.

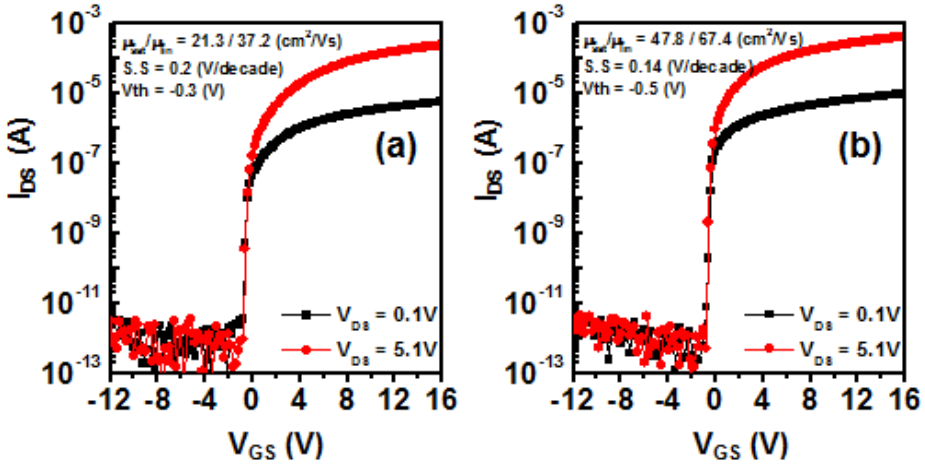

Fig 1. (a) Control Device (IZO TFT) (b) Ti CL IZO TFT 전기적 특성의 비교

[1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, and H. Hosono, Nature (London) **432**, 488 (2004).
[2] H.-W. Zan, C.-C. Yeh, H.-F. Meng, C.-C. Tsai, and L.-H. Chen, Adv. Mater. 24, 3509 (2012).

CLGO계 기반 Sm^{3+} 이온 도핑된 형광체의 주황색 발광 특성

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최근 희토류가 도핑된 이온 활성화 형광체는 형광램프, 백색 LEDs, 조명, 플라즈마 디스플레이 소자를 포함한 다양한 영역에 응용하기 위해서 고효율의 형광체를 개발하기 위해 많은 노력을 하고 있다. 란탄이온의 f-f 혹은 f-d 전이에 의하여 발생된 발광신호의 세기는 자리 대칭성에 따라 바뀌는 특성을 가지고 있으며, 란탄계열 Sm^{3+} 이온은 높은 색순도와 좁은 영역에서의 방출을 위해 높은 관심을 끌고 있다. Oxide 기반 형광체는 fluoride, sulfide, nitride 기반계열에 비하여 열적, 화학적으로 우수한 특성을 가지고 있으며 친환경이고 높은 효율의 발광특성을 보인다. 본 연구에서 $Ca_2La_8(GeO_4)_6O_2$ (CLGO) 모체에 Sm^{3+} 이온을 각각 0.25, 0.5, 1 및 2 mol%로 도핑하여 주황색 파장의 영역을 가지는 형광체를 제작하였다. 파장 401 nm 로 여기 시킨 Sm^{3+} 이온 함량비에 따른 CLGO 형광 스펙트럼은 전반적으로 각각 560, 597 및 607 nm 파장들에서 발광 피크 분포를 나타내었으며, 그 파장 영역에서는 황색, 주황색 및 적색 형광 스펙트럼을 각각 나타내었고, Sm^{3+} 이온 농도가 증가함에 따라 발광세기도 증가하였고, 0.5 mol% 에서 최대 세기를 갖는 형광스펙트럼이 관찰되었다.

Fabrication of GaN-based UV Active Pixel Sensor

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We proposed a gallium nitride (GaN) based ultraviolet (UV) active pixel sensor (APS) that is compromised of MSM-type GaN-based UV sensors and GaN MOSFETs. GaN epitaxial layer was grown on a silicon substrate by using MOCVD at 1070 °C. Fig. 1 shows a micro-photograph image of fabricated GaN-based UV APS array in which we used indium-tin-oxide (ITO) as a transparent electrode[1]. Fig. 2 shows the dark and photo-responsive I-V characteristics of fabricated GaN MSM UV sensor which is a part of the APS. It was measured under 365-nm UV irradiation with an optical power density of 357 mW/cm^2. Dark current density was 1.4 × 10^{-10} A/cm^2 and photo-responsive current density was 3.9 × 10^{-7} A/cm^2 at 10 V bias, respectively. There are five orders of magnitude of the photo-to-dark ratio under the bias from -8 V to 8 V. In our simulation on the APS operation using the circuit simulator HSPICE, we confirmed the output using a conventional circuit and the switched capacitor. Fig. 3 shows the simulation result where the currents value changed from 10 nA to 90 nA and V_{DD} of 15 V and reset pulse voltage of 15 V, select pulse voltage of 15 V, respectively.

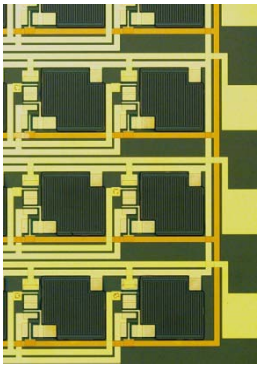

Fig.1 Micro-photograph image of fabricated 4x4 APS array [1].

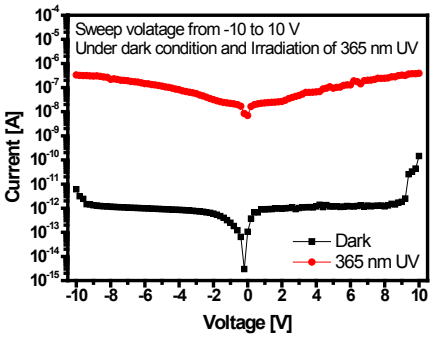

Fig.2 Dark and Photo-responsive I-V characteristics of fabricated GaN MSM UV sensor.

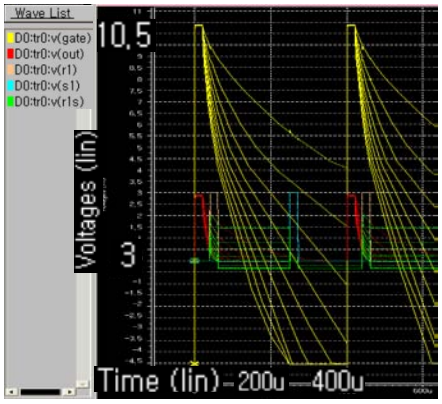

Fig.3 The output characteristics of simulated 1 pixel according to the variation of photo current.

[1] C. J. Lee et al, "Hybrid Approach to UV Active Pixel Sensor: Integration of GaN Photodetector and Si-MOSFET Circuit", MNC (2014).

A GaN MSM UV Photodiode

Using Multi-layer Graphene as a Schottky Electrode

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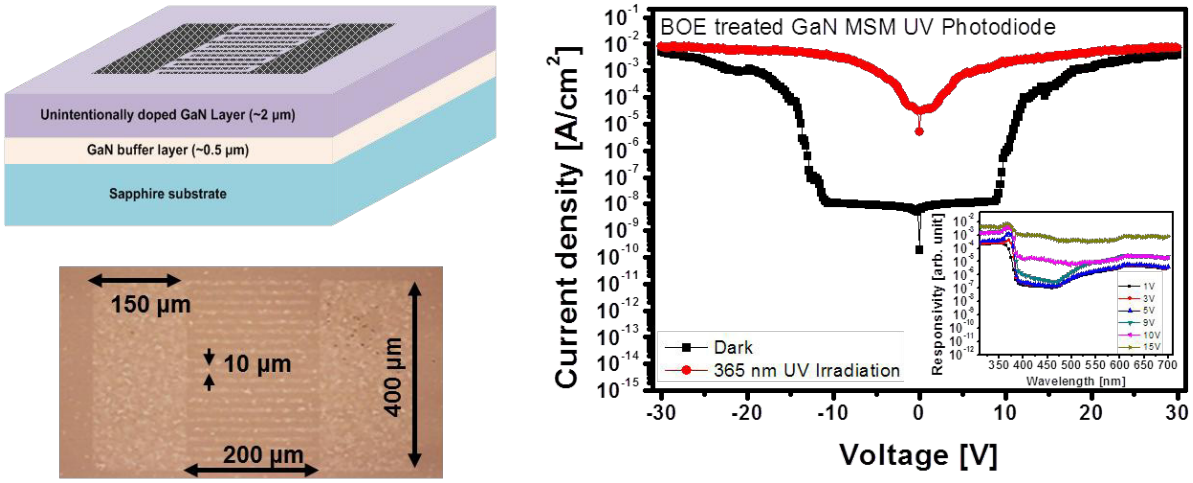
Metal-semiconductor-metal (MSM) type UV photodiode has been actively studied because of its fabrication simplicity and low leakage current. Considering a graphene as a highly transparent even at the UV region [1], we proposed and fabricated a GaN MSM UV photodiode by using multi-layer graphene as schottky electrodes. We measured the I-V characteristics of the fabricated GaN MSM UV photodiode under dark and irradiation of 365-nm UV. The dark current density and photo-responsive current density were 3.2 nA/cm^2 and 0.6 mA/cm^2 at 9 V, respectively. The UV to visible rejection ratio of the fabricated photodiode was 5,200 under irradiation of 365-nm UV, which is comparable with previous reported MSM diodes by using Pt, Al, Ni and ITO electrodes. On the other hand, after BOE treatment, the dark current density was 14.2 nA/cm^2 at 9 V and photo-responsive current density was 1.6 mA/cm^2 at 9 V. The photo-to-dark contrast ratio was five orders of magnitude at positive (negative) 9 V of applied bias and the UV to visible rejection ratio was 10,500 under irradiation of 365-nm UV as shown in the inset of Fig 1(b). The 365-nm UV irradiation power density was 357 mW/cm^2. We will also discuss the interface trapping and de-trapping effect to the characteristics of the fabricated GaN MSM photodiode.



(a) (b)

Fig. 1 (a) Schematic structure and micro photograph image and (b) dark/photo I-V characteristics (inset: spectral photo-responsivity) of the fabricated GaN MSM UV photodiode.

[1] X. Li et al., Nano lett. 9(12), 4359(2009)

Investigation of electrical performance degradation in p-AlGaN gate heterostructure field effect transistors under various off-stress conditions

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Electrical performance degradation under off-stress conditions has been considered as a serious problem in AlGaN/GaN heterostructure field effect transistors (HFETs) [1]. In this work, we investigate the effects of various off-state stresses on the electrical performance degradation in p-AlGaN gate HFETs which are especially devised for the normally-off operation. The devices were stressed under various off-stress conditions and the transfer curves were measured immediately. When the stress was applied only to the gate electrode, I_D decreases and V_{TH} moves to the positive direction. On the other hand, when the devices were stressed at V_G=-10V with increasing V_D, I_D remarkably decreased and V_{TH} does not move. This recoverable degradation may be the result of electron trapping, and we believe that the observed different phenomenon is due to the difference of charge trapping location. The V_{TH} shift can be understood of as result of electron trapping in the AlGaN buffer layer, and the decrease of I_D is mainly due to the trapped electrons in gate-drain access region. Various characterization methods including the pulsed I-V measurement technique were applied to investigate the electron trapping location under various off-stress conditions in our experiments.

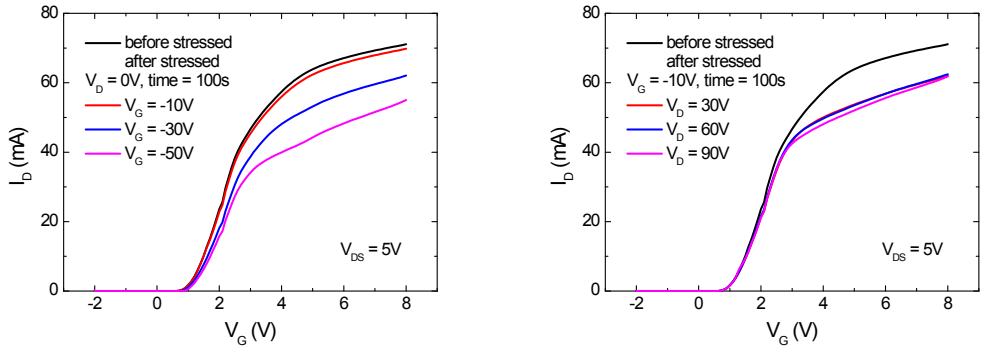

Fig. 1. Transfer curves before and after various off-state stresses in p-AlGaN gate HFETs

[1] Prashanth Makaram, et al., APPLIED PHYSICS LETTERS. 96, 233509 (2010).

Interface Engineering for InGaAs MIS Capacitor with Al_2O_3 employing PEALD-SiNx as an interfacial layer

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InGaAs has been extensively studied as a potential channel material because of their low electron effective mass and high electron velocity. However, III-V arsenide semiconductors have native oxides of poor electrical quality and readily form interface defects [1]. In the past, many groups have failed to yield accumulation and inversion carriers in the channel because of a poor interface state quality between the dielectric and the InGaAs channel. So it is desirable to improve gate insulator or interfacial layers. Recently, outstanding progresses have been made on the interface quality by using atomic layer deposition (ALD) [2]. The excellent interface quality between the high-k dielectric and the III–V channel is important issues. Especially, many groups use Al_2O_3 as an interfacial layer. The important factors for interfacial layer are hysteresis and interfacial trap rather than permittivity. However, the conventional Al_2O_3 dielectric film we proposed has high leakage current. SiNx could be a good candidate as an interfacial layer to improve leakage current for gate dielectric. In this work, we improved electrical characteristics and frequency dispersion on InGaAs. A 5nm-thick high quality dielectric film for an interfacial layer was deposited by our conventional ICP-CVD and ALD system. Our detailed PEALD SiNx process in this work was same as presented in [3]. The Al_2O_3 was deposited by ALD system and oxidant source has H_2O vapor. We first deposited 10 Å PEALD SiNx at 400℃. The rest of 40 Å ALD Al_2O_3 was deposited at 300℃.

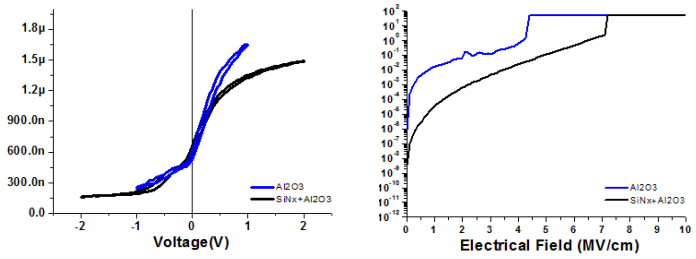

Fig 1. Distinct types of C-V characteristics

[1] R.M. Wallace, et al., MRS Bull. 34, pp. 493-503, 2009.

[2] Tae-woo Kim et al., Appl. Phys. Express. 7, 074201, 2014.

[3] Woojin Choi et al., *IEEE Electron Device Lett*., vol. 35, No. 1, 2014.

Acknowledgement

This research was supported by a grant from the R&D Program for Industrial Core Technology

funded by the Ministry of Trade, Industry and Energy(MOTIE), Republic of Korea.(Grant No. 10045216).
This work was supported by the Brain Korea 21 plus project in 2014.

Trapping and detrapping characteristics of TFT with p-type tin oxide channel for nonvolatile memory application

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Currently, the oxide semiconductor materials have attracted great interest in various applications including nonvolatile memory technology. However, some common oxide semiconductors such as indium gallium zinc oxide (IGZO), indium zinc oxide (IZO), etc. can have an issue of detrapping ability for erasing in NAND application since they have very few holes for detrap [1]. Due to the existence of both electron supply source (Sn^{4+}, Sn) and hole supply source (Sn^{2+}) which is confirmed by XPS spectra, p-type tin monoxide can be the solution for this issue. In our study, we fabricating TFT with p-type SnO channel exhibiting a threshold voltage of 1.5V, on/off current ratio of $4.5x10^{-3}$, and a symmetry trap and detrap characteristics. Under the negative bias stress (NBS) at V_g = -12V, the transfer curves shift to the negative direction without the degradation of transconductance (G_m) which indicates that the hole trapping/detrapping in the dielectric can be a main mechanism. During the relaxation at V_g = 12V, not only the hole detrapping but also the electron trapping at the interface and in the dielectric caused the left shift of transfer curves and G_m degradation.

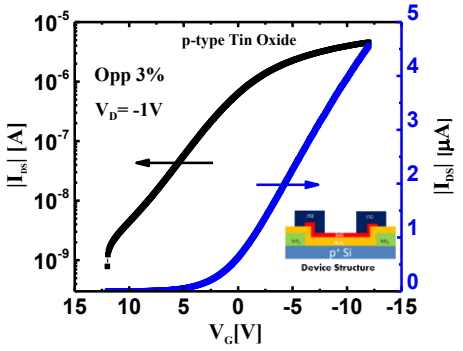

Fig 1. Transfer characteristic of SnO TFTs.

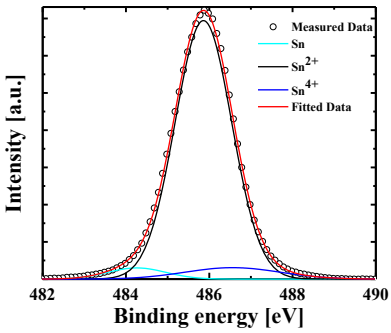

Fig 2. XPS spectra for SnO layer.

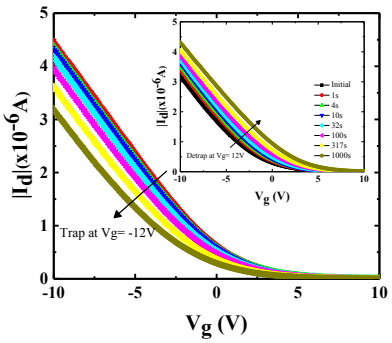

Fig 3. Trap and detrap characteristic of SnO TFTs.

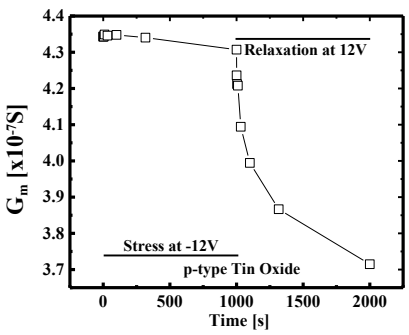

Fig 4. $G_{m,max}$ behavior under NBS and relaxation

[1] Huaxiang Yin, Member, IEEE, Sunil Kim, Hyuck Lim, Yosep Min, Chang Jung Kim, Ihun Song, Jaechul Park, Sang-Wook Kim, Alexander Tikhonovsky, Jaewoong Hyun, and Youngsoo Park, IEEE Transactions on electron devices, Vol. 55, No. 8, (2008).

Effect of In-situ Deposited Silicon Carbon Nitride Capping Layer Thickness on the Characteristics of AlGaN/GaN HEMTs

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The AlGaN/GaN HEMTs for high power and high frequency applications have been suffering from the surface trap states which is responsible for the leakage current and the current collapse. The dielectric materials, such as SiO_2, SiN_x, and Al_2O_3 deposited by ex-situ methods, have been widely used as surface passivation layer. It was also demonstrated that an in-situ grown Silicon Carbon Nitride (SiCN) capping layer is very effective in passivating AlGaN surface mainly due to increased n_s and protection of AlGaN surface from the air exposure [1]. In this work, we present a study on the characteristics of the in-situ SiCN capped AlGaN/GaN HEMT by varying the thickness of SiCN from 0 to 7nm. The defined gate length and width of the devices are 2 and 100 μm, respectively. The presence of a SiCN capping layer results in improvement of drain current ($I_{d,max}$) and maximum transconductance ($g_{m,max}$) due to the increased 2DEG density as shown in Fig. 1. The $G_{m,max}$ are gradually decreased with increasing the SiCN capping layer thickness because the distance between the gate to channel increases. Fig. 1 (c) shows the gate leakage current of the AlGaN/GaN HEMTs. The decrease of gate leakage current in the AlGaN/GaN HEMTs with 0.8 nm-thick and 3.3 nm-thick SiCN capping layers can be explained by decrease of the lateral surface leakage current and the trap-assisted tunneling probability. However, in the case of 7 nm-thick SiCN capping layer, the gate leakage current significantly increases, which is believed to be due to the increased direct tunneling probability caused by the decreased barrier height [1]. Further research is needed to clearly explain the increased leakage current.

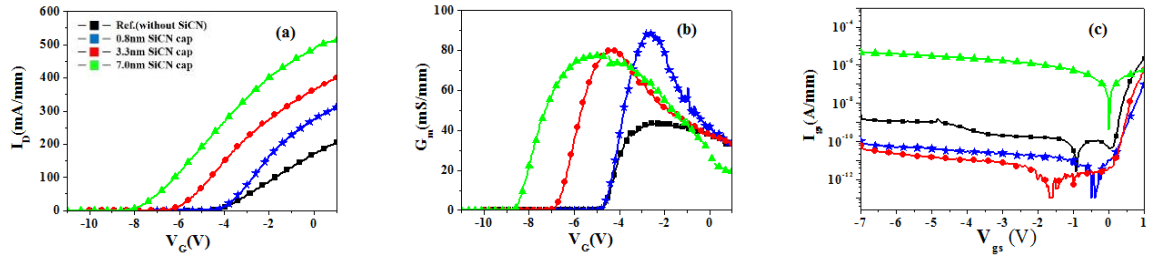

Fig 1. Measurement data of (a) Drain Current, (b) Transconductance and (c) Gate leakage current, respectively.

[1] J.-H Lee, et al., *IEEE Elec. Dev. Lett.*, Vol. 33, no. 4, pp. 492-494, Apr. 2012

AlGaN/GaN HEMT Using the Thick Metal Pad on 3D-BCB Structure

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The AlGaN/GaN high electron mobility transistor is emerging as an attractive candidate for power applications for its high breakdown voltage, high electron saturation velocity and high operating temperature.[1] Power devices in GaN can be either lateral devices on SiC and Si substrates or vertical devices preferably on GaN bulk substrate. Lateral devices are more mature and have demonstrated great promise. However, for higher power application where higher breakdown voltages are required, the lateral devices have issues due to very large chip areas inducing poor heat radiant, large on-resistance and operating at low current level.[2] In order to solve these issues, we propose thick drain and source pad (Au plating) sustained by 3D-BCB structure on the device. [shown in Fig1.] By comparing the proposed structure and the device before fabricating drain and source pad, we could verify the designed structure has remarkably improved heat emission problem, maximum operating current and on-resistance. When the pad was not applied, it shows low maximum operating current (~3.3 A) and large on-resistance (~2.6 Ω). [shown in Fig2.(a)] By contrast, drain and source pad which is vertically connected to the device through BCB via can minimize the device size by saving the room for drain and source pad. Also thick drain and source pad metal (>9 um) improve maximum operating current (~9.2 A) and reduce on-resistance (~0.8 Ω) [shown in Fig2.(b)]

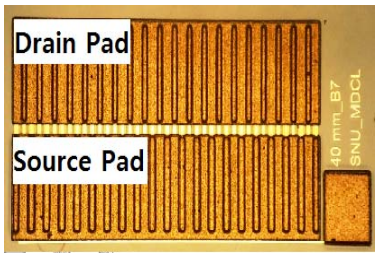


Fig1. AlGaN/GaN power HEMT with S/D pad on BCB structure.

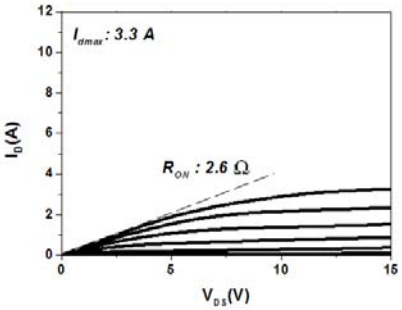
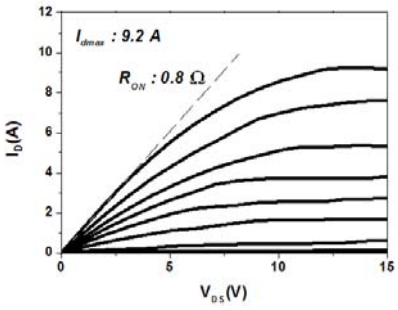


Fig2.(a) w/o topside pad.



(b) with topside thick metal pad.

Reference

[1] M.-S. Lee, *et.al IEEE Electron Dev. Lett.,* 35, 995 (2014).
[2] Chowdhury, S. *et.al*, *IEEE Electron Dev., Vol. 60, No 10.* (2013).

Acknowledgement
Program through the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. 2012M3A7B4035145) and the Brain Korea 21 Plus Project in 2014.

Improvement of transconductance by damage curing on AlGaN/GaN normally-on MIS-HEMT for RF application

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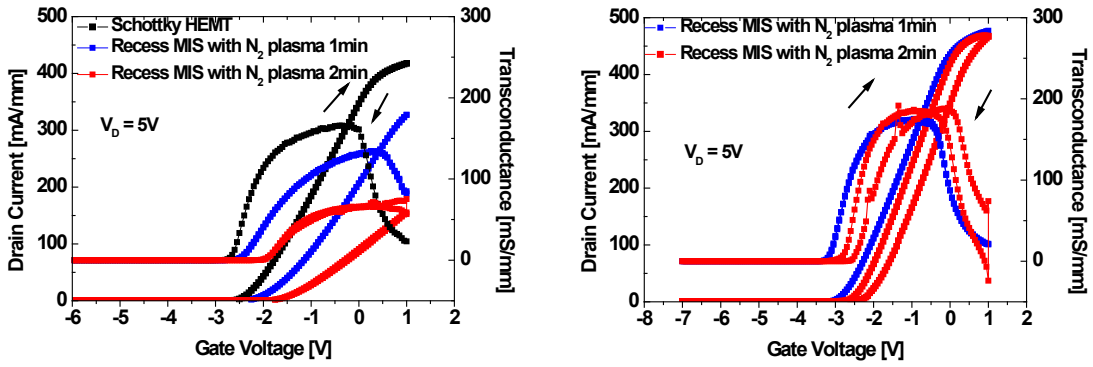
The importance of high-frequency and high-power amplifiers has rapidly increased with the development of wireless communications, GaN is the attractive material to overcome Si technologies because of high saturation velocity, high electron mobility and high breakdown electric field [1]. AlGaN/GaN high electron mobility transistors (HEMTs) have been researched for operating at high-frequency with high-power. But, there are still some issues to improve device performances, especially low gate leakage current for low loss. One approach to make thin AlGaN barrier is recess etching instead of growth. Compared with normally-off power MIS-HEMT, recess etching damage near the channel has more sensitive effects on 2DEG density and carrier mobility which are the key facts of improving transconductance and frequency response[2]. To evaluation carrier properties, Van der Pauw patterns were fabricated with mesa isolation and ohmic contacts on 24 nm AlGaN barrier and 2 nm GaN cap layer, and we etched active area with various depths. After that, post etch annealing and N_2 plasma treatment were conducted to know about damage recovery on the nearest depth from the channel that we able to apply at normally-on RF MIS-HEMT. Finally, we fabricated AlGaN/GaN normally-on MIS-HEMT (L_g = 2 ㎛) that has higher transconductance and lower gate leakage current than AlGaN/GaN schottky HEMT



[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, Nat. Nanotechnol. 6, 147 (2011).
[2] Z.Z. Chen*, Z.X. Qin, Y.Z. Tong, X.M. Ding, X.D. Hu, T.J. Yu, Z.J. Yang, G.Y. Zhang, PhysicaB: Condensed Matter 334.1 (2003)

Acknowledgement

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (NRF-2014R1A2A2A01007284) and by the Brain Korea 21 Plus project in 2014

애노드 구조 변화와 Al_2O_3 passivation을 통한 쇼트키 배리어 다이오드의 전기적 특성 분석

이현수 [1,2], 김정진 [1], 장현규 [1], 정동윤 [1], 나제호 [1], 박영락 [1], 장우진 [1],
전치훈 [1], 류상욱 [2], 문재경 [1], 고상춘 [1*], 남은수 [1]
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본 연구는 애노드 구조에 따른 순방향과 역방향 특성의 관계를 분석하여 턴온전압(V_T), 순방향 전류(I_F) 및 항복전압(V_{BD}), 역방향 누설전류(I_R) 등의 순방향과 역방향 특성을 동시에 향상시키기 위한 Schottky Barrier Diode(SBD)의 구조 및 제작 방법에 관한 것이다. 실험은 AlGaN/GaN on Si SBD에서 역방향 특성 향상을 위해 Al_2O_3 passivation을 적용한 Conventional(C), Recessed(R), Gated Ohmic(G)[1] 구조의 3가지 SBD를 제작하였다. C-SBD는 1.62V의 V_T와 0.57mA/mm의 I_F, 1.68uA의 I_R을 나타냈다. R-SBD는 C-SBD에 비해 순방향 특성을 향상시킬 뿐 아니라 I_R을 감소시키는 효과를 나타냈다. G-SBD는 0.94V의 V_T와 7.02mA/mm의 I_F로 C-SBD에 비해 순방향특성은 향상되었으나, 4uA/mm로 I_R 특성은 저하되었다. 이는 오믹 사이의 전류 흐름을 리세스된 애노드 영역이 제대로 제어하지 못한 것으로 판단된다. C-구조에 비해 순방향과 역방향특성이 동시에 향상된 R-구조를 기반으로, 리세스 깊이와 Al_2O_3두께를 조절함으로써 순방향과 역방향특성을 동시에 더 개선한 G-구조를 제작할 수 있다.

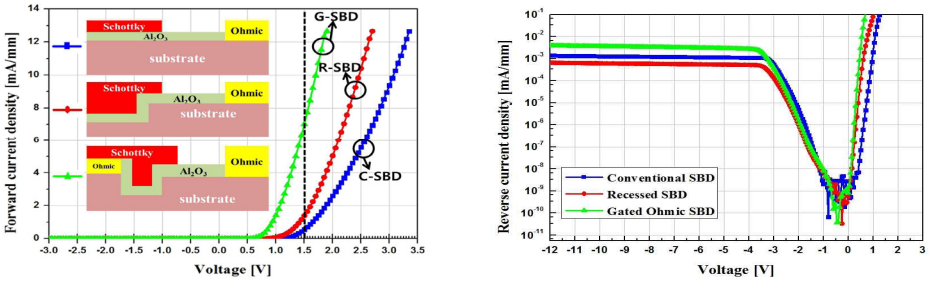

그림 1. Conventional, Recessed, Gate Ohmic SBD 구조와 전기적 특성 측정 결과

[1] J.-G. Lee, et al., IEEE Electron Device Lett., vol. 34, no. 2, pp. 214–216, Feb. 2013.

감사의 글: 본 연구는 미래창조과학부에서 지원하는 '스마트 데이터 센터용 차세대 광-전 모듈 기술' 사업(no. 10038766)과 산업기술연구회에서 지원하는 '고효율·내환경 GaN 전력반도체 모듈 국산화' 사업(no. B551179-13-02-06)으로 수행되었음.

Study the breakdown voltage characteristics of the SBD Floating Metal Ring with Mo Schottky Metal

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SiC 전력 소자는 고속전철 및 전기자동차의 전력제어, 증폭기, 발전기 송배전 분야에서 전력제어에 광범위하게 응용되고 있다. SiC SBD소자는 Si소자 대비 고내압, 고성능화 및 낮은 소비전력의 특징을 가지고 있으며 인버터 모듈에 장착할 경우 칩 면적이 작아지고 발열 및 리커버리 시간이 줄어든다. 기존의 SBD는 Von 전압이 낮고 역전압 인가 시 누설전류가 많은 담점이 있으며, 이를 극복하기 위해 JBS와 MPS 다이오드가 개발되었으나, 이를 위한 Implant 공정과 High Temperature Annealing공정이 필요하여 소자 재작에 어려움이 있다. 본 논문에서는 SiC SBD소자의 Schottky Metal을 SBH가 높은 Mo 물질을 사용 하여 이를 극복하였으며, 항복 전압을 담당하는 Edge Termination에 대하여 Schottky Metal(Mo)을 이용한 Floating Metal ring을 형성하는 방법으로 SiC SBD Edge Termination을 구성하였다. Mo Schottky metal을 사용한 Main metal과 Edge Termination역할을 하는 Floating Metal ring과의 항복전압을 Simulation 하여 분석 하였다

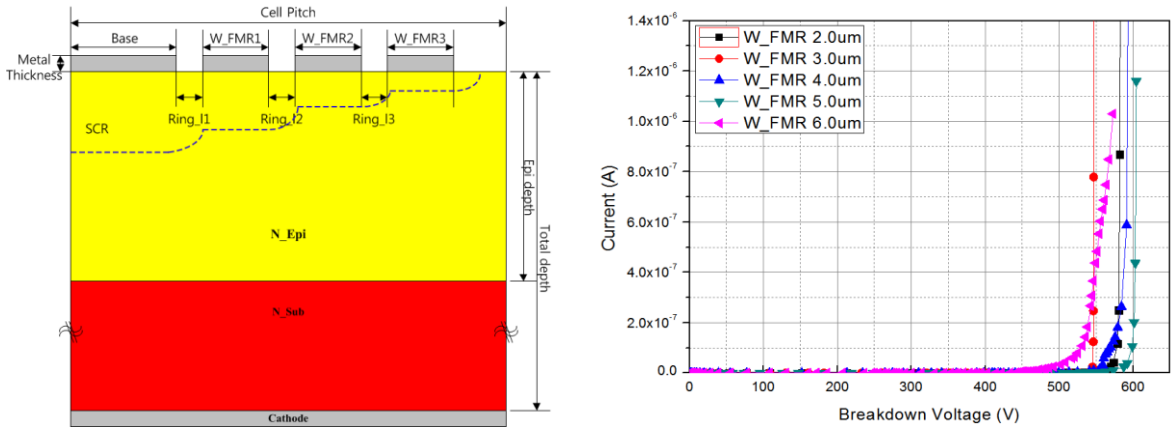

Fig 1. Sturcture of SiC Floating Metal ring and Breakdown voltage depending on FMR size

[1] B. J. Baliga, “Modern Power Device”, Wily, New York 1987.
[2] B. J. Baliga “Fundamentals of Power Semiconductor Devices”

GaN-based LEDs with subwavelength structures for enhanced extraction efficiency and uniform far-field patterns

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Light-emitting diodes (LEDs) have been widely used in many applications, such as the backlight for liquid-crystal display (LCD) and indoor/outdoor displays. These practical applications require high performance LEDs. However, the light extraction efficiency of LEDs is strongly limited by the internal reflection due to the high contrast of refractive index between LEDs and air. By using graded index layers, the internal Fresnel reflection can be significantly reduced. Since the subwavelength structure (SWS) with a conical profile can be considered as a homogeneous medium with a graded index, the SWS has excellent anti-reflection properties [1]. Thus, the SWS with a conical profile have been one of promising candidates for high-efficiency optical devices. While many researches have been reported on LEDs with SWS, there are only few reports on the theoretical modeling of SWS integrated LEDs. In order to apply high extraction efficiency LEDs on displays, far-field patterns of LEDs must be uniformly distributed. In this paper, we report results on the uniformity of far-field patterns for GaN-based LEDs with various periods. The simulation results and far-field patterns will be discussed.

* This work was partly supported by the KBSI grant (D34500) and by Basic Science Research Program through the NRF of Korea funded by the Ministry of Science, ICT & Future Planning (2014R1A1A1005945).

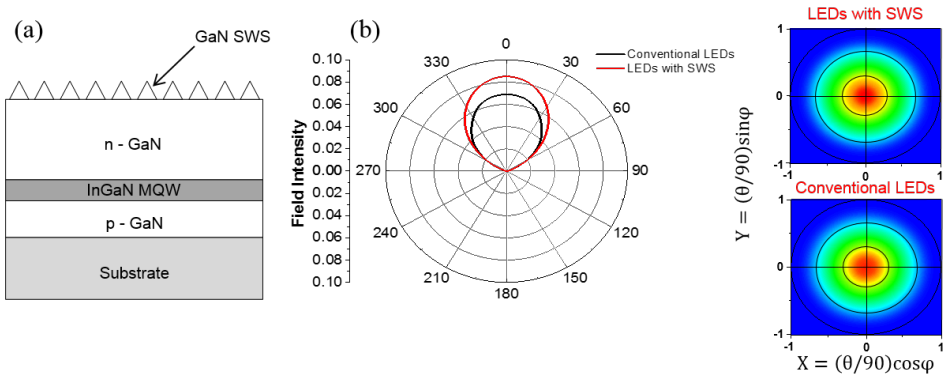

Fig 1 | (a) Illustration of GaN-based LED with SWS (b) Simulated far-field intensity and pattern

[1] Y. M. Song, E. S. Choi, G. C. Park, C. Y. Park, S. J. Jang and Y. T. Lee, Applied Physcis Letters 97(2010).

Extraction of Location and Energy Level of Oxide Trap Leading to Random Telegraph Noise in Gate-Induced Drain Leakage of p-MOSFET

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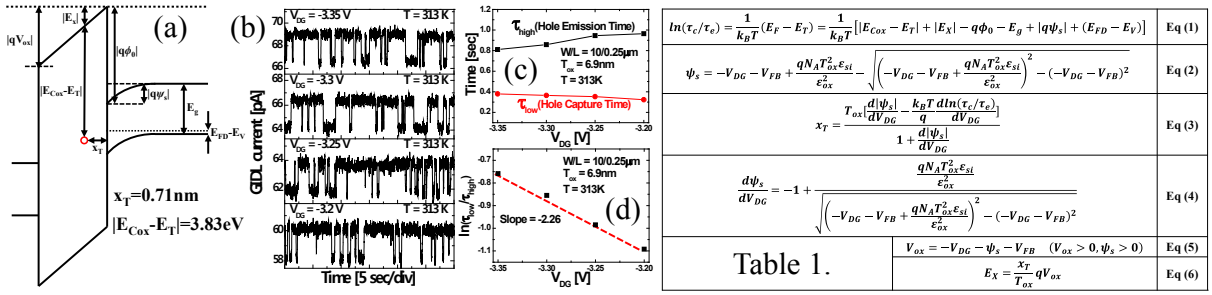
Until now, random telegraph noise (RTN) in the gate-induced drain leakage (GIDL) has been mainly researched in the n-MOSFET [1]. However, RTN of p-MOSFET should also be researched because RTN has large effects on the performance and reliability of CMOS devices [2]. In this paper, new equations are derived to obtain the vertical location and energy level of an oxide trap in gate/drain overlapped region that leads to RTN in GIDL of p-MOSFET. From Fig 1. (a), time constant ratio ($ln(\tau_c/\tau_e)$) of hole trapping is estimated in p-MOSFET as a function of bias as shown in Eq (1). By differentiating Eq (1) and Eq (2) with respect to V_{DG}, Eq (3) was obtained. As V_{DG} decreases, the Fermi level in gate/drain overlapped region moves relatively upward compared to the energy level of the oxide trap. As a result, hole capture time increases, whereas hole emission time decreases as shown in Fig 1. (c). The vertical location (x_T=0.71nm) and energy level (E_{Cox}-E_T=3.83eV) of the oxide trap were extracted by applying the measured results to the newly derived equations.

Acknowledge

This work is supported by Samsung Electronics Incorporation and Inter-university Semiconductor Research Center (ISRC).



$ln(\tau_c/\tau_e)=\frac{1}{k_BT}(E_F-E_T)=\frac{1}{k_BT}[\lvert E_{Cox}-E_T\rvert+\lvert E_X\rvert-q\phi_0-E_g+\lvert q\psi_s\rvert+(E_{FD}-E_V)]$		Eq (1)
$\psi_s=-V_{DG}-V_{FB}+\frac{qN_AT_{ox}^2\varepsilon_{si}}{\varepsilon_{ox}^2}-\sqrt{\left(-V_{DG}-V_{FB}+\frac{qN_AT_{ox}^2\varepsilon_{si}}{\varepsilon_{ox}^2}\right)^2-(-V_{DG}-V_{FB})^2}$		Eq (2)
$x_T=\frac{T_{ox}[\frac{d\lvert\psi_s\rvert}{dV_{DG}}-\frac{k_BT}{q}\frac{dln(\tau_c/\tau_e)}{dV_{DG}}]}{1+\frac{d\lvert\psi_s\rvert}{dV_{DG}}}$		Eq (3)
$\frac{d\psi_s}{dV_{DG}}=-1+\frac{\frac{qN_AT_{ox}^2\varepsilon_{si}}{\varepsilon_{ox}^2}}{\sqrt{\left(-V_{DG}-V_{FB}+\frac{qN_AT_{ox}^2\varepsilon_{si}}{\varepsilon_{ox}^2}\right)^2-(-V_{DG}-V_{FB})^2}}$		Eq (4)
Table 1.	$V_{ox}=-V_{DG}-\psi_s-V_{FB}\quad(V_{ox}>0,\psi_s>0)$	Eq (5)
	$E_X=\frac{x_T}{T_{ox}}qV_{ox}$	Eq (6)

Fig 1. (a) Energy band diagram of gate/drain overlap region, (b) RTN of p-MOSFET in time domain, (c) time constant and (d) time constant ratio according to V_{DG}.

[1] B. Oh, et al., IEEE Trans. Electron Devices, VOL. 58, NO. 6, pp. 1741-1747, June (2011).
[2] K. Ito, et al., IEEE IRPS, pp. 710-713, (2011).

The Comparison of Electrical Characteristics Between Nanoplate Fet and FinFET for 5 nm node Technology

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While the FinFET has been used as the FET beyond the planar MOSFET, a new type of FET is needed for the next generation. In this paper, we proposed the Nanoplate FET as the new device for sub-5 nm node technology and investigated the electrical characteristics of Nanoplate FET by comparing it with the FinFET in the same node. TCAD simulation [1] was used for analysis and the device specifications follow the ITRS 2013 [2]. Figure. 1 shows the structure of Nanoplate FET and FinFET, respectively. Both FETs have the same physical device size for accurate comparison. The effective channel length is 9.8 nm and threshold voltage is 0.447 V. Figure. 2 shows the transfer characteristics of Nanoplate FET and FinFET in the 5 nm node technology. Nanoplate FET shows better performance than FinFET in on current, SS (subthreshold swing), and DIBL (Drain Induced Barrier Lowering) due to the perfectly surrounded gate structure. Figure. 3 shows the mobility of both FETs extracted by the improved method based on Campbell method [3]. Nanoplate shows larger mobility than FinFET. These results show that Nanoplate FET is a promising FET beyond the FinFET for 5 nm node and below.

Acknowledgement

This work is supported by Samsung Electronics Incorporation and Inter-university Semiconductor Research Center (ISRC).

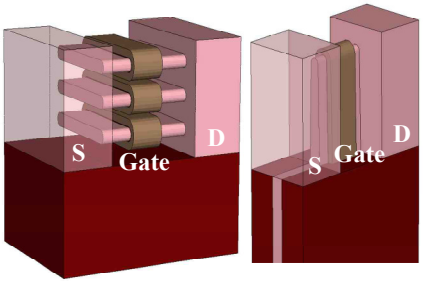

Figure 1. The structures of Nanoplate FET and FinFET

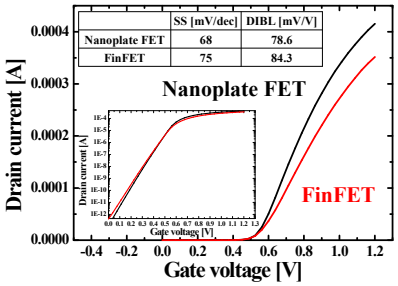

Figure 2. Comparison of the drain current in both FETs

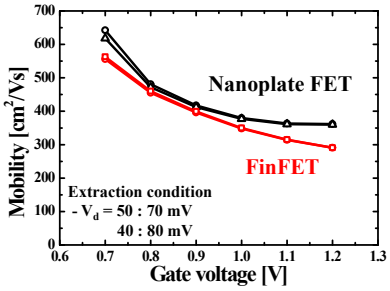

Figure 3. Mobility extraction

[1] Sentaurus (VL-2013.12), Synopsys
[2] The International Technology Roadmap for Semiconductors (ITRS), 2013. http://public.itrs.net
[3] J.P. Campbell, K. P. Cheung, J. S. Suehle, and A. Oates, IEEE EDL. Vol. 32, No. 8 (2011)

Investigation of Work-Function Variation for Germanium-Source Tunnel Field-Effect Transistor

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To alleviate the technical challenge of ever-increasing power density in CMOS devices, it is steep switching devices with high I_{ON}/I_{OFF} ratio of > 10^6 at low power supply voltage of 0.5 V or below that attracts much attention in industry. One of the steep switching devices, tunnel field-effect transistor (TFET), enables to surmount the physical limit of subthreshold slope (*i.e.*, SS = 60 mV/decade at room temperature) in conventional CMOS devices by exploiting not thermionic emission process but band-to-band tunneling (BTBT) process. However, the performance of TFET is not satisfactory for mobile consumer electronics. To boost up the performance of TFET, hetero-junction structures such as germanium-source TFET [1] are being adopted in TFET. In this study, the impact of random variation [particularly, work-function variation (WFV)] on high-κ/metal-gate Ge-source TFET is quantitatively evaluated, to see if the process-induced threshold voltage (V_{TH}) variation is marginal for mass production or not. It is noteworthy that a novel metric to evaluate the WFV-induced V_{TH} variation, RGG (ratio of grain size to gate area) [2], is used in this work.

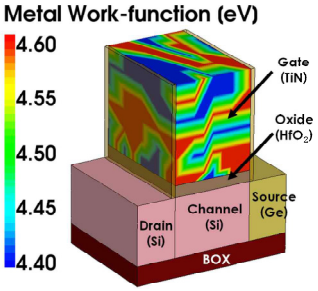

Fig. 1. 3-D bird's-eye view of Ge-source tunnel FET. Note that the grains in metal gate material are randomized.

Reference

[1] S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2009, pp. 178–179.

[2] H. Nam and C. Shin, "Study of high-k/metal-gate work-function variation using Rayleigh distribution," *IEEE Electron Devices Lett.,* vol. 34, no. 4, pp. 532-534, Apr. 2013.

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637).

Device design of P-N Tunneling Field-Effect Transistor based on AlGaSb/InGaAs Heterojunction

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In this work, we designed a nanowire vertical tunneling field-effect transistor (TFET) with AlGaSb/InGaAs heterojunction which consist a broken bandgap type by using device simulation ATLAS. The broken bandgap type structure by having thin tunneling barrier width can increase the probability of tunneling between source and channel region. Also, channel doping profile makes equally to concentration of the drain, it becomes p-n TFET consist of AlGaSb source, InGaAs channel and drain [1]. The channel region where the doping concentration is altered to equate it with the drain is n-type, but it is more specifically the intrinsic region. This is due to the nanowire, because gates surround the channel region in structure, gate controllability leads to the depletion of channel region. Fig. 1 shows proposed TFET achieves S is 19.5 mV/dec at V_{DS} = 0.1 V without change of on-state currnet (I_{on}). It has been confirmed that the proposed TFET have possibility by achieve steep S and high I_{on} for efficient switching operation.

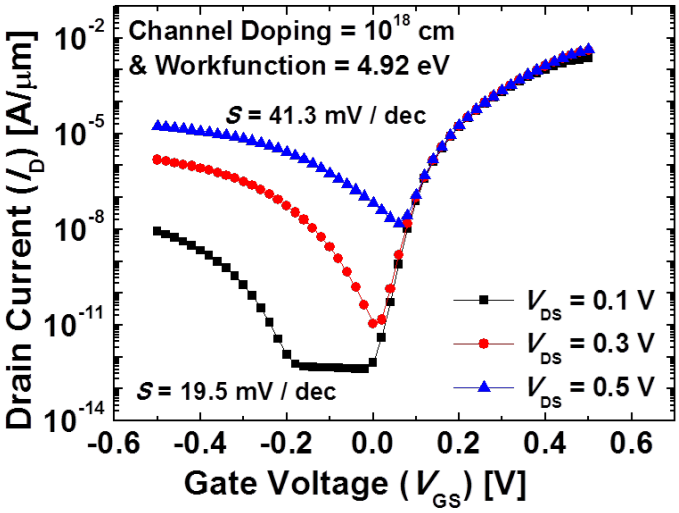

Fig 1. Transfer curve of proposed TFET with AlGaSb/InGaAs as function of drain voltage (V_{DS})

[1] A. W. Dey, B. M. Borg, B. Gangipour, M. Ek, K. A. Dick, E. Lind, C. Thelander, and L. E. Wernersson, *IEEE Electron Device Lett.* 34, 211(2013)

[2] SILVACO International, ATLAS User's Manual, 2012

Graphene Barristor 를 이용한 Ternary Inverter

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현존하는 전자처리 시스템은 이진법 체계를 사용하고 있는 데, 이는 MOSFET 과 같은 소자를 이용하여 0 과 1 을 구현하는 것이 매우 쉽기 때문이다. 삼진법(Ternary logic)은 정보를 0, 1, 2 세 가지로 표현하기 때문에 2 진법보다 적은 자리수로도 같은 정보를 표현할 수 있으며, 0 과 1 이외에도 2 가 있어 쉽게 음수를 표현할 수 있다는 장점이 있다. 그러나 삼진법을 용이하게 구현할 수 있는 전자소자가 없었기 때문에, 70 년대이후 사용되지 않고 있었지만, 최근 이진법기반 시스템의 복잡도가 증가하면서, 이를 단순화하여 소모전력을 절감하는 방안으로 삼진법기반 정보처리 시스템이 주목받게 되었다.

최근 Gate 단자에 전압을 걸어 Source 단의 Graphene 과 Drain 단의 Semiconductor 사이의 Schottky Barrier Height 를 조절하여 약 ~10^5 정도의 매우 큰 On/Off 비를 구현하는 Barristor 라는 소자가 발표된 바 있는 데 [1], 본 연구에서는 Barristor 의 문턱전압 크기 조절이 매우 용이하다는 점에 착안하여, Barristor 를 모사한 SPICE model 를 개발하고, 이를 이용하여 ternary inverter 를 설계한후 그 특성을 분석했다. 이때 V_{dd} 를 3V, V_{ss} 를 0V 로 설정했으며, 0, 1.5, 3V 가 각각 Ternary logic 값 0, 1, 2 를 의미하도록 회로를 구성했다. 2 개의 Noise margin 을 가지는 Binary inverter 와 달리 Ternary inverter 는 4 개의 Noise margin 을 가지는데 각각의 Noise margin 의 크기는 약 0.5V 로 균일하게 설계했다. 추가적으로 Diode logic 을 응용해 Ternary AND/OR 를 Barristor 로 설계했다. 이 연구에서 제시한 Ternary inverter, AND, OR 의 세가지 기본 Ternary logic 회로를 조합하면, 매우 큰 Ternary 정보처리 시스템도 설계할 수 있을 것으로 예상되며, 약 40%이상 획기적인 소자 수 절감이 가능하게 될 것이다.

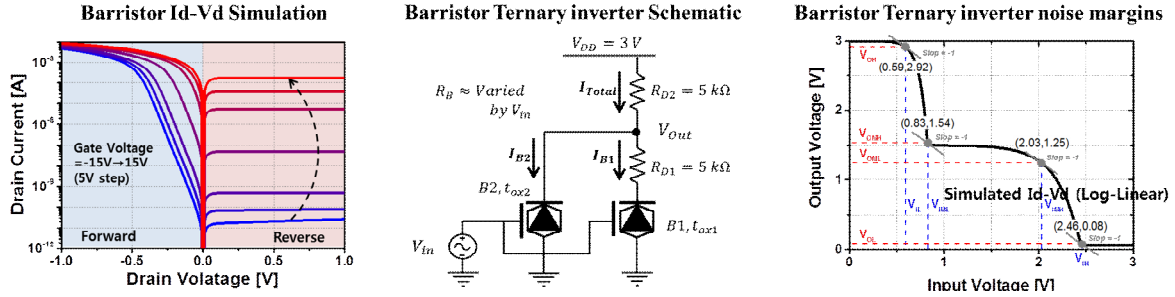

Figure 1 Barristor IV characteristics and Barristor Ternary inverter simulation result

Acknowledgments: This work was supported by the Future Semiconductor Device Technology Development Program (10044842) funded By MOTIE and KSRC(Korea Semiconductor Research Consortium and supported by the Global Frontier R&D Program (**2014043596**) on Center for Hybrid Interface Materials (HIM) funded by the Ministry of Science, ICT & Future Planning

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DIBL Suppression in Edge-Over Schottky Barrier Field Effect Transistor

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As the device size shrinks continuously by scaling in the current Si CMOS technology, the drain induced barrier lowering (DIBL) that is one of short channel effects and causes the increase of sub-threshold slope and leakage current become severe more and more in device operation. We propose a new device structure, edge-over Schottky barrier field effect transistor (SBFET), suppressing DIBL efficiently. Edge-over SBFET has a unique pillar structure where the transistor channel is elongated by going over the edge of pillar. Hence, an edge-over SBFET has a much longer channel compared with a planar FET with the same transistor pitch. The interfaces between a thin poly-silicon channel and Al electrodes (source and drain) form Schottky jucntions with small Schottky barriers < 0.2 eV. We performed 2-dimensional TCAD modeling on an edge-over SBFET with horizontal channel length of 5.5 nm and ultra-thin channel thickness of 2 nm. The TCAD modeling predicts subthreshold slope of ~71 mV/dec and OFF-state current of ~8 nA. It is also noticed that DIBL gets suppressed further as the pillar height increases.

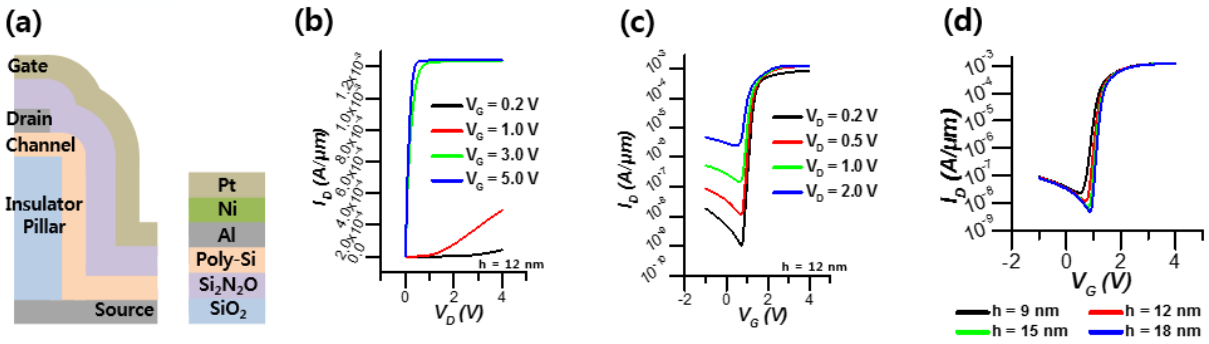

Figure 1. (a) The cross-sectional view of an edge-over SBFET device structure and its (b) I_D-V_D and (c) I_D-V_G characteristics when the pillar height is 12 nm. The pillar-height dependence of I_D-V_G characteristics with V_D = 0.5 V is also shown in (d).

Effects of oxygen adatoms on the atomic and electronic structures of various Ge surfaces by ab-initio study

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In recent years, with silicon-based field-effect transistor (FET) technology approaching its limits, semiconductor manufacturers have been searching for the non-silicon based materials that have high mobility charge carriers to replace the current silicon-based transistor channel [1]. Among various candidate materials, Ge has been attracting a lot of research interest due to its low band gap (0.67eV) and high carrier mobility [2]. However, the poor oxide properties have hindered the practical use of Ge. Therefore, controlling the quality of interface layer between germanium and gate dielectric will be critically important for application of Ge in new generation transistors.

In this study, we perform ab-initio calculation on the effects of oxygen adatoms on various Ge surfaces, such as (100), (110) and (111), as the properties of non-(100) surface become more important with the scaling-down of the devices. Based on our preliminary calculation on the reconstruction configuration of clean Ge surfaces, the atomic structures and electronic properties of Ge surfaces with the insertion of oxygen atoms are characterized. The bonding configurations of oxygen adsorption on Ge surface are revealed, and differences in electronic structure, such as local density of states (LDOS) and band structure around Fermi level, are specifically discussed. A detailed knowledge on the reaction of oxygen with Ge surface may provide the way toward a more effective next-generation switching device surface configuration.

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A Study of the effects of the surface roughness and temperature of magnetic tunnel junctions on resistance drift

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As magnetic tunnel junctions (MTJs) applied with Magnesium Oxide(MgO) as tunneling barriers have been extensively studied, now, the necessity of studies for more reliable MTJs is coming to the pore[1]. In particular, we have focused on the resistance drift according to the degree of surface roughness and changes in the temperature of buffer layers. To have different surface roughness conditions of buffer layers, we have made samples with different temperatures during deposition processes and with different annealing temperatures. To see the effects of temperatures on resistance drift, we have changed temperatures during interval stress tests. According to the results, samples with higher degrees of buffer layer roughness and higher temperatures showed higher resistance drift. In conclusion, magnetic tunnel junctions‘ resistance drift was shown to be very sensitive to surface roughness and temperatures. This study should be very helpful for understanding of magnetic tunnel junctions‘ degradation and resistance drift phenomena.

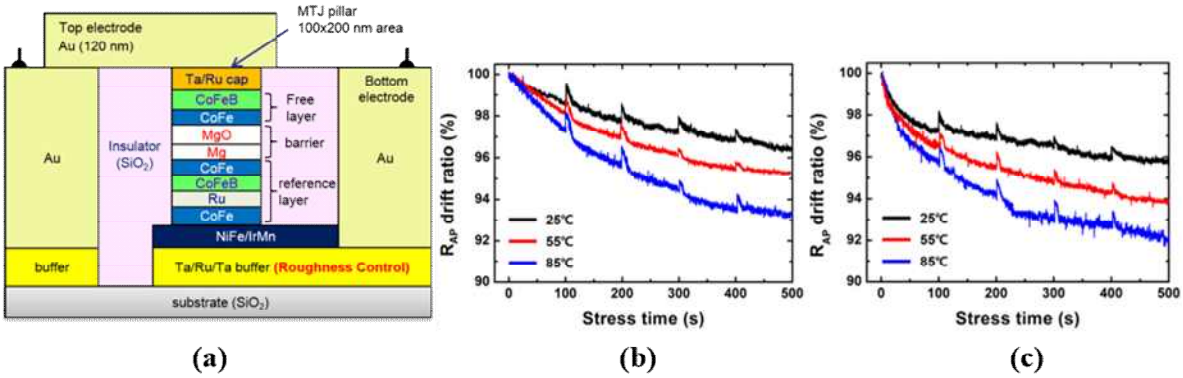

Fig 1. (a) Schematic of MgO barrier based MTJs made with different buffer layer roughness conditions. Interval Stress data of (b) Flat condition (c) Rough condition.

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Effect of stacking sequence on the electronic properties of layered MoS_2: Polytypism and heterostructure

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Molybdenum disulfide (MoS_2) is one of the promising channel materials for the next generation switching devices due to its low dimensional structure and possibility for the low power and high frequency operation [1][2]. This layer-structured material shows the polytypism depending on the stacking sequence (semiconducting 2H and 3R) of monolayer MoS_2 or local symmetry around a Mo atom (metallic 1T). Recently, it was revealed that the number of layers and the sequence of stacking have striking effects on the electronic properties, such as the indirect-direct band gap transition [3] and valley polarization [4][5]. In this study, we investigate the detailed atomic and electronic structures of MoS_2 polytypes by using density functional theory calculations including van der Waals interaction. The energetic stability of the stacking variants and corresponding perturbation of electronic structures are examined. Finally, we present the electronic structure of bi- and tri-layer heterostructure of MoS_2 and discuss the relation of the electronic structure and interlayer interactions.

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Effect of Program/Erase Cycling Stress on Reliability Properties in MONOS memory devices

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Recently, metal-oxide-nitride-oxide-semiconductor (MONOS) type based 3D-stacked NAND flash memories have been investigated as promising candidates for next-generation NAND flash memory. [1] However, there are some issues to be addressed such as instability of Program/Erase (P/E) window and degradation of retention time by electrical stress.[2] In this study, the effect of P/E cycling stress on performance of MONOS memory devices was investigated. The MONOS type capacitors were fabricated on p-type Si substrate. The gate stack consists of a 3-nm SiO_2 tunnel oxide layer, a 4-nm SiN charge trapping layer, and a 6-nm SiO_2/ 3-nm HfAlO (HA) blocking oxide bilayer. The memory window instability and retention time are monitored by changes of flat-band voltage with C-V curve. It is found that the slope of C-V curve decrease after erase bias cycling and the slope changes due to interface-state generation. MONOS erase occurs mainly through holes from the channel. Thus, hole injection is the main cause of the reliability degradation during P/E cycling.

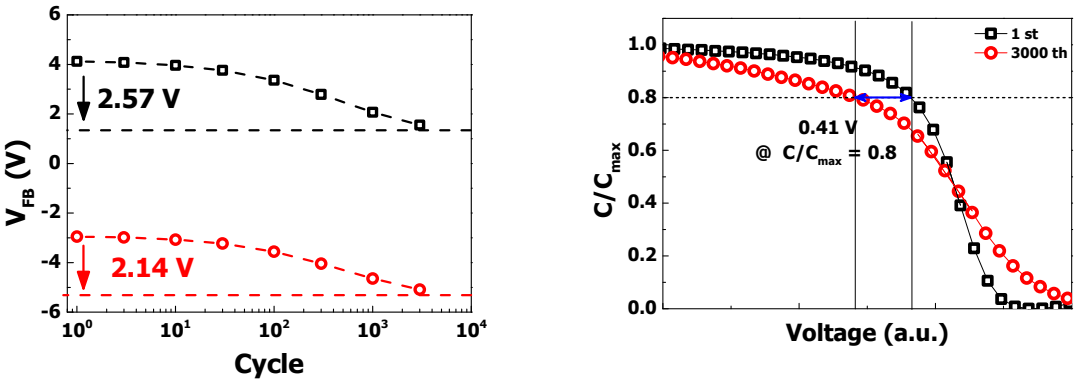

Fig 1. Endurance characteristics and C-V curve after erase cycling

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Border Trap Change of Solution Processed ZrO_2 Layer with Bias-Temperature Stress

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ZrO_2 has became promising gate dielectric instead of SiO_2 due to the scaling of the MOS device dimension.[1-2] In this work, the border trap change of solution processed ZrO_2 layer was characterized using capacitance-voltage (*C-V*) measurement with bias-temperature stress (BTS).[3] Solution processed ZrO_2 was stressed with an electric field of 0.5 MV/cm at 200 °C for 10 min to investigate effect of BTS in Figure 2. There is no notable change on ZrO_2 during the positive and negative bias stress at room temperature. However, in case of the BTS, V_{FB} shifted in the positive direction as +25 V. Especially border trap density was increased from $2.77x10^{10}$ to $3.5x10^{11}$ $v^{-1}cm^{-2}$ by measureing hysteresis curve after ZrO_2 layer was NBTS in Figure 3. Contrastively the change of the interface trap density was not huse increased from $1.88x10^{12}$ to $2.38x10^{12}$ $v^{-1}cm^{-2}$ with conductance method. From this result, high temperature can make enviroment to generate trap level in the bulk and then bias stress induced electron trapping at trap level generated in ZrO_2 layer. It is important role that ZrO_2 layer has negative charge type.

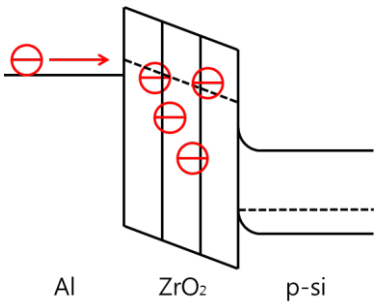

Fig 1. ZrO_2 layer structure

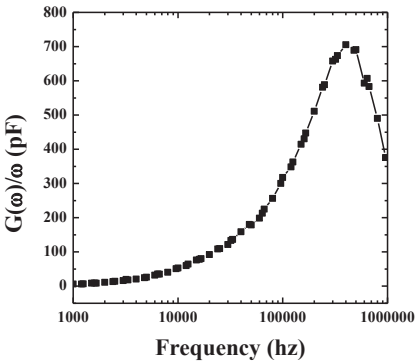

Fig 2. $G(\omega)/\omega$ versus ω for D_{it}

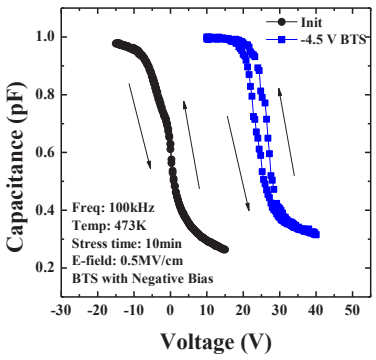

Fig 3. Hysteresis *C-V* curve

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A Study on Threshold Voltage Control of Lateral DMOS

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In this paper, we studied Vth(threshold voltage) behavior of LDMOS(Lateral Double diffused MOS) according to Pbody structure. The channel length of LDMOS is fixed by diffusivity difference between boron and arsenic implanted to channel region, about 0.2~0.3um.[Fig1] Although Pbody structure is changed, it's expected that LDMOS's Vth should not change except for the case thermal condition is changed. However, we confirmed various Pbody shapes like Pbody PR(Photo Resist), POA(Pbody Open Area) and Pbody overlay to gate can cause the change of Vth.

In the above experiments, Vth is decreased in condition of steeper PR slope and larger POA. From TCAD simulation, we confirmed the more PR slope is tilted, more boron atoms are transmitted through the inclined PR surface. Increased boron concentraion of the surface causes Vth shift.

We could also know the reason Vth is decreased as POA is increased is because of boron segregation during thermal gate oxidation through simulation. Boron concentraion along the channel direction is decreased in the larger POA after gate oxidation while boron amount is almost same regardless of POA before the oxidation process. It is generally known that the amount of out diffused impurity per unit area is constant if doped atoms per unit area is same. However, boron out diffusion was more dominant than arsenic when total amount of dose is increased. Finally, we could confirmed total amount of doping is also important to boron segregation and it causes Vth shift.

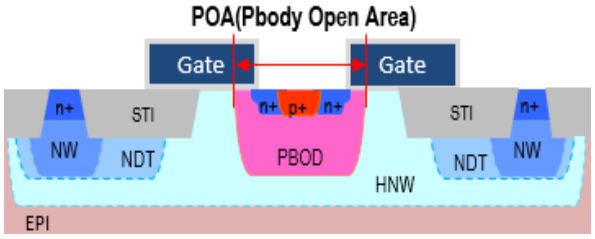

Fig1. LDMOS Structure

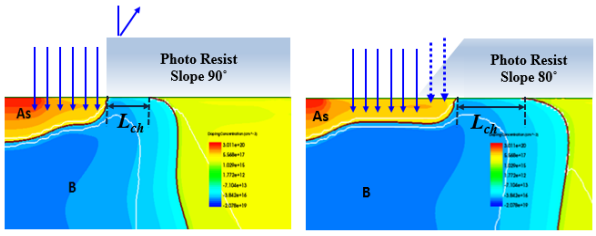

Fig2. Channel structure according to pbody slope

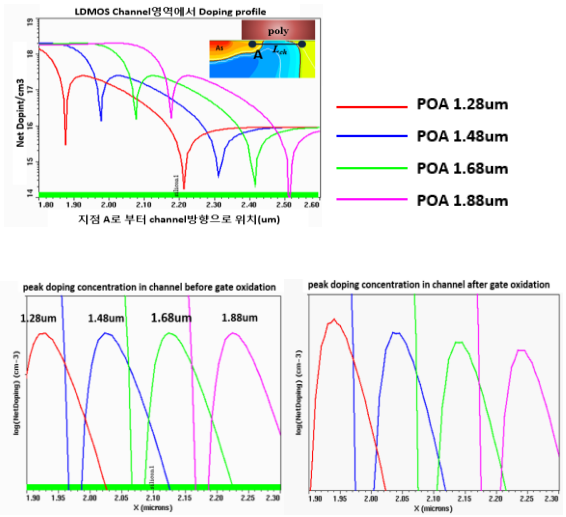

Fig3. (a) Doping profile in channel along the POA, zoomed peak concentration (b) before -, (c) after gate oxidation

Analysis of reliability for different device type in 65nm CMOS technology

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VLSI 시스템이 점차 소형화 되어감에 따라 고성능의 소자 특성뿐만 아니라, off −state 에서도 낮은 전력 소모까지 요구 되고 있다. 이를 위해 한 Chip 내에서 다중 문턱전압 CMOS(Multi− Threshold Voltage CMOS) 기술을 통해 높은 문턱 전압 (High threshold volage, HVT), 기준 문턱 전압 (Regular threshold voltage, RVT), 낮은 문턱 전압 (Low threshold voltage, LVT) 을 갖는 소자를 선택적으로 사용함으로써, 저전력 및 고성능 사양을 얻는 것이 주요 핵심 기술이 되고 있다. 따라서 한 wafer 에 다양한 문턱전압을 가지는 소자들을 구성하는 것이 필수화 되고 있어서, 같은 Technology 에서 다른 문턱전압을 갖는 소자들의 신뢰성 확보가 중요시 되고 있다. 0.18 μm 기술 이전의 소자에서는 CHC 보다 DAHC 에 의한 열화가 심했지만, 0.18 μm 이후 소자에서는 DAHC 보다 CHC stress 에서 열화가 커진다는 것으로 알려져 있다. [1]

그러나 본 논문에서는 제작된 LVT 와 HVT 소자 모두 DAHC 스트레스에서 열화가 더 심한 것을 볼 수 있었다. 이는 CHC 보다 DAHC stress 시에 Interface state generation 비율이 크기 때문에 DAHC stress 에 의한 열화가 심한 것이라 추측이 가능하다. 또한 Charge pumping 기술을 통해 두 소자 모두 DAHC 스트레스에서 더 많은 Interface trap 이 발생 되는 것을 확인 할 수 있었다.

Acknowledgment: 본 논문의 일부는 삼성전자의 지원으로 이루어졌음.

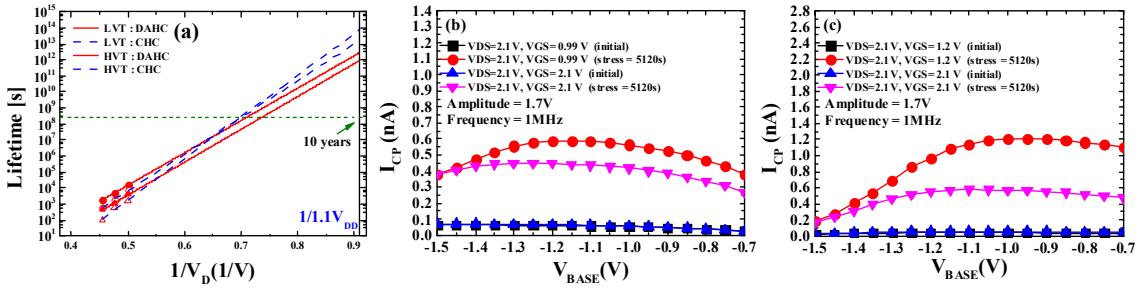

Fig. 1. (a) Extraction of hot carrier lifetime, and (b-c) increase of charge pumping current by channel hot carrier and drain avalanche hot carrier stresses.

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amorphous-Si TFT design 에 따른 Photo leakage 특성 분석

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Amorphous Si TFT 소자 design 에 따른 photo leakage 특성 확인 결과, 광 유입 부(W 광)의 길이에 따라 hole current 가 linear 하게 증가함을 확인하였고 특정 V_{GD} 이하에서는 hole current 가 saturation 되는 경향을 확인하였다. Photo current saturation 현상은 bottom light 인가 시, drain side 로 주입되는 유한한 과잉 hole carrier 에 의한 것으로 S/D-Gate overlap 면적이 증가할수록 saturation curent level 이 증가하는 것을 실험 및 TCAD simulation 을 이용하여 확인하였다.

또한 simulation 을 통해 active 두께를 감소함에 따라 photo leakage 는 감소하는 것을 확인하였다. Active 두께 감소는 수광 되는 반도체 전체 부피를 감소하게 되고 photo generation 에 의한 EHP(electron hole pair) 생성량도 감소시킨다. 결국 photo leakage 를 유발하는 hole 농도의 크기는 상대적으로 감소하게 되어 leakage current 가 감소하는 것으로 분석하였다.

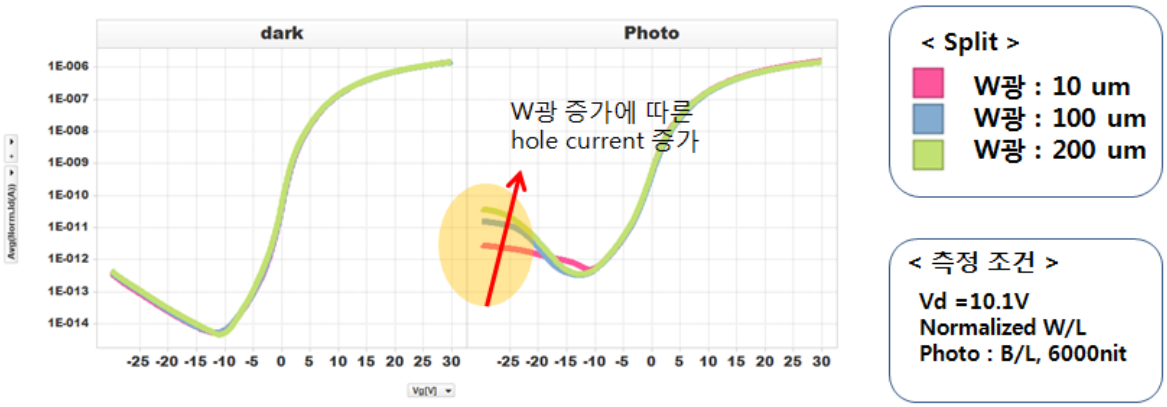

Figure.1. W 광 split 에 따른 Photo leakage 특성

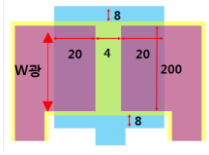

Figure.2. W 광 split 구조

Geometrical effect of silicon nanostructures on absorption efficiency

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Thin-film crystalline silicon (c-Si) solar cells are one of the promising candidates for low-cost photovoltaic applications because of commercially compatible mass-production processes. A way consists in the nanoscale patterning of the absorbing layer itself, which could then behave as a planar photonic crystal (PC). It was recently proposed to make use of surface addressable slow light mode in order to collect the incident light, and to couple it to waveguided slow light resonances that stand within the absorbing layer [1]. An alternative way is submicrometer grating (SMG) structures with a tapered feature for broadband and omnidirectional antireflections. While excellent antireflection properties of SMG structures have been demonstrated via reflectivity characterizations, thin-film c-Si solar cells integrated with SMGs are proposed for the enhancement of light absorption [2]. We report in this paper the light trapping characteristics of 2DPC which is composed of nanorod arrays for photovoltaics and quantitatively compare them to that of SMGs composed of parabola shape arrays. We change the shape gradually from rod to paraboloid and investigate the geometrical effect of silicon nanostructures on optical absorption efficiency. This study provides design guidelines for high-efficient thin film solar cells.

* This work was partly supported by the KBSI grant (D34500) and by Basic Science Research Program through the NRF funded by the Ministry of Science, ICT & Future Planning (2014R1A1A1005945).

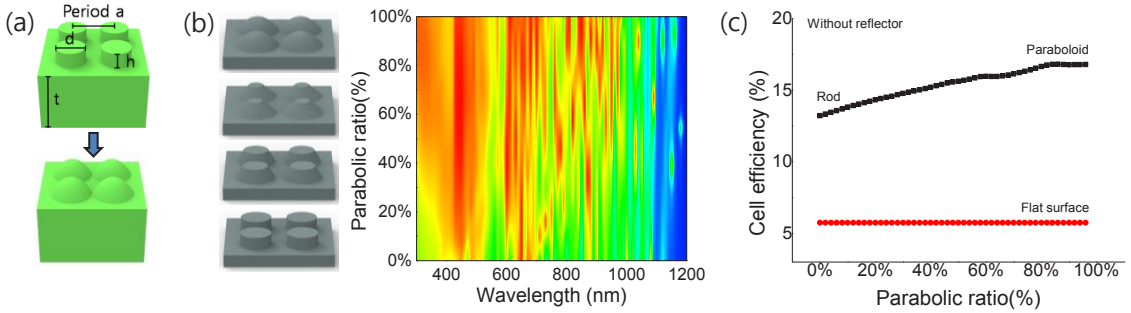

Fig 1. (a) Schematics of the c-Si thin film solar cells, (b) Contour plots of the absorption spectra of the c-Si thin film for the shape variation of the Rod to Paraboloid, (c) Calculated cell efficiency of thin-film c-Si solar cells with gradual change of shape from Rod to Paraboloid.

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Numerical analysis of the variation of the band-to-band tunneling current by acoustic waves effect

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On a heavily doped p-n diode, an electron of the valence band in a p-type region can transfer to the conduction band in a n-type region by tunneling, when a reverse voltage is applied.[1] In this tunneling of an electron, the potential barrier is determined by the energy band gap, and this energy bands can be shifted resulting from dilation of crystal.[2],[3] It means that the tunneling current of electron reflects this dilation of crystals. When there exist acoustic waves in the device, the dilation associated with the acoustical waves can also generate a shift of energy bands periodically in time. Consequently, the modulation of the tunneling current is caused by the harmonic perturbation of the potential barrier. The idea can be extended to the silicon junction detector for the acoustic wave.

We evaluate the variation of the tunneling current on strain associated acoustic waves. Firstly, the quantification of the relation between strain and the energy shift can be done with deformation potentials.[3],[4] And, by using Kane's model, we estimate the harmonic tunneling current resulting from the energy band shift. With this study, we can anticipate the convergence of acoustic and silicon devices.

Acknowledgement: This work was partly supported by the IT R&D program of MOTIE/KEIT[10049162] and the Brain Korea 21 Plus Project in 2014.

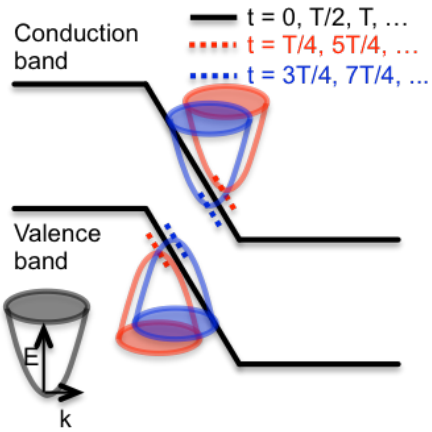

Figure 1. band diagram of p-n diode when there are acoustic waves with period T.

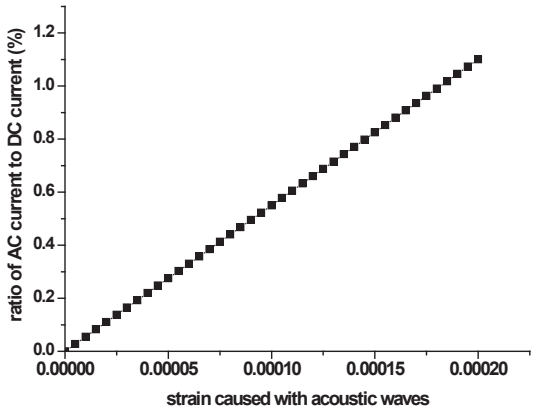

Figure 2 . ratio of AC current to DC current at 3V reverse bias. the dopping concentration is about 1E19[cm-3]. The direction of acoustic waves propagation is [k00] and tunneling direction is [100].

[1] E.O.Kane, J.Appl.Phys.32, 83 (1961).
[2] J.Bardeen and W.Shockley, Phys.Rev.80, 72 (1950).
[3] M.V.Fischetti and S.E.Laux, J.Appl.Phys.80, 2234 (1996).
[4] Chris G. Van de Walle, Richard M. Martin, Phys.Rev.B.34, 5621 (1986).

ReRAM Crossbar Array: Reduction of Access Time by Reducing Parasitic Capacitance of Selector Device

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Resistive Random Access Memory (ReRAM) is one of the most promising devices for nonvolatile memory application [1]. As technology nodes shrink continuously, the effort to increase the density of memory has been continued. Crossbar array architecture is expected to show best performance among various 3D stacking technologies. However, theoretical investigations are insufficient for parasitic capacitance of selector devices or resistors. In this research, the crossbar array architecture is consisted of selector and resistor (1S+1R cell architecture) for ReRAM as shown in Fig.1. Transient simulation was carried out using HSPICE and the read access time was measured for various parasitic capacitances and array sizes. As the magnitude of parasitic capacitance and array size increases, the access time increases significantly as shown in Fig. 2. In comparison to the resistor, the selector capacitance exhibits more impact on access time because the high resistance of selector induces much larger RC delay. As the selector capacitance increases from 1 fF to 50 fF, the access time shows more than an order of magnitude increase. However, the access time does not increase as much as the case of selector for the change of resistor capacitance. Therefore, the reduction in parasitic capacitance of selector is more important for the fast operation of ReRAM.

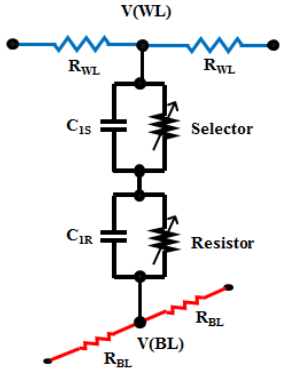

Fig. 1. The unit structure of crossbar array.

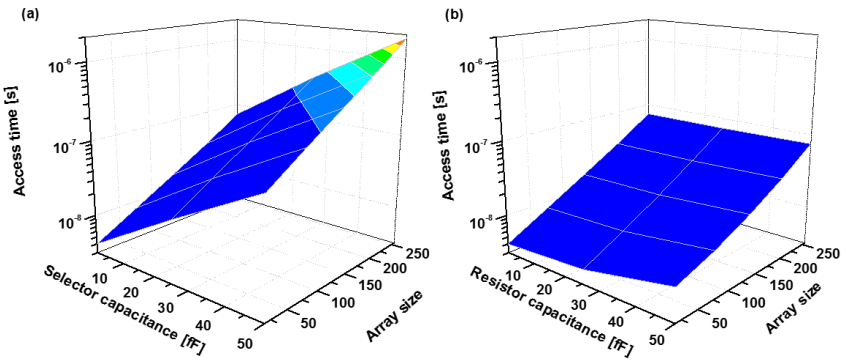

Fig. 2. The access time of target cell as functions of array size and (a) selector capacitance or (b) resistor capacitance.

[1] H. –S. P. Wong, H. Lee, S. Yu, Y. Chen, Y. Wu, P. Chen, B. Lee, F. T. Chen, and M. Tsai, *Proceedings of the IEEE*, vol. 100, No. 6, pp. 1951–1970, June 2012.

Analysis of read preferred SRAM bit-cells in 22nm FinFET technology

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V_{th} variation has been critical issue in VLSI circuit design. In FinFET technology, V_{th} variation is relieved by the lightly doped (or undoped) channel. However, SRAM bit-cell is very susceptible to V_{th} variation because it is designed with small transistor for high capacity. Thus, it is still challenging to achieve the enough read stability and write ability of SRAM. Read and write assist circuits are widely used to improve the read stability and write ability of SRAM. However, using both read and write assist circuits requires high circuit complexity. Therefore, it is attractive to apply only write (or read) assist circuit to read (or write) preferred bit-cell that has enough read stability (or write ability). In this study, we analyze various options to make read preferred bit-cell based on 22nm FinFET technology. The read stability of SRAM is proportional to pull-down (PD) to pass-gate (PG) strength ratio (β-ratio) and pull-up (PU) to PD strength ratio (ϒ-ratio). β-ratio can be improved by increasing the fin number of PD, and ϒ-ratio can be improved by increasing the fin number of PU or NFET V_{th}, or by decreasing PFET $|V_{th}|$. Reducing fin thickness also improves read stability because DIBL is suppressed [1]. To achieve 6σ read stability yield, 5 fins of PU are required causing large area overhead. On the other hand, only 2 fins of PD are enough to achieve 6σ read stabiltiy yield because β-ratio is more dominant than ϒ-ratio for read stability. Decreasing PFET $|V_{th}|$ causes large standby leakage because leakage is exponentially related to V_{th}. On the other hand, by increasing NFET V_{th}, 6σ read stability yield can be achieved without leakage increase although read delay is increased somewhat. 6σ read stability yield is not achieved by reducing the fin thickness because there is limitation in reducing the fin thickness. Consequently, read preferred SRAM bit-cell can be made by increasing the fin number of PD or NFET V_{th}.

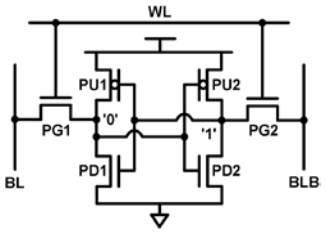

Fig. 1. SRAM bit-cell

Options	Note
PU fin number ↑	Large area overhead
PD fin number ↑	Proper for high performance
PFET $\|V_{th}\|$ ↓	Large leakage current
NFET V_{th} ↓	Proper for high density
Fin thickness ↓	Cannot achieve 6σ read stability yield

Fig. 2. Options for read preferred FinFET SRAM bit-cell

[1] M. Kang, S. C. Song, S. H. Woo, H. K. Park, M. H. Abu-Rahma, L. Ge, B. M. Han, J. Wang, G. Yeap, S. O. Jung, IEEE Trans. Electron Devices, 57, (2010), 2785.

Illumination effect on the nonvolatile memory device based on a-InGaZnO thin-film transistors with Ag nanoparticle storage

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NAND flash memory는 비휘발성, 낮은 소비전력, 간단한 입출력 등의 장점들로 인해 핸드폰, MP3, 디지털 카메라, USB 와 같은 전자 기기의 주요 소자로 많이 이용된다. 특히, 최근에는 smart watch, wearable device 와 같은 차세대 디스플레이 소자에 대한 관심이 증가하면서 투명하고 유연한 메모리 소자에 대한 연구가 진행되고 있다. 기존 실리콘 기반의 메모리 소자는 광학적으로 투명하지 않고 또한 고온의 열처리 공정 때문에 플라스틱과 같은 저온 공정이 요구되는 기판에서는 사용이 제한되며, 이를 극복하기 위해 실리콘을 대체할 수 있는 산화물 기반 기술이 연구되고 있다[1]. 최근, 금속 나노 입자를 플로팅 게이트로 이용하는 차세대 비휘발성 메모리 소자에 대한 연구가 많이 보고되고 있으며 charge trapping 확률을 높임과 동시에 메모리 윈도우 조절이 용이하다는 장점을 가지고 있지만, charge 들이 충분히 detrap 되지 않는다는 문제점도 있다[2]. 따라서, 본 연구에서는 이러한 문제점을 극복하고 System-on-pannel (SoP)에도 적용이 가능하도록 Ag nanoparticles (NPs)를 산화물 TFT 에 적용하였고, 빛을 이용한 소거방법으로 detrap 효과가 극대화되는 비휘발성 메모리 소자를 제작하였다 [그림 1(a)]. 소거 과정에서 IGZO 채널 층의 oxygen vacancy 들이 빛에 의하여 이온화가 촉진되며, 이때 생성된 정공들이 터널링에 의하여 Ag NPs 에 trap 된 전자들과 재결합하여 소멸된다 [그림 (b)]. 결과적으로, 간단한 구조의 a-IGZO TFT 에 Ag NPs 를 storage 로 적용하여 빛 조사를 이용함으로써 메모리 특성의 향상을 달성하였고, 향후의 SoP 에 매우 유망한 비휘발성 메모리 기술을 확보할 수 있었다.

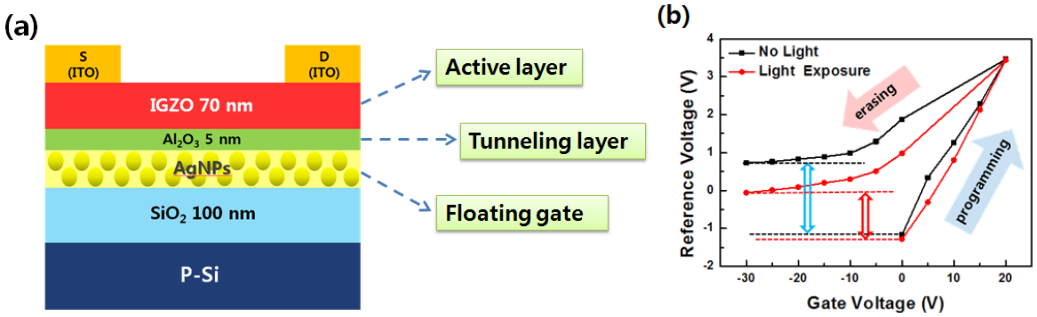

Fig 1. (a) Schematic structure of device. (b) P/E operation under dark and illumination condition.

[1] D. Gupta et al., Appl. Phys. Lett., Dec. (2008)
[2] Z. Liu et al., *IEEE* Trans. Electron Devices, (2002).

Resistive switching characteristics in HfO_x - PMMA blend Thin-film

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용액공정을 이용한 Resistive random access memory (ReRAM)는 간단한 공정과정, 대면적화, 저렴한 공정단가 등의 장점으로 최근 많은 주목을 받고 있으며, HfO_x, TiO_x, AlO_x 등의 산화물이 ReRAM 절연막으로 주로 연구되고 있다[1]. 최근에는 유연성이 뛰어난 organic 물질을 메모리 소자로 사용한 wearable 또는 flexible system에 관한 연구도 증가하고 있다. 그러나 organic 재료는 산화물과 같은 inorganic 재료에 비해 열에 취약하며, 소자의 신뢰성과 전기적인 특성이 뒤떨어진다는 단점이 있다 [2].

따라서, 본 연구에서는 organic과 inorganic 재료들이 가진 각각의 장점을 활용하기 위하여 polymethylmethacrylate (PMMA) 용액과 HfO_x 프리커서 용액을 혼합한 후 spin coating 방식으로 형성된 절연막을 이용하여 메모리 소자를 제작하였다. 이렇게 제작한 메모리 소자는 organic 물질인 PMMA의 전기적 특성을 개선시킬 뿐 아니라, HfO_x를 유연한 기판에 적용했을 때 발생하는 기계적·물리적 결함을 해소할 수 있는 방법이다. 제작된 메모리 소자는 높은 투과도와 유연성을 가지면서도 3 V이하의 낮은 동작 전압과 뛰어난 endurance 특성을 가지는 것을 확인하였다. 결론적으로 HfO_x - PMMA blend thin film을 갖는 ReRAM 소자는 organic 소자와 inorganic 소자의 장점을 가지면서도 wearable 및 flexible system용 비휘발성 메모리 소자에 적용이 가능한 경제적인 기술로 판단된다.

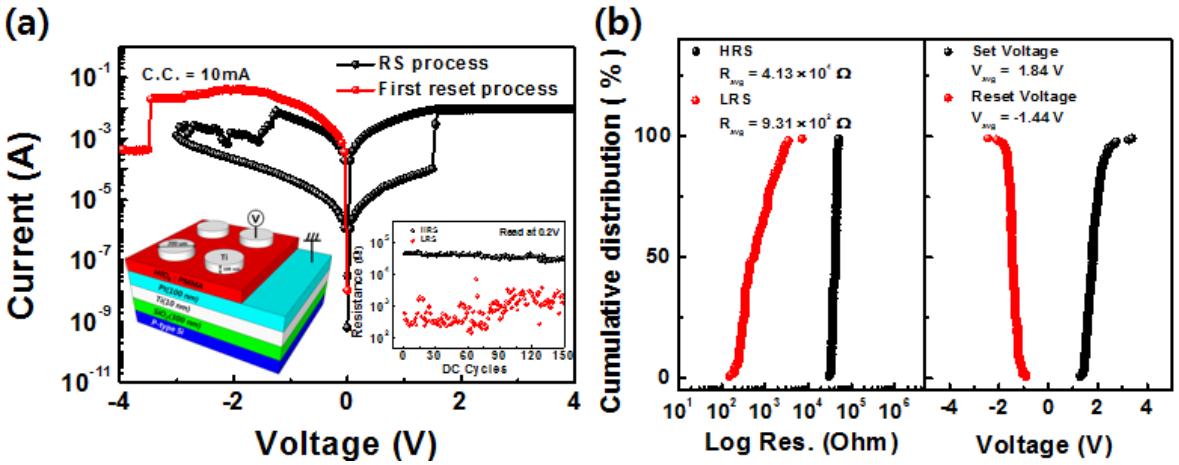

그림 1. (a) HfO_x - PMMA blend thin film 을 갖는 ReRAM 의 소자 구조, 스위칭 및 DC endurance (inset) 특성. (b) 저항 및 전압 분포.

[1]] N. Gergel-Hackett et al., IEEE Electron Device Lett. 30 (2009) 706–708

[2]L. P. Ma et al., Appl. Phys. Lett. 80, 362 (2002)

Resistive switching in Ta_2O_5/IGZO double layer for System on Panel applications

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Nowadays, In-Ga-Zn-O thin film transistors (TFTs) have attracted to a promising candidate for intergrated devices of a system-on-panel (SOP) applications. The SOP concept proposed to enable various device, not only control devices, but also non-volatile memory devices, such as resistive switching random access memory (ReRAM), integrated on a sigle panel. There are some key aspect that these active layer of TFTs and the resistive switching layer of ReRAMs are fabricated with the same material and similar processes for the SOP technology integration [1].

In this paper, we demonstrated the resistive switching characteristics of Ta_2O_5/InGaZnO double layer using the Ti/Ta_2O_5/InGaZnO/Pt structure. To optimize the thickness of Ta_2O_5 layer, the different thickness of Ta_2O_5 devices were fabraicated and evaluated for resistive switching operations.

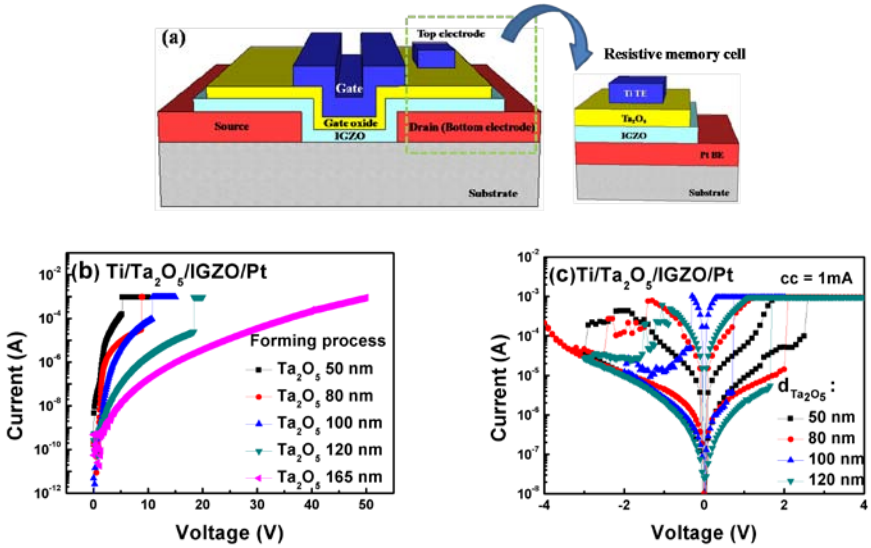

Fig 1. (a) Schematic diagram of one ReRAM cell and (b) forming process, (c) *I-V* hysteresis.

[1] Y. Nakajima, Y. Kida, M. Murase, Y. Toyoshima, and Y.Maki, Journal of the Society for Information Display, 12(4), 361 (2004).

Acknowledgement: This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education, Science and Technology(NRF-2010-0024000)

Asymmetric bipolar resistive switching in a $Pt/Ta_2O_5/ZrO_2/TiN$ Structure

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전이금속 산화물 기반의 저항변화메모리(ReRAM) 소자는 외부에서 전압을 인가하여 저항 상태를 가역적으로 바꿀 수 있는 현상을 적용한 차세대 비휘발성 메모리이다. Crossbar 구조의 ReRAM 에서는 인접 cell 로부터의 sneak current 를 막을 수 있는 diode 등의 selector 가 필요하다. 그러나 selector device 는 cell performance, integration density, scalability 측면에서 제한을 주므로 메모리 소자가 자체적으로 selector 역할을 하는 self-rectifying 거동이 주목 받고 있다[1-2]. 본 연구에서는 비대칭적인 barrier 를 형성하기 위해 $Pt/Ta_2O_5/ZrO_2/TiN$ 적층 구조의 ReRAM 소자를 제작하였다. Forming process 이후에 bipolar swicthing 을 관찰할 수 있었고 [그림 1]과 같이 ReRAM 소자의 저저항 상태가 전압이 인가되는 방향에 따라 비대칭적인 rectification 특성을 관찰할 수 있었다. 이는 Pt/Ta_2O_5 계면과 ZrO_2/TiN 계면의 barrier height 이 서로 다르기 때문으로 생각된다. ZrO_2 10nm, Ta_2O_5 5nm 를 적층한 소자의 경우 3V reading voltage 에서 On/Off ratio~10^2, rectification ratio~10^3 의 저항변화 특성을 확보할 수 있었다. 각 switching layer 의 물리 화학적 특성에 따른 저항변화현상을 관찰하기 위해 각 층의 두께와 공정 변수를 조절해 저항변화특성의 최적화를 모색하고자 한다.

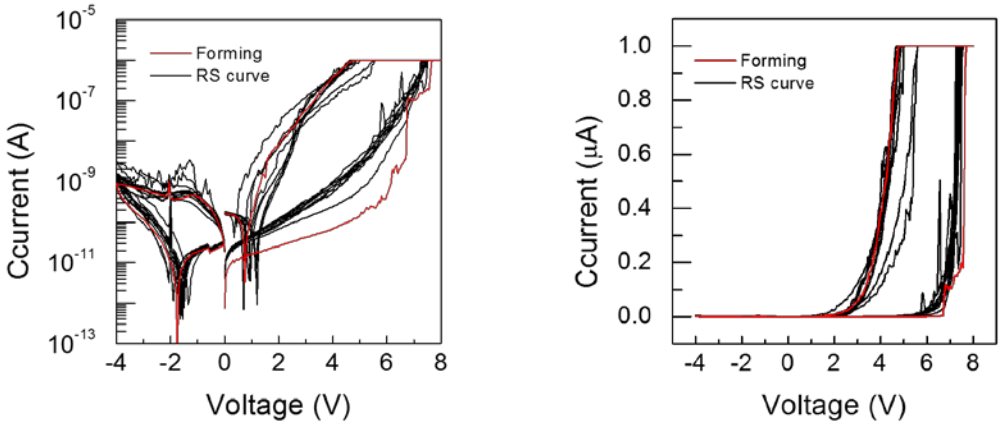

그림 1. Pt/Ta_2O_5 (5nm)/ZrO_2 (10nm)/TiN 구조에서 저항 변화 I-V 특성

[1] Jung Ho Yoon, et al., Adv. Funct. Mater., 2014, 24, 5086–5095
[2] Hangbing Lv, et al., IEEE Electron Device Letters, 2013, 34, 229-231

Effect of physical/chemical characteristics of electrolyte on the cation migration in Electro-Chemical Metallization cell

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ECM (Electrochemical metallization switching) 효과에 기인한 저항 변화 메모리는 set 전압을 인가했을 때 산화 전극에서 발생한 양이온이 전해질을 통해 이동하여 환원 전극과 전해질 사이의 계면에서 환원되는 전기 화학적 방법에 의거하여 필라멘트가 형성되고, 전압의 방향을 바꿨을 때 발생하는 reset은 산화전극과 전해질의 계면에서 산화 반응이 일어나 필라멘트가 용해되는 방식으로 작동되는 것으로 알려져 왔다. 그러나 최근 계면에서의 산화환원에 의한 필라멘트의 생성뿐 아니라 전해질 내 양이온의 이동도와 산화환원 반응 속도에 따라 필라멘트의 성장 양상이 달라지는 현상들 또한 새로이 보고되었다. [1][2] 이러한 필라멘트의 성장방향 및 그 모양의 차이는 set 과정 이 후의 reset 거동에의 차이로 이어진다. 본 연구에서는 reset 과정에서 필라멘트의 모양에 따라 달라지는 전계 및 줄열 효과에 주안점을 두고 reset 시 전기적 거동을 바탕으로 필라멘트의 성장 및 소멸 거동에 대해 간접적으로 추적하고자 한다. 이에 더하여, 필라멘트 성장 및 소멸 거동을 직접적으로 관찰하기 위해 [그림 1]과 같은 Cu/TiO_2/Pt 평면 소자를 제작하여 SET 과정에서의 필라멘트 모양을 시간에 따라 ex-situ SEM으로 관찰하기로 한다. 또한 RF 반응성 스퍼터를 이용한 TiO_2 전해질의 물리적, 화학적 특성 변화에 따른 관찰로부터 set 과정에 기여하는 소자 내 전계 및 전류의 효과와 더불어, 전해질의 두께, 밀도, 조성 및 밴드 구조 특성에 기인한 양이온의 이동도 및 전자의 유입 속도에 의해 총괄되는 필라멘트의 성장 메커니즘에 대해 평가하기로 한다.

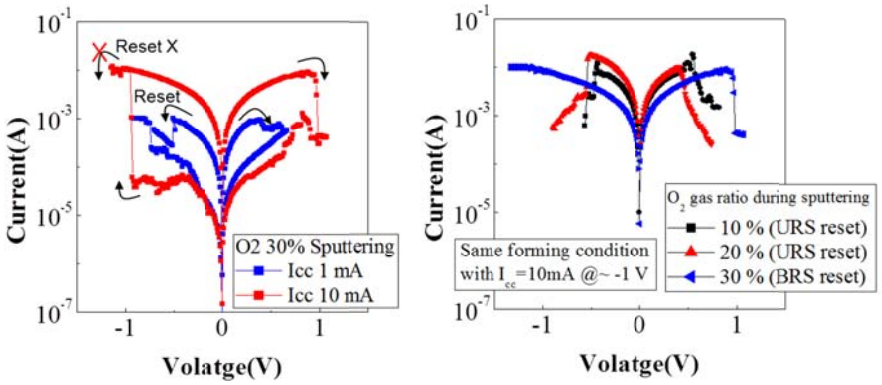

그림 1. (좌) Compliance current에 따른 RS 동작 모드의 변화 (URS at 1 mA, BRS at 10 mA), (우) 스퍼터 증착 시 산소 분율에 기인한 TiO2 전해질의 reset I-V 거동 차이 (forming 조건 모두 동일 Icc=10 mA, voltage ~-1V)

[1] Yang, Yuchao, et al. "Observation of conducting filament growth in nanoscale resistive memories." *Nature communications* 3 (2012): 732.

[2] Yang, Yuchao, et al. "Electrochemical dynamics of nanoscale metallic inclusions in dielectrics." *Nature communications* 5 (2014).

A PRAM-aware Modification of Linux Operating System

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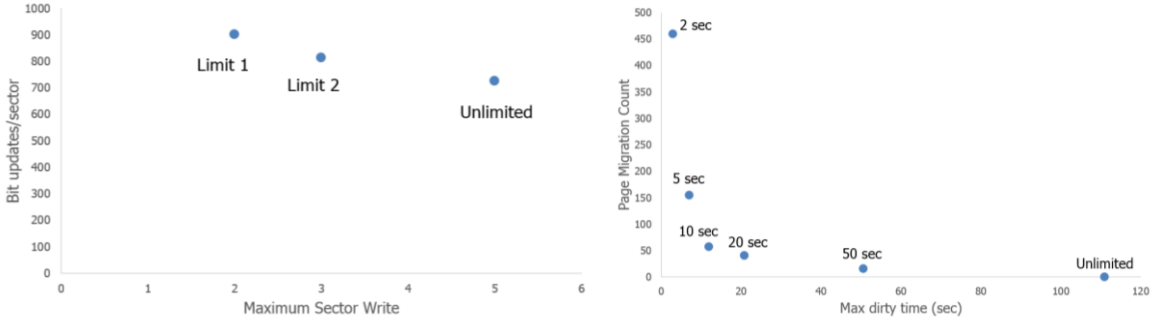
PRAM 은 집적 한계에 다다른 DRAM 을 대체할 수 있는 소자로 연구되고 있다. 소자 크기가 작아질수록 신뢰성과 전력 면에서 문제가 커지는 DRAM 과 달리 PRAM 은 DRAM 대비 더 나은 집적능력을 제공하고, 비휘발성이면서도 바이트 단위로 접근이 가능한 특성을 지녀 다양한 분야에서 연구되고 있다[1]. 본 연구에서는 PRAM 을 swap memory 와 page cache 로 사용할 수 있는 가능성에 대해 실험해 보았다. 특히 PRAM 이 제공하는 differential write 기능을 소프트웨어에서 최대한 활용하는 가능성 및 이에 따라 유발되는 문제점에 대한 솔루션에 대해 실험하였다. 소프트웨어에서 differential write 를 이용하기 위해서는 데이터 블록을 재활용하는 것이 필요하다. 이러한 자원재활용을 통해 기존 데이터와 새 데이터 사이의 상관관계를 최대한 활용하여 PRAM 에 대한 bit update 를 최소화할 수 있다. 이러한 자원 재사용을 통한 bit update 감소는 반대로 특성 PRAM cell 에 쓰기가 집중되는 문제를 야기할 수 있다. 따라서, 쓰기 수명에 한계가 있는 PRAM 을 위해 wear-leveling 을 통해 수명을 조절할 필요가 있다. 우선, Linux 커널의 분석을 통해 swap memory 와 page cache 의 구현이 differential write 를 최대화시키는 형태로, 즉, 기존 자원을 재사용하는 방식으로 이미 구현되어 있다는 것을 확인하였다. 따라서, wear-leveling 을 통해 쓰기 수명을 향상시키기 위해, 자원 재사용의 횟수를 제한하도록 하여, 아래 그림과 같이 최대 재사용횟수 임계값(그림 (a)에서 Limit, 그림 (b)에서 max dirty time)을 변화시키면서 수명과 PRAM 쓰기량 간의 trade-off 관계를 얻을 수 있었다.



(a) Swap memory on PRAM (b) Page cache on PRAM

그림 1. 수명(x 축에 반비례)과 PRAM 쓰기량(y 축)의 관계

[1] G. H. Koh, et al., "PRAM process technology," Proc. International Conference on Integrated Circuit Design and Technology (ICICDT), 2004.

Pt/SiN_x/Pt and TiN/SiN_x/Pt for ReRAM device

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In this paper, resistive switching (RS) properties of plasma enhanced chemical vapor deposited silicon-nitride (SiN_x) thin film deposited on Pt and TiN substrates are reported. After deposition of SiN_x thin film, Pt dot pattern is deposited as top electrode to make MIM structure. Auger electron spectroscopy (AES) data shows low impurity level in SiN_x thin film and ~ 3:2 atomic ratio of Si and N. Pt/SiN_x/Pt device showed unipolar resistive switching (URS) and TiN(BE)/SiN_x/Pt(TE) device shows bipolar resistive switching (BRS) behaviors. The origin of different type of RS operation is due to the difference of work function between top and bottom electrode, Pt(~5.2eV) and TiN(3.5~4.4eV). Pt/SiN_x/Pt device shows unstable RS showing the unfavorable overlap of set and reset voltages. In contrast, TiN/SiN_x/Pt device shows stable BRS behavior having -1V set voltage and 2V reset voltage. It is believed that trap and detrap of electrons in SiN_x are responsible for the RS.[1] By optimization of growth process and film thickness, it is expected to achieve excellent RS property from SiN_x thin film.

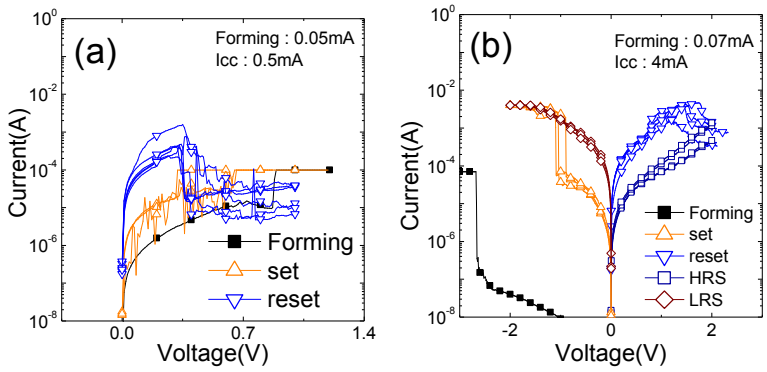

Figure 1. I-V characteristic of (a) Pt/SiN/Pt device and (b) TiN/SiN/Pt device showing URS and BRS behavior, respectively

[1] D. H. Li, Y. Kim, G. S. Lee, D.-H. Kim, J. H. Lee and B.-G. Park, "Charge Trapping and Memory Behaviors of the UltraThin SiN Layer", AIP Conference Proceedings, vol. 1399, 2011

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Doping Effect in Space Region of 16 nm NAND Flash Memory Cell String

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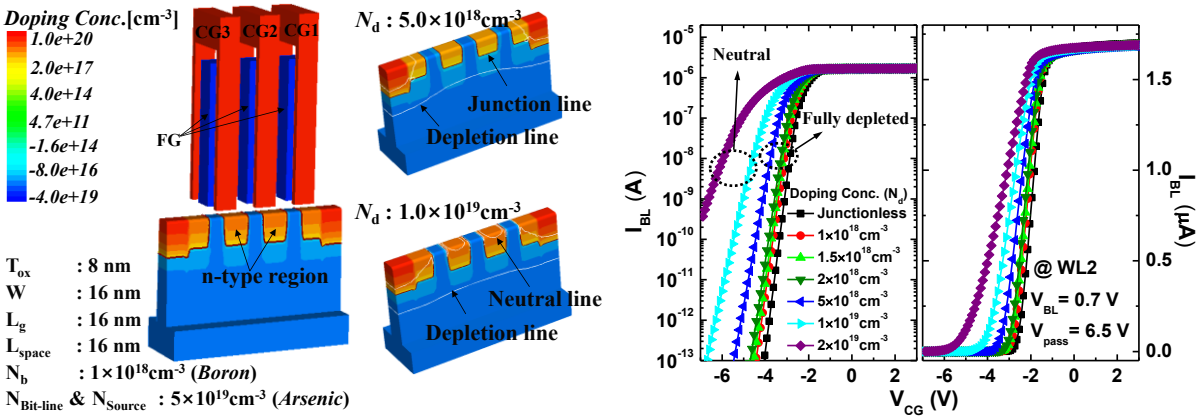
Recently, NAND flash memory faces critical scaling barriers such as cell V_{th} distribution influenced by floating-gate (FG)-coupling interference at the 40-nm node and beyond [1]. To improve V_{th} distribution of cells, NAND flash memory cell string without neutral source/drain regions in the sapce region between adjacent cells has been reported [2]. Although the doping in the space region is very imporant in V_{th}, short channel effect, and V_{th} distribution beyond ~20 nm technology node, however, the quantitative analysis of the doping in the space region V_{th} has not been reported. In this paper, we investigate various properties including I_{BL}-V_{CG} characteristics as a parameter of peak n-type counter-doping concentration (N_d) in the space region of 16 nm NAND flash memory using TCAD tool: Sentaurus Synopsys. Fig.1 (a) shows simplified 3-D structure of a cell string at 16 nm node, depletion region in the string with the N_ds of 5×10^{18} cm^{-3} and 1×10^{19} cm^{-3} at equilibrium. Here, the body doping (N_b) is uniform (1×10^{18} cm^{-3}) and the junction depth of the n-type region is 30 nm. As shown in Fig. 1(a), the n-type region with the N_d of 5×10^{18} cm^{-3} is fully depeleted, while a part of the n-type region with the N_d of 1×10^{19} cm^{-3} remains as a neutral region. Fig. 1(b) shows I_{BL}-V_{CG} curves with several N_ds. For N_d larger than 2×10^{18} cm^{-3}, the sub-threshold swing (SS) starts to increase appreciably due to the punch-through. The SS for the N_d of 1×10^{19} cm^{-3} is ~430 mV/dec. Thus the N_d needs to be less than 5×10^{18} cm^{-3}, which is eqivalent to a implantation dose of ~4×10^{12} cm^{-2}, to enhance control-gate controllability over the space region.



(a) (b)

Fig 1. (a) 16 nm NAND flash memory structure with N_ds of 1×10^{19} cm^{-3} and 5×10^{18} cm^{-3} (b) I_{BL}-V_{CG} curve with accoding to variation of N_ds in n-type region

[1] K.-T. Park et al., IEEE Trans. on Electron Devices, vol. 55, no. 1, p.404, (2008)
[2] Y. M. Kim et al., Japanese Journal of Applied Physics, vol. 50, 114201, (2011)

Acknowledgments
This work was supported by the Brain Korea 21 Plus Project in 2014 and by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186)

Characterization and modeling of $Ge_2Sb_2Te_5$ crystallization time in phase change random access memory operation

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상변화메모리 (Phase change Random Access Memory; PRAM) 는 빠른 쓰기 (programming: set 및 reset) 특성을 가지는 비휘발성 메모리 중 하나이고, 차세대 메모리 및 뇌신경모방 (neuromorphic) 단위소자로의 응용 가능성이 큰 기술이다. 이 기술이 향후 보다 높은 경쟁력을 가지기 위해서는 reset 전류 감소, set 속도 증가 [1], 저항 드리프트 감소, 쓰기 내구성 개선 등의 해결 과제들이 중요하게 인식되고 있다. 본 연구에서는 set 속도 증가를 위해 주어진 소자에서 동작 조건을 최적화 하는 방법에 대한 연구를 수행하였다. Set 속도는 의 결정화 시간에 의해 결정되는 성능이고, set 동작시의 파형 관측을 통해 결정화 시간을 측정할 수 있었다. 그림 1 에 나타난 것과 같이 결정화 시간은 인가한 펄스 전압의 변화에 따라 지수함수 관계를 가지고 변화한다. 이러한 결정화 시간이 펄스 전압 이외에 펄스의 폭 및 모양과 가지는 함수 관계를 모델링하여 최소의 결정화 시간을 가지는 동작 방법을 정량 기술하고자 한다. 또한, 소모 전력을 최소화 할 수 있는 동작 방법을 별도로 평가하고, 최대 속도 조건과 최소 전력소모 조건과의 관계를 수립 및 토의할 예정이다.

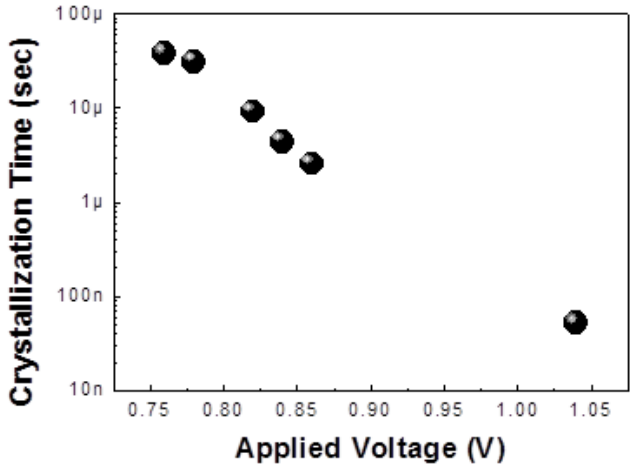

그림 1. 결정화 시간과 인가한 전압의 함수 관계

[1] Choi, Youngdon, et al., "A 20nm 1.8 V 8Gb PRAM with 40MB/s program bandwidth." Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International. IEEE, 2012.

Resistive switching characteristics depending on defects in silicon nitride-based RRAM

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Recently, silicon nitride (Si_3N_4)-based RRAM has attracted a lot of attentions due to outstanding resistive switchng characteristics such as high endurance, good retention and fast swtiching speed. We have fabricated two types of Si_3N_4-based RRAM devices to investigate defect effects on the resistive switching. One is the device with Si_3N_4 as swiching layer deposited by low-pressure chemical vapor deposition (LPCVD) [1], and the other is that by plasma-enhanced chemical vapor deposition (PECVD) [2]. Compared with the former group, the latter has more initial defects that might act as traps for the conducting path. The devices by PECVD need lower forming voltage because of larger number of initial defects. We also have confirmed that devices by LPCVD show sharper distribution over all the resistive switching parameters including forming/set/reset voltages and LRS/HRS.

Acknowledgment This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186).

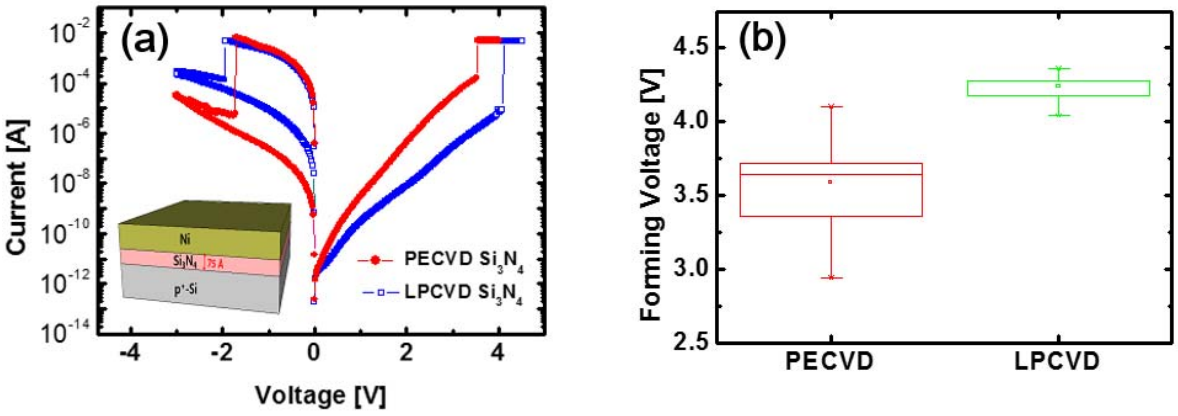

Fig 1. Measured device characteristics. (a) Typical bipolar resistive switching characteristics. (b) Distributions of forming voltages of LPCVD/PECVD Si_3N_4-based RRAM devices.

[1] S. Kim, S. Jung, and B.-G. Park, *Int. J. Nanotechnol.*, vol. 11, no. 14 (2014)
[2] H.-D. Kim, H.-M. An, and T. G. Kim, *J. Appl. Phys.*, vol. 109, no. 016105 (2011)

Programming pulse width variation and its microstructural model of phase-change memory

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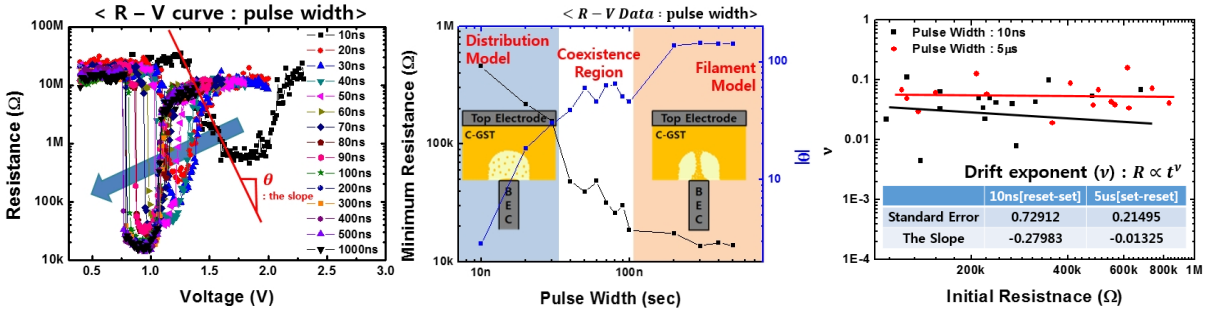
Phase-change memory is one of the next-generation non-voltile memories due to its fast programming, good data retension, low power consumption and low cost [1]. Recently, We have proposed microstructural models of PRAM cell with programming pulse width variation as shown in Fig. 1 (middle). Programming with short pulse width seems to give nucleation enhancement (distribution model) and programming with long pulse width may result in filament crystallization (filament model). Resistance drift means that resistance state is changed by defect, structural relaxation etc. We have characterized resistance drift at various resistance states with various applied programming pulse widths as shown in Fig. 1 (right). The functional relation of drift exponent ν and resistance exhibits some variations with applied voltage pulse widths. We plan to explain these variations using out microstructural models along with other characterization results such as resistance drift, activation energy, and endurance.



	10ns[reset-set]	5us[set-reset]
Standard Error	0.72912	0.21495
The Slope	-0.27983	-0.01325

Fig 1. (Left) Resistance vs. voltage characteristics for different pulse widths.

(Middle) Microstructural models of PRAM cell with pulse width variation.

(Right) Resistance drift characteristics.

[1] J. Bae, H. Shin, D. Im, H. An, J. Lee, S. Cho, D. Ahn, Y. Kim, H. Horii, M. Kang, Y. Ha, S. Park, U. I. Chung, J. T. Moon, and W. S. Lee "Recent progress of phase change random access memory (PRAM)," E* PCOS, (2000).

Influence of Electron and Hole Distribution on Embedded SONOS Nonvolatile Memory

Da Som Kim[1], Tae Ho Lee[2], Young Jun Kwon[2], Jae Gwan Kim[2], Sung Kun Park[2], In Wook Cho[2], Kyung Dong Yoo[2], Gyu Han Yun[1], and Woo Young Choi[1*]

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Silicon-oxide-nitride-oxide-silicon (SONOS) memory cells have been considered as an attractive option to embedded nonvolatile memory due to their low voltage operation, good scalability, immunity to defect and CMOS process compatibility [1]. Generally, embedded SONOS memory cells are programmed by channel hot electron injection (CHEI) and erased by band-to-band-tunneling-induced hot hole injection (BTBT-HHI). This localized charge trapping may accumulate the mismatch between electron and hole (EH) distribution as program/erase (PE) cycles are repeated. The mismatch between trapped EH distribution may degrade the reliability of cells [2]. In this study, focuses on the influence of EH distribution mismatch on embedded SONOS memory cells based on two-dimensional device simulation results. It has been observed that the pile-up of electrons over the channel and graded drain junction during each PE cycle results in threshold voltage (V_T) shift, subthreshold slope (SS). However transconductance (Gm) degradation can be observed over the graded drain junction.

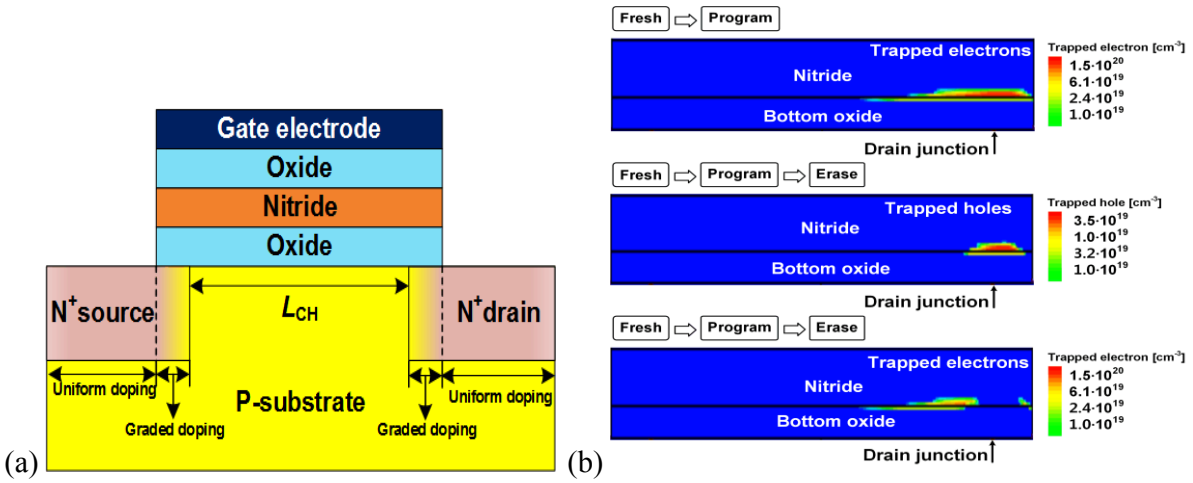

Fig 1. (a) Schematic of the simulated SONOS cell. (b) Simulated trapped charge distribution.

Acknowledgments: This work was supported in part by the NRF of Korea funded by the MSIP under Grant NRF-2012R1A2A2A01006159 (Mid-Career Researcher Program), in part by the NIPA funded by the MSIP under Grant 1711014140 (Information Technology Research Center), and in part by the KEIT funded by the MOTIE under Grant 10041855 (IT R&D Program)

[1] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, *IEE Electron Device Lett.*, 21, 11, 543 (2000).
[2] N. K. Zous, M. T. Lee, W. J. Tsai, A. Kuo, L. T. Huang, T. C. Lu, C. J. Liu, T. Wang, W. P. Lu, W. Ting, J. Ku, and C.-Y. Lu, *IEEE Electron Devices Lett.*, 25, 9, 649 (2004).

A 1.5-Gb/s analog pre-emphasis driver with 40-dB cable loss compensation

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Recently, the demand of high quality multi-media contents has been rapidly increased even in the applications of high-speed data communications. Particularly for gigabit operations, there are a number of issues to overcome, such as cable loss, inter-symbol-interference(ISI), HF compensation, etc. The pre-emphasis technique is a very well known algorithm exploited at transmitter(TX) [1].

In this paper, we present a gigabit analog transmitter designed in a standard 0.13-μm CMOS technology which can effectively compensate the electrical cable loss up to 40 dB by incorporating the pre-emphasis technique in the main driver [2]. The TX front-end circuit consists of four blocks, i.e. an input buffer, a pre-amplifier, a D-FF, and a main driver. The driver compares the original incoming bit sequence with the other bits delayed by the D-FF, and emphasizes the rising edges of each bit. Only the main driver utilizes 3.3-V power supply, while other circuitry uses a 1.2 V.

Post-layout simulations reveals that the proposed TX provides 14.1-mV_{pp} eye-openings at 1 Gb/s, and 4-mV_{pp} eye-openings at 1.5 Gb/s even with 40-dB cable loss for 900-mV_{pp} NRZ PRBS inputs. For comparison, the TX without pre-emphasis results in no eye-openings at 1 Gb/s. The TX chip dissipates 63.7 mW in total, and the core occupies the area of 136x180 μm^2.

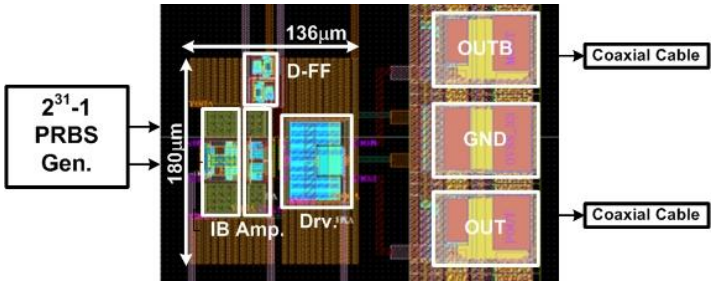

Fig 1. Layout of the proposed TX.

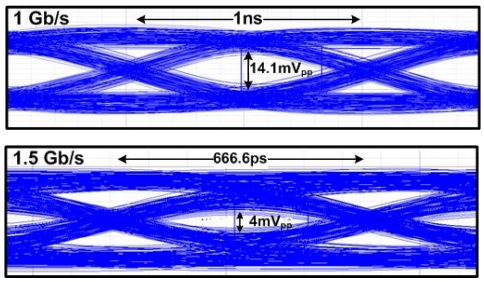

Fig. 2 Eye-diagrams of (a) 1 Gb/s, (b) 1.5 Gb/s.

[1] H. Higashi et al., "5-6.4 Gbps 12 channel Transceiver with Pre-emphasis and Equalizer", IEEE VLSI Circuits, Digest of Technical Papers (2004).
[2] K. Kim et al., "HDMI Transmitter with a pre-emphasis technique", 대한전자공학회 하계학술대회, 제 33 권 1 호 (2010).

Acknowledgment: 본 연구는 미래창조과학부 및 정보통신산업진흥원의 대학 IT 연구센터육성지원사업의 연구결과로 수행되었음" (NIPA-2014-(H0301-14-1008)). This work was supported by IDEC(EDA Tool)

A 1-Gb/s digital transmitter with 3-tap FIR pre-emphasis in 0.13-μm CMOS

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For the applications of high-speed serial data links, it is well known that electrical cables suffer significant line losses due to skin effet, conductor losses, dielectric losses, and etc. Particularly, the frequency-dependent attenuations cause intersymbol interference(ISI) to increase severely at the receivers, which creates difficulty for clock and data recovery and thus yields higher bit-error-rate(BER). To compensatie these losses, typically transmitter(TX) employs pre-emphasis whereas receiver incorporates equalization [1]. In this paper, we present a 1-Gb/s digital TX with pre-emphasis circuit in a 0.13μm CMOS technology to compensate 40-dB line losses in maximum. Here, a 3-tap FIR filter is exploited to realize the pre-emphasis driver, which first applies delays and then adds them back to the original bits with proper weighting, thereby compensating the significant ISI from the data symbols nearby. The three diffential mode-tap consists of original signal-tap, 1st post-tap which is most effective, and 2nd post-tap. A D-FF is utilized to give rise to delays. Fig. 1 shows the layout of the proposed digital TX where the chip core occupies the area of 130 x 90 μm^2. Fig. 2 depicts the post-layout simulation results of eye-diagrams for 900-mV_{PP} 2^{31}-1 NRZ PRBS inputs at the data rates of 500 Mbps, 750 Mbps, and 1 Gb/s, respectively. It is clearly seen that the proposed TX with a 3-tap digital pre-emphasis guarantees clear eye-openings up to 1 Gb/s through the 40 dB lossy channels. The whole TX chip dissipates 122.7mW in total.

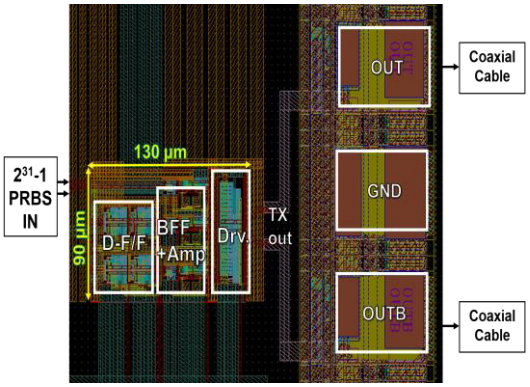

Fig. 1. Layout of the proposed digital TX.

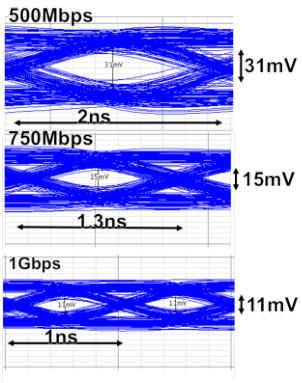

Fig. 2. Simulated eye-diagrams w/ 40dB channel loss.

[1] R. Farjad-Rad et al, "A 0.4-μm CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter", *IEEE J. of Solid-State Circuits*, (1999).

Acknowledgment: 본 연구는 미래창조과학부 및 정보통신산업진흥원의 대학 IT 연구센터육성 지원사업의 연구결과로 수행되었음" (NIPA-2014-(H0301-14-1008)). This work was supported by IDEC(EDA Tool).

A Switching-based Fast Li-Ion Battery Charger by Continuously Compensating Built-In Resistance for Mobile Devices

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Recently, the more functions have been implemented into mobile devices, the more capacity of Li-Ion battery in mobile devices is required. Moreover, the reduction of battery charging time becomes more crucial to accomodate the user's convenience. The charging operation of battery consists of trickle charging (TC), constant current (CC), and constant coltage (CV) modes [1]. The charging time can be shortened by reducing the time in CC and CV modes, which can be reduced by increasing the charging current and compensating the built-in resistance of battery, respectively.

In this paper, a switching-based fast Li-Ion battery charger is proposed by increasing the charging current and continuously compensating the built-in resistance of battery. The compensation block supplies the adaptive reference voltage (V_{aref}) to switch the CC mode to the CV mode. The V_{aref} is determined by calculating the built-in resistance (R_{ESR}) using the ratio of ripples of inductor current and battery voltage. The proposed charger in Fig. 1 (a) is simulated using a 0.18 μm CMOS process technology with high voltage devices of 5 V. The charging current in CC mode is set to 2 A, and Li-Ion battery is modeled with a capacitor of 1000 μF and a built-in resistance of 200 mΩ. The simulation results in Fig. 1 (b) show that the proposed charger reduces the charging time by 33% compared with the conventional one. Consequently, the proposed charger is well suited to achieve the fast charging for Li-Ion battery in mobile devices.

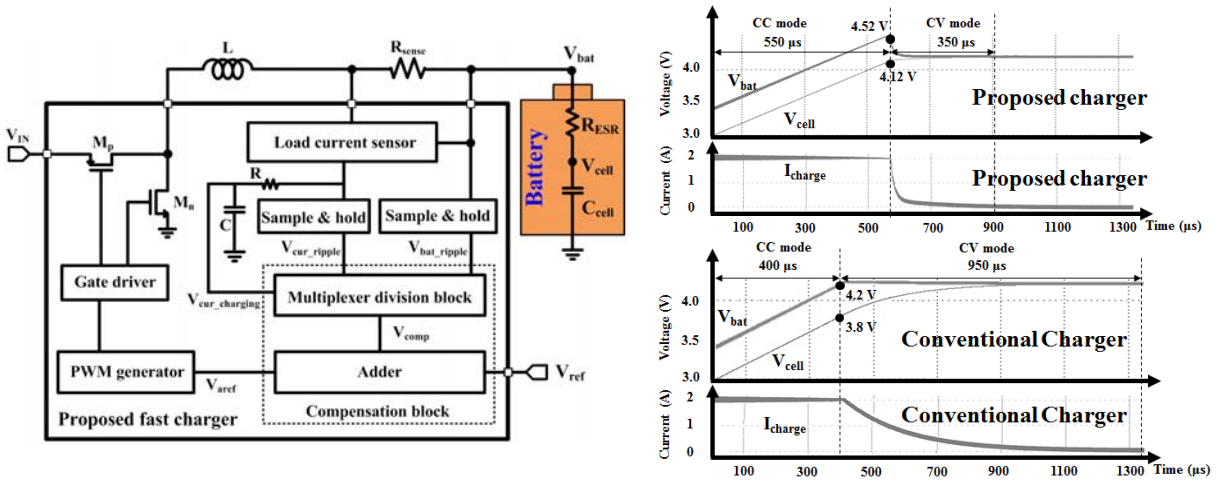

Fig. 1 (a) Schematic diagram, and (b) Simulated results of the proposed and conventional chargers.

[1] R. H. Peng, T. W. Tsai, and Z. H. Tai, ESSCIRC (2013).

A 1.5-Gb/s equalizer and limiting amplifier for 33-dB cable loss compensation

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Recently, gigabit-speed digital links via copper cables have mostly been implemented in submicron CMOS technologies [1]. Typically, the cables (which is called 'channel') demonstrate considerable signal loss at high-speed, thus yielding the characteristics of low-pass filter. This, however, results in severe inter-symbol interference(ISI) and the detrimental bandwidth shrinkage. In order to alleviate these issues, transmitter normally exploits pre-emphasis circuit while receiver(RX) employs equalizer(EQ) [1]. The EQ, having known the frequency attenuation phenomena of the utilized channels in advance, precisely compensates the signal loss at high frequencies, thereby recovering the originally transmitted data. Limiting amplifier(LA) is followed to provide enough gain for boosting and wide bandwidth for reducing ISI.

In this paper, we present a 1.5-Gb/s RX with EQ and LA realized in a 0.13-μm CMOS technology. The proposed RX can compensate the signal loss up to 1.5-Gb/s operation speed. Post-layout simulations demonstrate the gain boosting of 33.4 dB in maximum. The RX chip dissipates 18mW from a single 1.2-V supply in total, and the chip core occupies the area of 390 x 340 μm^2.

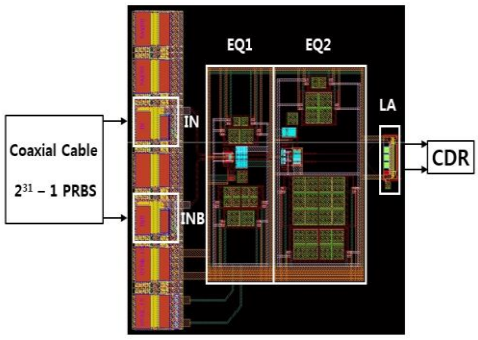

Fig. 1. Layout of the proposed RX.

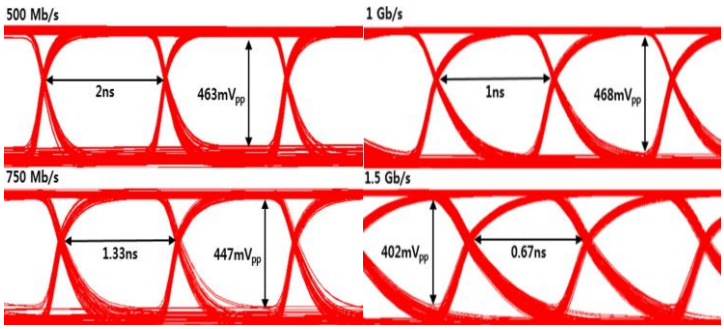

Fig. 2. Eye-diagrams at 500 Mb/s, 750 Mb/s, 1 Gb/s, and 1.5 Gb/s for 10mV$_{pp}$ 2^{31}-1 PRBS inputs.

[1] J. Lee, "A 20-Gb/s Adaptive Equalizer in 0.15-um CMOS Technology," *IEEE J. of Solid-State Circuits*, vol. 41, pp. 2058-2066, Sep. 2006.

Acknowledgment: 본 연구는 미래창조과학부 및 정보통신산업진흥원의 대학 IT 연구센터육성 지원사업의 연구결과로 수행되었음" (NIPA-2014-(H0301-14-1008)). IDEC 의 EDA Tool 에서 지원하여 수행하였음.

Switched-capacitor reconstruction filter with reduced sensitivity to reference noise for sigma-delta audio DAC

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Switched-capacitor (SC) circuits are widely used for analog reconstruction filtering in audio digital-to-analog (D/A) converters because of less sensitivity to clock jitter compared to switched-current circuits. One of key design issues in designing audio D/A converters is that they typically need to drive single-ended output loads such as external speakers. This can be implemented using differential-to-single-ended (D2S) buffer with attendant high power dissipation, large area, and increased noise power [1]. A possible solution to this problem is to use a single-ended SC circuit, where D2S is removed and the op amp in the SC filter directly drives an external single-ended load [2]. But a large disadvantage of the circuit in [2] is that it suffers from high sensitivity to reference noise and thus requires very low noise reference generators. In this paper, a new single-ended SC circuit is proposed to reduce sensitivity to reference noise. By sampling a single reference voltage with its polarity depending on digital input, the reference noise is attenuated by a first-order difference to appear at filter output. Along with the single-ended structure, the overall power and area is further reduced by the use of op amp chopping. Implemented in a 28-nm CMOS technology, the prototype D/A converter, consisting of left and right stereo channels, achieves 95-dB dynamic range while dissipating 4.2mW from a 1.8-V supply. It occupies only 0.05 mm^2.

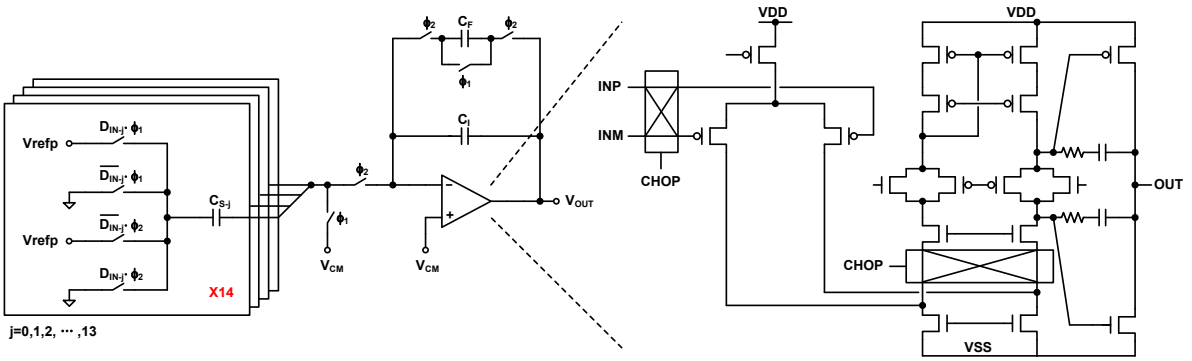

Fig 1. SC filter structure and its single-ended op amp topology

[1] I. Fujimori, A. Nogi and T. Sugimoto , IEEE JSSC, vol. 33, no.12, pp. 1863-1870, Dec 1998.
[2] V. Colonna, M. Annovazzi, G. Boarin, G. Gandolfi, F. Stefani and A. Baschirotto, IEEE JSSC,vol. 40, no. 7, pp. 1491-1498, July 2005.

A Spread Spectrum Clock Generator Using the Clock-Clipping Technique for Reduction of Time Interval Errors

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Nowadays, faster operation speed of automotive electronics causes functional failures due to electromagnetic interference (EMI) generated among the components. An effective solution to diminish EMI is to modulate the system clock frequency with a spread spectrum clock generator (SSCG). This method reduces EMI energies of a fundamental frequency and harmonic frequencies by spreading energies over a wide range of frequencies. However, an asynchronous serial interface requires a strict time interval error (TIE) range because the receiver circuitry may detect wrong data when the TIE is out of spec range [1-2]. In this paper, we propose a novel SSCG with a low EMI and the TIE limited within 3/4 clock cycle which is the maximum TIE (MTIE). Fig. 1 shows the block diagram and its simulated results. The simulated MTIE is limited within 3/4 clock cycle with a very simple clock-clipping block. With the operation frequency of 10MHz, the proposed method can reduce EMI levels by about 9dB at the fundamental frequency and by 19.1dB, 17.8dB, 20.9dB and 20.5dB at the 3rd, 5th, 7th and 9th odd harmonic, repectively.

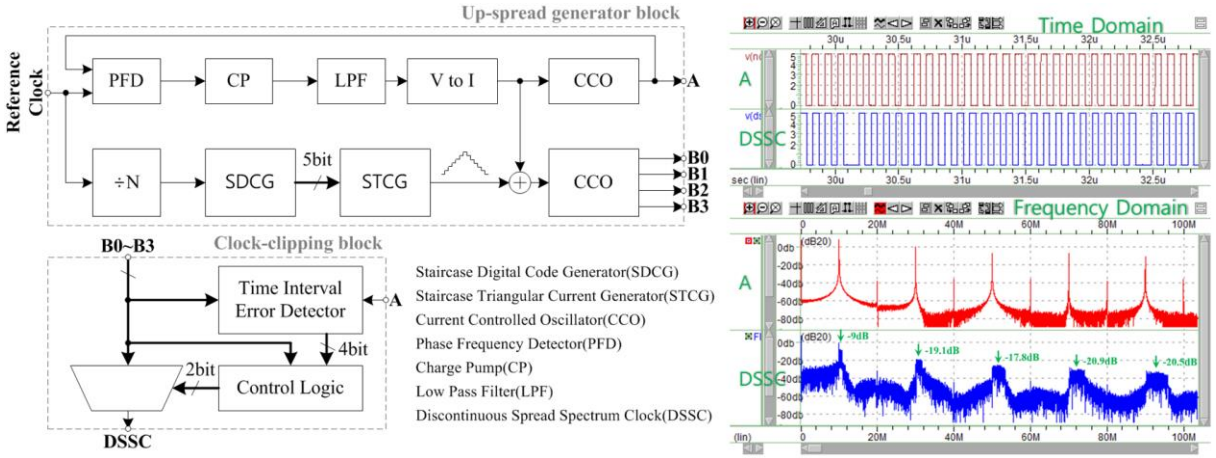

Fig 1. Circuit block diagram and simulation results

[1] J. Zhou and W. Dehaene, "A synchronization-free spread spectrum clock generation technique for automotive applications," IEEE Trans. Electromagn. Comp., vol. 53, no. 1, pp. 169–177, Feb. 2011.

[2] N. Da Dalt et al., "An all-digital PLL using random modulation for SSC generation in 65nm CMOS," ISSCC, pp. 252-253, Feb. 2013.

Bootstrapping Technique with PWM/PFM Dual Mode for Wide load Range High Efficiency Buck Converter

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Conventional DC-DC Buck converter input is Li-ion Battery. So, input voltage may be 2.2V~5V. If input voltage Li-ion Battery, Power MOSFET VGS voltage issue not exist. But High voltage Input will be exist problem which is Power MOSFET VGS issue. VGS voltage must sustain 5V, because it is almost device's characteristic. Bootstrapping Technique sustain VGS in DC-DC Converter. But Bootstrapping Technique is used to large power application. For this reason, Bootstrapping Technique is based on PWM mode and is used to heavy load. Light load efficiency will be low and it is not proper wide range high efficiency. Nowadays, in Power management IC field, light load efficiency is more important. Smart phone, mobile application has sleep mode, low power standby, etc. So, these application must have high efficiency at light load. In this paper, PWM/PFM dual mode Control DC-DC Buck converter with Bootstrapping Technique will be proposed.

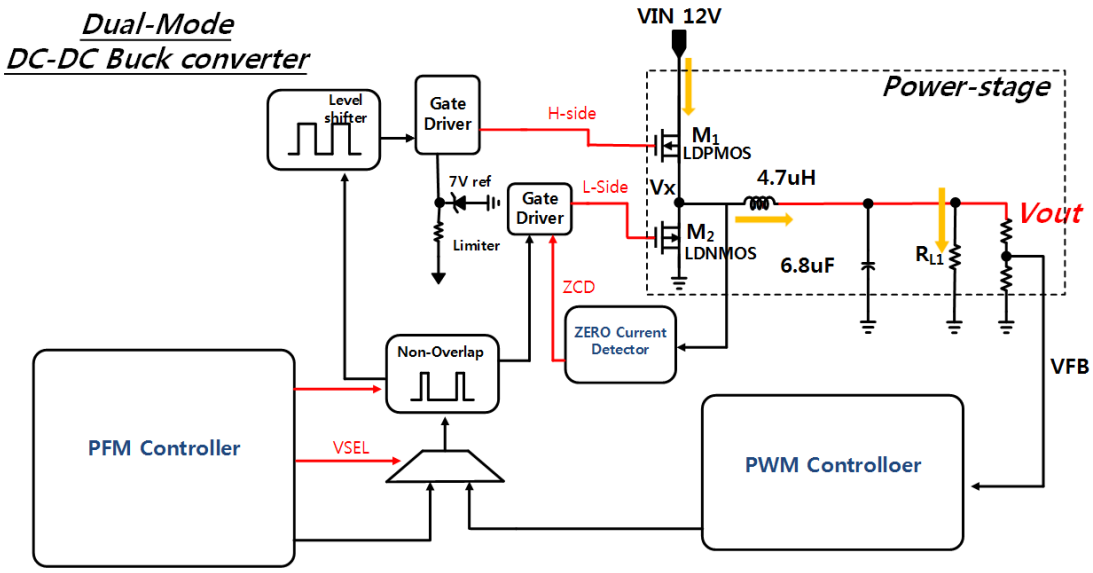

Fig 1. Proposed Dual Mode DC-DC Converter.

[1] A. Morra, M. Piselli, A. Gola, "PFM Mode Buck Converter: A Mathematical Model to Calculate the Maximum Switching Frequency", Electronics, Circuits and Systems, 15th IEEE Ineternational Conference on, September 2008.

[2] Tsz Yin Man, Philip K. T. Mok, Mansun Chan, "Analysis of Switching-Loss-Reduction Methods for MHz-Switching Buck Converters", Electron Devices and Solid-Stage Circuits, IEEE Conference on, December 2007.

Standby Power Reduction Technique due to the Minimization of Voltage Difference between Input and Output in AC 60Hz input

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Recently, standby power reduction techniques of AC/DC adaptor were developed, consuming power almost arrived to 300mW level. The standby power losses are composed of the input filter loss 11.8mW, the control IC for AC/DC adaptor 18mW, the switching loss 9.53mW and the feedback loss 123mW[1]. And there are the standby power reduction techniques (1) the reduction of power consumption in startup resistor, (2) the reduction of switching frequency, (3) the reduction of output voltage disconnection and the output voltage drop, (4) the use of a low-power auxiliary power supply[1] and (5) the feedback loss reduction by the control of primary side regulation in SMPS(Switched Mode Power Supply).

In this paper, in order to reduce the standby power of SMPS more, the loss due to a voltage difference between input and output is reduced by the control circuit which is composed of the low voltage driving circuit and voltage regulator. The low voltage driving circuit operates on the low voltage of input and off the high voltage in Fig 1 (c). The low voltage driving IC was produced by the 1.0um, high voltage DMOS process.

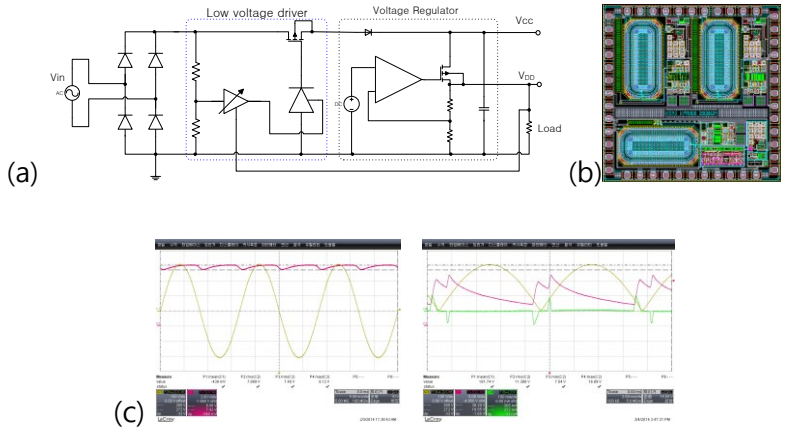

Fig 1. (a) Proposed circuit, (b) layout and (c) operational waveform @ load 5.6kohm, V_{out}=7.7V

[1] Byoung-Hee Lee, Ki-Bum Park, Chong-Eun Kim and Gun-woo Moon “No-Load Power Reduction Techniques for AC/DC Adapters”, IEEE Transactions on Power electronics, Vol. 27, No. 8, august 2012

Portable Sensor Platform using Constant Current Source

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Recently, environmental sensor market accounts for a large market. There is also growing demand for not using by a laboratory level, but also mobile devices. We investigated the system that controls voltage and current for electrical environment in small size platform. Sensor system requires high accurate and wide range of driving condition while mobile system require small, high efficiency, and fast processing at the same times. In order to meet these requirements, using the one of the power unit SMPS [Switching Mode Power Supply] that converts the high voltage from the low voltage battery, and CCS [Constant Current Source] to give a high precise current can make it possible [1]. It also uses the MCU [Microcontroller Unit] to effectively controlling the equipment. We make CCS unit that can source that can source any constant current and voltage range with fast recovery [2]. In our lab, over 90V voltage range and less than 1nA range current resolution can be possible. By using small integrated chip (like operational amplifier) small size portable with high accuracy can be possible. As shown as Fig.2, this graph is simple current and voltage curve of resistor and resistor with diode. This module meets the high accuracy of driving and measuring with compared with lab level device (like semiconductor analyzer). Especially, this module is also the platform for sensing and analyzing the physical environment and the state with small size that is smaller than mobile phone with various applications. This study will be helpful in designing sensor devices for using mobile applications and applied to other kinds of mobile devices with ease.

Acknowledgement: This work was supported by Giparang Inc. and the Brain Korea 21 Plus Project in 2014

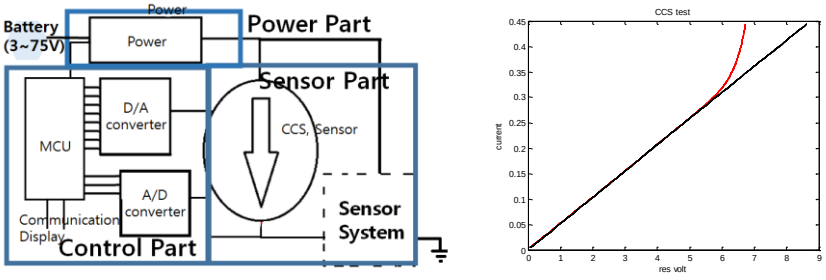

Fig 1. System block diagram and simple voltage-current curve.

[1] P. Bertemes-Filho, A. Felipe, V.C. Vincence, Circuits and Systems, 4-7, pp. 451-458 (2013)
[2] J. Anudev, I.J. Raglend, ICCEETK, pp. 314 - 318 (2012).

A Mutual Capacitive Touch Controller Robust to Display Noise for Ultrathin Displays Based on Differential Sensing

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A capacitive touch-screen became an essential user interface mean especially in tablet PCs and smart phones. Nowadays, in addition to sense fingers, it is required to sense smaller objects like a conductive stylus to support a user to write a small letter or draw a detailed picture. To support the feature, higher sensitivity is required. Meanwhile, touch sensor panels are being integrated into either the cover tempered glass or the display glass for thinner screen, so that provides more volume could be allocated to a battery. However, it implies that touch sensor becomes more prone to display noise coupling. It is because gap between touch sensor and display electrodes becomes smaller. Increasing sensitivity to sense smaller objects like the stylus makes it worse because the noise would be amplified too and might incur internal voltage saturation in the sensing circuit, which might damage signal's quality such that it is unrecoverable in the later stages. In this paper, we propose a method that does not need synchronization, and thus, high reporting rate is possible, and that does not hurt signal quality by rejecting the display noise at the very front-end of the analog read-out circuit. Fig. 1 shows outstanding display noise compensation performance of the proposed IC as compared with conventional mutual capacitance sensing architecture.

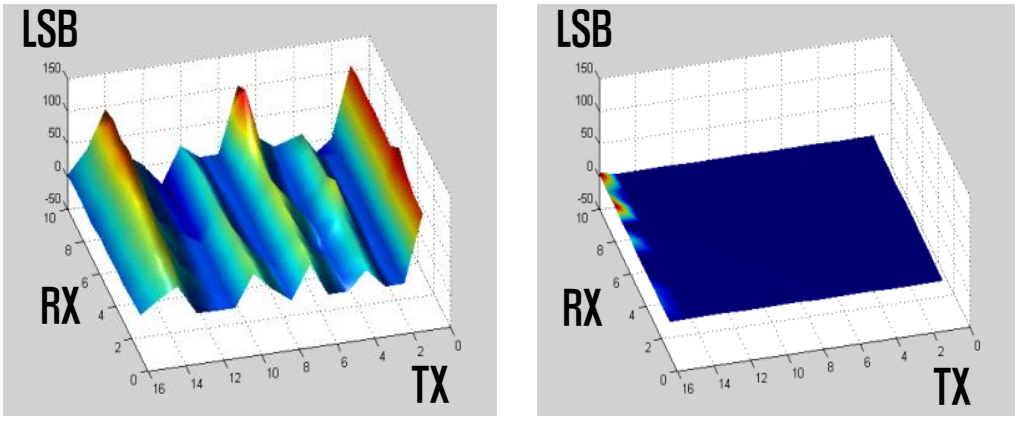

Fig 1. Display noise interference value at conventional mutual capacitance sensing (left) and proposed differential mutual capacitance sensing (right).

A Compact Frequency Quadrupler With Subharmonic Injection-Locked Ring Oscillator

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This paper presents a compact frequency quadrupler with a subharmonic injection-locked ring oscillator (SHILRO). Conventionally, a phase-locked loop (PLL) is used for frequency multiplication which consists of a phase detector, a loop filter, a voltage-controlled oscillator and a divider. However, the high performance PLL is burden to generate quadruple frequency of a reference signal in the limited die area since it needs high power consumption and large area. The frequency quadrupler is proposed to achieve a compact area, low power consumption and low phase noise based on subharmonic injection-locked scheme. The design is composed of a voltage controlled delay line (ΔT), an output driver (DRV) and a SHILRO. Simulated in a 65 nm CMOS process, the frequency quadrupler measures 2.24 GHz output frequency with 56 MHz reference pulsed clock source and it only occupies 0.0208 mm^2. The power consumption of the frequency quadrupler is 7.1 mW at 2.24 GHz.

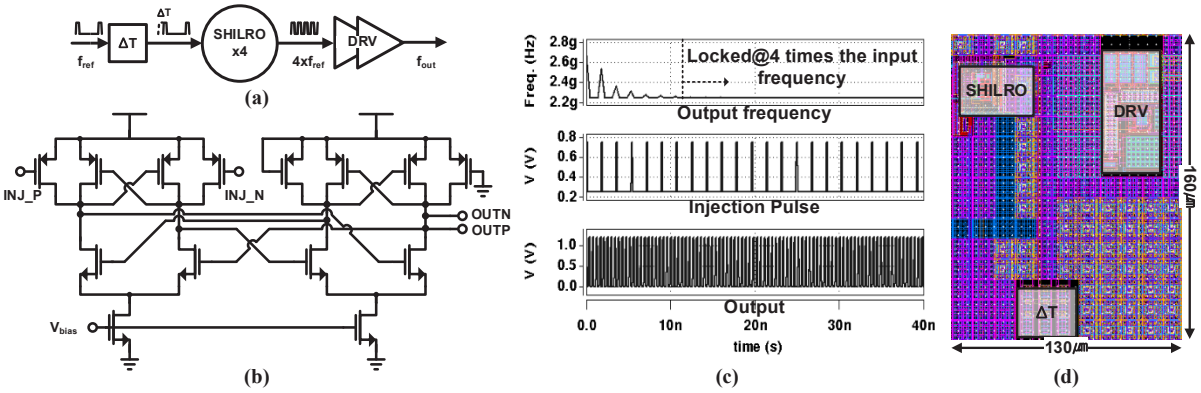

Fig 1. (a) Top block diagram, (b) SHILRO, (c) simulation result, (d) layout micrograph

[1] B. M. Helal, et al, "A Low Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop," *IEEE J. Solid-State Circuits*, vol. 44, pp. 1391–1400, May 2009.
[2] K. Takano, et al., "4.8GHz CMOS frequency multiplier with subharmonic pulse-injection locking," *IEEE Asian Solid-State Circuits Conference*, pp. 336-339, Nov. 2007.

Clock and data recovery system with digitally controlled phase interpolator

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This paper proposes a clock and data recovery (CDR) system with digitally controlled phase interpolator (PI) for forwarded clocking system. Proposed CDR whose block diagram is shown in the figure 1, is separated into two parts. First is delay locked loop (DLL) that generates multi-phase clocks by using forwarded clock (F-CLK). Second is PI based de-skewing circuit. PI based CDR has advantages of that PI, different from voltage controlled oscillator (VCO), can be controlled easily and complicated high-order loop filter is unnecessary. So, simple digital controller can be used to control PI. Test chip is fabricated in Samsung 65nm CMOS technology. The die area of proposed CDR is about 0.048mm^2. Operating clock frequency is 5GHz and data bit rate is 10Gb/s. Post layout simulation result shows that power dissipation of overall CDR is 16mW. DLL uses 6mW and PI, without controller, consumes 1mW.

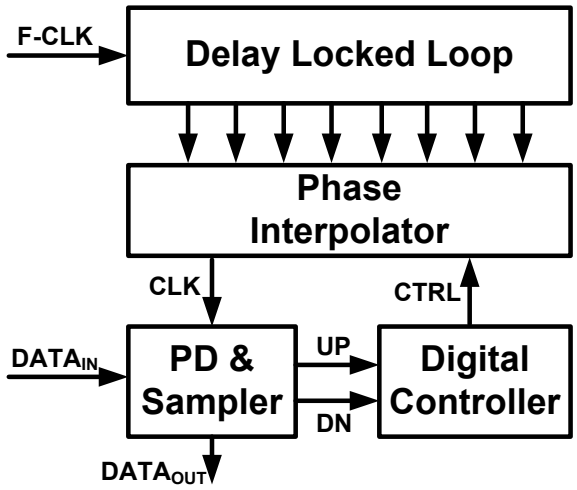

Fig 1. Block diagram of proposed CDR

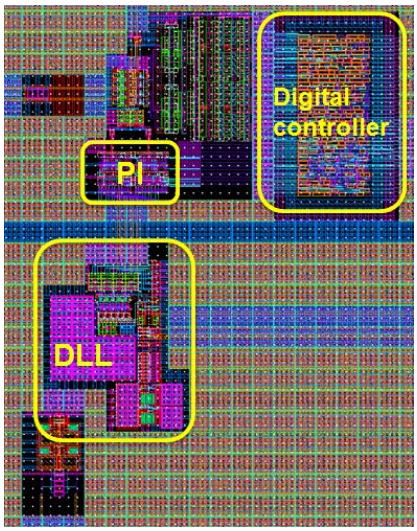

Fig 2. Layout of proposed CDR

[1]

Event-Driven Simulation of Input-Dependent Nonlinear Behaviors

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Most of the input-dependent nonlinearities of analog circuits are analyzed only in steady states (i.e., using input-to-output DC characteristics), assuming its transient behavior is memoryless. However, in many cases such as in equalizers and voltage regulators, it is necessary to assess their dynamic nonlinearities caused by poles and zeros whose locations change with the input level. This paper proposes a simulation methodology which can simulate both the static and dynamic nonlinearities of analog circuits in an event-driven fashion. The proposed method divides the input range into multiple sections and models each section as a piecewise linear system with its representative gain and pole/zero's. When the input signal crosses the boundary of the section, the gain and pole/zeros are switched to the new values accordingly. As each section is modeled as a linear system, this switching model can be simulated using the event-driven method presented in [1]. Fig. 1 depicts a simple inverter example. Its operation can be divided into three states depending on the input level: (1) only PMOS is conducting, (2) both PMOS and NMOS are conducting, and (3) only NMOS is conducting. The proposed method extracts the DC gains and the dominant pole locations for each state, and constructs a switching system between those states. Fig. 1(c) shows the simulation results of the inverter output V_{out} when the input V_{in} is increased from 0V to 1V with a rising time of 200ps. The proposed method is in good agreement with the SPICE simulation. For comparison, the model with a fixed pole is simulated, which shows discrepancies when the output decreases below 0.5V.

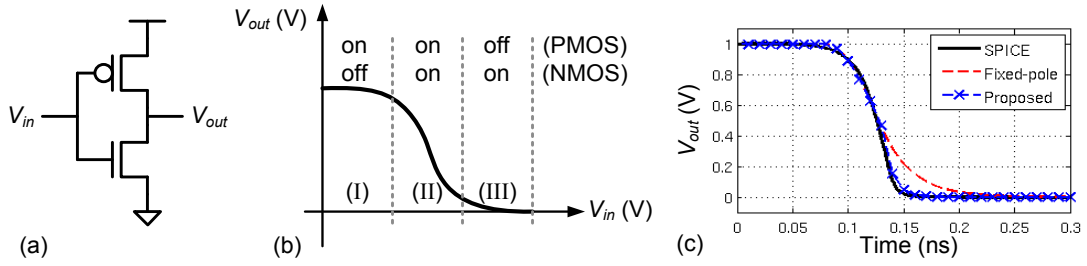

Figure 1. (a) An inverter example, (b) its input-dependent operating states, and (c) simulation results in comparison with SPICE and a fixed-pole model.

[1] J.-E. Jang, et al., "An event-driven simulation methodology for integrated switching power supplies in SystemVerilog," in *Proc. ACM/IEEE Design Automation Conf.* (*DAC*), pp. 1-7, May 2013.

Delay Defect Localization by Silicon Data Mining

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Delay defect localization is a crucial step in post-silicon debug and manufacuring test, and it is becoming more challenging because delay defects are getting more subtle as technology scales. Our knowleadge on a silicon chip is superfical due to limited observability, low measurement resolution, and model-silicon miscorrelation. This paper tackles these obstacles using a data mining technique. It shows that a mathematical algorithm can combine low-resolution path delay measurements and inaccurate pre-silicon models, predicting unobservable segment delays accurately. These segment delays can be used to enhance path delay measurement resolution. We also propose a delay defect diagnosis method using the segment delays. The proposed method ranks potentially defective segments by likelihood and provides significant first hit rank (FHR) and runtime improvement over exising methods.

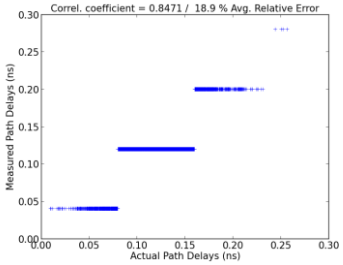

Figure 1. Low resolution path delay measurements

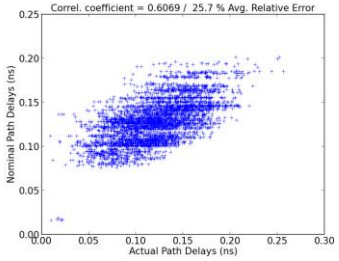

Figure 2. Model-silicon miscorrelation

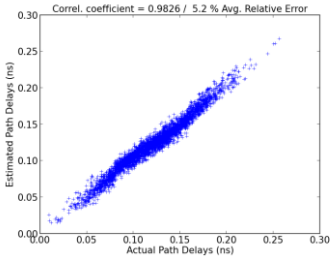

Figure 3. Enhanced resolution by the proposed method

[1] Y. Chen, M. Kuo, and J. Liou. Diagnosis framework for locating failed segments of path delay faults. In Test Conference, 2005. ITC 2005. IEEE International, pages 387–394, 2005.
[2] Y.-Y. Chen and J.-J. Liou. A non-intrusive and accurate inspection method for segment delay variabilities. In Asian Test Symposium, 2009. ATS'09., pages 343–348. IEEE, 2009.

* This work was supported by the Korea Foundation for the Advancement of Science & Creativity(KOFAC), and funded by the Korean Government(MOE).

High-Performance of Piezoelectric Nanogenerator using Depletion Width engineering of Surface treatment

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Piezoelectric semiconductor materials have emerged as the most attractive material for nanogenerator (NG)-based prototype applications, such as piezotronics, piezophotonics and energy harvesting, due to the coupling of piezoelectric and semiconducting dual properties. Understanding the mechanisms for high power generation, charge transport behavior, energy band modulations, and role of depletion width in piezoelectric semiconducting p–n junction, through piezoelectric charges developed by external mechanical strains, are essential for various NGs. Here, we demonstrate enhancement of the output power of one-dimensional zinc oxide (ZnO) nanowires (NWs)-based NG using a p-type semiconductor polymer, by controlling their energy band at depletion width in the piezoelectric semiconducting p–n junction interface and native defects presented in as-grown ZnO NWs. The piezoelectric output performance from the P3HT-coated ZnO NWs-based NG was several times higher than that from the pristine ZnO NWs-based NG, under application of the same vertical compressive strain. Holes from the p-type P3HT polymer significantly reduced the piezoelectric potential screening effect caused by free electrons in ZnO. Theoretical investigations using COMSOL multiphysics software were also carried out, in order to understand the improvement in the performance of surface passivated ZnO NWs-based NG, in terms of free carriers concentration and holes diffusion, due to the formation of p–n junction at the interface of ZnO and P3HT, and depletion width change.

Chemically-sintered, binder-free TiO_2 films for low-temperature photoelectrodes

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Dye-sensitized solar cells (DSSCs) have attracted great interest for scientific research and industrial applications because of transparency, color tenability, and low-cost fabrication compared with silicon solar cells [1]. In DSSCs, porous TiO_2 photoelectrodes are usually prepared on transparent conducting glass substrates by coating and calcinating at 450–500 °C. Recently, considerable efforts have focused on developing low-temperature processable TiO_2 pastes to apply them to flexible DSSCs that have the advantages including lightweight, thin structure, bendability, and large-area processing [2]. In this study, we report viscous, binder-free TiO_2 pastes composed of TiO_2 nanoparticles and ammonia water that is processable at low temperatures. The viscous TiO_2 pastes were obtained by the addition of a small amount of ammonia to the TiO_2 nanoparticle solution, which enables the formation of uniform and thick TiO_2 films. An energy conversion efficiency of the solar cells with the mesoporous TiO_2 films reached a maximum of 3.4% when the TiO_2 pastes were dried at 150 ^oC.

[1] B. O'Regan and M. Grätzel, Nature 353, 737 (1991).
[2] N.-G. Park, K. M. Kim, M. G. Kang, K. S. Ryu, S. H. Chang, and Y.-J. Shin, Adv. Mater, 17, 2349 (2005).

무반사 나노구조 PDMS 필름 코팅을 이용한 염료감응형 태양전지의 효율 향상 연구

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3세대 태양전지 중 하나인 염료감응형 태양전지(DSSC)는 최근 친환경적인 특성과 저렴한 제조공정으로 큰 관심을 받고 있다. 현재에는 이러한 DSSC 내부의 나노입자에 염료를 더 잘 흡착시키기 위해 재료적으로 연구가 진행될 뿐만 아니라, 무반사 및 광산란 효과를 높이는 등의 광학적인 측면에서도 효율 향상을 위한 많은 실험이 활발히 진행되고 있다. 특히, 나노구조를 이용한 무반사 코팅은 광대역 파장 및 다방향 태양광에 대해서 효과적으로 태양전지 표면 반사를 줄일 수 있다. 본 연구에서는 소프트 임프린트 리소그라피 기법을 통해 비주기적 나노구조가 형성된 몰드를 이용하여 polydimethylsiloxane(PDMS) 필름 표면에 나노패턴을 전사하였다. 나노구조가 형성된 PDMS 필름을 FTO 유리 기판에 부착하여 광학적 특성을 조사/분석하였다. 또한 DSSC의 효율을 향상시키기 위해 빛이 입사하는 DSSC 유리기판에 무반사 나노구조 PDMS를 부착하여 소자의 전압-전류 특성을 측정하였다. 나노구조 PDMS 필름이 부착된 FTO 유리는 FTO 유리기판보다 광대역 파장 (350-800 nm)에서 낮은 반사율을 보였고, DSSC에 적용한 결과, 소자의 효율이 개선되는 것을 확인할 수 있었다.

Flexible piezoelectric / photovoltaic hybrid device for energy harvesting applications

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버려지는 다양한 형태의 에너지원을 전기에너지로 변환하는 기술은 표준화 되어있지 않은 분야로서 융합 개념을 통한 신기술 도출이 필요한 분야이다. 본 연구에서는 빛 에너지를 전기에너지로 변환하는 태양전지 기술과 역학적 에너지를 전기에너지로 변환하는 압전소자 기술을 융합한 소자를 제안하고자 한다. 압전소재 중 PVDF(Poly vinylidene fluoride) 는 고분자 유기물로 유전율이 크고, 유연하며, 인체에 무해한 재료로 다양한 압전 소자 기술로 응용이 가능하다 [1]. 그림 1(좌) 와 같이 코팅 된 PEDOT:PSS/PVDF 박막을 물리적으로 박리 후 후면전극 ZnO 를 증착 함으로써 제조 하였다. 유기태양전지는 별도로 제작한 후 위에서 박리 된 압전 소자를 부착하는 방법으로 융합 소자를 제조 가능 하다 (그림 1 우). 제안하는 융합소자는 빛과 바람 또는 진동이 공존하는 환경에서 효과적인 에너지 하베스팅을 구현할 것으로 기대 된다.

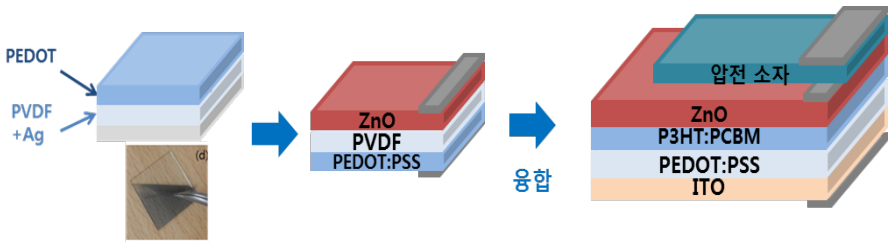

그림 1 . 압전 소자 모식도 (좌) 및 압전 · 광전 융합 소자 모식도 (우).

본 연구는 한국과학창의재단에서 지원하는 대학생창의융합과제 (유연한 압전 · 광전 융합소자 개발) 의 일환으로 수행하였음.

[1] Khaled S Ramadan, D sameoto and S Evoy, “A review of piezoelectric polymers as functional materials for electromechanical transducers”, Smart Mater. Struct. 23 (2014). 033011. 26pp.

JBS구조의 p-grid 영역과 FLR 간격에 따른 4H-탄화규소(SiC) 쇼트키 장벽 다이오드(SBD)의 전기적 특성 분석

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접합 장벽 쇼트키(Junction Barrier Schottky, JBS) 구조를 가지는 탄화규소(SiC) 쇼트키 장벽 다이오드(Schottky Barrier Diode, SBD)는 unipolar 구조의 실리콘 소자에 비하여 스위칭 손실이 적어 초고속 스위칭이 가능하며 고온에서의 동작이 가능하여 전력소자의 냉각 시스템을 간단이 할 수 있다는 장점이 있다[1], [2].
본 연구에서는 1700V급 SiC SBD 소자를 제작하기 위해 JBS 구조의 p-grid(0, 25, 50, 75 %)영역과 FLR 간격(space 1, 2, 3 um), 그리고 annealing 온도를 변수로 하여(425, 475, 550 ℃) 소자를 최적화 하였다. 각 소자의 변수에 따라 순방향 전류-전압 및 역방향 항복전압(Breakdown Voltage, BV)과 누설전류를 측정하였다. 그 결과 p-grid 면적이 넓을 때 누설전류가 감소하였으며 이는 reverse bias 인가 시 p-grid 주변의 공핍층의 확장으로 인하여 전류를 shielding 하기 때문이다. 그리고 FLR 의 간격이 2um 일 때 역방향 항복전압이 가장 높으며 p-grid 면적에 따른 누설전류의 경향성이 가장 뚜렷하게 관측되었다. 또한 annealing 온도가 높을수록 쇼트키 전위 장벽(Schottky Barrier Height, SBH)이 증가하는 것을 확인 하였다.

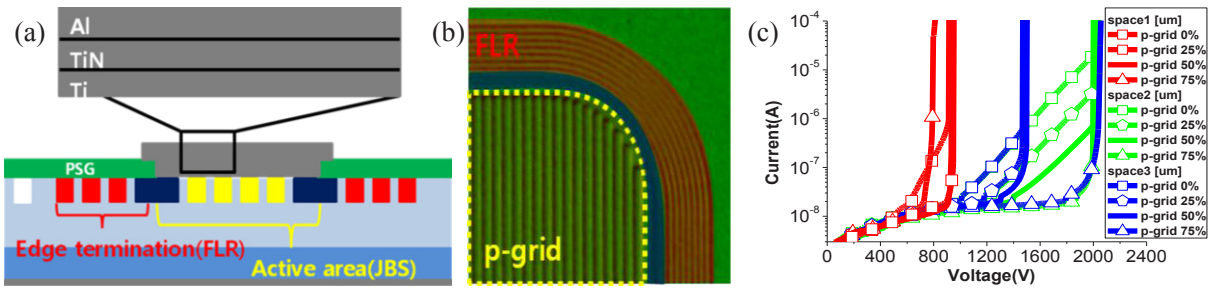

Fig 1. (a) Fabricated SBD device structure, (b) p-grid area of JBS, and FLRs surface image, and (c) Reverse BV characteristics

[1] 파워 반도체 디바이스 활용 기술. 월간 전자기술 2004 (2004).
[2] T. Hayashi, H. Tanaka, Y. Shimoida, S. Tanimoto, and M. Hoshi“, New High-voltage Unipolar Mode p+ Si/n- 4H-SiC Heterojunction Diode,”*Mater. Sci. Forum,* **953** 483-85 (2005).

Normally-off AlGaN/GaN MOSHFETs의 Differential Subthreshold Ideality Factor Technique을 통한 Interface Trap Density 추출

최준영 [1], 강영진 [1], 최성주 [2], 김대환 [2], 차호영 [1], 김형탁 [1,*]
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2) 전기 공학과, 국민대학교, 서울 136-702, 한국
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최근 GaN 반도체 소자에 gate recess 를 사용하여 normally-off 를 구현한 연구가 보고되고 있다.[1] 절연체와 GaN 간의 계면에서의 트랩 특성은 높은 성능과 소자의 신뢰성에 중요한 문제이다. 우리는 Differential subthreshold Ideality Factor(DIF) Technique 을 사용하여 절연체와 GaN 계면의 트랩을 추출 방법을 연구하였다. 이 방법은 threshold voltage 에 영향을 받지 않고 transfer characteristic 의 subthreshold 영역에서 interface state 를 추출할 수 있다. ICPCVD SiO_2/GaN 계면에서 trap density 를 추출해보면 약 $D_{it}(E) = 2\times10^{11}\sim2\times10^{12}$ [$eV^{-1}cm^{-2}$]의 결과가 나오고, 이는 conductance method[2]를 사용한 추출 값과 유사한 것을 확인할 수 있다. On state Stress test 와 5 MeV proton 이 조사된 normally-off AlGaN/GaN MISHFETs 소자에 DIFT 를 적용하여 interface trap density 를 추출하였고, 그 결과 stress 전후, irradiation 전후로 D_{it} 가 증가하는 것을 확인할 수 있다.

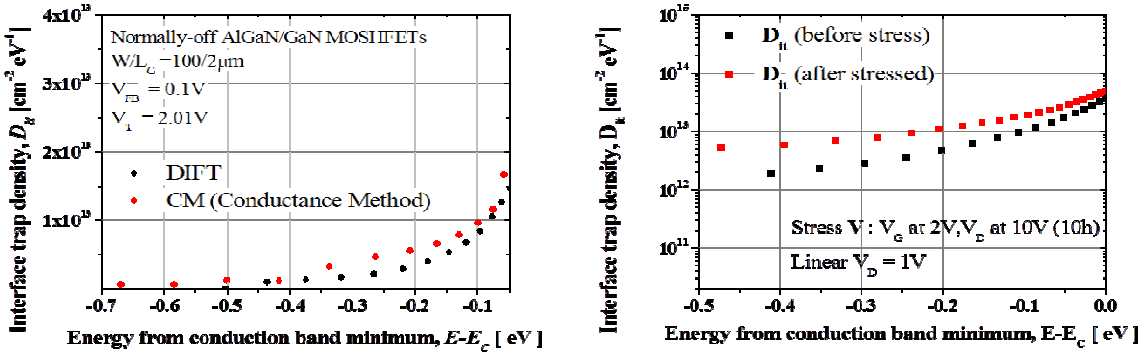

Fig 1. Normally-off AlGaN/GaN MOSHFETs structure and DIFT extraction data

[1] B. R. Park, J. G. Lee, W. J. Choi, H. T. Kim, K. S. Seo, and H. Y. Cha, IEEE Electron Device Lett., 34, 354 (2013).
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Thermoelectric devices based on H_2SO_4-treated poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) thin films

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Recently, polymer-based thermoelectric (TE) devices, which can convert heat to electicity via Seebeck effect, have attracted attention as a power generator due to the advantages of both TE devices and organic electronic devices. Among typical conducting polymer TE materials, poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) is one of the most representative materials owing to its high electrical conductivity. To increase the performance of PEDOT:PSS based TE devices, several methods have been reported by increasing the electrical conductivity of PEDOT:PSS thin-films using polar solvent such as dimethyl sulfoxide (DMSO), ethylene glycol (EG), glycerol, D-sorbitol [1]. In this work, we treated the PEDOT:PSS thin-films with H_2SO_4 at different temperature (from 200 °C to 260 °C) to enhance the electrical conductivity. The electircal conductivity at room temperature was increased approximately over 3 oders of magnitude from 1.15 S cm^{-1} to 1167.03 S cm^{-1}. As a result, the maximum power factor (PF) was obtained as 16.99 μW m^{-1} K^{-2} for PEDOT:PSS film treated with H_2SO_4 at 220°C. The effect of the H_2SO_4 treatment on the thermoelectric property of the PEDOT:PSS thin-films depending on the temperature condition will be presented in this work. This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2014R1A1A2055322).

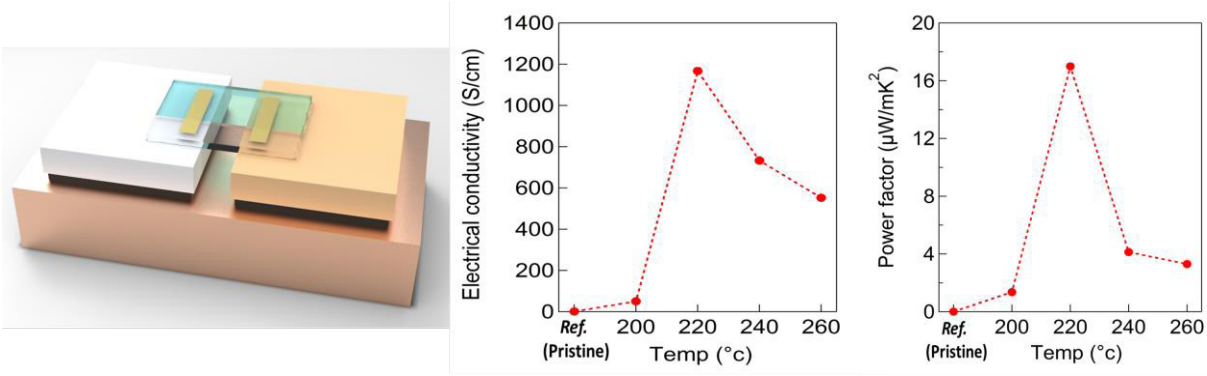

Fig 1. Schematic diagram of the TE device and measurement system, and the electrical/thermoelectric properties of H_2SO_4-treated PEDOT:PSS thin-films

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Optimization of InGaP/InGaAs/Ge solar cells by InGaAs middle cell growth temperature

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Compound semiconductor based triple-junction structures on Ge substrates have been studied for realizing high efficiency solar cells under high concentrated illuminations [1]. The short circuit current density enhancement by optimizing the epitaxial growth temperature is essential to further understand the multi-junction structures and realize high efficiency. We investigate the photovoltaic conversion efficiency of the InGaP/InGaAs/Ge triple-junction solar cells as a function of the InGaAs middle cell growth temperature. The growth temperature is varied in the range of 600 ~ 655 ^{o}C for the InGaAs middle cells, which are epitaxially grown on Ge substrates using metalorganic vapor phase epitaxy (MOVPE). The InGaP/InGaAs/Ge triple-junction solar cells are fabricated using a standard photolithography, metal deposition, rapid thermal annealing, and wet chemical etch processes. Under AM1.5 global light illuminations, the InGaAs middle cell grown at 635 ^{o}C has the highest short circuit current density and conversion efficiency as shown in Fig. 1.

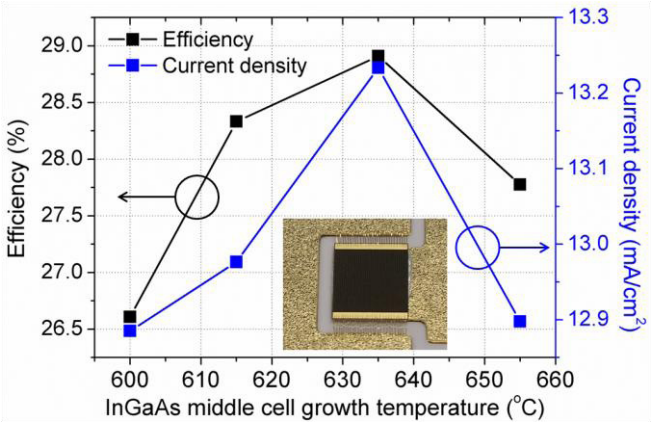

Fig 1. Efficiency and current density of the InGaP/InGaAs/Ge solar cells at 1-sun as a function of the InGaAs middle cell growth temperature. The inset shows the packaged solar cell (0.3025cm^2) used in this study.

[1] R.R. King, D.C. Law, K.M. Edmondson, C.M. Fetzer, G.S. Kinsey, H. Yoon, R.A. Sherif, and N.H. Karam, Appl. Phys. Lett., 90, 183516 (2007)

Enhanced field-effect passivation performance of atomic-layer-deposited Al_2O_3 layer for Si nanostructured solar cells using interface S incorporation

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In Si photovoltaics, nanostructures such as nanowires and nanoholes are necessary to maximize the optical absorption for higher efficiency solar cells. Recently, Al_2O_3 passivation via atomic layer deposition(ALD)have been commonly used as high efficient passivation layer for Si solar cells by field effect passivation with negative fixed charges. However, in case of nanostructured Si, higher index planes are exposed with increasing surface area and degrade the property of Al_2O_3 passivation. At the roughness Si interface, higher index planes such as (110) and (111) exposed and easily forming thick SiO_2 interfacial layer which containing positive fixed charges. Moreover, SiO_2 layer which formed by higher index planes have high density of interface defect states(D_{it}) compare with (100) Si plane[1]. The D_{it} can act as not only recombination center but also affect as positively charges when donor-like states are unoccupied. For the reason, positively charges caused by SiO_2 and D_{it} screen negative fixed charge of Al_2O_3 and reduce field effect passivation. Therefore, an additional process to restore the Al_2O_3 is required and S incorporation is shown as one of effective way to enhance the negative charges at the Al_2O_3/Si interface.

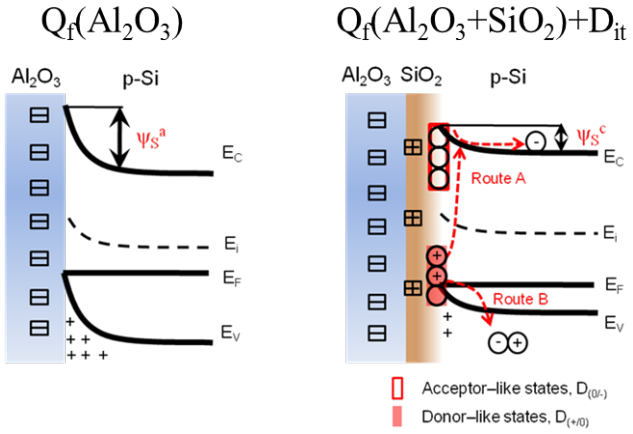

Fig 1. Electronic band structures showing the interface between Al_2O_3 and Si with the consideration of fixed charges and interface charges

[1] Jae-Won Song, J.Y Jung, H.D Um, Xiaopeng Li, M.J Park, Y.H Nam, S.M Shin, Tae Joo Park,* Ralf B. Wehrspohn,* and Jung-Ho Lee*. *Adv. Mater. Interfaces*, **1400010**(2014).

Atomic switch using electro-migration for a programmable logic circuit

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Recently, a programmable logic circuit, which allows flexible and timely development, has attracted a lot of attention. The atomic switch provides a reversible on/off, and has the potential to provide the dynamic programming of logic circuits, where circuits are re-programmed during operation, as well as static programming. The electrochemical atomic switch has shown smaller size, lower wiring resistance and shorter signal delay, while the conventional programming circuit has disadvantages such as slow speed and high power consumption due to the large size of the programmable switches.

Technology trend and application of atomic switches such as electrochemical switch and eFuse will be reviewed. The structure, programming mechanism, and reliability of the atomic switches will be covered as well. One notable progress in atomic switches is three-terminal atomic switch based on the gate-controlled nucleation of a metal cluster, where high on/off ratio and low power consumption have been demonstrated. The atomic switch was developed using fully CMOS compatible materials in the metal layers of CMOS. In terms of eFUSE reliability, a sensing circuit trip point consistent with the fuse resistance distribution, process variation, and device degradation in the circuit such as hot carrier or NBTI, as well as fuse resistance reliability must be considered.

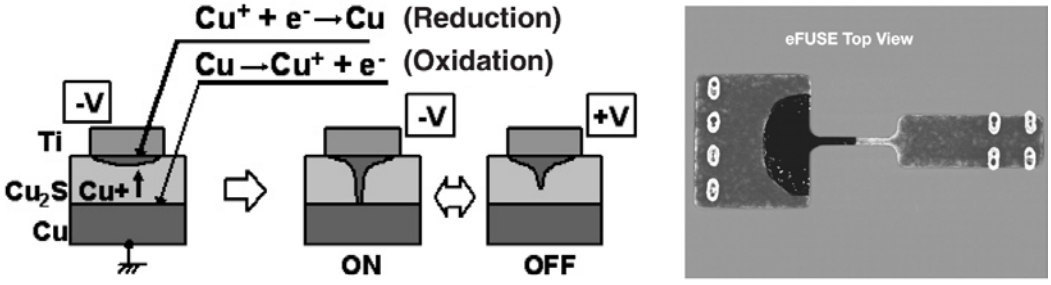

Fig 1. Atomic switch using metal ions in a solid electrolyte (left) and top view eFuse (right)

Nanoplasmonics for On-Chip Photonic Interconnection: Photodetection of Broadband Incoherent Light

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Photonic interconnects have emerged as an alternative to conventional electronic interconnection with their advantages such as design simplification and architectural and physical benefits [1]. However, feasible and practical component technologies are yet to be demonstrated to enable on-chip photonic integrated circuits. With unique properties originating from the localization of surface plasmons, metal photonics or plasmonics offers a promise of enabling novel photonic components and systems for highly efficient integrated solutions and on-chip photonics [2,3]. Nanoplasmonics, or plasmonics in nanometallic structures, provides material and dimensional compatibility with ultra-small silicon electronics and integrative functionalities such as light generation, concentration, and manipulation for integrated photonic applications [5,6].

Compared to long range optical communication, extremely short communication range and strong light-matter interaction for on-chip plasmonics allow us to extend beyond a conventional approach of integrating more expensive and complicated light source such as coherent and narrowband laser with silicon electronics. Such hybrid electronic and photonic interconnection desires a highly responsive on-chip photodetector to broadband incoherent light and more elegant design for nanoscale integration. As one of the enabling nanoplasmonic technologies, we demonstrate an ultracompact broadband photodetection with a greatly enhanced photoresponsivity using a ridge-like metallic nanostructure. The nanoridge photodetector confines a wide spectrum of electromagnetic energy in a nanostructure through the excitation of multiple plasmons, thus enabling detection of weak and broadband light for on-chip photonic interconnection.

This research was supported by the MSIP (Ministry of Science, ICT and Future Planning), Korea, under the “IT Consilience Creative Program” (NIPA-2014-H0201-14-1002) supervised by the NIPA (National IT Industry Promotion Agency).

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Strain-dependent Optical Properties of Ge Thin Films on Si Substrates Formed by Thermal Annealing

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Germanium (Ge) is a promising group-IV element for silicon (Si)-based optical interconnection at telecommunication frequency. Its application to optical component such as waveguide or modulator has been developed. However, Ge-based light emitting source has less been investigated due to several obstacles such as low efficiency and difficulty of frequency-matching at a proper wavelength. In this research, we suggest controlling tensile strain by thermal annealing method to achieve strain induced enhancement of photoluminescence (PL) by inducing direct–bandgap transition.[1] Tensile strain could be achieved by SiGe alloy at the interface resulted by thermal annealing. We performed temperature dependent PL and absorbance spectroscopy for samples with various annealing and etching conditions to characterize the optical properties of strained Ge-on-Si. We could clarify that the optical properties of Ge-on-Si can be modified by thermal annealing and etching method, and telecommunication frequency can be achieved by strain control. This research may suggest a new possibility of on-chip light source at a telecommunication frequency.

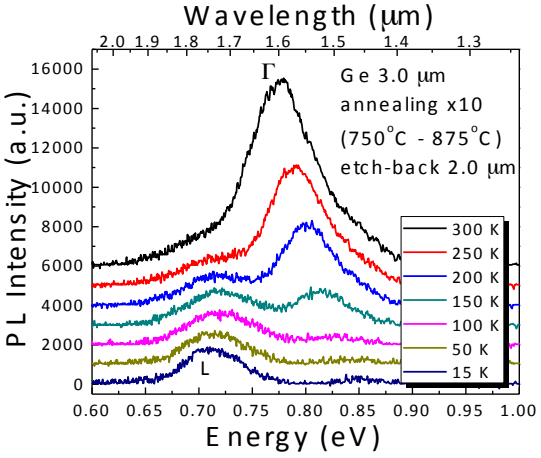

Fig 1. Temperature dependent photoluminescence spectra of thermally annealed and etched Ge

[1] T.-H. Cheng, et.al., Applied Physics Letters, 96,211108 (2010)

Raman depth profiles for non-linearly strained Ge-on-Si lasers

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Optical interconnection is projected to replace Cu wires as the data bandwidth exceeds the capability of chip-to-chip application processors. For compatibility with Si technologies, Ge layers hetero-epitaxially grown on Si substrates are appropriate platform for fabricating optical detectors and lasers for interconnection system [1]. Challenges of Ge-on-Si lasers include intrinsic characteristics of indirect band energy versus momentum. With a tensile strain applied to Ge, band structure is converted to the direct gap having minimum band offset at Γ valley [2]. In this work, we induced the tensile strain in the epitaxial Ge layers after post growth annealing at 25ºC to 850 ºC. Due to the difference of thermal expansion coefficients (TEC) of epitaxial films and substrates, the tensile strain increased from 0.14% for as-deposited to 0.24% after post annealing (XRD). For in-depth analysis with micro-Raman, strain distribution was measured repeatedly with subsequent etch-back processes. As the etch-back proceeded towards the Ge-Si interface, the tensile strain increased substantially. Non-linear strain distribution of out-of-plane Ge is presumably caused by higher impact of TEC at the Ge-Si interface. Another possible cause is SiGe formation during post growth annealing, which should be taken into account to the increase in the tensile strain. With comprehensive physical characterizations of epitaxial Ge-on-Si, we have demonstrated tunable Ge tensile strain for the applications of optical sources.

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벤젠을 이용한 그래핀의 저온 합성 및 배선 특성

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그래핀은 이차원 구조의 벌집 격자로 배열된 탄소나노 소재로, 우수한 전기적, 광학적, 화학적, 물리적 특성으로 인해 실리콘 및 구리 배선을 대체할 차세대 전자소재로 각광받고 있다[1]. 2004 년 그래핀의 발견 이후, 화학 기상 증착법(chemical vapor deposition, CVD)을 이용하여 대면적으로 고품질 그래핀을 합성하는 연구가 활발히 진행되고 있다. 그러나 메탄 및 에틸렌 가스 등의 기체 탄소소스를 이용한 CVD 방법은 고온 (800-1000 °C)에서 그래핀을 합성하기 때문에 반도체 소자 위에 직접 그래핀 합성 시 소자에 물리적 손상을 일으킬 수 있는 문제가 있다. 따라서 본 연구에서는 저온에서 CVD 방법을 이용하여 그래핀을 합성하고, 구리/그래핀의 배선 특성을 연구하고자 한다. 그래핀과 유사한 방향족 탄화수소인 벤젠을 탄소 소스로 이용하여 500 °C 이하의 저온에서 고품질의 그래핀을 합성하였다[2]. 또한 구리 배선 위에 직접 그래핀을 합성하여 구리/그래핀 적층 구조의 배선을 제작하고, 구리/그래핀 배선의 전기적 특성을 연구하였다.

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Nonvolatile Memory Cell Composed of Oxide Thin-Film Transistors and Ferroelectric Memory Transistors for Low-Power Reflective LCD Panels

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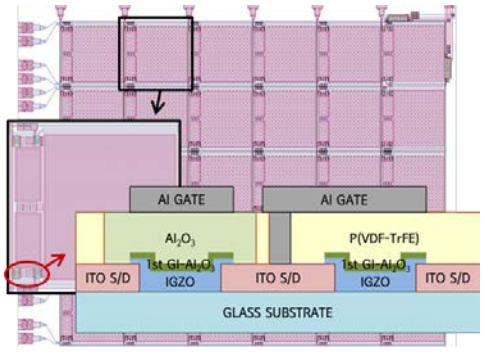
Nonvolatile memory cells integrated in a pixel of liquid crystal display (LCD) panel have been developed for a low-power driving. However, conventional memory cell with multiple devices occupies a larger footprint and do not provide a nonvolatility. In this work, a new type of a low-power LCD pixel circuit composed of two oxide thin-film transistors (Ox-TFTs), two ferroelectric memory TFTs (Fe-MTFTs), and two capacitors was proposed and fabricated. The organic ferroelectric poly(vinylidene fluoride-trifluoroethylene) was employed as a main gate insulator (GI) to realize nonvolatile memory characteristics in the Fe-MTFTs. In the Ox-TFTs, Al_2O_3 layer is prepared as a main GI. In both TFTs, In-Ga-Zn-O was employed as an active channel. Figure 1 shows the top-view of the proposed LCD pixel layout and the schematic cross-sectional diagram of the fabricated memory cell. Figure 2 shows drain current-gate voltage characteristics of the Ox-TFT and Fe-MTFT, respectively. For the Ox-TFT, the field-effect mobility, subthreshold swing, and on/off raio were estimated to be approximately 11.9 $cm^2V^{-1}s^{-1}$, 0.29 V/dec, and 6.03×10^7, respectively. Furthermore, a large memory window was obtained to be 8 V with a gate voltage sweep from -14 to 12 V for the Fe-MTFT. Both Ox-TFT and Fe-MTFT were successfully fabricated without any critical damages even after the full integration processes. The feasiblilty of low-power operation of reflective LCD panel and the detailed results of driving operations will be discussed.



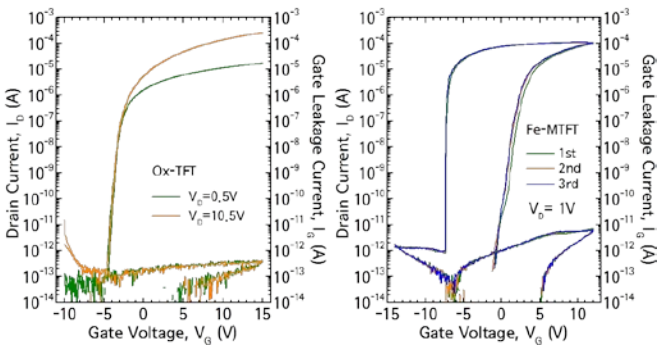


Fig.1 (Left) Top-view of the proposed LCD pixel and schematic cross-sectional diagram of the fabricated devices.
Fig.2 (Right) Transfer characteristics and gate leakage currents of Ox-TFT and Fe-MTFT.

An AMOLED Display Pixel Structure to Compensate Variations in Mobility and Threshold Voltage of Poly-Si TFTs in Every Gray Level

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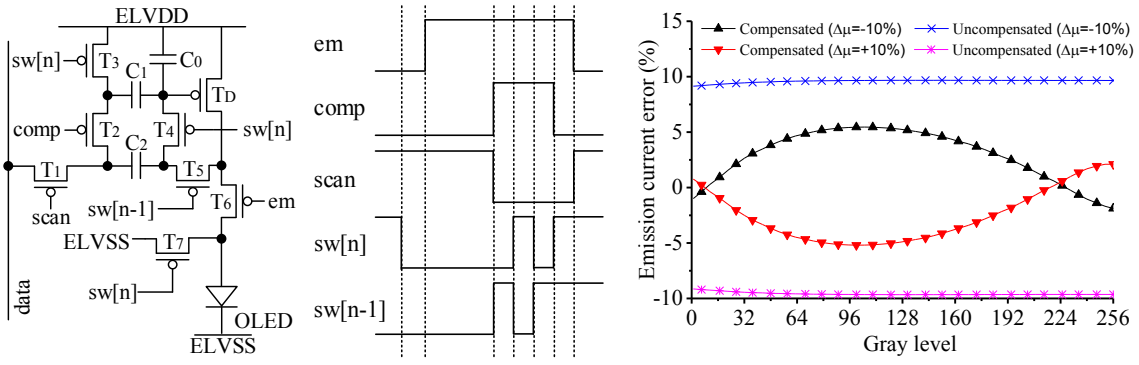
The image quality of active matrix organic light emitting diode (AMOLED) display using poly-crystalline silicon (poly-Si) thin-film transistor (TFT) backplane is heavily influenced by the variations in the threshold voltage (ΔV_{th}) and mobility ($\Delta\mu$) of poly-Si TFTs. A pixel structure for compensating ΔV_{th} and $\Delta\mu$ has been researched [1], but the compensation capability for $\Delta\mu$ varies according to the gray levels because the compensation is optimized only at the single gray level. To solve the aforementioned problem, we proposes a pixel structure which can compensate $\Delta\mu$ in every gray level. The proposed pixel structure in Fig. 1 (a) with the driving timing diagram in Fig. 1 (b) compensates not only ΔV_{th} by using the diode-connection of T_D, but also $\Delta\mu$ by storing the current difference caused by $\Delta\mu$ of T_D. The compensation voltage (V_{comp}) is generated by the current of T_D and stored in the compensation capacitor (C_2). Then, V_{comp} is controlled by adjusting the current of T_D in the proposed pixel structure according to the gray levels, and thereby $\Delta\mu$ can be compensated in every gray level. The simulation result in Fig 1 (c) shows that the proposed pixel structure improves the maximum emission current error from $\pm$9.8% to $\pm$5.4% in every gray level when $\Delta\mu$ of T_D is $\pm$10%. Therefore, the proposed pixel structure is suitable for improving the image quality by compensating $\Delta\mu$.



(a) (b) (c)

Fig 1. (a) Schematic, (b) timing diagram, and (c) simulation results of proposed pixel structure

[1] J.-S. Na, and O.-K. Kwon, Jpn. J. Appl. Phys. 53, 03CD01 (2014)

Fabrication of Integrated Febry-Perot Type Color Reflector for Reflective Display

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Improving reflectance of color reflectors has been a main issue for the development of reflective type displays[1]. Structual color reflectors such as Fabry-Perot type cavity reflecor and distrubted bragg refelctor (DBR) have better reflectances compared with those made with color filters. But, structural color reflectors are very difficult to fabricate as an integrated reflector, which has red/green/blue 3 primary colors as sub-pixels. In present study, we designed Fabry-Perot type color reflecor and architectured simple fabricaiton processes based on the standard Si technology. The integrated Fabry-Perot type color reflectors, which have red/blue/green sub-pixels in a single substrate, have been successfully fabricated. An Ag metal film was used as a bottom reflecting layer, silicon oxide thin films were used as cavity layers and a thin W film was used as a half reflective layer for Fabry-Perot type cavity. To minimize the variation of the cavity length, a differential deposition scheme was applied for the silicon oxide deposition processes. The color reproducibility of the fabricated color reflector was ~17% of the NTSC(National Television System Committee) standard and the average reflectance was >45%.

(a) (b)

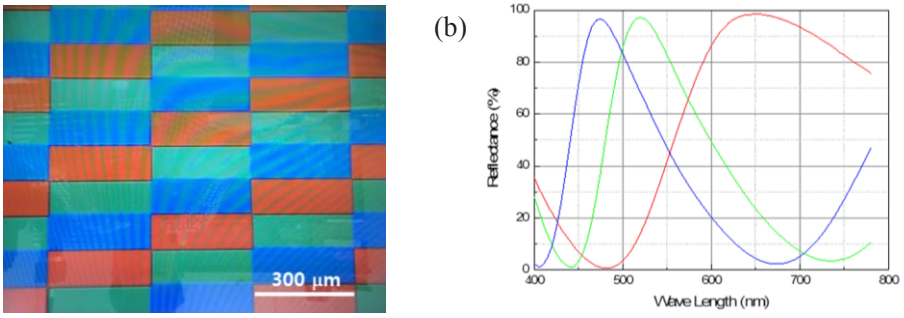

Fig 1. The optical microscope image of the fabricated color reflector(a) and the color spectra of the each color pixels(b).

[1] D. Chung, C. Shin, B. Song, M. Jung, Y. Yun, S. H. Nam, C. Noh and S. Lee, Appl. Phys. Lett., **101**, 221120 (2012)

The Solution of Electric Power Reduction in the Capacitor-less LED Driver Circuit

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LED조명에서 High-power LED(고전력 발광소자)의 효율적인 열전달을 위해 COB(Chip on Board)형태의 구조들이 개발 되었으며[1]-[2], 5만시간 이상의 수명시간(life time) 보장할 목적으로 <그림-1>과 같이 전해 커패시터(capacitor)가 없는 단일칩을 이용한 회로들이 개발되고 있다. <그림-1>은 Lumens사의 단일칩을 사용하여 설계된 전해 커패시터가 없는 LED driver와 LED 모듈을 포함한 LED조명으로 총 소비전력은 9.5W이다.

<그림-2>는 1차로 제작된 전해 커패시터가 없는 LED driver로 BJT와 NMOSFET이 각각 5개로 구성된 5단 회로로, LED 디밍(dimming)이 가능하지만 <그림-4>에서 보는 바와 같이 초기전력 P_1=15W를 기준으로 약 600초 이후 P_2=6W로 감소하여 소비전력 변화률 Δ_P=60%인 전력감소문제가 발생하였으며, 이는 BJT로의 전류주입에 의한 BJT 발열 및 이로 인한 베이스(base)와 에미터(emitter) 사이의 전압 Vbe의 감소로 인해 NMOSFET이 ON되는 시간의 감소로 발생된 것이다.

<그림-3>은 전력감소 문제을 해결하고자 BJT로의 전류주입을 감소시킬 목적의 베이스 저항 R_B와 발열에 의한 Vbe 감소를 좀 더 줄이고자 제너다이오드를 추가하여 제작된 2차 LED driver(4단 회로)로 약 30W급 LED 모듈을 구동할 수 있으며, PCB 반경 r=20mm이고, 모든 부품이 SMT(surface Mount Technology)로 구성되었다. 초기전력 P_1=15W를 기준으로 약 600초 이후 P_2=17.3W로 증가하여 소비전력 변화률 Δ_P=15.3%으로 개선하였다. <표-1>은 25W급의 소비전력을 가지는 LED module 구동을 하는 데, 보다 저가격으로 구성할 수 있는 하이브리드 방식으로 제작된 전해 커패시터가 없는 LED driver 구동회로의 특성을 구분하여 나타낸 표로 기존 60%에서 15.3%로 전력감소문제를 개선하였고 Driver의 자체전력과 98%의 고효율을 가지고 있음을 보여주고 있다.

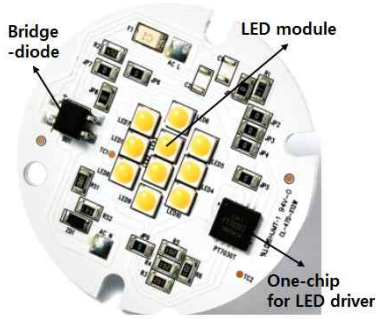

그림 1. L사의 통합 Capacitor-less LED driver와 LED module (구동(소비)전력=9.5W)

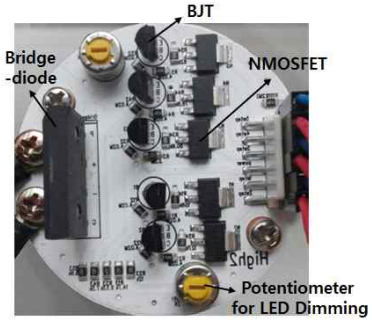

그림 2. 초기 제작된 하이브리드 방식의 Capacitor-less LED driver (1차 5단 회로, 구동(소비)전력=25W)

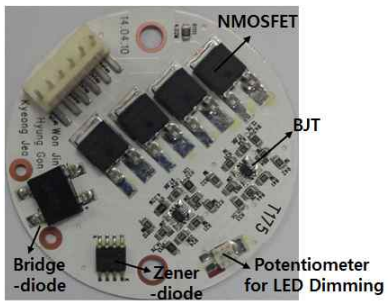

그림 3. 전력감소 해결한 하이브리드 방식의 Capacitor-less LED driver (2차 4단 회로, 구동(소비)전력=25W)

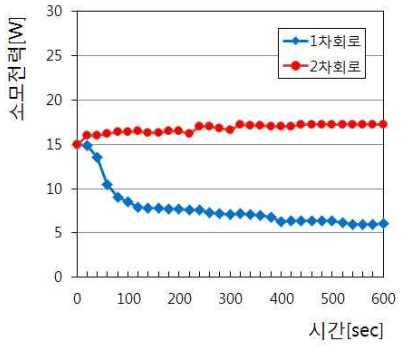

그림 4. 1차 및 2차(개선) 구동회로를 사용한 LED조명의 소모전력 변화도표

표 1. 1차(초기) 및 2차(개선) LED driver 비교표

Capacitor-less LED driver		1st	2nd
LED contorl stage		5	4
Base Resistance[Ω]	R_B	0	2M
Zener Diode	Dz	X	O
초기소비전력(@t=0sec)[W]	P_1	15	15
나중소비전력(@t=600sec)[W]	P_2	6	17.3
전력변화율(%)	Δ_P	60	15.3
LED driver 소모전력[mW]	P_d	118	343
소비전력효율(%)	E_P	98.03	98.02

[1] Mi-Hee Jee, Choong-Mo Nam, High Power LED Packaging by MOAMP(Multichip On Aluminum Metal Plate) Technology, The 17th Korean Conference on Semiconductors, 106 (2010).
[2] Mi-Hee Jee, Choong-Mo Nam, Multi-chip On Aluminum Metal Plate Technology for High Power LED Packaging. Journal of Measurement Science and Instrumentation, 297-299. (2010).

Inverted organic light-emitting diodes using various types of solution-processable ZnO for efficient electron injection

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Compared to a conventional organic light-emittind diodes (OLEDs), inverted OLEDs have more advantages in the interconnection between the bottom cathode of the OLED and the drain line of the thin-film transistors (TFTs) of the display backplane, because the backplane is generally manufactured using n-type TFTs based on a-Si or oxides [1]. However, due to the high work function of indium-tin-oxide (ITO) based bottom electrodes, electrons hardly injected into the electron transporting organic material. Therefore, efficient electron injection layer (EIL) is required to achieve high efficiency in the inverted OLEDs. In this work, we compared the effect of various types of ZnO on the electron injection efficiency by using ZnO nanoparticles, sol-gel processed ZnO, and n-doped ZnO. The devices showed reduced turn-on voltages, high luminance and efficiency with ZnO EIL. Also, we enhanced the device performance by doping various n-type materials into ZnO. Systematic study and discussion on the properties of the EIL using various types of ZnO will be presented in this work.

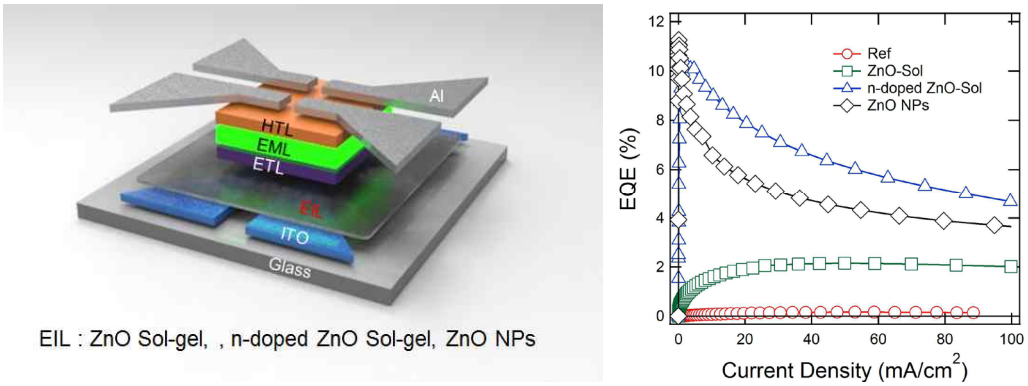

Fig 1. Device structure and the external quantum efficiency using various types of ZnO EIL

[1] H. Lee, I. Park, J. Kwak, D. Y. Yoon, and C. Lee, Appl. Phys. Lett. 96, 153306 (2010).
[2] This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF-2011-0022716) funded by the Ministry of Education.

The Influence of Variability Sources on SRAM Stability in 90 Å Non-rectangular Bulk FinFET SRAM cell

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The device degradation caused by statistical variability sources (WFV, RDF, and LER) has been one of the primary bottleneck for aggressively scaled Bulk FinFET. This cause variation in SRAM read static noise margin (RSNM), which results in SRAM instability [1],[2]. In this paper, the influence of temperature variation for above three variability sources on SRAM stability was investigated in 90 Å non-rectangular Bulk FinFET SRAM cell. Fig. 1 (a) shows variation in the butterfly curves in presence of all variability sources at 375K. Fig. 1 (b) shows RSNM distribution in presence of all variability sources at two temperatures. In addition, Fig. 1 (c) shows σ(RSNM) in presence of each variability source as a function of temperature. From the Fig. 1 (c), it can be known that RDF is the most dominant variability source. It is also shown that σ(RSNM) by WFV and RDF decreases with temperature due to the less influence from electron energy barrier variation by WFV and RDF near the source, whereas σ(RSNM) by LER increases with temperature due to the increase of scattering event with LER by increased electron kinetic energy.

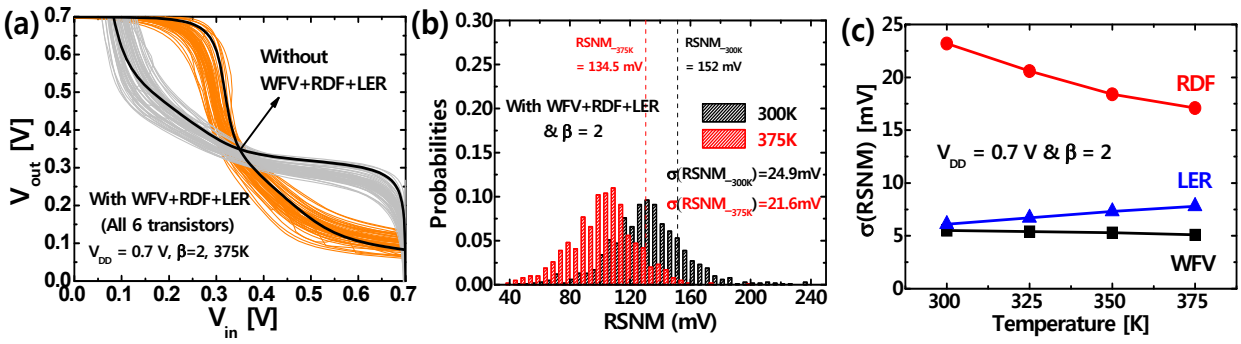

Fig. 1. (a) Butterfly curve variation at 375K, (b) RSNM distribution in presence of three variability sources at two temperatures (300 & 375K), and (c) σ(RSNM) in presence of each variability source with various temperatures

Acknowledgement

This work was supported by Samsung Electronics Corporation, and CISCO Research Center.

[1] R.-H. Baek et al., *SISPAD*, 2012, pp. 105-108.
[2] Andrew R. Brown et al., *IEEE Trans. Electron Devices.*, Vol. 60, no. 11, pp. 3611-3617, 2013.

Analysis of Structural Variation in 10-nm Double Gate-All-Around (D-GAA) Transistor with Asymmetric Channel Width

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The scaling limits of CMOS technology make it hard to follow the Moore's law, which requires novel device structures to increase gate controllability and suppress the short channel effects (SCEs) [1]. Beyond 10 nm technology node, the gate-all-around (GAA) FET is considered as a promising solution for continuing the Moore's law [1]. However, it was revealed that a conventional top-down process produces asymmetric channel structure [2]. We investigated the electrical characteristics of double-gate-all-around (D-GAA) transistor with asymmetric channel width using 3D TCAD device simulation. The D-GAA has two gate terminals, inner and outer gate, and the gates can either be tied together to enhance device performance or be controlled independently for threshold voltage (V_{th}) modulation. Two types of D-GAA structure are investigated as shown in Fig. 1, (a) Big-Source Small-Drain (BSSD) and (b) Big-Drain Small-Source (BDSS). Variations of the diameter of nanowire in topmost and bottommost are same value but opposite sign, thus silicon channel maintains same area with nominal cylindrical channel. As shown in Fig. 1(c) and (d), variations in source and drain side have different effect on the electrical properties. I_{off} becomes better (less leaky) in both structures as the diameter variation gets larger. On the other hand, I_{on} improves only when the source side becomes wider (i.e., BSSD) but degrades by the smaller source side diameter (BDSS). As a result, BSSD structure (Fig. 1(a) and (c)) is expected to be preferable structure in terms of providing greater current drivability and maintaining lower off-current. Our ongoing work seeks to analyze the impact on the circuit-level (or logic-level) property by the asymmetric channel width variation and to find the optimal channel shape both in the performance and the leakage.

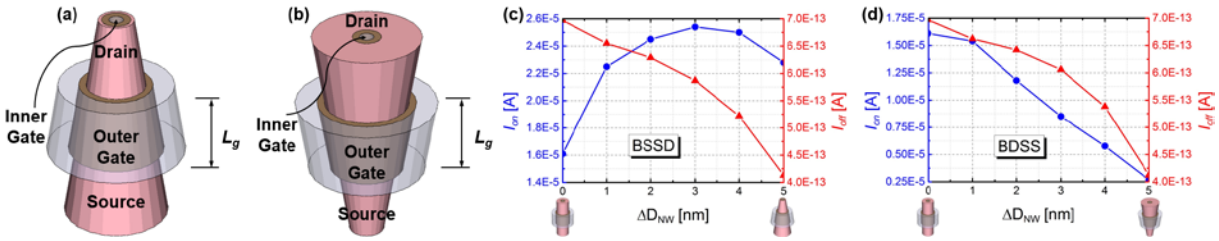

Fig. 1. D-GAA FET structure used in device simulations and the results. Structures of (a) BSSD, (b) BDSS, simulation results of (c) BSSD, and (d) BDSS.

[1] H. M. Fahad and M. M. Hussain, *Scientific reports* 2, (2012).
[2] S. Sato, K. Kakushima, K. Ohmori, K. Natori, K. Yamada, and H. Iwai, *Applied physics letters*, vol. 99, no. 22 (2011).

Analysis of Current Fluctuation Due to Trap in Nano-scale Bulk FinFETs

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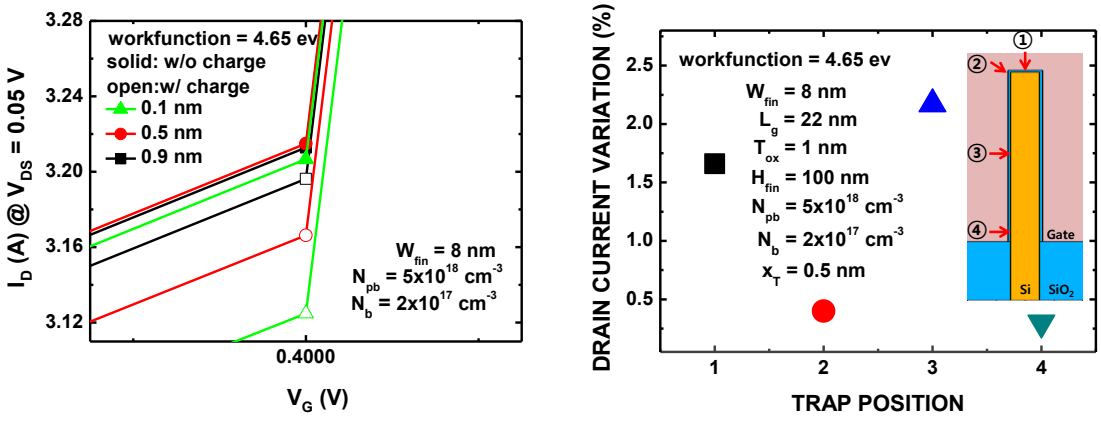
Recently, continual transistor scaling has led to the demonstration of sub-20 nm CMOS devices using transistor structures such as tri-gate bulk FinFET [1]. As transistors scales down, drain current fluctuation (ΔI_D) due to trap and detrap of an electron becomes significant. The behavior of RTN in SOI FinFETs depending on the trap position has been reported [2]. But the behavior has not been reported in bulk FinFET. In this work, we investigate ΔI_D by trapping and detrapping of one electron in Bulk FinFET using commercial TCAD simulator: SILVACO ATLAS. Fig. 1(a) shows the change of I_D-V_G of 22 nm bulk FinFET according to trap depth (x_T) in the gate oxide on the top of the fin body. Here, the fin body doping (N_b) is uniform (2×10^{17} cm^{-3}). The punchthrough stopper located at 110 nm from the fin top has a peak concentration (N_{pb}) of 5×10^{18} cm^{-3}. The V_{th} of the device is 0.35 V. The smaller x_T gives the larger ΔI_D, because an electron trapped at a shallower trap affects more significantly induced channel carrier density. Fig. 1(b) shows the dependence of ΔI_D on the position of a trap placed on the surface of fin body. The trap located in the middle-side of FinFET (position '3' in the inset) gives the biggest ΔI_D, since an electron trapped at the position '3' decreases induced electron density under the trap as well as the induced eletron density in the channel facing each other.



(a) (b)

Fig 1. (a) Drain current change in I_D –V_G curves of 22 nm bulk FinFET as a parameter of trap depth (x_T). (b) Dependence of ΔI_D on the position of a trap on the fin body.

[1] S.-Y. Wu et al., IEDM, p.973, (2013).
[2] M. L. Fan et al., IEEE Trans on Electron Devices, vol. 59, p. 2227, (2012).

Acknowledgement:
This work was supported by the Brain Korea 21 Plus Project in 2014 and the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186)

Hump characteristics generated by bias stress in a-IGZO TFTs

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a-IGZO TFTs have considered as promising AOS materials for TFTs because of their high mobility, exellent uniformity, and low temperature process [1]. But, their instabilities with bias/temperature/illumination stress should be guaranteed for stable operation in swithcing and driving TFTs. Hump effect among them is observed subthreshold and operating region with high bias stress. Although some group has studied about hump effect in subthreshold region in view of edge effects or backchannel conduction [2], it in operating region has been seldom studied. It should be investigated clearly due to possibility to cause unexpected pixel signal of current-driven AMOLED displays. In this work, hump effect in operating region under positive bias stress was investigated. We propose that the hump effect can be caused by the local electron trapping in gate insulator near source overlapped region, which is directly modulated by high gate bias. This phenomenon can be modeled as series connection of two transistors consisting of main and parasitic transistors. The parasitic transistor has higher threshold voltage and shorter channel length than main transistor due to more electron trapping in gate insulator. The proposed mechanism was verified by various measurements and Technology Computer-Aided Design simulation.

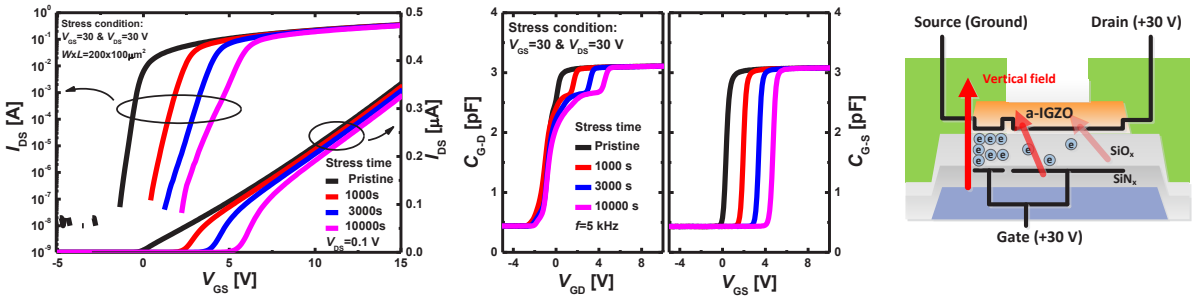

Fig 1. (a) Transfer characteristics and (b) *C-V* characteristics under V_{GS}=V_{DS}=30 V stress in a-IGZO TFTs. (c) Schematic view of a-IGZO TFTs for the proposed mechanism

This work was supported by BK+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No: 22A20130000042) and in part by IC Design Education Center (IDEC).

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The Statistical Distribution of Electrical Characteristics with Random Grain Boundary in Vertical NAND Unit Cells

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3D Vertical NAND (V-NAND) flash memory has been developed for ultra-high density. The V-NAND flash memory use a polysilicon (poly-Si) channel which has grain boundary (GB) issues, in terms of subthreshold swing (SS) degradation and threshold voltage (V_{th}) variation. However, the GB is randomly located in poly-Si channel and the shape of GB is also different, causing the V_{th} and SS distribution in V-NAND unit cells [1].

In this work, using TCAD Sentaurus (Synopsys Co, Ltd.), we simulated 100-samples of V-NAND unit cells with random grain boundary. The relation of V_{th} and SS shows a positive correlation as shown in Fig.1(b). Even though the V_{th} (or SS) values of different samples are same, the SS (or V_{th}) values can be different. This is because different GBs can induce similar peak and dissimilar portion of conduction energy band profiles, resulting from the random location and shape of GBs.

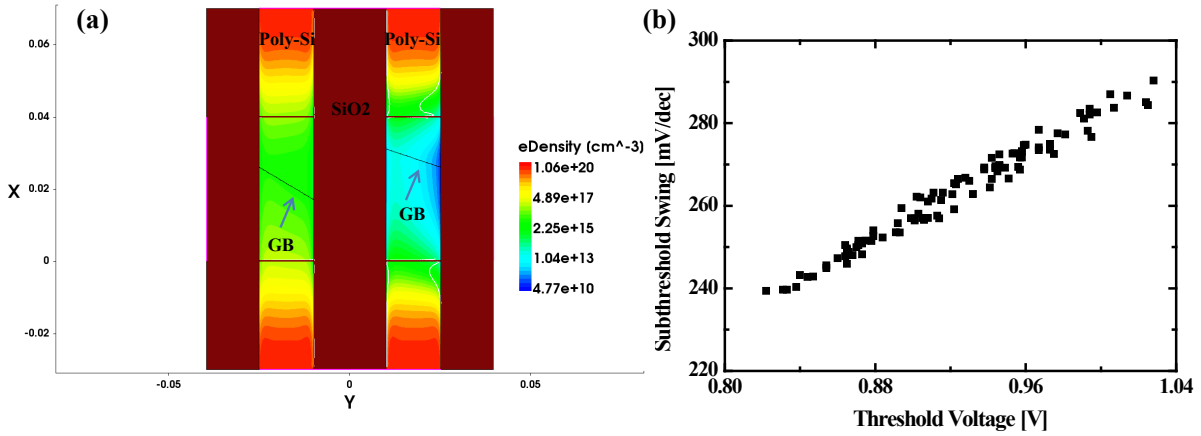

Fig 1. (a) The schematic of Vertical NAND (V-NAND) unit cell with random grain boundary and (b) I_d-V_g characteristics of 100-samples.

[1] Y.-H. Husiao, et al, IEEE Trans. Electron Devices, Vol. 61, No.6, (2014).

Interconnect line-induced 1/f noise in printed circuit board (PCB)

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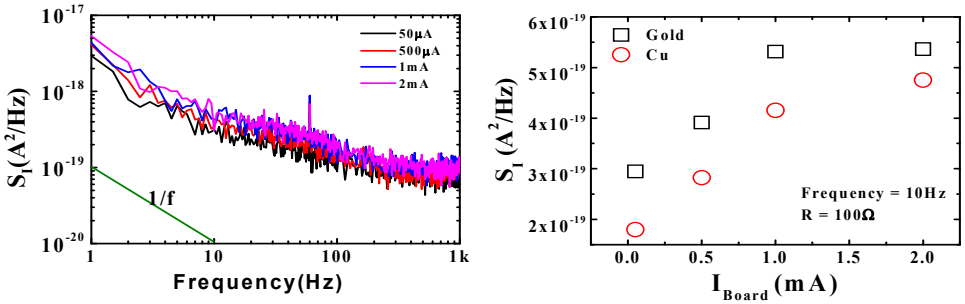
1/f noise of active and passive devices is known as one of the key factors which determine the performance of analog circuit or analog system. For example, in case of an amplifier, there is always a limit to the smallest signal that can be amplifed because of electronic noise [1]. For this reason, the analysis of the 1/f noise and its suppression are highly necessary to design high quality analog circuits. In general, MOSFETs, poly-silicon gates, and interconnection lines contribute to the 1/f noise in analog circuits [2]. However, there has been little study on the 1/f noise of interconect lines in printed circuit board (PCB) where many kinds of analog chips are implemented and connected. In this paper, we studied the 1/f noise charcterstics of intereonnect lines in PCB. It is shown that 1/f noise happens at the PCB level interconnect lines as shown in Fig. 1(a). When the applied voltage increases, power spectral density (PSD) of noise current increases as shown in Fig. 1(b). It is also shown that 1/f noise of interconnect line depends on the material type of metal lines as in Fig. 1(b). This study will be helpful in understanding the 1/f noise characteristics of metal lines in PCB and will also give insight into the design of low noise electronic system [3].



(a) (b)

Fig. 1. (a) 1/f noise characteristics of PCB metal lines and (b) its dependence on the metal material.

Acknowledgment: This work (Grants No. C01910840100415260) was supported by Business for Cooperative R&D between Industry, Academy, and Research Institute funded Korea Small and Medium Business Administration in 2015.

[1] W. Marshall Leach JR. “Fundamental of Low-Noise Analog Circuit Design”, Proceedings of the IEEE, Vol. 82, Issue 10, pp 1514-1538, October 1994.
[2] M. A. Elgamel M. A. Bayoumi, “Interconnection Noise Analysis and Optimization in Deep Submicron Technology”, IEEE Circuits and Systems Magazine, pp. 6-12, Fourth Quarter 2003.
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Evaluating the Top Electrode Material for Achieving an Equivalent Oxide Thickness Smaller than 0.4 nm from an Al-doped TiO_2 Film

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Al-doped TiO_2 (ATO) has been extensively studied as the most promising capacitor dielectric material for the next generation dynamic random access memory (DRAM) with design rule of ~ 20 nm owing to its excellent leakage property as well as high dielectric constant. However, with ATO, the minimum equivalent oxide thickness (EOT) with the acceptable leakage current density (< 10^{-7} A/cm^2 at 0.8 V) was limited at about 4.5 Å, which was achieved a structure composed of RuO_2 (bottom electrode)/ ATO / Pt (top electrode). The simulated current density vs. EOT relationship based on quantum mechanical tunneling on the above structure, indeed, showed EOT of 4.4 Å at the leakage current density of 10^{-7} A/cm^2 at 0.8 V. Therefore, an alternative method to improve the dielectric performance is necessary.

The effects of Pt and RuO_2 top electrodes on the electrical properties of capacitors with Al-doped TiO_2 (ATO) films grown on the RuO_2 bottom electrode by an atomic layer deposition method were examined in this manner. The rutile phase ATO films with high bulk dielectric constant (> 80) were well grown due to the local epitaxial relationship with the rutile structured RuO_2 bottom electrode. However, the interface between top electrode and ATO was damaged during the sputtering process of the top electrode, resulting in the decrease in the dielectric constant. Post-metallization annealing at 400 ºC was performed to mitigate the sputtering damage. During the post-metallization annealing, the ATO layer near the RuO_2 top electrode/ATO interface was well-crystallized because of the structural compatibility between RuO_2 and rutile ATO, while the ATO layer near the Pt top electrode/ATO interface still exhibited an amorphous-like structure. Despite the same thickness of the ATO films, therefore, the capacitors with RuO_2 top electrodes showed higher capacitance compared to the capacitors with Pt top electrodes. Eventually, an extremely low equivalent oxide thickness of 0.37 nm with low enough leakage current density (<10^{-7} A/cm^2 at 0.8 V) for the next-generation dynamic random access memory was achieved from ATO films with RuO_2 top electrodes.

Influence of Reduced Al-Doping Concentration with Modified Atomic Layer Deposition Recipes on Electrical Properties of TiO_2 Films

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Rutile TiO_2 thin films were grown on Ru surface even at 250 °C with atomic layer deposition (ALD) using $Ti(OC_3H_7)_4$ and O_3.[1] However, high dielectric TiO_2 thin films have limitation of high leakage current because of low Schottky barrier height resulting from the n-type nature of the rutile TiO_2.[2] So, Al-doped TiO_2 (ATO) thin films have been studied for improving leakage current problems because Al dopants make acceptor level.[3] In ALD system, the Al doping concentrations were controlled by inserting Al_2O_3 layer into the TiO_2 films discretely. Inserted Al_2O_3 layer blocks epitaxial growth of rutile TiO_2, so anatase TiO_2 peaks appear in XRD pattern and film dielectric constant decrease. Therefore, we need to optimize ATO thin films which are suitable for DRAM capacitor. For this reason, we use modified ALD recipes like Fig. 1 (a), (b), (c) which limit Al doping site for finer concentration control.[4] In the modified recipes, $Ti(OC_3H_7)_4$ is pre-feeding or co-feeding for occupying several deposition site. Then, Al doping site will decrease and film electrical properties change like Fig. 1(e). Through fine adjustment of ALD recipes, we can expect small equivalent oxide thickness and low leakage current ATO thin films for DRAM capacitor.

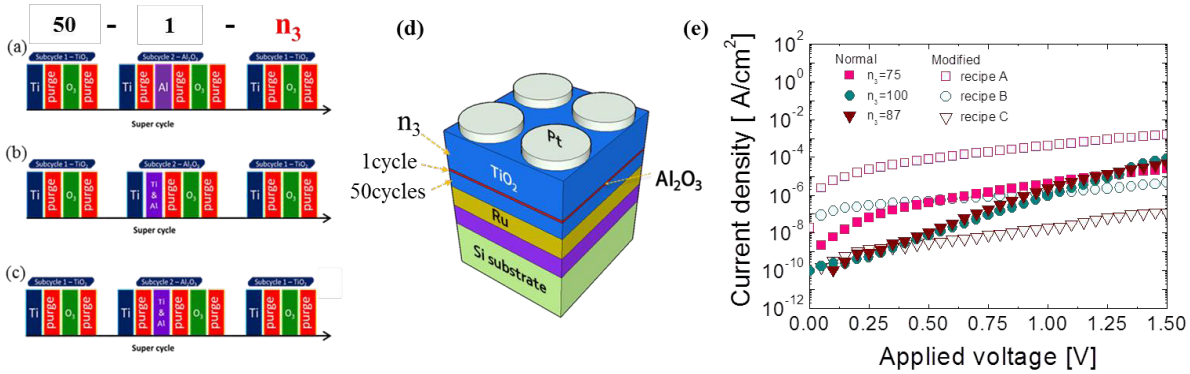

Fig 1. Modified ALD recipes (a), (b), (c) and (d) ATO MIM capacitors (e) I-V plot

[1] S. K. Kim, W. D. Kim, K. M. Kim, and C. S. Hwang, Appl. Phys. Lett. **85**, 4112 (2004).

[2] S. K. Kim, S. Y. Lee, M. Seo, G. J. Choi, and C. S. Hwang, J. Appl. Phys. **102**, 024109 (2007).

[3] W. J. Jeon, S. H. Rha, W. Lee, Y. W. Yoo, C. H. An, K. H. Jung, S. K. Kim, and C. S. Hwang ACS Appl. Mater. Interfaces, **6** (10) (2014).

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Atomic Layer Deposition of Chalcogenide Films using Novel Ge Precursor

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Phase change random access memory (PCRAM) is one of the strongest candidates for next-generation high density non-volatile memory. In fabricating PCRAMs with a design rule under 20nm, atomic layer deposition (ALD) of the phase changing chalcogenide materials is indispensable. The authors reported ALD of materials with compositions lying on the $GeTe_2$-Sb_2Te_3 pseudobinary tie line using $Ge(OCH_3)_4$, in which Ge is in the +4 oxidation state, and $((CH_3)_3Si)_2Te$ as the Ge- and Te-precursors, respectively[1].

In this report, novel precursor $HGeCl_3$, in which Ge is in the +2 oxidation state, was used to develop ALD process for chalcogenide films. First, GeTe film was deposited using $HGeCl_3$ and $((CH_3)_3Si)_2Te$ as Ge- and Te-precursors, respectively. ALD saturation behavior with increasing precursor feeding/purge time was confirmed. Smooth film with low impurity level was obtained by stoichiometric reaction.

Second, in the try to make GeTe-Sb_2Te_3 pseudobinary film using new GeTe deposition process combining with Sb_2Te_3, the authors found that novel Ge precursor reacts with Sb_2Te_3 to make Ge-richer film without increasing impurity level. To utilize the reaction, chalcogenide films were treated to make diverse compositional films. Resultingly, the authors make $Ge_2Sb_2Te_5$ film by treating $GeTe_2$-Sb_2Te_3 pseudo binary film.

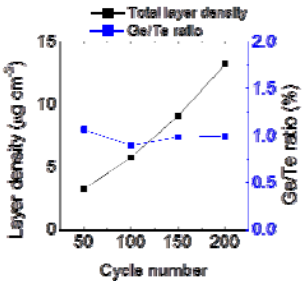

Figure 1 Growth rate of stoichiometric GeTe film

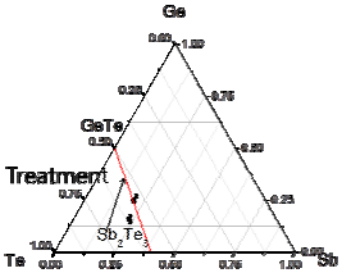

Figure 2 $Ge_2Sb_2Te_5$ film formation by $HGeCl_3$ treatment on $GeTe_2$-Sb_2Te_3 pseudo binary film

[1] Eom, T. et al., *Chem. Mater.*, 24, 2099 (2012)

Conformal formation of $Ge_2Sb_2Te_5$ film for phase change memories realized by controlling non-ideal behaviors of ALD.

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Phase change random access memory (PCRAM) is one of the strongest candidates for next-generation high density non-volatile memory. In the case of phase changing chalcogenide materials, which are most typically the $Ge_2Sb_2Te_5$ (GST) compounds, fabrication of ultra-high density phase change memory (>> 1 Gb) depends heavily on the thin film growth technique. Atomic layer deposition (ALD) at low temperatures is the most preferred growth method for depositing such complex materials over surfaces possessing extremely narrow holes. However, the investigation of GST ALD has been hindered by the non-ideal behaviors for the ALD-type reaction, and the non-availability of a Ge precursor with an oxidation state of +2 to form GeTe.

In this study, $Ge(OCH_3)_4$, $Ge(OC_2H_5)_4$, $Sb(OC_2H_5)_3$, $[(CH_3)_3Si]_3Sb$, and $[(CH_3)_3Si]_2Te$ metal-organic precursors were used to deposit various phase change materials with compositions lying on the $GeTe_2$–Sb_2Te_3, Sb_2Te_3-Sb, and $GeTe_2$-Sb_5Te_3 tie lines shown in Fig. 1 (a). While the incorporation of an Sb in $Sb(OC_2H_5)_3$ and Te in $[(CH_3)_3Si]_2Te$ into the film occurred in a genuine ALD manner, that of the Ge in $Ge(OCH_3)_4$ and $Ge(OC_2H_5)_4$, Sb in $[(CH_3)_3Si]_3Sb$ was governed by an non-ideal manner.

In spite of the non-ideal ALD behaviors, a conformal GST film was deposited by combining $GeTe_2$ and Sb_5Te_3 processes as shown in Fig. 1 (b). More detailed study revealed that such conformality of the $GeTe_2$ layer was due to the sub-monolayer level Ge adsorbate. The formation of sub-monolayer Ge was possible through the dynamic balance between the ad- and de-sorption of Ge. Additionally, the limited incorporation of Sb at the surface region has facilitated the formation of conformal Sb_5Te_3 layer.

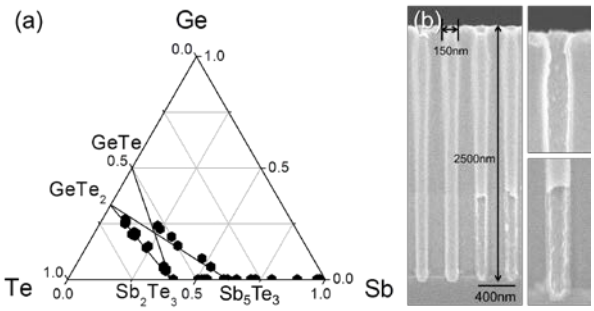

Figure 1 (a) Ternary phase diagram for Ge, Sb, and Te. Black dots represent actual thin film samples prepared by ALD. (b) SEM image of $Ge_2Sb_2Te_5$ film deposited in contact hole.

Electronic type Self-rectifying Resistive Switching Memory with Excellent Uniformity and Multi-level Functionality in Pt/Ta_2O_5/HfO_{2-x}/Ti Structure

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Although resistance switching random access memory (ReRAM) has attracted a great deal of attention as one of the most promising next-generation non-volatile memory devices, it has several obstacles to overcome presently to be used in mass-production. Among them, development of RS memory cell which contains rectification functionality in itself, highly reproducible RS performance, multi-level functionality and electroforming-free characteristics are the impending tasks. The method for solving these problems can be generally stated as having a two-layered dielectric structure, where one layer (in this case HfO_2) works as the resistance switching layer by changing its chemical state, while the other dielectric layer (in this case Ta_2O_5) remained intact during the whole switching cycle, which provides the rectification. Also, new feasible operation method is proposed which occurred not conventional bipolar RS which is occurred by ionic switching mechanism but just electronic switching.

The present combination of the Ta_2O_5 and HfO_2 layers, which were in contact with the Pt and Ti, respectively, is the most appropriate structure for achieving the feasible self-rectifying RS system. In previous two-layered structure system[1], where TiN was adopted as the bottom electrode (BE), scaling voltage and widening the on/off and F/R window for storage memory were critical problems to solve. It could be nicely resolved by using Ti as BE which influenced on the chemical states of HfO_2 layer and formed stable (quasi-) ohmic contact at HfO_2/Ti. Consequently, The magnitude of operation voltage is drastically decreased and the on/off and F/R ratio is also larger as the current level of LRS is increased. The result can be competitive with the conventional ReRAM device and even flash memory devices.

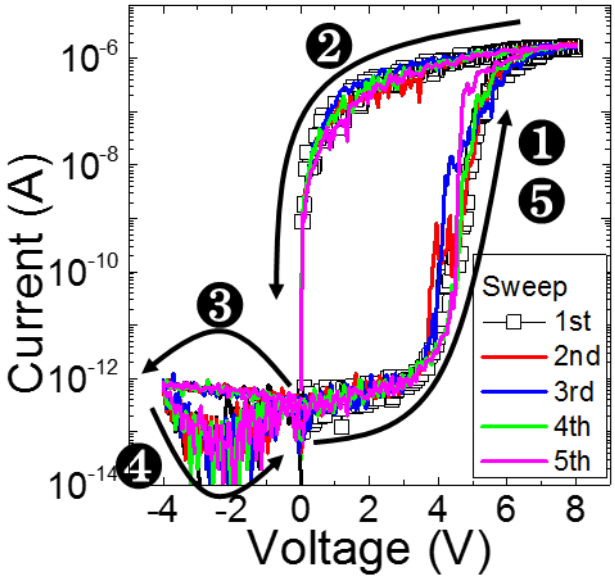

Figure 1. Self-rectifying resitive switching behavior of Pt/Ta_2O_5/HfO_{2-x}/Ti structure and its operation sequence

[1] Jung Ho Yoon, et al. Adv. Func. Mat., 24, 5086 (2014).

Al-doped ZnO Thin Films as Switching Layers for Nonvolatile Resistive-Change Memory Devices

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Resistive-change-type switching characteristics between a high-resistance (HR) and low-resistance (LR) states for the oxide semiconducting thin films have significant interests for promising nonvolatile memory applications [1]. Especially, oxide semiconductors provide us great benefits in realizing the future transparent and flexible electronic systems composed of driving transistors and memory devices. In this work, Al-doped ZnO (AZO) thin films were employed as oxide semiconducting resistive switching materials for the memory devices. AZO films were prepared by atomic layer deposition and two-terminal memory devices were designed as Al/AZO(20 nm)/Mo/SiO_2/Si, in which doped Al amounts were varied to 5 and 20 at%. Fig. 1(a) shows I-V characteristics of the AZO devices with various Al amounts. The compliance current was set as 1 mA for the forming process. The memory on/off ratios for the AZO devices were modulated from 10^2 to 10^4 when the Al amounts was increased from 5 to 20 at%. I-V curves were replotted in a logarithmic scale to clarify the current transport behaviors, as shown in Fig. 1(b). The LR states show linear dependences on voltage with a slope of about 1, which indicates that the ohmic behavior dominates the conducting behaviors. On the contrary, the HR states were observed to be dominated by a space-charge-limited current behavior and/or Child's law. It was concluded from these results that the AZO thin films could be promising materials for the resistive-change memory devices, and that Al-doped amounts have significant impacts on the device behaviors. The detailed results on the switching behaviors will be discussed at presentation.

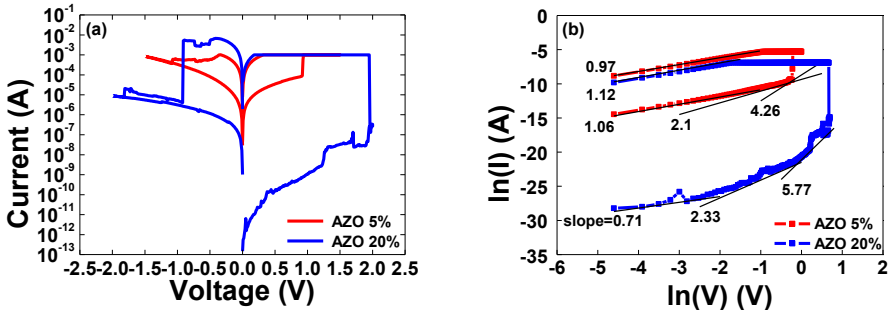

Fig. 1. (a) I-V characteristics of the AZO memory devices and (b) ln(I)-ln(V) plots for resistive switching.

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멤리스터의 저항 drift 문제 해결을 위한 멤리스턴스 복구회로에 관한 연구

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최근에 Von Neumann 구조의 에너지효율을 보다 뛰어넘는 새로운 컴퓨팅 구조를 찾아내기 위한 시도의 하나로 뇌 구조를 모방하여 동작하는 neuromorphic 시스템 및 회로에 관한 연구가 많은 관심을 끌고 있다. Neuromorphic 시스템 및 회로에 대한 연구는 지난 90 년대에 CMOS 기술을 이용해서 많은 연구가 되었으나 CMOS 소자는 연산과 기억의 통합적인 동작이 불가능하다는 점과 아날로그 동작에서의 노이즈와 variation 문제 등 때문에 neuromorphic 구조의 근본적인 장점에도 불구하고 CMOS 를 기반으로 한 neuromorphic 연구의 저변을 확대하지 못하였다. 그러나, 지난 2008 년 멤리스터의 발견 이후에 [1], 멤리스터의 저항 스위칭 특성을 이용해서 연산과 기억의 통합적인 동작을 수행할 수 있고, 또한 아날로그 특성과 비휘발성 특성을 이용하면 뉴론과 시냅스동작을 모방하기에 적합하다는 연구 결과가 제시되어 멤리스터를 이용한 meuromorphic 시스템 및 회로의 연구가 새롭게 많은 관심을 이끌어내고 있다.

그러나, neuromorphic 시스템 및 회로에서 멤리스터를 사용하는 이유는 멤리스터를 이용해서 아날로그 값을 저장하고 연산하기 위해서 인데, 이 경우에, 멤리스터에 지속적으로 전류 혹은 전압 펄스 신호가 인가되게 된다. 지속적인 전기스트레스가 멤리스터에 가해지는 경우에, 멤리스터의 state variable 이 변화할 만큼의 충분한 스트레스가 누적이 되게 되면 그 결과로 멤리스턴스 값이 시간이 지남에 따라 drift 하게 된다. 멤리스턴스 값의 drift 는 결국 미리 프로그램된 synaptic weight 값의 변화를 초래해서 neuromorphic 시스템 및 회로의 잘못된 동작을 야기할 수 있다. 따라서 neuromorphic 시스템의 연산의 정확도를 향상시키기 위해서는 멤리스턴스의 drift 를 억제하는 방법이 필요하게 된다[2].

본 발표에서는 주기적으로 멤리스턴스의 drift 를 감지하고, 감지된 멤리스턴스의 값이 원래 프로그램된 멤리스턴스와 다를 경우에, 원래의 프로그램된 synaptic weight 로 되돌리는 회로를 제안하고 이를 시뮬레이션을 통해서 검증한 결과를 보여준다. 본 발표에서의 CMOS-멤리스터의 복합회로의 시뮬레이션은 CADENCE SPECTRE 로 수행하였다. 멤리스터는 HP 멤리스터의 Verilog-A 모델을 이용하여 시뮬레이션 하였고 [1], CMOS 소자는 SAMSUNG 0.13-μm 공정의 모델 파라미터를 사용하였다.

본 발표에서 제안한 멤리스턴스 복구회로를 neuromorphic 회로의 일종인 cellular neural network 회로에 적용하여 보았다. 적용의 결과로, 100 cycle 의 반복적인 아날로그 연산 후에 synaptic weight 가 21.1%나 원래의 프로그램된 값으로부터 이탈했으나, 본 발표에서 제안된 복구회로를 사용하면 원래 프로그램된 값의 0.12%까지 근접하게 복구가 가능함을 확인하였다[2]. 또한, 멤리스턴스 복구회로를 32X8 의 셀들로 이루어진 cellular neural network 회로에 적용하여 잘 동작함을 확인하였다.

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The work was financially supported by NRF-2011-220-D00089, NRF-2011-0030228, NRF-2013K1A3A1A25038533, NRF-2013R1A1A2A10064812, and BK Plus with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No: 22A20130000042), funded by the National Research Foundation of Korea (NRF), and by Global Scholarship Program for Foreign Graduate Students at Kookmin Univ. The CAD tools were supported by IC Design Education Center (IDEC), Daejeon, Korea.

Disturbance-Suppressed ReRAM Write Algorithm for High-Capacity and High-Performance Memory

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ReRAM is considered as one of the promising candidates that could replace the NAND flash memory because of its fast speed, scalability and reliability [1-3]. However, undesirable write disturbance, which is a unique phenomenon of ReRAM, is reported as one of big hurdles in implementing memory array [4-5]. In this work, we identified experimentally the mechanism of write disturbance in the array and quantified it by using fabricated 8Mb test array. Furthermore, we successfully demonstrated the feasibility of high capacity and high performance ReRAM memory by proposing new write algorithm for disturbance-suppression.

Fig.1(a-b) explains the mechanism of write disturbance in the array. Resistive switching from high to low state is occurred when the write voltage is applied to two-terminal device, and its LRS is adjusted by controlling its compliance current(I_{comp}). In ideal case, BL should be immediately arisen to an equilibrium level after the state is switched. However, the rising speed is limited by parasitic BL capacitance ($C_{BL\_parasitic}$) and another peak current (I_{peak}) is superimposed on I_{comp} due to the low resistance transition of cell until BL is charged up. This additional current makes LRS transition uncontrollable and might lead permanent damage to the cell in worst case. It becomes more severe as the array size increases or target operation current is precisely controlled for multi-bit memory. Therefore, its disturbance plays as a key obstacle against future high capacity/high performance ReRAM memory. To quantify it, we performed the test with the condition that the write voltage is applied but I_{comp} is set to zero so that cell transition is not intentionally happen. As shown in Fig.1(c), cells can be switched to even lower than LRS only with charges stored in the parasitic capacitance in the array, and it is aggravated as the array size increases.

Fig.2(a) illustrates the proposed algorithm to address this problem. In the algorithm, BL is pre-charged to a predetermined level (Vpre_eq) which is close to the equilibrium, and WL is over-driven for a limited time period (dT) to initiate state transition and driven down to a normal level to further reduce a unnecessary current flow after the cell is switched to LRS. As a result, most of uncontrollable I_{peak} is remarkably reduced and only I_{comp} flows through cell so that the write disturbance in the array can be suppressed. The algorithm was evaluated using fabricated 8Mb ReRAM array (Fig.2(b)). As shown in Fig.2(c), LRS distribution was tightly controlled (60% reduction) by employing the proposed algorithm.

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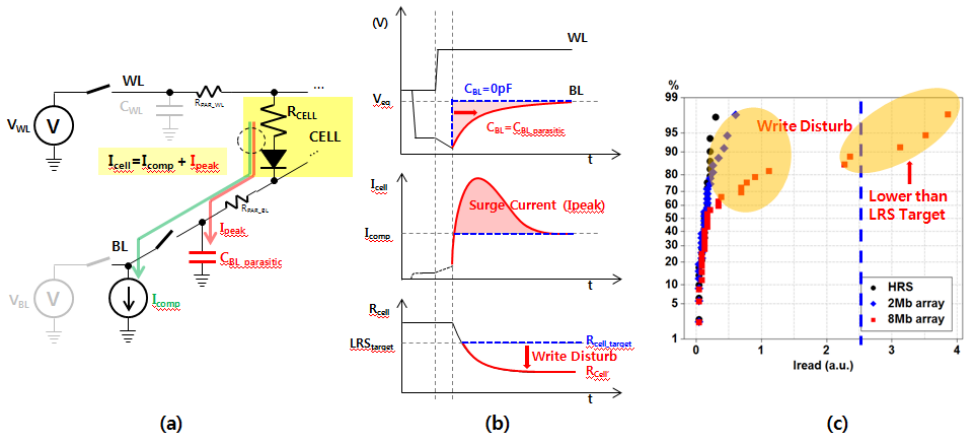

Figure 1. (a) write operation in ReRAM array (b) Mechanism of write disturbance in ReRAM array. (c) Measured results of write disturbance with different array size.

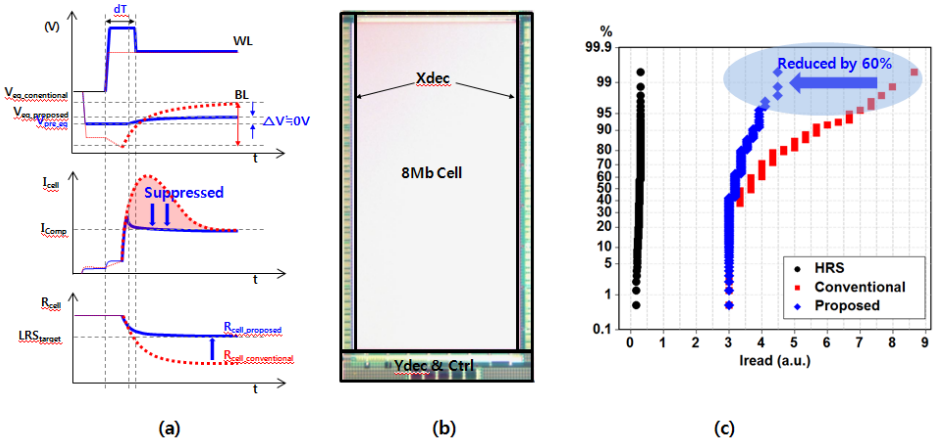

Figure 2. (a) The proposed disturbance-suppressed write algorithm. (b) Fabricated 8Mb ReRAM test array. (c) Comparision of cell distribution.

Novel self-reference sense amplifier for spin-transfer-torque magneto-resistive random access memory

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Recently, the shrinkage of memory devices has serious problems due to process variation. Especially, STT-MRAM which is nonvolatile resistive memory has suffered from unwanted resistance distribution by thin tunnel barrier thichness less than 1nm. The read failure can occur due to overlap of resistance distribution between each state. Therefore many researchers have designed functional sense amplifier such as self-reference sense amplifier (SRSA) to eliminate read failure and to improve sense margin [1]. However, the destructive SRSA has typically high sense margin but low speed due to complicated operations, while the non-destructive SRSA has high speed but low sense margin. In this work, we can improve operation speed as well as sense margin by proposed parallel reading self-reference sense amplifier (PRSA) during writing operation. Since writing operation of STT-MRAM has delay about 10ns due to thermal agitated switching, and writing delay is also continuously reduced (less than 10ns) by low damping [2], the proposed PRSA will be possible fast read operation and maximum sense margin.

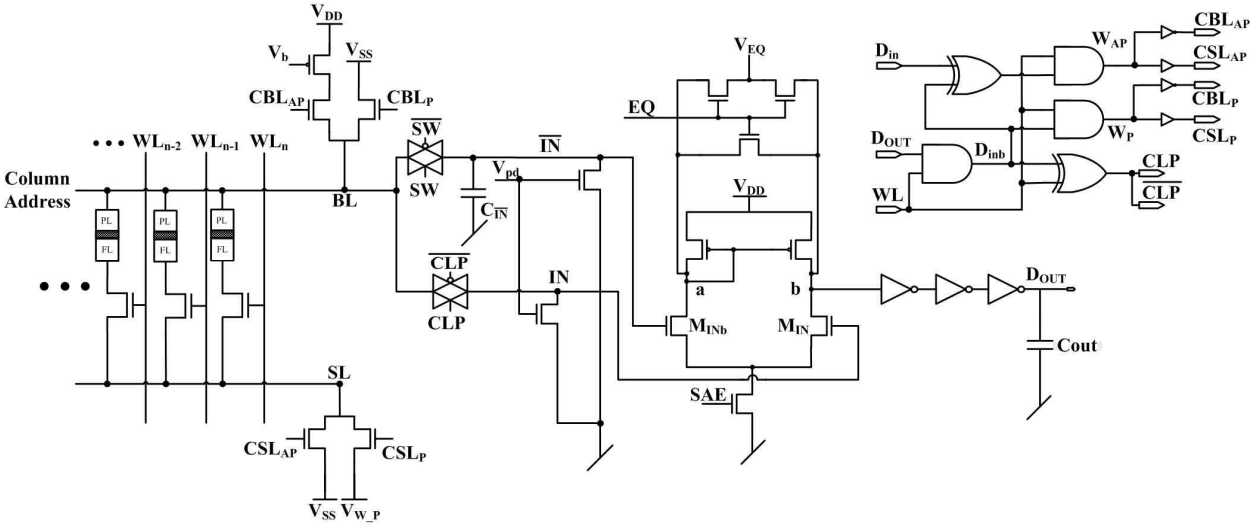

Fig 1. Schematic diagram of proposed self-reference sense amplifier

[1] Zhenyu Sun *et al*., *IEEE Trans. on VLSI Systems*, Vol. 20, No. 11 (2012)
[2] Guenole Jan et al., IEEE 2014 Symposium on VLSI Technology Digest of Technical Papers, pp. 1 (2014)

멤리스터 어레이 회로를 위한 읽기전압 마진의 개선에 관한 연구

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기존의 DRAM 과 FLASH 메모리 소자에 대한 2 차원 스케일링을 향후에 지속하는 것이 어렵기 때문에 새로운 메모리소자에 대한 연구가 활발하게 진행이 되고 있다[1]. 새로운 메모리 소자 중에서 저항 스위칭 특성을 갖는 멤리스터를 이용하여 메모리 어레이를 구성하려고 하는 시도가 최근에 많은 관심을 얻고 있는데, 이는 멤리스터 소자가 고밀도, 저전력, 비휘발성 그리고 3 차원 집적에 대한 가능성을 갖고 있기 때문이다. 그러나, sneak-path 누설전류와 배선저항 등의 문제로 읽기전압의 margin 이 나빠져서 멤리스터 어레이의 크기가 제한 된다는 문제가 있다 [2]. 이러한 문제를 극복하기 위한 멤리스터용 선택소자 개발에 대해서 여러 가지 가능성이 나오고 있기는 하지만, 아직까지 완전한 해결책이라도 할 만한 방법은 제안되지 않았다.

본 연구에서는 멤리스터 어레이의 읽기 동작을 두 개의 과정으로 분리하여, 첫번째 과정에서는 선택되지 않은 멤리스터들의 background data pattern 과 선택된 멤리스터 셀의 어레이 상의 위치를 고려하여 읽기 전압의 마진을 최대한 확보할 수 있는 기준전압을 찾아내고, 두번째 과정에서 첫번째 과정에서 찾아낸 기준전압을 이용해서 선택된 셀의 저장값이 0 인지 1 인지를 판단하게 하였다. 본 연구에서 제시하는 방법과 기존의 읽기 방법과의 제일 큰 차이는 다음과 같다. 기존의 읽기 회로에서는 background data pattern 과 선택된 셀의 어레이 상의 위치를 고려하지 않고 고정된 기준전압을 사용했기 때문에, 최악의 조건에서의 읽기 전압의 마진이 매우 많이 열화되었다. 그러나, 본 연구에서 제안하는 새로운 읽기 회로에서는 선택되지 않은 멤리스터들의 background data pattern 과 선택된 셀의 어레이 상의 위치에 따라서 최적의 기준전압을 자동으로 찾을 수 있기 때문에, 상황과 조건에 따라서 읽기기준전압을 변화시켜서 어떤 경우에도 읽기전압의 마진을 더 좋게 할 수 있다는 장점이 있다.

본 논문에서 제안된 새로운 읽기회로는 기존의 회로보다 읽기전압의 마진을 개선하여 멤리스터 어레이의 크기를 56% 더 크게 만드는 것을 가능하게 한다. 또한 읽기전압의 마진은 100% 개선이 됨을 시뮬레이션을 통해서 확인하였다. 시뮬레이션은 CADENCE SPECTRE 로 수행하였고, 멤리스터는 HP 멤리스터의 Verilog-A 모델을 이용하여 시뮬레이션하였고, CMOS 소자는 SAMSUNG 0.13μm 파라미터를 사용하였다.

The work was financially supported by NRF-2011-220-D00089, NRF-2011-0030228, NRF-2013K1A3A1A25038533, NRF-2013R1A1A2A10064812, and BK Plus with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No: 22A20130000042), funded by the National Research Foundation of Korea (NRF), and by Global Scholarship Program for Foreign Graduate Students at Kookmin Univ. The CAD tools were supported by IC Design Education Center (IDEC), Daejeon, Korea.

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[2] J. Liang, and H. P. Wong, IEEE Trans. Electron Device. 57, 10(2010)

TiO_x-based Filamentary ReRAM Synapse for Neuromorphic Systems

Jaesung Park, Amit Prakash, Kibong Moon, Daeseok Lee, Jiyong Woo, Euijun Cha, Sangheon Lee, Jeonghwan Song,Yunmo Koo, Jaehyuk Park, Seokjae Lim and Hyunsang Hwang
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Resistive random-access memory (ReRAM) is one of the promising candidates for electronic synapse because of simple device structure, CMOS compatability, low power consumption [1]. ReRAM has two types of operation mehcanism in terms of interface type and filamentary type. The filamentary type ReRAM shows better switching properties and retention characteristics even at <10nm physical size than interface type ReRAM [2]. However, the filamentary ReRAM has obstacle of leraning process due to abrupt set behavior [3]. In this research, we reported the gradual set behavior in TiO_x-based filamentary ReRAM by using various reset condition. After conducting reset operation by applying modified pulse, the set behavior shows the gradual resistance change while the abrupt set was shown after direct current (DC) condition [Fig 1. (a)]. Based on the gradual resistance change, we overcame the obstacle of filamentary ReRAM in learning process. During learning process, the potentiation/depression pulse signals were applied with the stepwise increase of pulse amplitude in order to acheive linear-like spike-timing-dependent plasticity (STDP) characteristics for high accuracy of system [4].

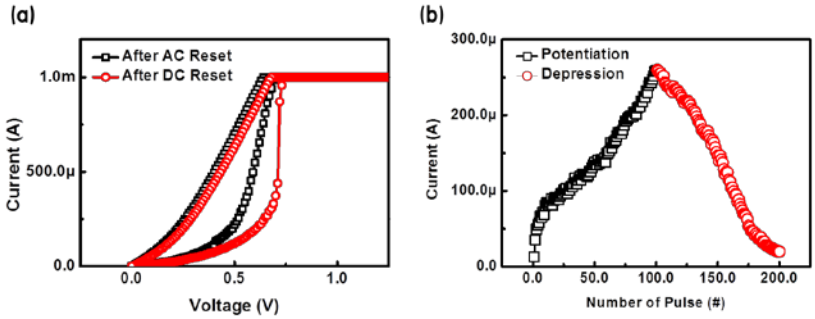

Fig 1. (a) Set behavior after DC and pulse reset (b) STDP characteristics with the stepwise increase of pulse amplitude

[1] Y. Wu et al., International Memory Workshop (2012)
[2] Y. Y. Chen et al., IEEE International Electron Device Meeting (2011)
[3] M. Suri et al., IEEE International Electron Device Meeting (2011)
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Acknowledgement: This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009460).

Cross point array의 sneak path 문제 최소화를 위한 멤리스터 소자특성연구

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트랜지스터의 미세화에 따른 소모전력 증가 등의 문제를 근본적으로 해결하기 위하여 Artificial Neural Network(ANN)[1]와 같은 병렬 처리 아키텍쳐가 연구 되고 있다. 이 때문에 ANN 에 적용 가능할 것으로 생각되는 two ternial 멤리스터(memristor) 소자가 주목 받고 있는데, 이 소자들은 Fig. 1 과 같이 Cross Point Array(CPA) 구조로 집적되어 junction 에서의 전도도를 뇌신경과 같이 아날로그방식으로 미세 조정하는 방법으로 정보를 처리 하게 된다. 하지만, CPA 구조에서의 sneak path 문제로 인해 read/write disturbance 문제가 심각하기 때문에 이를 제어하기 위한 체계적인 연구가 필요하다.

그림 Fig. 2 (a)는 CPA 구조에서 sneak path 로 인하여, 여러 셀에서 원하지 않는 저항 상태의 변화가 발생한다는 것을 보여준다. 이 문제를 해결할 수 있는 방법을 제시하기 위해, sneak path 문제를 최소화할 수 있는 멤리스터 소자의 특성을 추출하고, 이를 실제 멤리스터용 소재개발에 반영할 수 있도록 하는 것이 본 연구의 목적이다. 멤리스터 소자의 이론적 특성에 기반한 HP lab 의 소자모델[2]은 이러한 연구에 적절하기 않기 때문에, 실제 멤리스터 소자의 특성과 유사한 semi-emphirical 소자모델을 개발하고, 이를 변형하여 다양한 소자특성을 시스템에 적용하여 보았다. 그 결과 전류가 아닌 전압에 따른 선형적인 conductance 변화, 특정 전압 구간에서의 conductance 변화 억제가 필요한 것을 알 수 있었으며, Fig. 2 (b)는 이러한 소자를 사용할 경우 sneak path 문제가 발생하지 않는 다는 것을 보여준다. Semi-emphirical 소자모델을 이용하여, 기존의 방향과 상당히 다르지만, 매우 유효한 새로운 멤리스터 소자개발방향을 제시할 수 있었다는 것이 본 연구의 성과이다.

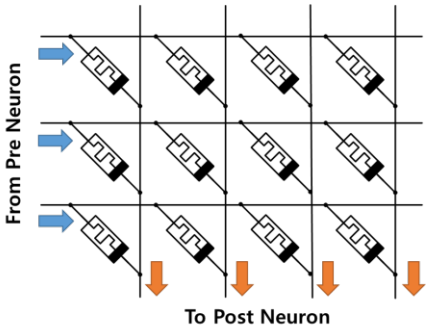

Fig. 1. Memristor cross point array

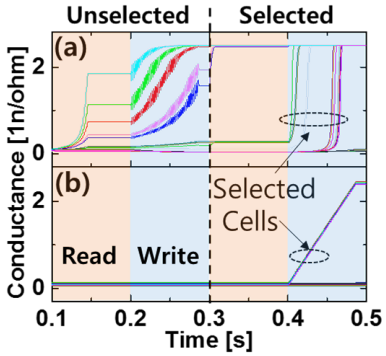

Fig. 2. Conductance change of the memristors on one Post Neuron line (a) HP memristor (b) modified memristor

Acknowledgments : This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2014-002529). NRF-2012-0009462).
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[2] D. B. Strukov, G. S. Snider, D. R. Stewart and R. S. Williams, nature, 453, 80 (2008)

Neuromorphic system based on CMOS analog neuron circuit

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The neuromorphic system based on biological neuron enables parallel and adaptable information processing with high efficiency and low power consumption. We designed the CMOS analog neuron circuit as shown in Fig. 1 (a). The system consists of synaptic integration part and action-potential generation part. The integration part integrates and transmits the signal from pre- to post-neurons. As an input signal is applied to synaptic device, the device current will flow into capacitors using current mirrors. We used the SFST [1] utilizing floating-body effect as synaptic device and it has excitatory or inhibitory characteristics and modulates the conductance of signals. The generation part creates an action potential if the capacitor voltage passes over the threshold values of inverters. In order to generate the action potential from minus to plus value, we used two normal inverters, one modified inverter and feed-back MOSFET. The modified inverter [2] was designed to change the positive pulse into negative. Through controlling the node delay, we completed the generation part and confirmed the output characteristics as shown in Fig. 1 (b).

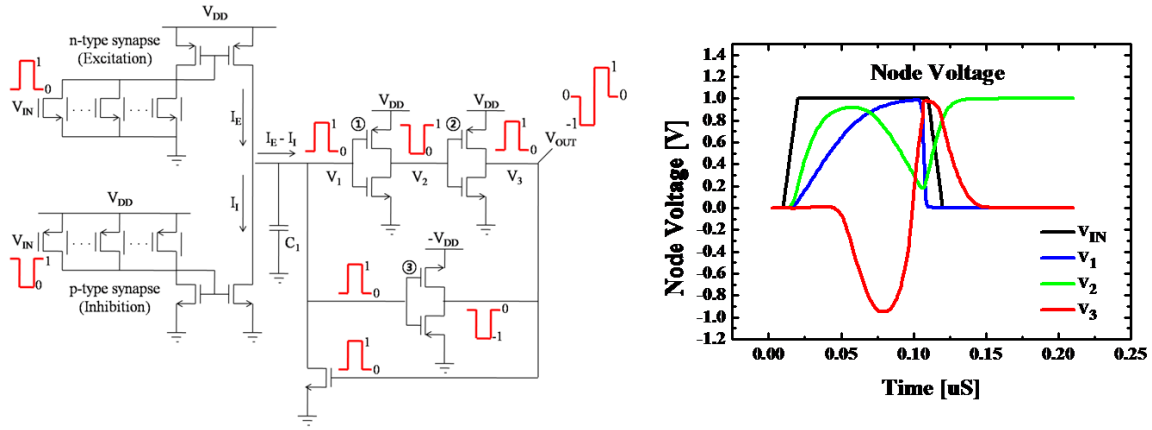

Fig. 1. (a) CMOS analog neuron circuit and (b) its output characteristics.

[1] H. Kim, J. H. Lee, G. Kim, M.-C. Sun, and B.-G. Park, SSDM (2012)
[2] J. Park, H. Kim, M.-W. Kwon, R. Ranjan, and B.-G. Park, ICEIC (2014)

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Self-boosted tunnel field-effect transistor using nitride charge trapping layer

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Recently, the tunnel field-effect transistrs (TFETs) have been studied as a promising candidate for low-power device due to the remarkable subthreshold swing (SS) characteristics and low-voltage operation [1]. However, the TFETs suffer from small on-current (I_{on}) due to large tunneling resistance and there have been many researches to improve the performance. In this study, we investigated the self-boosted TFET using the nitride charge trapping layer between oxide and gate for the enhancement of I_{on} and SS [2]. The operation mechanisms are summerized in figure 1. The nitride layer is positively charged at on-state because electrons are emitted from the acceptor-like traps, hence reducing V_{TH} of the device. On the other hand, the nitride layer is neutral at off state because the acceptor-like traps are filled, so there is no change in the subthreshold characteristics. Figure 2 shows transfer characteristics of the self-boosted TFET. The charges in the nitride layer vary with gate bias condition when V_G increases slowly. Therefore, we can obtain low V_{TH} and high V_{TH} at on-state and off state respectively and improve I_{on} characteristics while keeping subthreshold characteristics with this concepts.

Acknowledgement This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186).

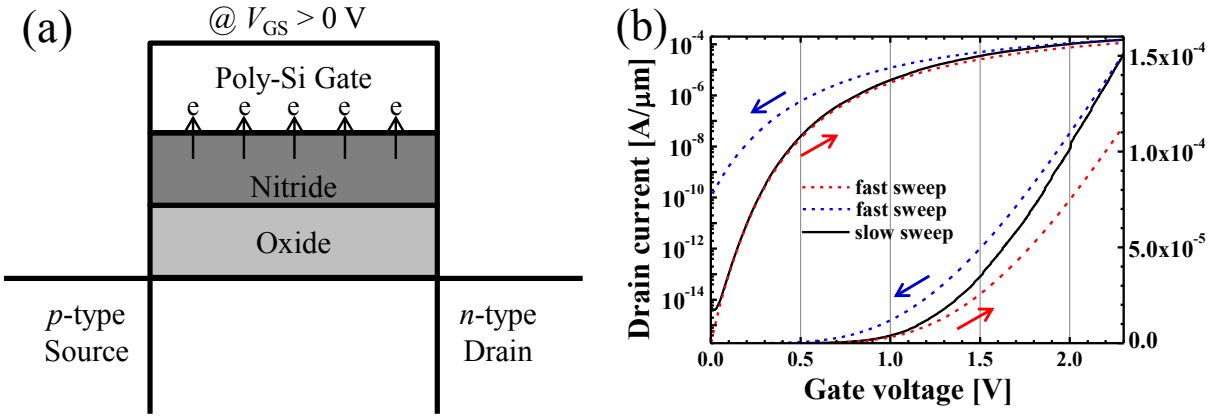

Fig 1. (a) Schematic diagram of the operation mechanisms and (b) transfer characteristics.

[1] W. Y. Choi, B.-G. Park, J. D. Lee and T.-J. K. Liu, IEEE Electron Devices Lett. 28 (8), 743 (2007).
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Work-Function Variation and Random Dopant Fluctuation of Tunneling Field-Effect Transistors (TFETs)

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A tunneling filed-effect transistor (TFET) has attracted much attention as one of the most promising abrupt switching devices because its subthreshold swing can be smaller than the physical limit of a metal-oxide-semiconductor FET (MOSFET) [1]. However, analogous to MOFSETs, TFETs suffer from statistical variability which will be detrimental to TFET circuit design. In order to minimize TFET variability, this manuscript focuses on the influence of the random number and position on TFETs in terms of random dopant fluctuation (RDF) and work-function variation (WFV) in comparison with MOSFETs. Unlike MOSFETs, in the case of TFETs, the random number and position effect of channel dopants rarely influences σV_{th}. Because it is assumed that channel doping concentration is low, the channel energy barrier of TFETs is not determined by channel doping. With the WFV effects, TFETs also show a different V_{th} distribution compared to MOSFETs. As in MOSFETs, the WFV effects modulate lateral energy band profile according to the random distribution. However, the V_{th} of TFETs is not determined by overall WF. The electrical characteristics of TFETs are mainly determined by gate metal WF values near the source region where band-to-band tunneling mainly occurs [2]. This analysis provides a detailed insight into the sources of variation related to underlying physics of TFETs.

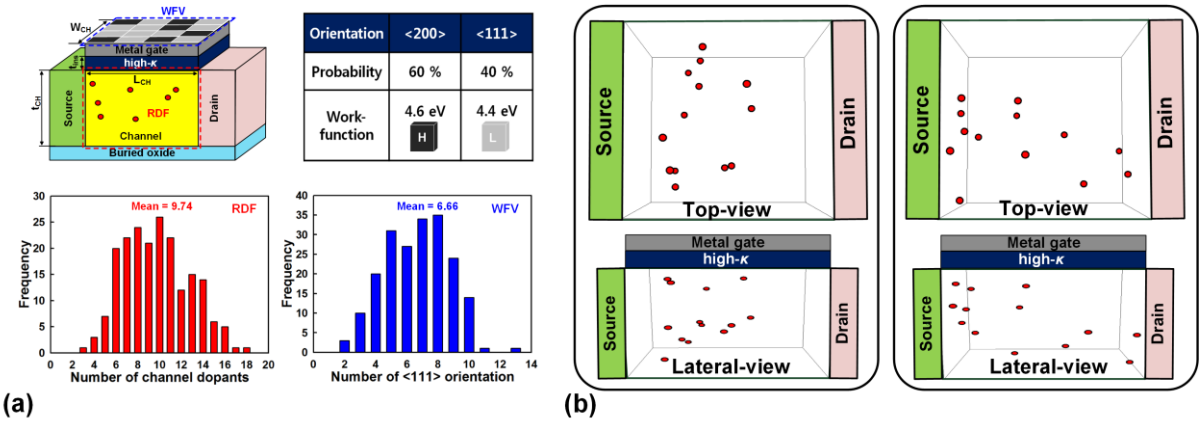

Fig. 1. (a) Simulated device structure with random discrete dopants and gate metal grain orientation. (b) Randomly generated channel dopants profile when the number of channel dopants is the same.

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Study of Work-function Variation with Various Gate Materials in High-k/Metal (HK/MG) MOSFETs

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Recently, in order to enhance gate-to-channel capacitive coupling, high-κ/metal-gate (HK/MG) technology is being widely used in industries. This technology can not only restrain short-channel effects, but can also suppress gate-leakage current. However, threshold-voltage variation induced by work-function variation (WFV) is one of the technical challenges in HK/MG CMOS technology [1]. In this work, we ran TCAD [2] simulations with various gate materials such as TiN, WN, TaN, and MoN to determine the implications of WFV in HK/MG FinFET and planar-type device structure [*e.g.*, fully-depleted silicon-on-insulator (FD-SOI) MOSFET]. We ascertained that the extended gate area (EGA) effect [3] in fin-shaped field effect transistors (FinFETs) extensively varied depending on the gate materials used.

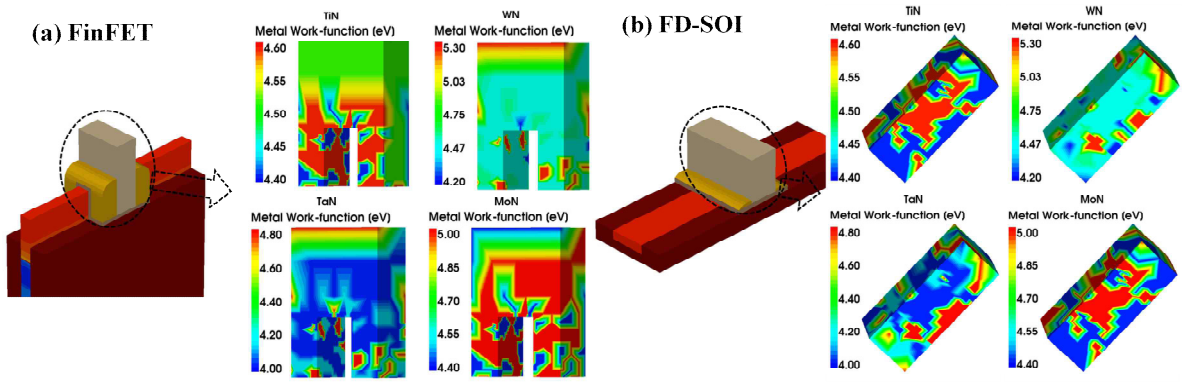

Fig 1. Examples showing randomized work-function values of grains in (a) FinFET and (b) FD-SOI MOSFET with TiN, WN, TaN, and MoN gate materials in HK/MG CMOS technology.

[1] H. Dadgour *et al*., "Modeling and analysis of grain-orientation effects in emerging metal-gate devices and implications for SRAM reliability," in *Proc. IEEE IEDM*, Dec. 2008, pp. 1-4.
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Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637).

Low-power and high-speed optically readable charge-trap flash memory with sub-10-ps read time

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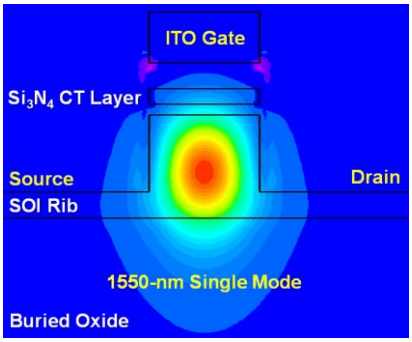
Si photonics is being highlighted for making a breakthrough out of the technical issues with which the Si electron devices in efforts for scaling are confronted and for moving to the next-generation 3-D VLSI systems with the optical interconnect as their backbones [1]. Si or Si-compatible optical components have been widely researched for realizing the Si electronic and photonic integrated circuits. In this work, another active effort is made to take a forward step to Si electronics and photonics convergence by bringing the lightwave technology into the Si nonvolatile memory. The device consists of Si rib microring waveguide, oxide-nitride-oxide (ONO) charge-trap flash (CTF) memory cell, transparent gate (ITO), and is eventually coupled to a bypass waveguide. Simulation results demonstrate the 1550-nm single-mode light signal is effectively confined in the optimally designed device (Fig. 1) [2], and the refractive index (n_{Si}) traced at the center of Si rib is changed by the electron and hole distributions depending on program and erase states of the cell (Fig. 2). [3]. A small change in n_{Si} in the order of 10^{-4} is converted to a 50% or higher difference in the transmitted optical power and the propagation speed over the n_{Si} swing warrants ultrafast read time below 10 ps.

Acknowledgement This research was supported by the Center for Integrated Smart Sensors funded by the Korean Ministry of Education, Science and Technology as Global Frontier Project (CISS-2012M3A6A6054186).



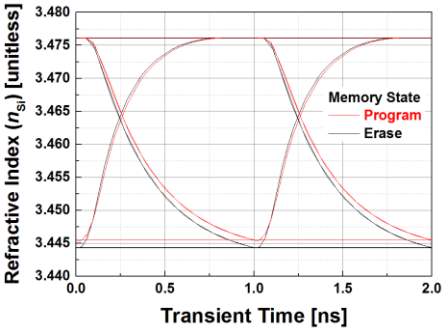


Fig. 1. Nonvolatile memory cell as an optical waveguide. Fig. 2. Eye-diagrams of n_{Si}'s in different memory states.

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A study on room-temperature photoluminescence of RF-sputtered GaN for cost-effective III-V-on-Si beyond-CMOS technology

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Recently, Si technology is exploiting the paths out for future in various ways through more Moore (MM), more-than-Moore (MtM), and beyond-CMOS approaches [1]. III-V-on-Si heterogeneous integration can be a strategy, which allows to merge III-V devices and Si CMOS logic blocks on Si platform monolithically and cost-effectively [2]. GaN has broad applicability by its high electron mobility for fast electron devices and wide bandgap suitable to visible-light sources. In this work, room-temperature photoluminescence (PL) charactersitics of GaN-on-Si are studied. GaN was deposited by an RF sputtering on p-type (100) Si sub. at a power of 200 W (Fig. 1). The samples went through RTA at 1000 °C for different times in the N_2/H_2 (4.8%) mixture gas. The GaN-on-Si sample annealed for 30 s showed a relatively stronger PL and the tests were further preceded with a tunable laser to confirm that the signals originated from GaN, not from the higher-order harmonics. The results show that the peak location near 425 nm is invariant with excitation wavelength (Fig. 2), and support that a partially crystallized GaN is obtained on Si by a low-temperature RF sputtering followed by conventional CMOS processing with a low thermal budget and cost-effectiveness.

Acknowledgement This research was supported by Nano·Material Technology Development Program through NRF funded by the Korean Ministry of Sciecne, ICT & Future Planning (2009-0082580).

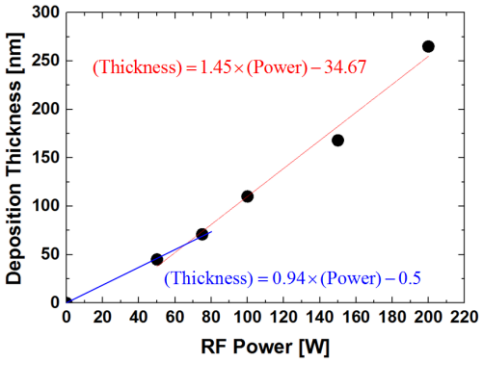

Fig. 1. Deposition thickness of GaN vs. RF power.

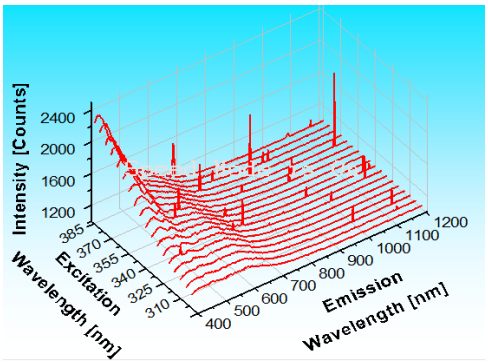

Fig. 2. 2-D mapping of PL measurement results.

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Physical synthesis of monolithic graphene oxide sheets with tunable composition

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Graphene oxide (GO) is a material of great interest for potential multiple applications. However it is typically prepared by solution based harsh chemical treatments for large-volume manufacturing. To date, the synthesis of a monolithic form of graphene oxide that is crucial to the precision assembly of graphene-based devices has not been achieved. Here we report the physical approach to produce monolithic graphene oxide sheets on copper foil using solid carbon, with tunable oxygen-to-carbon composition. Experimental and theoretical studies show that the copper foil provides an effective pathway for carbon diffusion, trapping the oxygen species dissolved in copper and enabling the formation of monolithic graphene oxide sheets [1]. Unlike chemically derived graphene oxide, the as-synthesized graphene oxide sheets are electrically active, and the oxygen-to-carbon composition can be tuned during the synthesis process. As a result, the resulting graphene oxide sheets exhibit tunable bandgap energy and electronic properties according to O/C composition. Our solution-free, physical approach may provide a path to a new class of monolithic, two-dimensional chemically modified carbon sheets.

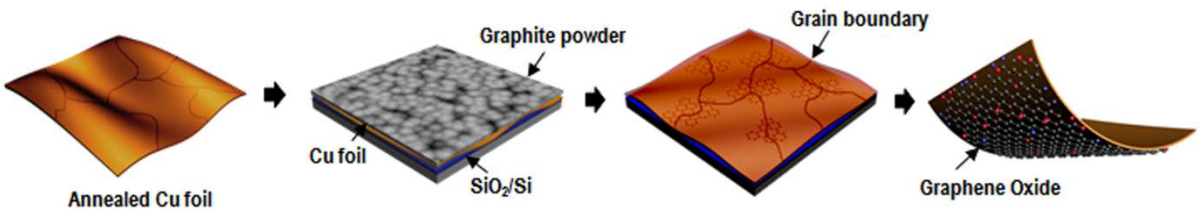

Fig 1. Schematic representation of the modified DAS process.

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Wrinkle-Free Graphene grown on Controlled Pt (200, 220) films and Thermal-Assisted Transfer of Large-Scale Patterned Graphene

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We report the growth of wrinkle-free, uniform monolayer graphene films via chemical vapor deposition on a Pt (200, 220) substrate with texture-controlled giant grains and the thermal-assisted transfer of large-scale patterned graphene onto arbitrary substrates. The designed Pt surfaces with limited numbers of grain boundaries and improved surface perfectness as well as small lattice constant and thermal expansion coefficient differences to graphene provide a venue for uniform growth of monolayer graphene with wrinkle-free characteristic. The thermal-assisted transfer technique allows the complete transfer of large-scale patterned graphene films onto arbitrary substrates without any ripples, tears or folds and the Pt substrates can be reused repeatedly. The transferred graphene shows high crystalline quality with an average carrier mobility of ~5,500 $cm^2V^{-1}s^{-1}$ at room temperature. Furthermore, this transfer technique shows a high tolerance to variations in types and morphologies of underlying substrates, which is essential for the various applications proposed for graphene.

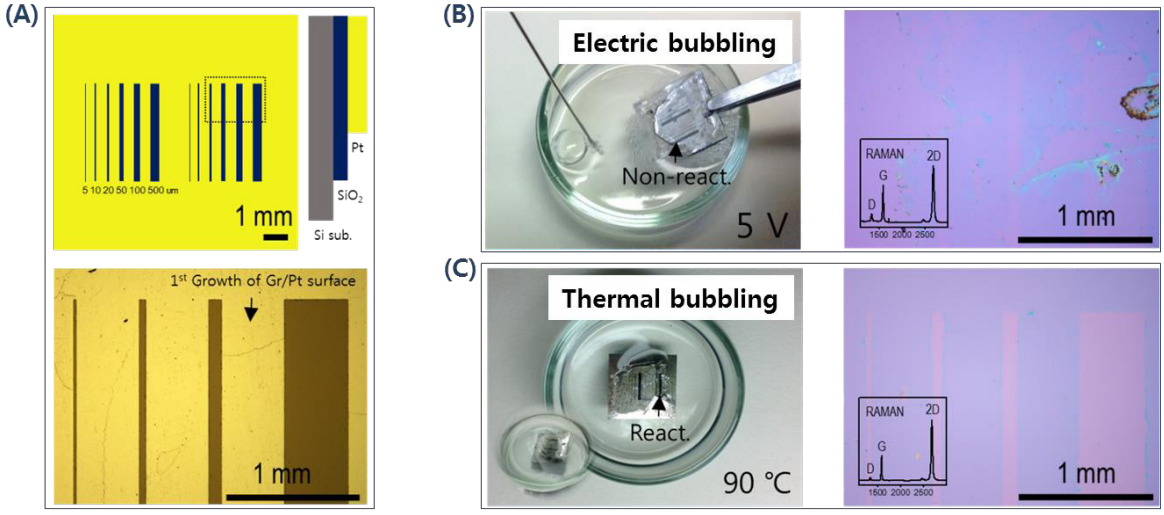

Fig 1. Comparison of graphene transfer for (A) patterned Pt film. The transferred graphene on SiO2/Si using (B) an electrochemical transfer method and (C) the thermal assisted transfer method.

Improvement in Electrical Conductivity, Mechanical and, Thermal Stabilities of Graphene/Carbon Nanotube Composite Electrodes with $AuCl_3$ doping

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Graphene, a two dimension material have received great attention in various research field due to its unique properties such as low electron-phonon scattering, high carrier mobility, ambipolar electrical field effect, and quantum hall effect[1]. However, chemical vapor deposition (CVD) method grown graphene often have higher sheet resistance (R_s) (>1 kohm/sq) than ITO based TCEs. To overcome this limitation, a noble, high performance graphene/single-walled carbon nanotube (SWCNT)-composite doped with gold chloride ($AuCl_3$) has been prepared by a simple spray coating method for use as transparent conducting electrodes (TCEs)[2]. A significant synergistic effect of monolayer, polycrystalline graphene grown by chemical vapor deposition and SWCNTs provided enhanced electrical conductivity and mechanical, thermal stabilities on the hybrid structure. The coatings, prepared at varying 1ml of SWCNTs graphene/polyethylene terephthalate (PET) substrates, demonstrated significantly lower sheet resistance values(215±15 ohm/sq) than graphene (775±100 ohm/sq) or SWCNTs (552±35 ohm/sq) alone. Furthermore, a 62.5% bending of graphene/SWCNT-composite increased the linear resistance from 300 ohm to 318 ohm while a 62.5% bending of graphene showed linear resistance increment from 1100 ohm to 2860 ohm. The improved bending property is attributed to the unique structure of composite in which the SWCNTs act as efficient conductive channels by bridging crystalline defects presented in polycrystalline graphene sheet. To achieve an optimal condition for commercial TCE sheet resistance value, $AuCl_3$ was further doped on the graphene/SWCNT-composite and the resulting composite showed an average sheet resistance of~100±15ohm/sq with high transmittance of ~90% at 550nm. The thermal stabilities of $AuCl_3$ doped graphene/SWCNT-composite were superior to those of $AuCl_3$ doped pristine graphene and the unique structure of composite helped to have a stable bonding between Au^{3+}, Cl^- ions and C atoms after thermal treatment. Our novel hybrid structure could potentially facilitate the commercial mass production of high-quality TCEs.

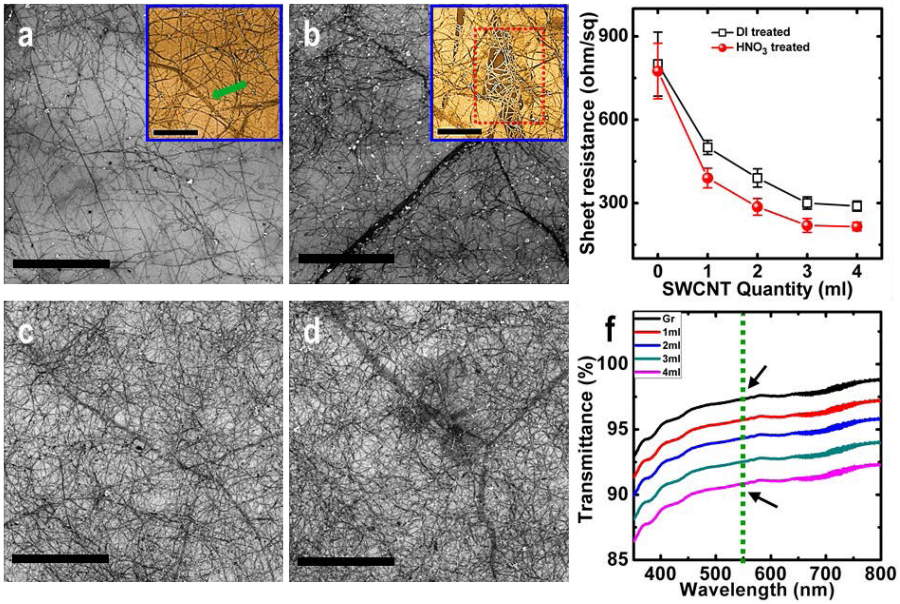

Fig 1.SWCNT spray coating on a single layer graphene and its properties.

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Study on the resistive switching phenomena in AlN and $Al_xGa_{1-x}N$ films grown by atomic layer deposition

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In this study, feasibility of nitride memristors made of AlN film is demonstrated. It was able to switch these nitride memristors at 100 *ps* speed, and further scaled the device down to 50 nm and demonstrated a switching energy lower than that of a typical Ti oxide memristor. (Fig.1) As a plausible switching mechanism, the formation of conduction channels of Al(N) solid solution is suggested, and correlation of oxygen contaminant was considered from extensive TEM and EELS characterizations. Low solubility and melting temperature of Al(N) conducting channels are attributed to the ultra-fast under 100 *ps* regime and energy-conservative memristive switching characteristics of AlN memristors. In addition, resistive switching in $Al_xGa_{1-x}N$ will be demonstrated for the first time. Atomic-layer-deposited $Al_xGa_{1-x}N$ film showed a reproducible and uniform switching behavior with lower forming voltage compared to the device made of pure AlN film.

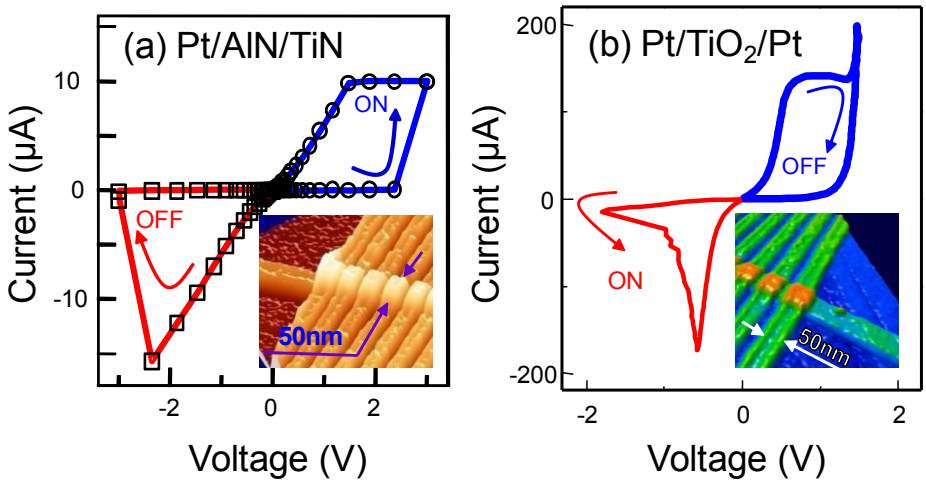

Fig 1. DC switching characteristics of (a) Al nitride and (b) Ti oxide memristors at nanoscale (50nm X 50nm).

Analysis of GaN-based Light-Emitting Diodes Using Near-field Scanning Optical Microscopy in Various Modes

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Near-field scanning optical microscopy (NSOM) has been a critical role in nanoscopy since it can overcome resolution limit of conventional microscopy by using near-field that rapidly decays on the sample surface with high-frequency component. Recently, GaN-based light-emitting diodes (LEDs) were analyzed using photoluminescence NSOM (PL-NSOM), which is a combination of NSOM and spectroscopy, for analyzing carrier dynamics in quantum wells (QWs) [1]. PL-NSOM can be divided into three types including illumination mode (I-mode), collection mode (C-mode) and illumination-collection mode (I-C mode) by use of NSOM probe. In case of I-mode and C-mode, they provide averaged information of carrier dynamics since PL is excited through NSOM probe and collected through objective lens in I-mode (C-mode is reverse situation of I-mode). On the other hand, since PL is excited and collected simultaneously through NSOM probe in diffraction limited size, I-C mode provides more local information compared to I-mode and C-mode. Therefore, comparison with each mode in same area is important for analyzing of carrier dynamics. We built lab-made, tuning fork-based PL-NSOM system, which can measure the same area in each mode. Using our PL-NSOM system, we measured PL mapping of various GaN-based LED samples and analyzed carrier dynamics of the samples with the comparison of three different modes.

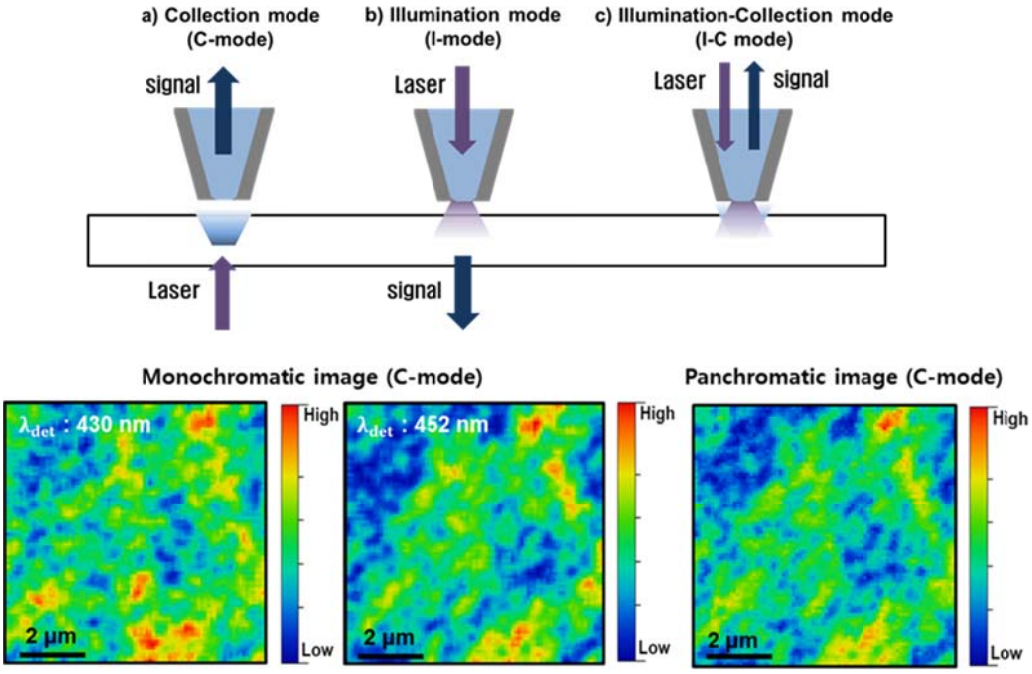

Fig 1 (Upper) Operation schematic of each mode of PL-NSOM
(Lower) Monochromatic and Panchromatic PL mapping image of C-mode

[1] Marcinkevicius, S., Gelzinyte, K., Zhao, Y., Nakamura, S., DenBaars, S. P., & Speck, J. S., Applied Physics Letters, 105. 11, 111108-111108 (2011).

Growth of GaN layer with conductive $Al_xGa_{1-x}N$ buffer on SiC substrate using Metal Organic Chemical Vapor Deposition

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GaN-based semiconductors have been grown on sapphire substrate, but the sapphire substrate has large lattice mismatch with GaN (~16%). This lattice mismatch generates many dislocations and thereby deteriorates device performance. On the other hand, SiC substrate has electrical conductivity, small lattice mismatch with GaN (~3.4%) and high thermal conductivity ($4.9Wcm^{-1}/k$), so that it is suitable for high efficiency GaN-based optoelectronic vertical device applications. AlN buffer layer has been normally used to grow high quality GaN layer on SiC substrate. However, it is very difficult to fabricate vertical device because AlN has electrical insulating property. By constrast, conductive Al_xGa_{1-x} N buffer layer enables us to fabricate fully vertical conducting devices through simple process by forming an electrode on the backside of the substrate as shown in Fig. 1 [1]. Cree, Inc. recorded significant high power LED milestone with the demonstration of 303 lumens per watt using vertical InGaN LED chip structure grown on conductive $Al_xGa_{1-x}N$ buffer (Fig. 2) [2,3]. A few studies have shown that the conductive $Al_xGa_{1-x}N$ buffer layer has low-resistance at low Al composition [4,5]. On the contrary, the crystal quality of GaN layer was improved by increasing Al composition [6]. However, the study on the effect of $Al_xGa_{1-x}N$ buffer layer over the whole composition range on GaN layer has not been reported so far. In this study, we investigate the characteristics of the GaN layers grown on SiC substrate using conductive $Al_xGa_{1-x}N$ buffer layer with different Al composition including high Al contents (x=0~1). All samples were grown by high-temperature metalorganic chemical vapor deposition (HT-MOCVD) with varying trimethylaluminum (TMAl) rates. The detailed experimental results will be reported and discussed at the conference.

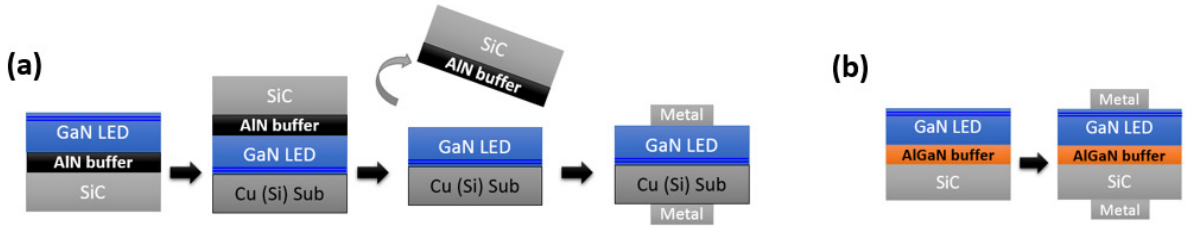

Fig.1. The schematic diagram of vertical LED fabrication process with (a) AlN buffer and (b) conductive $Al_xGa_{1-x}N$ buffer

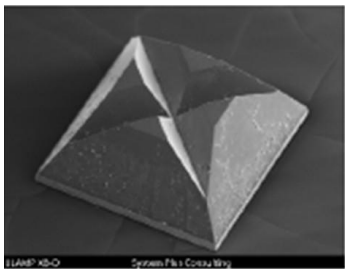

Fig. 2. The high power vertical InGaN LED chip on SiC based on the Cree's SC3 technology.

[1] B. Moran, M. Hansen, M.D. Craven, J.S. Speck, S.P. DenBaars J. Cryst. Growth 221, 301 (1998)
[2] K.Doverspike, G.E.Bulman, S.T.Sheppard, H.S.Kong, M.Leonard, H.Dieringer, T.W.Weeks, Jr., J.Edmond, J.D.Brown, J.T.Swindle, J.F.Schetzina, Y-K Song, M.Kuball and A.Nurmikko Mater. Res. Symp. Proc. 482, 1169 (1997)
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[4] K. Jeganathan, M. Shimizu, and H. Okumura J. Appl. Phys. 97, 013524 (2005)
[5] Atsushi Nishikawa, Kazuhide Kumakura, Tetsuya Akasaka, Toshiki Makimoto J. Cryst. Growth 298, 819 (2007)
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Crystallographic study of *m*-plane GaN grown on *m*-plane sapphire by hydride vapor phase epitaxy

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In this paper, we report a study on the evolution of surface morphology and microstructure of nonpolar *m*-plane GaN (*m*-GaN) by selective area growth (SAG) using wagon wheel pattern, which was done as preliminary work for making bulk *m*-GaN substrates masked with stripe openings to perform SAG. A crystallographic tool was developed to calculate the facets growth rates, the condensation surfaces and the surface recovered by *m*-GaN stripe in order to establish a correlation between the growth morphologies and the experimental conditions [1]. It is shown the growth rates of the facets, and so the morphologies, depend on the variations of the V/III ratio and temperature. The growth morphologies of the *m*-GaN stripes were systematically investigated by scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

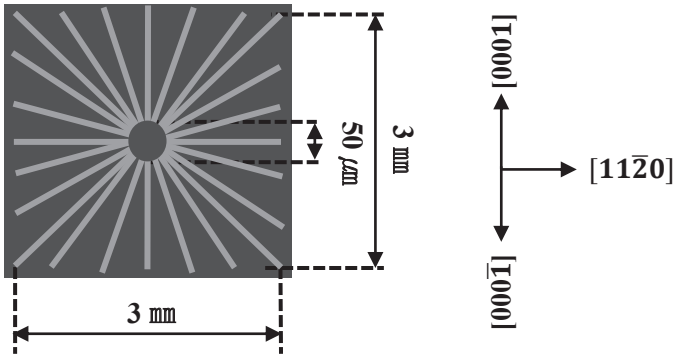

Fig 1. Schematic image of wagon wheel mask for fabricating SAG pattern.

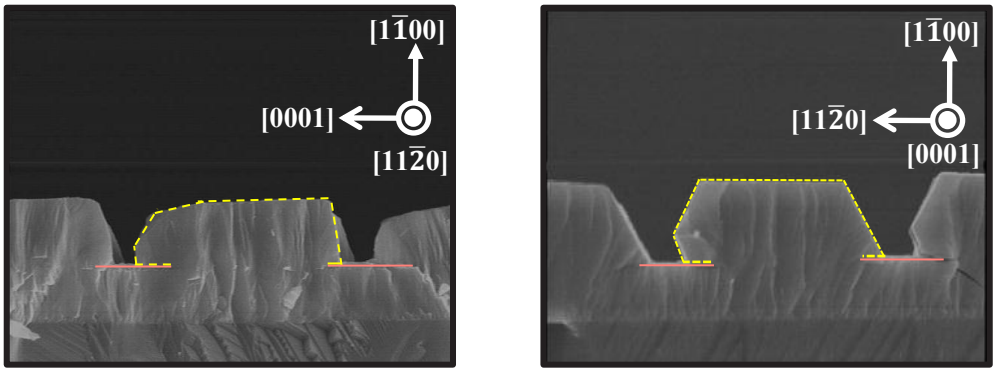

Fig 2. Cross-sectional SEM images of *m*-GaN fabricated between the SiO_2 window.

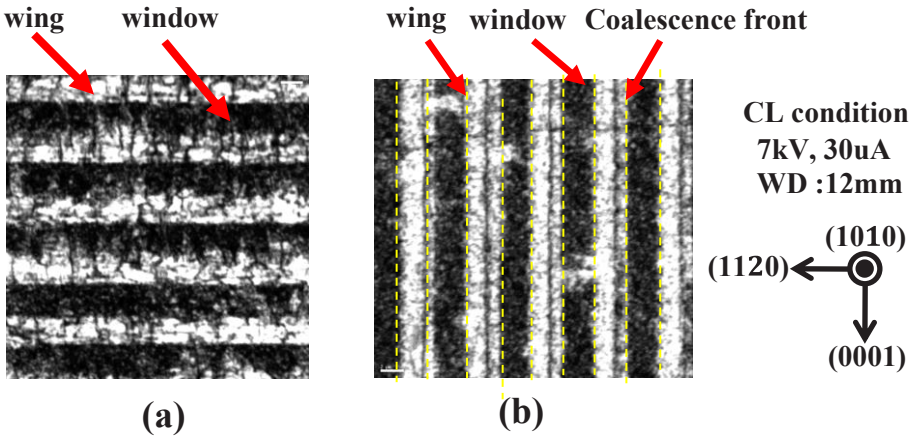

Fig 3. Cross-sectional cathodoluminescence images of *m*-GaN grown on (a)*a*-axis stripe pattern window and (b)*c*-axis stripe pattern window.

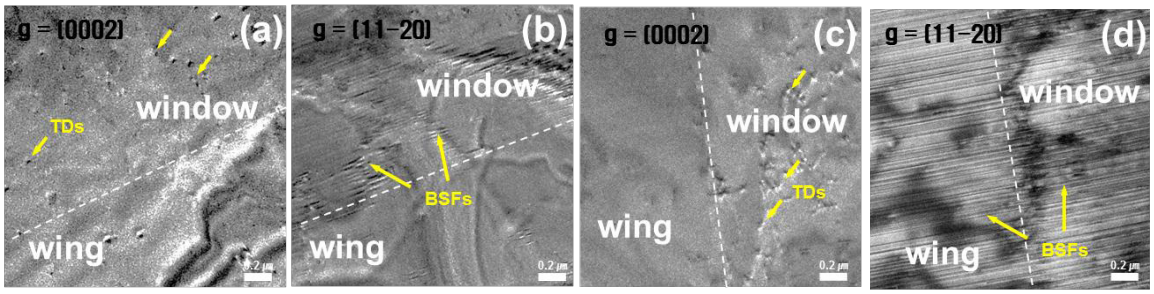

Fig 4. Planar transmission electron microscopic images of *m*-GaN grown on (a, b) *a*-axis stripes and (c, d) *c*-axis stripes.

[1] J. Tourre, O.Gourmala,Y.Andre´ , A.Trassoudaine, E.Gil, D.Castelluci, R.Cadoret. Journal of Crystal Growth 311(2009)

Spatially aligned nanostructures fabricated via lithographic techniques and their applications into photovoltaics

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Nanoimrpint lithography is an emerging lithographic technique, which can fabricate nanoscale features easily in academic laboratory. By using this technique, periodically aligned sub-micron features were generated in an array, which were then utilized to improve device efficiencies in various solar cells.

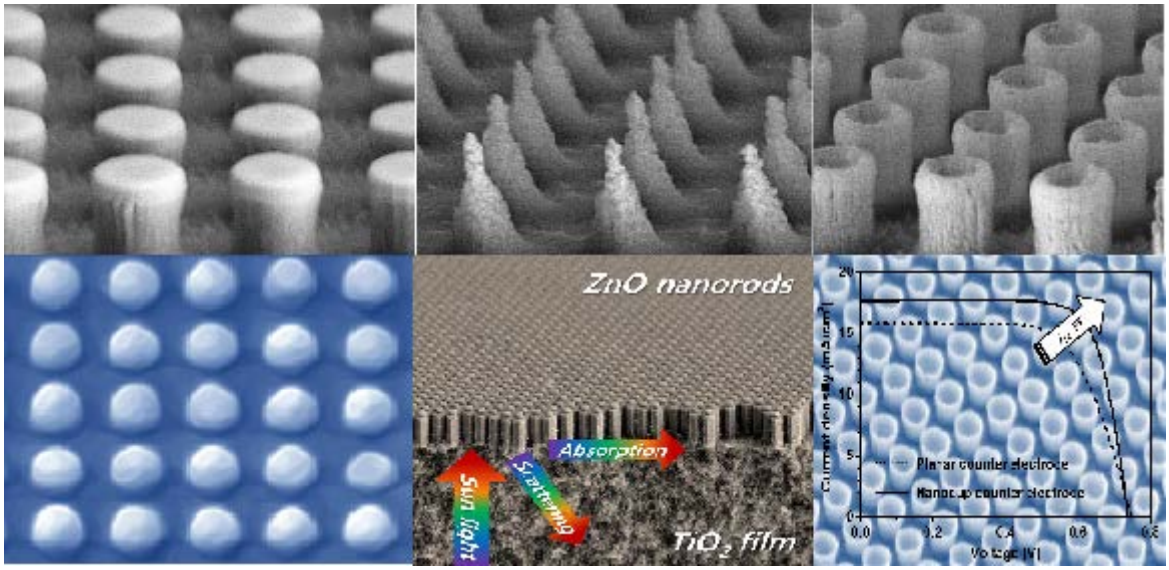

Figure 1. Various spatially aligned nanostructure arrays; Si rod, Si cone, Si tube, ZnO hemisphere, ZnO nanorods-embedded TiO_2 film, and Pt nanocups

Acknowledgments

This work was supported by the Basic Science Research program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (NRF, No. R15-2008-006-03002-0, CLEA, NCRC), the Pioneer Research Center Program (NRF, No. 2013M3C1A3063046) and a grant funded through the MEST (2011-0029414).

Solution-Based Synthesis of 2D Core/Multi-Shell Nanoplates through a Successive Epitaxial Growth of Bi_2Se_3 and Bi_2Te_3

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Bismuth chalcogenides have been intensively studied owing to their superior properties as thermoelectric and topological insulating materials.[1] Although, the nanomaterials of bismuth chalcogenides have been well synthesized by various techniques, however, the earlier works are mainly focused on synthesis of single-phase two-dimensional (2D) nanostructure.[2] Controlled synthesis of 2D heterostructures that are heterogeneous both in structure and composition, are highly desirable not only from fundamental scientific perspective but also to take advantage of the emergent properties that cannot be achieved from each individual counterpart. Herein, we demonstrate, for the first time, a scalable synthesis for preparing 2D bismuth chalcogenide heterostructures such as core/shell (Bi_2Se_3@Bi_2Te_3) and core/multi-shell nanoplates (Bi_2Se_3@Bi_2Te_3@Bi_2Se_3, and Bi_2Se_3@Bi_2Te_3@Bi_2Se_3@Bi_2Te_3),through a successive epitaxial growth of Bi_2Se_3 and Bi_2Te_3. By rational manipulation of the reaction conditions including molar ratios of precursors, amount of seed nanoplates and temperature, we could obtain various nanoplates in gram-scale quantities with controllable shell dimension, and tunable composition between Bi_2Se_3 and Bi_2Te_3 in a single nanoplate. During the seeded growth, newly formed nanoparticles were preferentially attached at the side and edge of seed nanoplates, followed by migration along the top/bottom surfaces and ultimately lead to epitaxial recrystallization into a single-crystalline nanoplate. After the whole series of seeded growth process, the lateral dimension of nanoplates grew up from 100 to 620 nm, while the thickness was slightly increased from 5 to 20 nm. We anticipate that this strategy can be further applied to prepare other 2D layered structures, as well as can also pave way for novel practical applications.

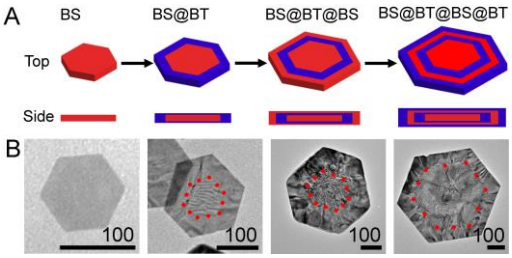

Fig. 1 Shape evolution from a seed Bi_2Se_3 (BS) nanoplate to multi-shell bismuth chalcogenide nanoplates

[1] Min, Y.; Roh, J. W.; Yang, H.; Park, M.; Kim, S. I.; Hwang, S.; Lee, S. M.; Lee, K. H.; Jeong, U. *Adv. Mater.* **2013**, *25*, 1425.

[2] Min, Y.; Moon, G. D.; Kim, B. S.; Lim, B.; Kim, J.-S.; Kang, C. Y.; Jeong, U. *J. Am. Chem. Soc.* **2012**, *134*, 2872.

Three-dimensional Si nano- and miro-structures using metal-assisted chemical etching

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Three dimensional (3D) device architectures with high aspect ratio are being introduced to address recent challenges associated with high performance and power consumption. We used metal assisted chemical etching technique to fabricate the 3D silicon nano-structures. Metal-assisted chemical etching is a wet-based solution, which enables damage-free and isotropic 3D nano-structures. Despite many advantages, metal-assisted chemical etching of Si tends to occur non-uniformly on Si wafers when the coverage of metal catalyst-on-Si extends in micron-scale [1]. We have investigated the lateral and vertical mass transports of reactants and products during the etching as a function of metal catalyst thicknesses. As the metal thickness becomes thinner, the overall chemical reaction occurred faster as a result of activated mass transport through vertical paths. When mass transport occurred through lateral and vertical paths for thin catalyst, chemical etching of Si occurred uniformly without typical metal bending problems. Results suggest that metal-assisted chemical etching of Si is not necessarily limited to nano-scale 3D fabrication. The mechanism proposed in this work advances the feasibility of metal-assisted chemical etching of Si for a variety of high aspect ratio nano- and micro-scale 3D fabrication.

[1] N. Geyer, B. Fuhrmann, Z. Huang, J de Boor, H.S. Leipner and P. Werner, JPCC, 116, 24. (2012)

압축기반 SSD에서 낸드 플래시 컨트롤러를 이용한 읽기 성능 향상 기법

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일반적으로 SSD(Solid State Drives)는 성능을 향상 시키기 위해 낸드(NAND) 플래시 메모리의 읽기/쓰기가 동시에 여러 채널에서 이루어지는 다중 채널(multi-channel) 구조를 사용한다. 또한 낸드 플래시 메모리의 수명 및 성능을 더욱 향상시키기 위한 압축기반 SSD에 대한 연구도 진행되고 있으며, 압축 알고리즘을 사용하는 상용 제품까지도 쉽게 접할 수 있다[1]. 일반적으로 압축기반 SSD에서 압축(Compression) 및 압축해제(Decompression) 과정은 특정 CPU 혹은 압축 H/W가 담당하도록 설계하여 데이터 압축 및 압축해제의 오버헤드를 감소시키기 위해 노력한다. 그럼에도 불구하고 압축기반 SSD에서의 읽기 요청은, 호스트로부터 순차적으로 도착하는 데이터를 압축하는 쓰기 요청과 달리, 다중 채널에서 요청된 데이터를 동시에 읽은 뒤에 압축 해제하는 과정이 진행된다. 따라서 압축해제가 단일 압축 하드웨어로 처리되는 경우 그림1과 같은 병목(bottleneck)현상을 발생시킨다. 다시 말해, 동시에 여러 채널로부터 페이지 읽기가 완료되더라도 압축해제 과정이 동시에 처리되지 못하므로 성능이 감소하게 된다. 따라서 우리는 낸드 플래시 메모리로부터 읽은 페이지에서 특정한 논리 페이지를 구분하여, 압축해제를 할 수 있는 낸드 플래시 컨트롤러를 제안하며 제안하는 기법을 사용하면 그림 2와 같이 읽기 과정에서 발생하는 병목 현상이 사라져 압축기반 SSD의 읽기 성능이 향상된다.

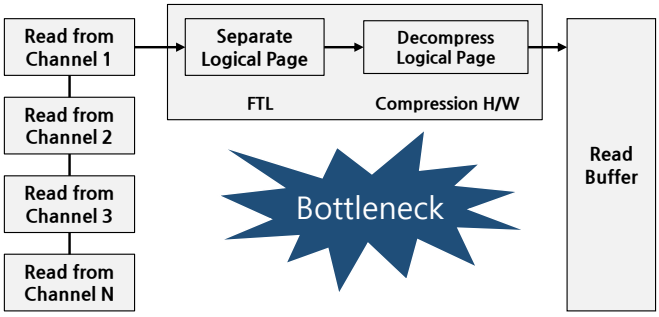

그림 1. 압축기반 SSD에서 읽기(Read)의 병목현상

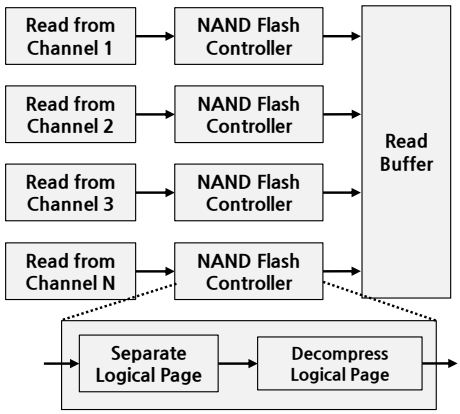

그림 2. 제안하는 NAND 플래시 컨트롤러

[1] Y. Park, and J. S. Kim. zFTL: power-efficient data compression support for NAND flash-based consumer electronics. IEEE Transactions on Consumer Electronics vol. 57, no. 3, 2011

Optimizing Fsync Performance with Dynamic Queue Depth Adaptation

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Recent storage devices such as eMMC and SSD support the command queueing [1] in order to improve the storage I/O bandwidth. The command queueing allows multiple read/write requests to be pending. Since the multi-channel and multi-way architectures of eMMC and SSD can handle multiple requests simultaneously, the command queueing is indispensable technique for them. However, the command queueing can be harmful to the latency of fsync system call, the latency of which is critical to application responsiveness. All pending I/O requests should be completed before the fsync system call. We investigated the fsync latencies under different queue depths. As shown in Fig 1, the fsync latency increases as the queue depth increases since the fsync latency is affected by the number of queued I/O requests which have arrived before the fsync-related requests. However, the I/O bandwidth reaches the maximum value when the queue depth is equal to 4, and there is no significant changes when the queue depth is larger than 4. Therefore, too large number of queue depths will be detrimental to fsync latency without any improvement on I/O bandwidth. We propose a queue depth adaptation technique, which reduces the queue depth before user application sends fsync calls as shown in Fig 2. We profiled the file system behavior, and found several file types for which the fsync calls are frequently used. For example, SQLite DB and .xml files are flushed into the storage by the fsync calls. The proposed technique monitors the opened files, and reduces the queue depth if there is a high probability of fsync calls in order to provide fast responsiveness.

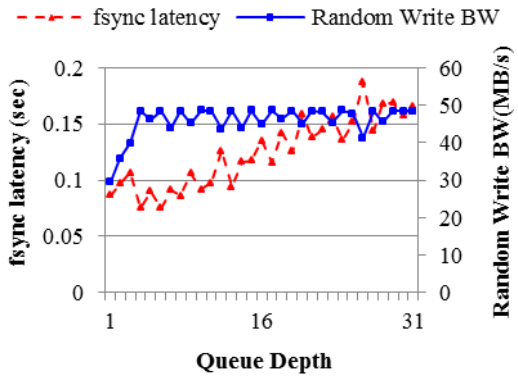

Fig 1 Increment of fsync latency w/ random writes

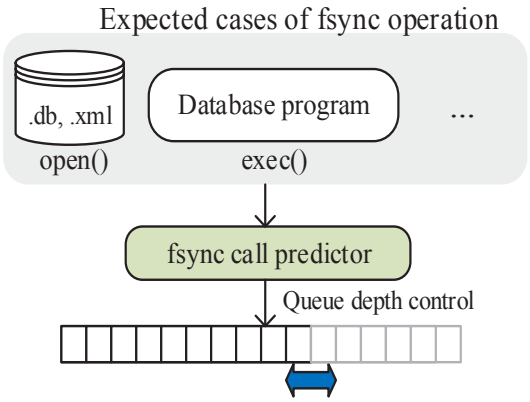

Fig 2 Queue depth Adaptation technique

[1] Dees, Brian. "Native command queuing-advanced performance in desktop storage." Potentials, IEEE 24.4 (2005): 4-7.

Optimization of Streaming Application with Limited Scratch-pad memory on Coarse-grained reconfigurable architecture.

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Coarse-grained reconfigurable architecture(CGRA) present an appealing hardware platform by providing the potential for high computation throughput, scalability, low cost, and energy efficiency. [1]. StreamIt is a programming language and a compilation infrastructure, specifically engineered for modern streaming systems. It is designed to facilitate the programming of large streaming applications, as well as their efficient and effective mapping to a wide variety of target architectures. [2]. In our previous work, we developed the special processing elements of CGRA architecture In this paper, we propose the optimization technique of streaming applications for the previously developed CGRA architecture in two steps. First of all, we optimize streaming applications to exploit a high degree of instruction level parallelism (ILP) on CGRA. Secondly, we increase the work count parameter within limited local memory size. The work count refers to the number of iterations of each filter in streaming benchmarks. And we compare our experimental results to general purpose GPUs (GPGPUs), in terms of performance and energy consumption.

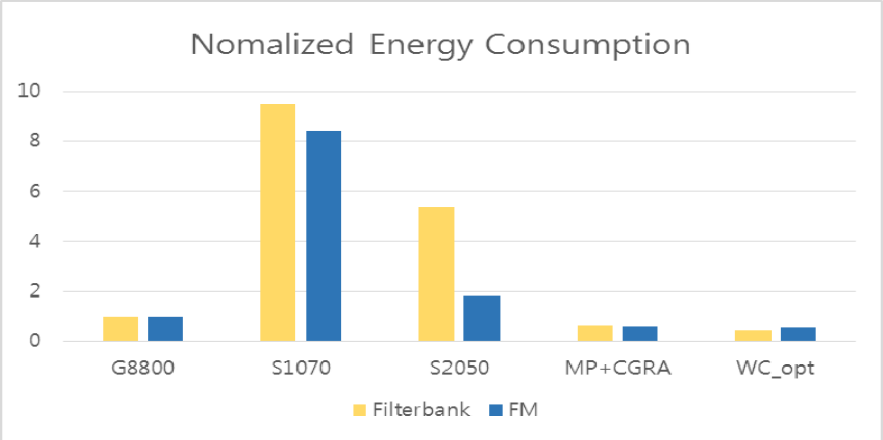

Fig 1. Performance and Energy consumption of CGRA compared to GPGPUs

[1] THIES, W., Karczmarek, M., AND Amarasinghe, S. 2002. StreamIt: a language for streaming applications. In Proc. Intl. Conf. on Compiler Construction.

[2] . Park, H. Park, and S. Mahlke. Cgra express: accelerating execution using dynamic operation fusion. In CASES ’09: Proceedings of the 2009 international conference on Compilers, architecture, and synthesis for embedded systems
, pages
271–280, New York, NY, USA, 2009. ACM

Offline Deduplication with Lightweight Hash for Solid State Disk

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Deduplication technique can expand the lifespan and capacity of flash memory-based storage device by eliminating duplicated write operations. The deduplication techniques can be classified into two approaches, i.e., online and offline approaches, based on the time of deduplication processing. During runtime, the online deduplication [1] checks each incoming page, and drops it if there is a same page in the storage. Instead, an address translation entry is registered in order to remap the read request on the deduplicated page. The online deduplication may increase the write latency since it should generate a complicated hash key for each page and should check whether there is a same page in the storage. Furthermore, at sudden power-off situation, the storage device cannot recover the deduplicated page if the corresponding address translation information is not flushed into non-volatile storage. The offline deduplication [2], on the other hand, finds the duplicated pages during idle time. It can hide the deduplication overhead by exploiting idle time, and it is not vulnerable to the sudden power-off. The offline dedplication can reduce the garbage collection overehad by eliminating copy operations on duplicated pags.

While the previous offline technique used a high-cost hash algorithm, our new approach uses only a lightweight hash algorithm such as CRC as shown in Fig1. Therefore, the memory space for caching hash keys can be removed, and more pages can be examined for deduplication during short idle intervals. As a result, it can reduce the write latency compared to online approach, and can reduce the garbage collection overhead compared to the previous offline deduplication technique.

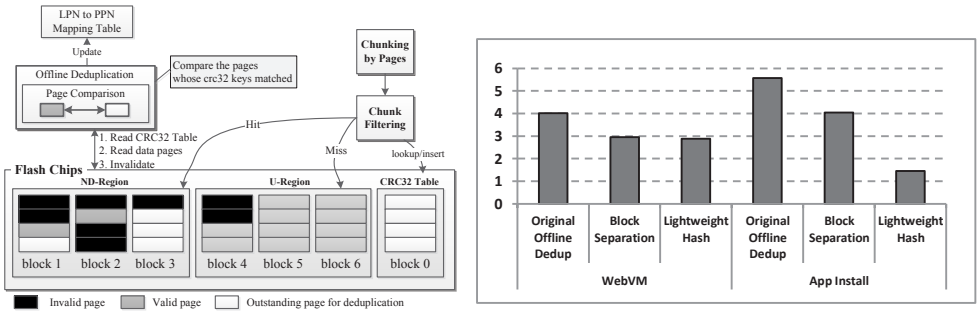

Fig 1 Architecture of suggested technique and normalized number of page copies in foreground GC

[1] F. Chen et al., "CAFTL: A Content-Aware Flash Translation Layer Enhancing the Lifespan of Flash Memory based Solid State Drives," FAST, 2011.

[2] A. Jeongcheol, S. Dongkun, "Offline Deduplication-Aware Block Separation for Solid State Disk," FAST, 2013.

Optimal Resource-aware Mapping of Stream Graphs to GP-GPUs

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General purpose applications running on GPGPU has significant performance improvement than compared to that running on traditional CPU. However, this performance benefit is ambiguous in case of streaming applications which are data-intensive and usually contains low computation to communication ratio. Conventional programming model such as StreamIT represents the streaming applications as a graph of filters and communication channels [1]. Communication channels are the FIFO buffers responsible for transferring data between filters. Due to the high communication data transfer rate between filters, placing the channels in GPU global memory may saturate the memory bandwidth and severely hinder the performance. Focusing on the problem, state-of-the-art [2] preferred allocating those channels in the much faster GPU shared memory. However, the shared memory along with other resources of GPU such as number of registers is limited and has to be exploited carefully. A large scale graph may violate the constraints of resources, leading to scarce shared memory. Due to this, it is infeasible to implement the graph on GPU. Additionally, oversized graph may lead to register spilling which severely degrades the performance. In this paper, we address this problem of partitioning the graph of streaming applications into smaller fractions in order to satisfy the resource constraints as well as maximize the performance. We propose a novel partitioning method based on the combined ILP-Genetic algorithm, targeting both single GPU and multi-GPUs case.

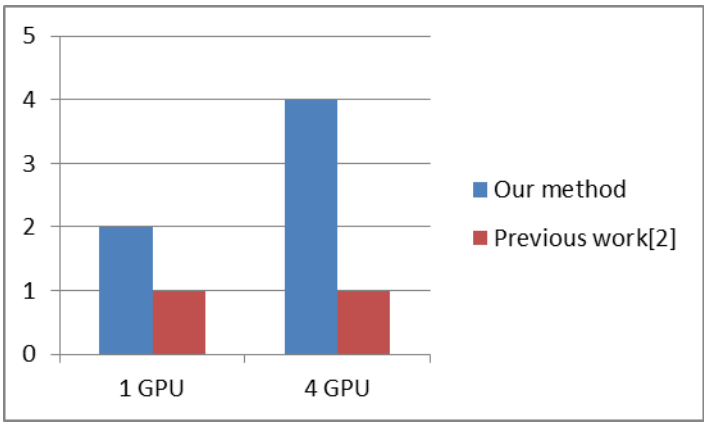

Fig 1. Number of partitions compared to previous work [2]

[1] W. Thies, M. Karczmarek and S. Amarasinghe, “StreamIt: A Language for Streaming Applications” in Proc. of the 11th International Conference on Compiler Construction CC '02

[2] A. Hagiescu, H. P. Huynh, W. F. Wong, and R. S. M. Goh, “Automated architecture-aware mapping of streaming applications onto GPUs” in 2011 IEEE International Parallel and Distributed Processing Symposium (IPDPS ’11), 2011.

[3] H. P. Huynh, A. Hagiescu, W.-F. Wong, and R. S. M. Goh, “Scalable framework for mapping streaming applications onto multi-GPU systems,” in Proc. of the 17th ACM PPoPP’12.

A Low Phase Noise 30GHz Frequency Synthesizer for 802.11ad

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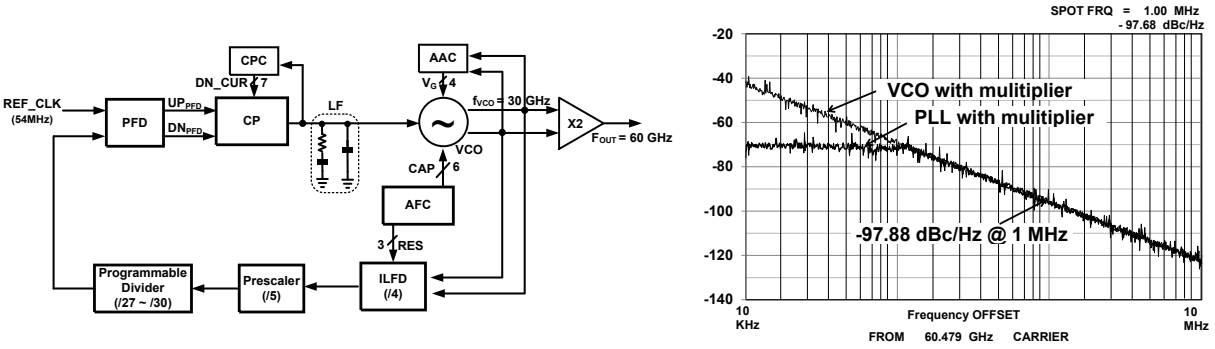
최근, 대용량 데이터에 대한 무선통신을 요구하고 있지만, 3G/4G 의 주파수 대역에서는 수 Gbps 의 데이터통신을 하기에 제한이 많다. 따라서 60 GHz 의 mmwave 대역을 이용함에 따라 수 Gbps 의 무선데이터통신을 할 수 있기 때문에, 이 분야에 대한 연구가 진행되고 있다.

본 논문에서는 60GHz 의 mmwave 대역에서 사용할 수 있는 30GHz 주파수 합성기에 체배기를 이용하여 60GHz 를 생성하였으며, 30GHz 의 주파수 합성기를 설계하기 위해서 높은 주파수를 발생하기 위해서 LC 전압제어발진기와 30GHz 의 발진주파수를 분주할 수 있는 Ring-type ILFD 가 제안된다. 그리고 디지털로 구성되어 있는 자동주파수보정기를 이용하여. 전압제어발진기와 ILFD 의 주파수를 보정한다. 그리고 체배기를 통한 주파수합성기의 주파수인 60.48GHz 의 phase noise 는 1MHz 에서 -98dBc/Hz 를 가지며, 제안하는 주파수 합성기의 1V 의 공급전압에서 전체 power 는 55mW 를 소모하며, 65nm CMOS 공정을 이용하여 설계하였다.



(a) (b)

Fig 1. (a) Block Diagram and (b) Phase noise measurement Result of 30GHz Frequency synthesizer

[1] B. Sadhu, M. Ferriss, A. Natarajan, S. Yaldiz, J.O. Plouchart, A. Rylyakov, A. Valdes-Garcia, B. Parker, A. Babakhani, S. Reynolds, X. Li, L. Pileggi, R. Harjani, J. Tierno and D. Friedman, "A Linearized, Low-Phase-Noise VCO-Based 25-GHz PLL With Autonomic Biasing," IEEE J. Solid-State Circuits, vol. 48, no. 5, pp. 1138–909, May. 2013.

[2] C.-C. Chen, Chi-Hsueh Wang, Bo-Jr Huang, Hen-Wai Tsao, and Huei Wang, "A 24-GHz divide-by-4 injection-locked frequency divider in 0.13-μm CMOS technology," in Proc. IEEE A-SSCC, 2007, pp. 340-343.

Wide Range Driver Amp for TVWS with tunable filter characteristic

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최근, 모바일 시대가 본격화 함에 따라 Wifi 라고 알고 있는 2.4GHz 대역에서 데이터 이용량이 급증하고 있다. 이렇게 한정된 주파수 내에서 여러 사람들이 동시에 통신을 하게 되면, 신호 간에 간섭이 발생하고 이는 신호 품질 저하를 야기시킨다. 이러한 문제점을 해결하기 위해, TV White Space (TVWS) 송수신기 연구 개발이 활발히 이루어지고 있다. TVWS 란 470M~698MHz 의 주파수 대역으로, DTV 방송대역 중 사용하지 않고 비어있는 주파수 대역을 의미한다. 이 대역은 방송과 공존을 통해 서비스가 가능한 지역으로 부족한 주파수를 충당할 수 있기 때문에 연구가 활발히 진행되고 있다.

TVWS 는 방송 주파수이기 때문에 인접 채널의 간섭 신호가 상당히 크다. 따라서 신호의 주파수를 제외한 다른 신호들은 차단하여 송신할 수 있는 높은 성능의 DA 가 요구된다.

본 논문에서는 TVWS 대역에서 송신하는 신호의 주파수를 제외한 간섭 신호는 차단될 수 있도록 Tunable 필터 특성을 가진 광 대역 Driver Amplifier(DA)를 제안한다.

신호 주파수에 따라, 필터의 중심주파수가 이동하면서 필터 특성을 가지는 구조이며, 필터의 중심 주파수가 신호 주파수에서 벗어나 있는 경우, 피드백 루프와 알고리즘을 통해 필터 중심 주파수가 신호의 주파수를 찾아 갈 수 있는 구조를 제안한다. 피드백 루프는 DA, Envelope Detector, 4Bit ADC, 디지털 알고리즘으로 구성된다. 또한, 파워컨트롤 비트<3:0>을 두어 -6~10dBm 의 파워 크기로 컨트롤하여 송신할 수 있다.

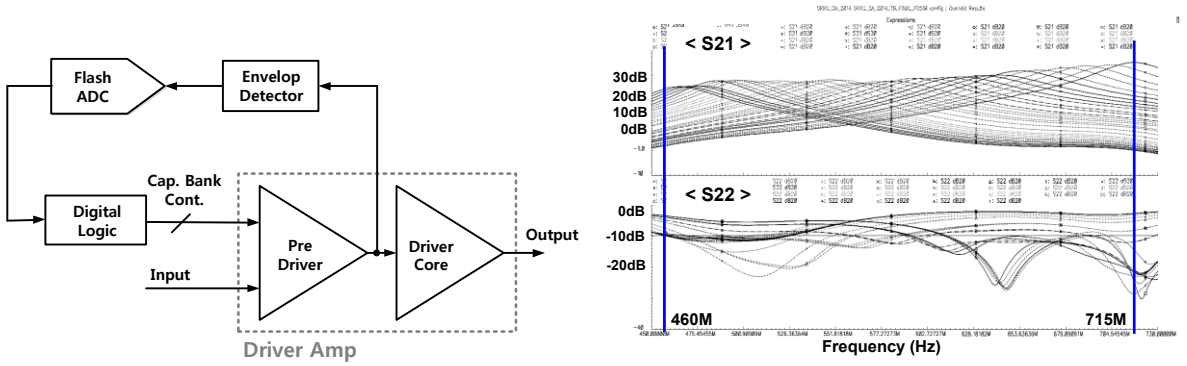

Fig 1. Block Diagram and results

[1] Desheng Ma, Fa Foster Dai, “A 7.27GHz Q-Enhanced Low Noise Amplifier RFIC With 70 dB Image Refection Ratio”, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 20, NO. 8, AUGUST 2010

[2] Razavi, 1999, Design of Analog CMOS Integrated Circuits.MC Graw Hill.

2 단계 자동 진폭 캘리브레이션 기법을 적용한 넓은 튜닝 범위를 갖는 클래스-C 타입 전류 재사용 전압 제어 발진기 설계

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최근 급성장하고 있는 무선 어플리케이션 시장에서는 RF 무선 송수신기의 저전력, 고집적 등의 성능을 요구하고 있다. 이와 같은 요구 사항을 만족하고 신뢰도 있는 통신 시스템을 구현하기 위해서는 RF 시스템을 구성하는 요소 중에 하나이고, 주파수를 구현하는데 사용되는 전압 제어 발진기 역할의 중요성이 점점 부각된다. 그리하여 현재 저전력, 저 잡음, 고주파 동작 등의 성능을 가진 수많은 전압 제어 발진기가 CMOS 공정을 사용하여 개발되고 있다[1]. 무선 송수신기를 구성하고 있는 블록들 중에서 전압 제어 발진기는 전류를 많이 소모하는 블록 중 하나이다. 그러므로 전압 제어 발진기에서 전력 소모를 최소화하면서 낮은 위상 잡음 특성을 갖는 저전력 전압 제어 발진기 구현이 필수적이다. 본 논문에서는 넓은 튜닝 범위를 갖는 클래스-C 타입 전류-재사용 전압 제어 발진기를 설계하였다. 전류-재사용 전압 제어 발진기의 차동 출력 전압 간의 불균형을 최소화하기 위해서 2-스텝 자동 진폭 캘리브레이션 기법을 적용하였고, 이 기법은 넓은 튜닝 범위를 갖도록 전압 제어 발진기의 DC 전류를 조절하는 역할도 하게 된다.

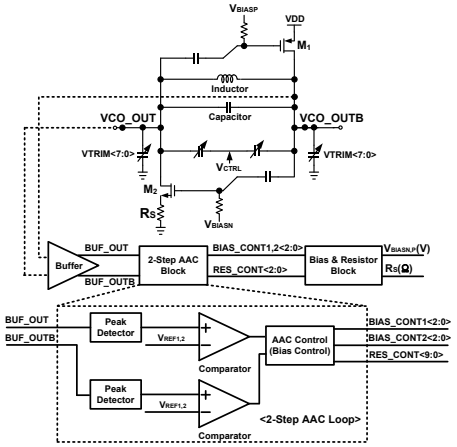

그림 1. 제안하는 클래스-C 전류 재사용 전압 제어 발진기 회로도 및 캘리브레이션 블록다이어그램

[1] Chin-Lung Yang, Yi-Chyun Chiang, “Low Phase-Noise and Low-Power CMOS VCO Constructed in Current-Reused Configuration”, IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS, VOL. 18, NO. 2, FEBRUARY 2008

Single to Differential Low Noise Amplifier with Automatic Mismatch Calibration Circuits

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A low power inductorless Low Noise Amplifier (LNA) applied to low power FSK transceiver is proposed. While general LNA has differential input and differential output, this paper presents single to differential conversion (StoD) structure in order to reduce cost and minimizing chip size eliminating external elements. But this structure has fatal drawback that is mismatch of differential output and it is more serious in PVT variation. To solve this problem , AMC(automatic mismatch calibration) loop for compensation of output signal mismatch is proposed. I not only compensates mismatch of output sognal but also enables low power design. Balance of gain and phase is also achieved. The gain of CS stage is re-used to boost the transconductance of CG stage, and hence, a noise and power efficiency is improved. This prototype was realized in 0.18um CMOS process and achieves a noise figure of 4.1dB, voltage gain above 17dB at FSK target frequency range902~928MHz) and power disspation of 2.1mW from 1.8 V supply.

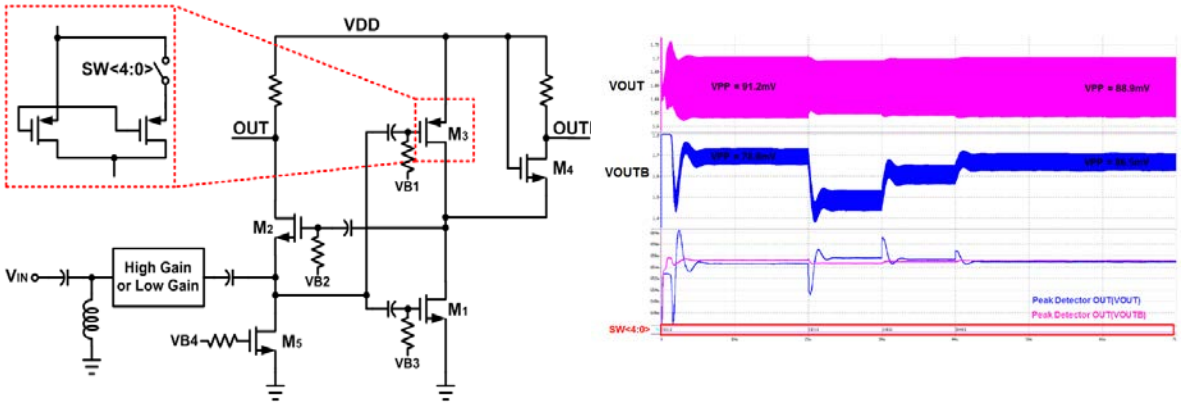

Fig 1. Proposed CS-CG stage based LNA circuit topology and AMC loop transient simulation results

[1] Ju-sung Kim, Jose Silva-Martinez, “Wideband Inductorless Balun-LNA Employing Feedback for Low-Power-Voltage Apllication,” *IEEE Trans. Microwave Theory & Tech.,* vol. 60, no. 9, pp. 2833-2842, September 2012.

[2] H.wang, L. Zhang, and Z. Yu “A wideband inductorless LNA with local feedback and noise cancelling for low-power low voltage applications,” *IEEE Trans. Circuits Syst.,* vol. 57, no.8, pp. 1993-2005, Aug. 2010.

A Low-Noise and Wide-Range VCO with Bias Voltage Compensation for Mobile Telecommunication

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최근 전자제품은 스마트폰, 태블릿 PC 등의 무선통신 단말기가 주류가 되어 출시 되고 있으며, 이러한 제품들은 이동통신사가 제공하는 3 세대, 4 세대 이동통신(LTE) 외에 Wi-Fi, Bluetooth 등 다양한 주파수 대역의 무선통신방식을 동시에 지원하고 있다. 무선통신 시스템의 성능은 주파수를 합성하는 전압 제어 발진기의 성능의 영향을 크게 받는다. 발진기의 위상잡음 성능은 공정, 전압 그리고 온도의 변화에 매우 민감하다. 본 논문에서 제안하는 전압 제어 발진기는 능동소자의 트랜스컨덕턴스 선형화 기반으로 설계하였다. 제안하는 전압 제어 발진기 구조는 낮은 바이어스를 전압이 낮을 수록 진폭 및 위상잡음 성능이 개선된다. 하지만 낮은 바이어스 전압 조건에서는 미세한 전압 변화에도 전류량이 급격히 줄어들어 최적을 성능을 낼 수 없거나 발진하지 못한다. 이에 바이어스 전압 보상회로를 적용하여 전압 변화에도 안정적인 바이어스 전압을 인가하고 낮은 위상잡음 특성을 유지할 수 있도록 하였다. 본 회로는 CMOS 0.18um 공정을 이용하여 설계하였으며 중심주파수 2.4GHz 에서 주파수 조정 범위 50%, 위상잡음은 1MHz 오프셋에서 -126dBc/Hz, 총 소모전류는 4mA 이다.

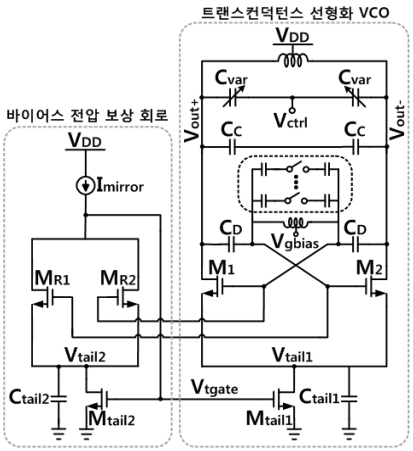

Fig 1. 바이어스 전압 보상회로 가진 트랜스컨덕턴스 선형화 VCO

[1] B. Sadhu et al., "A linearized, low-phase-noise VCO-based 25-GHz PLL with autonomic biasing", IEEE Journal of Solid-State Circuits, Vol. 48, No. 5, pp. 1138-1150, May 2013.

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A 2.4GHz 0.18um CMOS Self-Biased Cascode Power Amplifier

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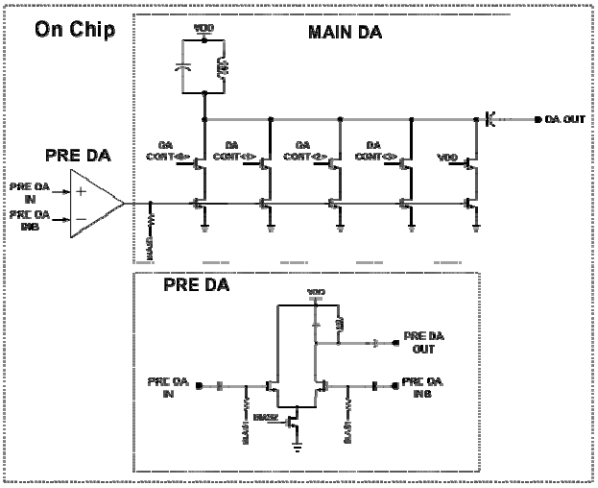
The wireless communication standard Bluetooth is one of the applications that requires CMOS integration to achieve low cost and therefore consumer acceptance. Recently, several fully integrated transceivers in CMOS technology for Bluetooth have been demonstrated.

There are two main issues in the design of power amplifiers in submicron CMOS, namely, oxide breakdown and hot carrier effect.Both of these get worse as the technology scales. The oxide breakdown is a catastrophic effect and sets a limit on the maximum signal swing on drain. The hot carrier effect, on the other hand, is a reliability issue. It increases the threshold voltage and consequently degrades the performance of the device.

we propose a self-biased cascode transistor that allows RF swing . This enables us to design the PA such that both transistors experience .



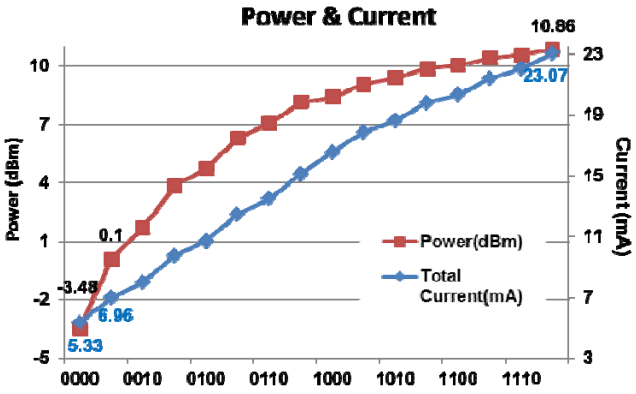


Fig 1. Schematic of Power Amplifier and Power, Current graph

[1] Tang, Y. ; Qualcomm, San Diego, CA, USA ; Chen, M. ; Leung, W. ; Narathong, C. more authors , “A configurable multi-band multi-mode transmitter with spur cancellation through digital baseband”, Symposium on VLSI Circuits (VLSIC)

Synthesis of Ru-Mn alloy thin films by atomic layer deposition as a Cu direct-plateable diffusion barrier

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As semiconductor devices are scaled down for better performance and more functionality, copper (Cu)-based interconnects suffer from an unwanted increase in the resistivity of the Cu wires due to the size effect on the resistivity of the metal film. One of the solutions to address it is to increase the volume of electroplated (EP)-Cu filled into the trench. One can increase the volume of EP-Cu filled into the trench using a thinner but conformal diffusion barrier and seed layer. The portion of Cu in the interconnects structure can be increased further using a direct plating because the electroplating of Cu can be achieved on a diffusion barrier without a seed layer. Ru has been suggested as a diffusion barrier that is compatible with the direct plating of Cu. However, previous studies showed that Ru itself is not a suitable diffusion barrier for Cu metallization due mainly to its poor microstructure with polycrystalline columnar grains [1]. This study developed Ru-based alloy thin films, RuMn, which is compatible with the direct plating of Cu, using atomic layer deposition (ALD) process at 225 ^{o}C. Mn was incorporated into the Ru by combining the Ru and Mn ALD sub-cycles [Fig. 1]. The results on ALD- RuMn were shortly described. SIMS analysis showed that the Mn content in Ru can be controlled by the ratio of the number of Ru and Mn ALD unit-cycles in the sub-cycles. XRD and TEM results indicate that ALD-Ru film prepared without Mn ALD cycle forms a polycrystalline structure with columnar grains. But, with incorporating the Mn cycles, RuMn films were formed with non-columnar grains and nano-crystalline microstructure [Fig. 2]. It should be noted that after annealing ALD-RuMn film at 500 ^{o}C, the self-formation of Mn silicate barrier between Ru(Mn) film and SiO_2 was confirmed based on XRD and TEM analysis, which was due to the diffusion of Mn into underlying SiO_2 [Fig. 3]. Diffusion barrier performance of ALD-RuMn was superior as compared to Ru counterpart. XRD analysis showed that the structure of Cu/ALD- RuMn (~5 nm)/Si was stable after annealing at 600 ^{o}C for 30 minute while Cu/Ru (~5 nm)/Si structure was failed after annealing at 500 ^{o}C. It was also shown that the electroplating of Cu was directly achieved on a very thin (~7-nm-thick) ALD-RuMn film.

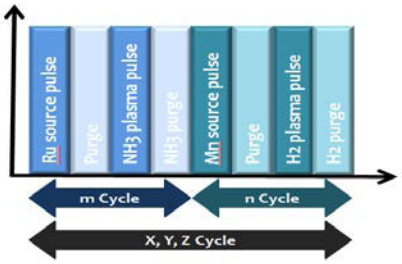

Fig. 1 Schematic diagram of process sequence of ALD Ru-Mn films.

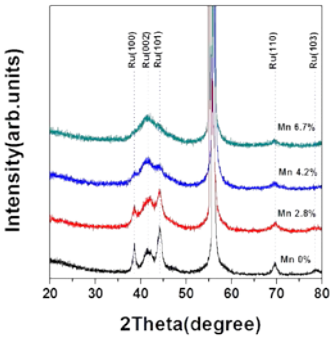

Fig. 2 The XRD of ALD-Ru and Ru-Mn films.

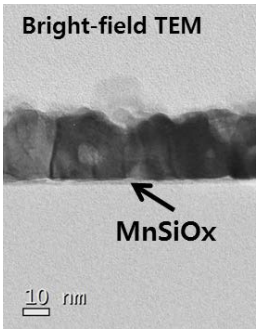

Fig. 3 XTEM image of the self-formation of Mn silicate barrier

References

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Acknowledgements

The precursor used in this study was provided by Hansol chemical (Ru precursor) and UP chemical (Mn precursor). This work was supported by the Technology Innovation Program (Industrial Strategic technology development program, 10035430, Development of reliable fine-pitch metallization technologies) funded by the Ministry of Knowledge Economy (MKE, Korea).

Highly reliable Cu interconnect using CVD Ru liner for 10 nm node logic device and beyond

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Superior gap-fill performance is demonstrated with CVD Ru liner/Cu reflow process for 10 nm and even 7 nm node equivalent patterns. According to our model for void generation, the key aspects for void-free gap-fill include higher bottom-up rate inside a trench with well-controlled Cu nucleation at the field area as well as uniform reflow topology inside the patterns. The initial TDDB issue was successfully addressed with stable post CMP passivation and robust ULK. A TDDB mechanism is also proposed for the Ru liner/Cu reflow scheme. Another reliability concern, which is lower EM activation energy, was eliminated by the application of metal capping which improves the EM lifetime to longer than 100 years. The SRAM yield for 10 nm node device was successfully achieved, making this optimized CVD-Ru/Cu reflow a promising candidate for 10nm beyond technology node.

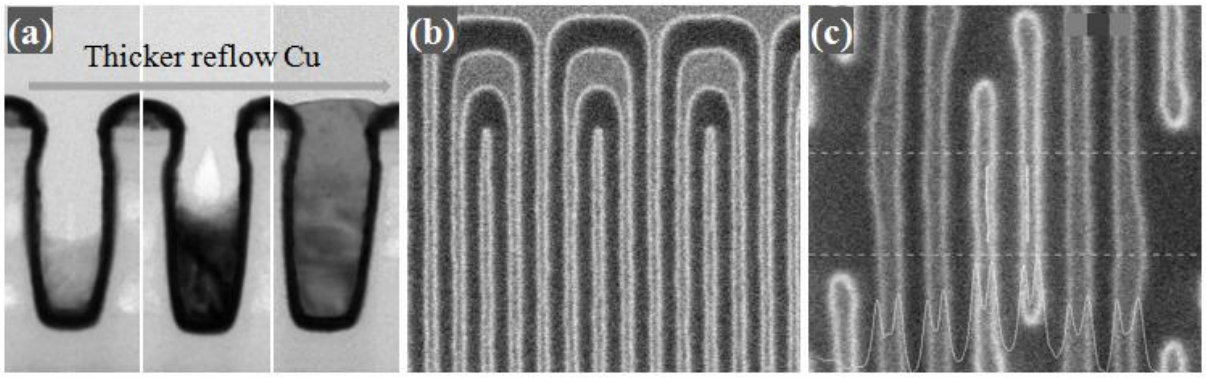

Fig 1. TEM images after Cu reflow for different reflow thickness at trench pattern which shows bottom up fill by reflow (a), Top down SEM image after Cu fill at 7 nm equivalent line and space pattern (b) and dual damascene pattern (c)

Ru thin films by thermal atomic layer deposition using H_2 molecules as a non-oxidizing reactant

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[1]*School of Materials Science and Engineering, Yeungnam University, 214-1, Dae-dong, Gyeongsan-si, 712-749, Korea.*
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[3]*Busan Center, Korea Basic Science Institute, 1275 Jisadong, Gangseogu, Busan, 618-230, Korea*
[4]*TANAKA Kikinzoku Kogyo K.K., 22, Wadai, Tsukuba, Ibaraki 300-4247, Japan*
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Ruthenium (Ru) thin films is an attractive material in the area of the semiconductor device technologies such as an electrode for the DRAM capacitor [1], a seed layer for Cu metallization [2], and a gate electrode[3] on account of their low resistivity of around 7 μΩcm, high chemical stability and high work function of around 4.7 eV. Ru thin films are expected to be used in various systems such as nonvolatile memory devices with Ru nano-crystals, the fabrication of nano-devices, and the formation of nano-catalysts. For these applications, the deposited Ru thin film needs the properties such as excellent step coverage and thickness uniformity. In these respects, atomic layer deposition (ALD) process can be considered as a potential solution to prepare Ru thin film. In the previous reports, the investigations on Ru ALD could be deposited by using molecular oxygen (O_2) as a reactant. These films showed excellent properties with the high conductivity and ~100 % of step coverage in the high-aspect ratio structure. However, an O_2-based Ru ALD process has the potential problem of an oxidation of the underlying Ta-based diffusion barrier and underlying W or Ti-based storage node contact when used as seed layer or Cu line or bottom electrode of DRAM capacitor. It is caused the increasing of structure's resistivity and poor adhesion in the device structure. To solve these problems, in this study, a thermal Ru ALD process was developed by using H_2 molecules as a non-oxidizing reactant. ALD-Ru films were deposited using travelling-wave type thermal ALD reactor (Lucida D100, NCD Technology, Korea) using a sequential supply of a new beta-diketonate Ru metallorganic precursor and H_2 molecules as a reactants. The deposition temperature was 250 °C. Figure 1 shows the XRD result of ALD-Ru. The clear crystalline peaks are shown the hexagonal Ru crystal structure was observed at the deposition temperature of 250 °C. It was also found that a high quality Ru film with the resistivity of ~37μΩ-cm could be deposited by using H_2 molecules as a non-oxidizing reactant by controlling the deposition condition. The step coverage of ALD-Ru films was excellent, approximately ~100 % over the trench structure of top opening width: 25nm with the aspect ratio of ~4.5 (Fig. 2). And, the deposited ALD-Ru films were evaluated as an application of a seed layer for Cu electroplating and bottom electrode of higk-*k* MIM capacitor.

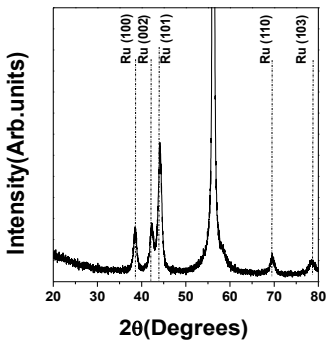

Figure 1. XRD result of thermally grown ALD-Ru film

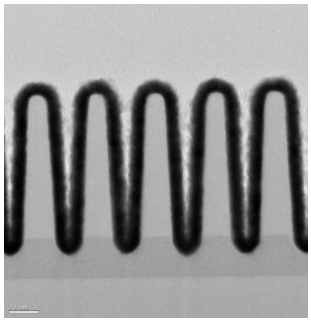

Figure 2. Cross-sectional view TEM image to show the step coverage of ALD-Ru film

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[3] Y.-S. Suh, H. Lazar, B. Chen, J.-H. Lee, and V. Misraa, J. *Electrochem. Soc*., **152**, F138 (2005).

Effect of Post-Annealing Treatments on the Interfacial Reliability of Co Capping layer for Advance Cu Interconnects

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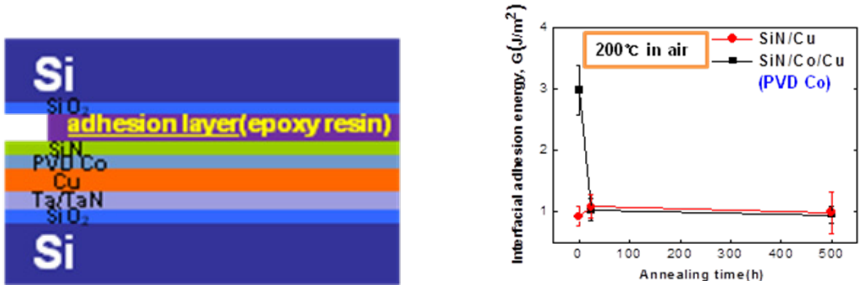
A recent trends in the interconnect application for semiconductor devices is miniaturized size and high performance, which is used to achieve multilevel devices with reliability and high conductivity. As the line width of microelectronic devices was reduced, the reliability problems of circuit devices become more important. The Cu line was delaminated, corroded and contaminated after chemical-mechanical polishing during damascene Cu process[1]. Therefore, interfacial adhesion is a key issue in integration and reliability of chip interconnect.

In this study, there were few reports on the systematic investigations of the post-annealing effects on the quantitative interfacial adhesion and reliability of Co capping layer system. In this work, the double cantilever beam technique was used to quantitatively the adhesion energy of the Co capping layer. Successfully demonstrated the capability of the double cantilever beam technique in determining the quantitative interfacial adhesion strength of SiN/Cu and SiN/Co/Cu thin film structures. The interfacial adhesion energy gradually decreased with increasing time in both conditions of post-annealing, which was closely correlated with the oxide layer formation SiN/Cu, SiN/Co interface.



(a) (b)

Fig 1. (a) Schematic diagram of SiN/Co/Cu/Ta/TaN/SiO_2 multilayer and (b) Interfacial Adhesion energy of SiN/Cu, SiN/Co/Cu multilayer during post annealing.

[1] J.K. Kim and Y.B. Park, Japanese Journal of Applied Physics, 52, 10MC05, (2013)

Enhancement of graphene-based Cu diffusion barrier properties by controlling grain size

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For Cu interconnects, diffusion barriers are essential to effectively prevent interdiffusion and reaction between Cu and semiconductor materials[1]. Numerous researches have investigated on the adequate materials as diffusion barriers of Cu, but, critical challenges have emerged with the continuous scaling down of feature size in ultra large scale integrated circuit (ULSI) technology. Tremendous efforts have been devoted in the past years to the development of an alternate diffusion barrier material of Cu [2]. However, it had been reported that the thermal stability of these layers are relatively poor compared to those of thicker diffusion barrier layers due to the high defect densities and fast diffusion resulting from grain boundaries [3]. Therefore, investigation on novel material for ultrathin diffusion barrier layer which can fulfill all the requirements such as low resistivity, thermal stability, and low interfacial reaction with Si is highly necessitated.

In this study, we demonstrate the capability of chemical vapor deposition (CVD)-grown single- and multi-layers of graphene as a diffusion barrier of Cu at different temperature regimes. In specific, the performance of single-layer graphene (SLG) and multi-layer graphene (MLG) that have different grain sizes and layers was evaluated in terms of thermal stability and time-dependent dielectric breakdown property. We found that the grain size of graphene layer is the main factor that determines the diffusion barrier properties of graphene-based Cu barriers.

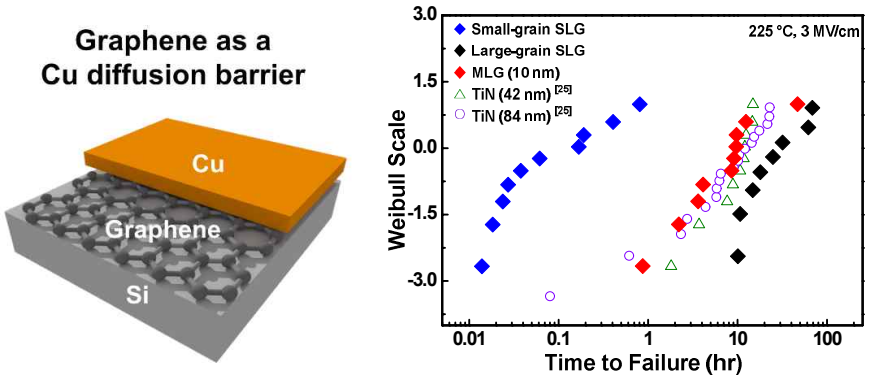

Fig 1. Schematics of Cu/graphene barrier/Si structures and time to failure for graphene and TiN diffusion barriers

[1] C. Chang, J. Appl. Phys. 1990, 67, 566; b) T. Nitta, T. Ohmi, M. Otsuki, T. Takewaki, T. Shibata, J. Electrochem. Soc. 139, 922 (1992).
[2] The International Technology Roadmap for Semiconductors, Available from www.itrs.net (2012).
[3] D. Josell, S. H. Brongersma, Z. Tokei, Annu. Rev. Mater. Res. 39, 231(2009).

구리 배선에서의 자기조립단분자막의 활용

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반도체 공정 기술의 발달 및 미세화에 따라 배선 금속 물질로 사용하던 알루미늄보다 높은 전도도를 가지면서 electromigration 에 덜 취약한 차세대 배선 물질로서 구리가 큰 주목을 받고 있다. 하지만 구리의 경우, 높은 확산성을 가지기 때문에 열처리 과정에서 구리 실리사이드($CuSi_x$)가 형성되는 등 소자의 신뢰성 및 성능을 감소시키므로, 이를 방지하기 위한 확산 방지막이 필요하다. 기존의 금속 기반의 확산방지막이 직면한 문제는 소자의 나노스케일화에 따른 배선 선폭의 감소로 인하여 확산방지막 두께 또한 감소되어야 하는 것이다. 확산 방지막의 두께가 감소함에 따른 방지막의 균일성 감소, 연속성 등이 큰 문제로 작용할 수 있어 이를 해결하기 위한 새로운 기술 또는 새로운 확산 방지막 물질의 개발이 시급하다. 자기조립단분자막 (Self-assembled monolayer, SAM)은 유기분자가 자가조립과정을 거쳐 단분자막 형태로 배열되는 물질을 일컫는다. 기존에는 SAM 의 작용기에 따라 표면의 화학적인 특성을 바꾸는데 많이 연구되었으나, SAM 이 조밀하게 코팅되는 것을 이용하여 금속의 산화방지나 구리의 확산방지막으로도 연구가 진행되고 있다. 본 연구에서는 구리 확산방지막으로 많이 연구되고 있는 SAM 의 한 종류인 3-aminopropyltrimethoxysilane (APTMS)에 또 다른 SAM 인 3-mercaptopropionic acid (MPA)을 화학적으로 결합시켜 구리의 확산방지막 특성 및 Cu-SiO_2 사이의 접착 특성을 향상시켰다. 이렇게 만들어진 SAM 층은 2 nm 의 얇은 두께로 낮은 표면거칠기를 가진다.

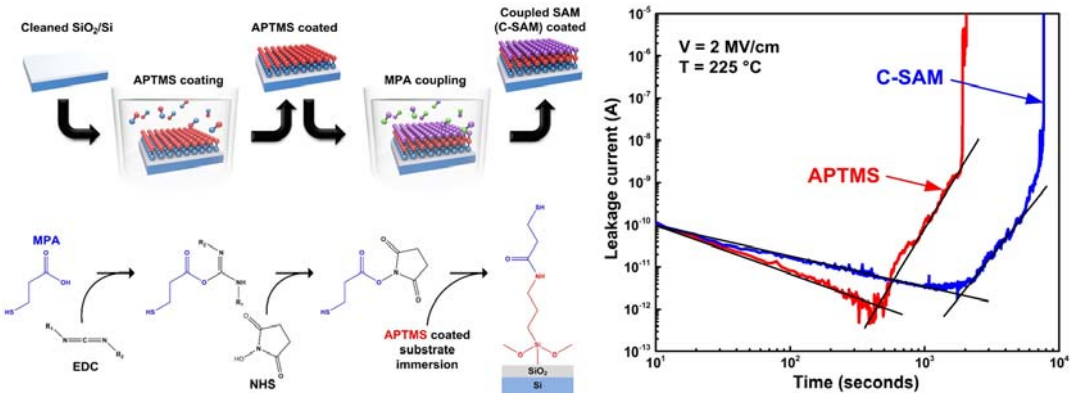

Fig 1. SAM 의 코팅 및 화학처리 과정과 누설전류 분석 그래프

The Capacitor-less LED Lamp using FR-4 PCB

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LED조명에서 High-power LED(고전력 발광소자)의 효율적인 열전달을 위해 COB(Chip on Board)형태의 구조들이 개발 되었으며[1]-[2], 5만시간 이상의 수명시간(life time) 보장할 목적으로 <그림-1>과 같이 Lumens사의 전해 커패시터(capacitor)가 없는 단일칩을 이용한 LED driver와 LED 모듈을 Metal PCB에 구현한 LED조명과 <그림-2>와 같이 하이브리드 방식으로 개별소자를 FR-4 재질의 일반 PCB에 SMT한 LED driver와 LED모듈이 분리된 10W급 LED조명이 최초로 개발되었다. <그림-3>은 소비전력 20W급의 LED조명으로 Metal PCB에 비해 저가격의 FR-4 재질의 PCB로 LED chip과 LED driver회로에 사용되는 N-MOSFET, BJT, Zener diode, Bridge diode, 저항들을 통합하여 SMT(Surface Mount Technology) 방식으로 구현한 것으로 전자소자들에서 발생되는 열은 PCB의 Via-hole을 통해 Heat-sink로 열전달시켰다. <표-1>은 FR-4 PCB로 제작된 LED조명(No 3(20W급), 4(10W급))과 기존의 LED조명과의 특성을 비교한 도표로 Metal PCB에 비해 저가격으로 구현이 가능하며, 전해 capacitor가 없어 장수명을 기대할 수 있고, 0.5[m]거리에서 수직으로 측정한 단위(소모)전력당 조도특성[lux/W]도 기존의 상용 LED 조명(삼성, LG, 포스코)에 비해 PCB 도료가 백색잉크가 아닌 녹색잉크임에도 우수하다는 것을 알 수 있다.

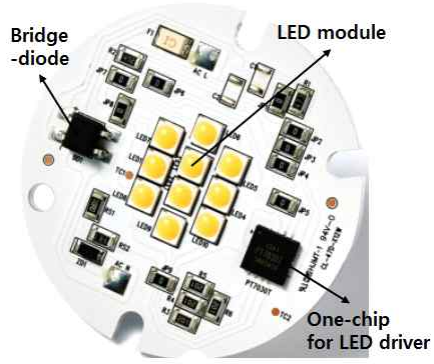

그림 1. L사의 통합 Capacitor-less LED driver와 LED module (소비전력=9.5W)

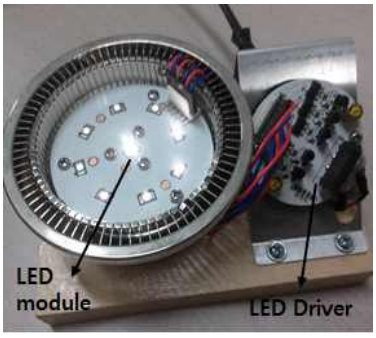

그림 2. 한국산업기술대의 분리된 Capacitor-less LED driver와 LED module(소비전력=10W)

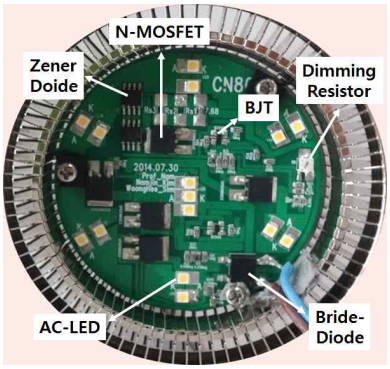

그림 3. 한국산업기술대의 통합된 Capacitor-less LED driver와 LED module(소비전력=20W)

표 1. LED조명 특성 비교표

No	1	2	3	4	5	6	7	8
제품명	EDD47C	VER01	CN80	CN40	VER02	LED 6.5W	6.5W(A19)	LED 9W
제조사	Lumens	KPU	KPU	KPU	KPU	SAMSUNG	LG	포스코 LED
사용된 PCB 종류	Metal	Metal	**FR-4**	**FR-4**	Metal	Metal	Metal	Metal
LED driver/module 집적형태	통합형	분리형	통합형	통합형	분리형	분리형	분리형	통합형
전해 Capacitor 유무	무	무	무	무	무	유	유	무
정격입력전압 [V]	120	220	220	220	220	220	220	220
Electric Power [W]	**9.5**	**8.4**	**23.1**	**11.5**	**18.0**	**6.2**	**6.5**	**8.2**
Efficiency [lm/W]	**101**	-	-	-	-	**85.0**	**76.0**	**85.0**
Power Factor [%]	99.0	96.0	93.3	93.4	90.0	57.9	91.1	95.4
색온도 [K]	4000	5000	5000	5000	4500	5000	5000	5000
Illuminance [lux](@l=0.5[m])	-	924	1860	960	2150	340	539	629
단위전력당조도[lux/W] (@l=0.5[m])	-	110	80	84	119	55	83	77
비고	그림-1	그림-2	그림-3	-	-	-	-	-

[1] Mi-Hee Jee, Choong-Mo Nam, High Power LED Packaging by MOAMP(Multichip On Aluminum Metal Plate) Technology, The 17th Korean Conference on Semiconductors, 106 (2010).
[2] Mi-Hee Jee, Choong-Mo Nam, Multi-chip On Aluminum Metal Plate Technology for High Power LED Packaging. Journal of Measurement Science and Instrumentation, 297-299. (2010).

Analysis of instability mechanism under simultaneous positive gate and drain bias stress in self-aligned top-gate amorphous indium-zinc-oxide thin-film transistors

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Simultaneous positive gate and drain bias stress (SPGDBS) is the most important instability in active-matrix organic light-emitting diode (AMOLED) displays. Under SPGDBS, both the self heating and the charge trapping are important instability mechanisms in amorphous oxide thin-film transistors (TFTs) with low thermal conductivity on glass substrate [1-2]. On the other hand, the self-aligned top-gate is a promising structure for commercializing oxide TFT due to a low RC delay. However, the SPGDBS-induced instability of self-aligned top-gate oxide TFTs has been rarely investigated. In this work, the SPGDBS instability of amorphous indium-zinc-oxide (a-IZO) TFTs were investigated.

After SPGDBS, both the parallel negative shift of transfer curve and the increased drain current were observed. In addition, the magnitude of threshold voltage shift increased with the increase of channel width [Fig. 1(a), (b)]. It was attributed to the combination of the donor creation by the increase of Joule heating effect [1] and the electron-hole pair generation followed by the back channel interface hole trapping [2] [Fig. 1(c)]. Discussed mechanism and the device simulation results are expected to be useful for characterizing a long-term instability of the self-aligned top-gate oxide TFT-driven AMOLED display backplanes.

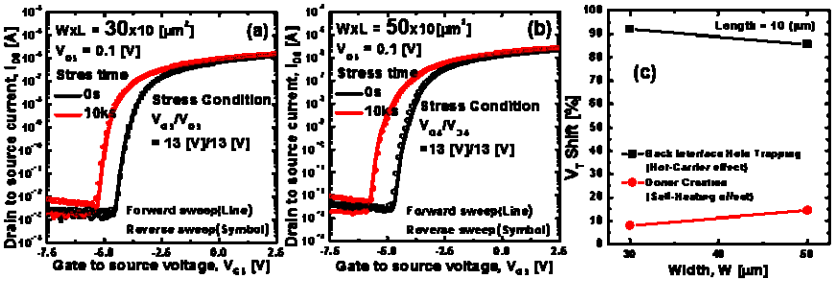

Fig. 1. Transfer characteristics of (a) W=30μm and (b) W=50μm, (c) V_T shift as a function of width in self-aligned top-gate a-IZO TFTs

[1] M. Fujii, *et al*., Jpn. J. Appl. Phys. vol. 48, p. 04C091 (2009)

[2] S. M. Lee, *et al*., Solid-State Electron. vol. 72, pp. 88-92 (2012)

Acknowledgements

This work was supported by BK21+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No. 22A20130000042) and National Research Foundation of Korea through the Ministry of Education, Science and Technology under (Grant No. 2013-013100).

A new ISP function to support gain control at each input code.

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When we tune image, sometimes we feel like applying gain differently at each input code. In this case we usually use gamma correction. But at dark area or saturated area, we cannot apply high gain by using gamma correction. If we have no this restriction, we can easily make HDR(high dynamic range) effect or more bright image according to the input code like Fig 1. In this paper, we propose new ISP block to support this requests. In previous paper[1], it was introduced similiar funcion. But it has performed in sensor not ISP, so it has problems to use it. Especially while we doing AE(auto exposure), previous function makes hunting and very low HDR effect. To avoid this problem, this function must be located after gamma function. Structurally, previous function has only one transformation point. This makes wrong color at that input code. To clear this problem, in this paper, we use many transformation points to change smoothly like Fig.1.

The ISP of this paper can be used with FW. FW can control this function according to the brightness and contrast of image. The strength of HDR should be dependent on the contrast. We can make this function by using FW or tuning table. The strong points of gain controlling type of HDR is faster than the integration time controlling type of HDR[2].

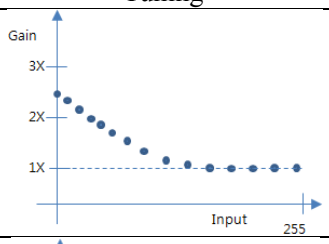
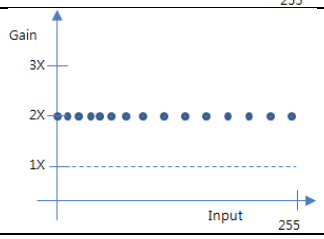
Case	Before	Tuning	After
High contrast			
Low light			

Fig 1. MoS_2 FET device and its electrical data

[1] YH Yun, MS Kim. “A WDR method with low noise in digital circuit. ” ISOCC (2012),
[2] 엄규회, 이상진 임나리, 최병선 ,”Wide Dynamic Range 를 얻기 위한 이미지 촬상 장치의 Integration Time Control 에 관한 연구” 대한전자공학회 하계종합학술대회 (2007) .

Low-temperature all-solution-processed indium oxide thin-film transistors

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Metal-oxide semiconductor thin-film transistors (TFTs) have attracted a lot of interest in recent years for their potential to high-performance, large area, low cost, and flexible electronics due to high mobility, good uniformity, and solution-processability [1]. And solution-process technology has received considerable attention because of its simple fabrication, low cost, and large area compatbility [2]. In this study, we report the effect of Al_2O_3 interlayer on a indium-oxide (In_2O_3)/ poly-4-vinylphenol (PVP) interface and the all-solution-processed In_2O_3 TFTs with maximum process temperature of 250 ^oC. Organic dielectrics are desirable to acheieve low-temperature solution-processed TFTs, because inorganic dielectrics require high annealing temperature. Hence, PVP dielectric layer was used for gate insulators of In_2O_3 TFTs. Fig.1 (a) shows the electrical behavior of In_2O_3 TFTs on PVP coated SiO_2 dielectric. All-solution-processed In_2O_3 TFTs with bottom gate and top contact structure were fabricated on glass substrate as shown in Fig. 1(b). PVP layer was inkjet-printed for the gate insulator and Ag ink was also inkjet-printed for gate, source, drain electrodes. Aquoues In_2O_3 solution was spin-coated on the Al_2O_3 interlayer coated PVP gate insulater. In_2O_3 TFT exhibited the mobility of 2 (max) and 0.633 cm^2/Vs with on/off ratio of $>10^6$ and 10^5 as shown in Fig. 1 (a) and (c). We found that In_2O_3 TFT with Al_2O_3 interlayer between PVP and In_2O_3 exhibited much improved electrical performance compared to TFT without Al_2O_3 layer. It is indicated that Al_2O_3 interlayer suppres hydroxyl groups of PVP surface and enhance the interface property. Details of device performance analysis and the inkjet-printing of the In_2O_3 TFT will be further discussed at conference.

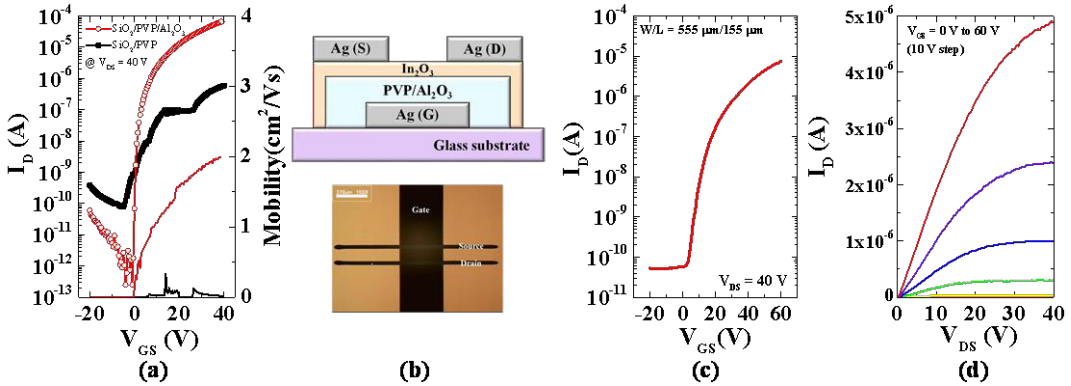

Fig. 1. (a) Effect of Al_2O_3 interlayer on the PVP/In_2O_3 interface (b) Device structure, (c) transfer characteristic, and (d) output characteristic of all-solution-processed In_2O_3 TFTs with Al_2O_3 interlayer

[1] K. Choi, M. Kim, S. Chang, T.-Y. Oh, S. Jeong, H. Ha, and B.-K. Ju, *Jpn. J. Appl. Phys.* **52**, 060204 (2013).

[2] S. Chung, M. Jang, S. -B. Ji, H. Im, N. Seong, J. Ha, S. -K. Kwon, Y. -H. Kim, H. Yang, Y. Hong, *Adv. Mater.* **25**, 4773 (2013).

Comparative analysis on positive bias stress-induced instability under HVGS and HVDS in amorphous InGaZnO thin-film transistors

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Although analysis on positive bias stress (PBS)-induced instability [1, 2] under various operating conditions (i.e., various configurations of V_{GS}/V_{DS}) was one of the important factors for commercializing amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) in active-matrix organic light-emitting-diode (AMOLED) display backplane and investigating their optimum driving scheme, the instability under low V_{GS}/high V_{DS} has been seldom investigated.

Thus, we comparatively investigated not only the high V_{GS}/low V_{DS} (HVGS), but also low V_{GS}/high V_{DS} (HVDS) PBS condition by combining the forward/reverse V_{GS} sweep with a low/high V_{DS} read-out conditions. The main method used in this work was carried out by reproducing the measured electrical characteristics via TCAD device simulation and the result turned out that the electron trapping into the gate insulator (GI) was dominanting in HVGS stress [Fig. 1. (a)-(b)] whereas the local electron trapping into GI near the drain and local hole trapping into etch stopper near the source were dominanting in the HVDS stress [Fig. 1. (c)-(d)]. We beleive that our results would play a useful role in optimizing the driving scheme for a-IGZO TFTs-driven AMOLED.

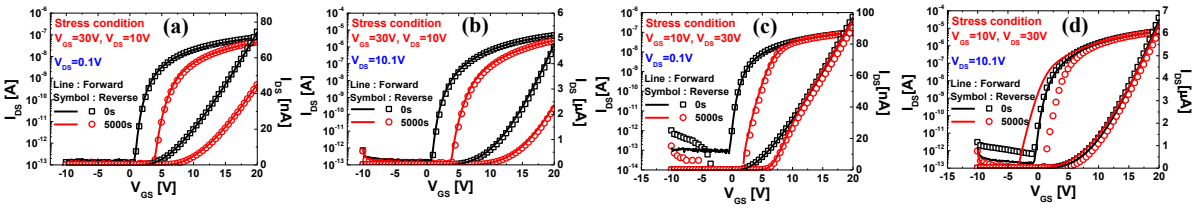

Fig. 1. (a)-(d) Stress time-evolution of transfer characteristics including the forward/reverse V_{GS} sweep and low/high V_{DS} read-out condition under HVGS and HVDS in a-IGZO TFTs

[1] S. M. Lee, *et al.*, *IEEE Trans. Devive Mater, Reliab.*, vol. 14, pp. 471-476 (2014)
[2] C.-Y. Jeong, *et al.*, *Semicond. Sci. and Technol.*, vol. 29, pp. 045023-1 – 045023-6 (2014)

Acknowledgments
This work was supported by BK21+ with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No. 22A20130000042) and National Research Foundation of Korea through the Ministry of Education, Science and Technology under (Grant No. 2013-013100).

Extraction of Distance between Interface Trap and Oxide Trap from Random Telegraph Noise in Gate-Induced Drain Leakage

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RTN in the gate-induced-drain-leakage (GIDL) causes the variable retention time (VRT) phenomenon, which has an influence on the retention characteristics of DRAM cells considerably [1]. In this paper, we accurately extracted the distance r between interface trap and oxide trap by considering the correct field enhancement factor Γ(F). Fig. 1(a) shows the cross section of n-MOSFET device. When the slow trap is filled with electron, the leakage current increases. Fig. 1(b) shows the measured RTN in drain leakage current with increasing V_{DG}. Fig. 1(c) shows the ratio of emission time (τ_e) to capture time (τ_c) as a function of V_{DG}. From the slope of the line, the distance between slow state and Si/SiO_2 interface (x_T) was extracted to be 0.68 nm. In addition, activation energy of TAT current was extracted to 0.54 eV. This value was used to obtain the energy level of fast trap (E_C-E_T) which is equal to 0.45 eV [2]. The distance between two traps is extracted in Fig. 2. In the figure, the red line represents I_{filled}/I_{empty} which is equal to 4.8 from measurement data. The value of r which corresponds to I_{filled}/I_{empty} of 4.8 is 1.31 nm from Eq. 4(a) and 2.16 nm from Eq. 4(b). The two extracted r have an error of 34%. Since F_{empty} is larger than 0.9 MV/cm in this case, the value of 1.31 nm extracted using Eq. 4(b) is more accurate.

Acknowledgement

This work is supported by Samsung Electronics Incorporation and Inter-university Semiconductor Research Center (ISRC).

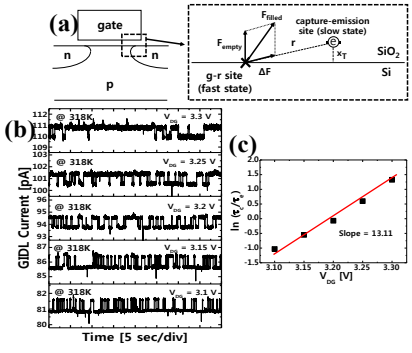

Fig 1. (a) Cross section of n-MOSFET. (b) RTN in GIDL. (c) The ratio of τ_e ,τ_c.

$I = I_{SRH}(1+\Gamma(F))$ $\quad I_{SRH} = qv_{th}\sigma n_i \exp(\frac{(E_t-E_i)}{k_B T})$	Eq. 1
$\Gamma(F)_{Low\_Filed} = 2\sqrt{3\pi}\frac{F}{F_\Gamma}\exp[(\frac{F}{F_\Gamma})^2]$ $\quad F_\Gamma = \frac{\sqrt{24m^*_{n,p}(kT)^3}}{q\hbar}$ (F < 0.9 MV/cm)	Eq. 2 (a)
$\Gamma(F)_{High\_Field} = \frac{1}{2}\frac{\Delta E_{n,p}}{kT}\sqrt{\frac{\pi}{a}}e^{(b^2/a-c)}\mathrm{erfc}(\frac{b}{\sqrt{a}})$ (F > 0.9 MV/cm)	Eq. 2 (b)
$a = 0.375\alpha\frac{1}{F}$, $b = 0.5\beta - 0.75\alpha\frac{1}{F}$, $c = \alpha\frac{1}{F} - \beta$ $\quad \alpha = \frac{4}{3}\frac{\sqrt{2m^*\Delta E_{n,p}^3}}{q\hbar}$ $\beta = \frac{\Delta E_{n,p}}{kT}$	
$(F_{filled})^2 = (F_{empty})^2 + (\Delta F)^2 + 2F_{empty}\Delta F\frac{x_T}{r}$	Eq. 3
$\frac{I_{filled}}{I_{empty}} = \frac{F_{filled}}{F_{empty}}\exp[\frac{F_{filled}^2 - F_{empty}^2}{F_\Gamma}]$ (F_{empty} & F_{filled} < 0.9 MV/cm)	Eq. 4 (a)
$\frac{I_{filled}}{I_{empty}} = \sqrt{\frac{a}{a'}}\frac{(1+3e^{(-b^2/3a)})}{(1+3e^{(-b^2/3a)})}e^{-(c'-c)}$ (F_{empty} & F_{filled} > 0.9 MV/cm)	Eq. 4 (b)

Table 1.

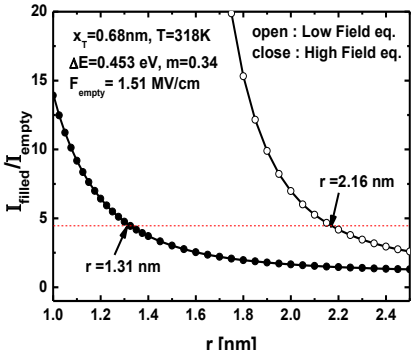

Fig 2. Extraction of distance between two traps

[1] M. Yuki, et al., *IEEE EDM*, 2005 [2] H. Kim, et al., *IEEE TED*, vol. 58, pp.1643-1648, 2011

The Influence of Dummy Pattern on the RF Inductor Characteristics in 90nm CMOS Chip Layout

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For several years, CMOS technologies have provided high density integration and advanced high RF performance on RF device[1]. Dummy layout play an important role to make well-forming RF CMOS device in the CMOS process. In this article, we studied the influence of dummy pattern on the performance of RF inductor device in the 90nm CMOS chip design.

Different type of dummy patterns were adopted under the inductor : All dummy blocking(Type A), ISO dummy only(Type B), ISO&Poly dummy(Type C), ISO&Poly&Metal dummy(Type D). First of all, Increasing of dummy layer had caused the degradation of effective inductance. In addition, we observed that Q-factor shifted to downward increasing insertion of dummy layer. Also, Q_{MAX} and self-resonance frequncy(f_{SR}) were decreased. This degradation of RF inductor performance is caused by increasing mutual inductance and paracitic capacitance with dummy layout.

According this result, the optimized inductor layout design to minimize dummy effect have been proposed.

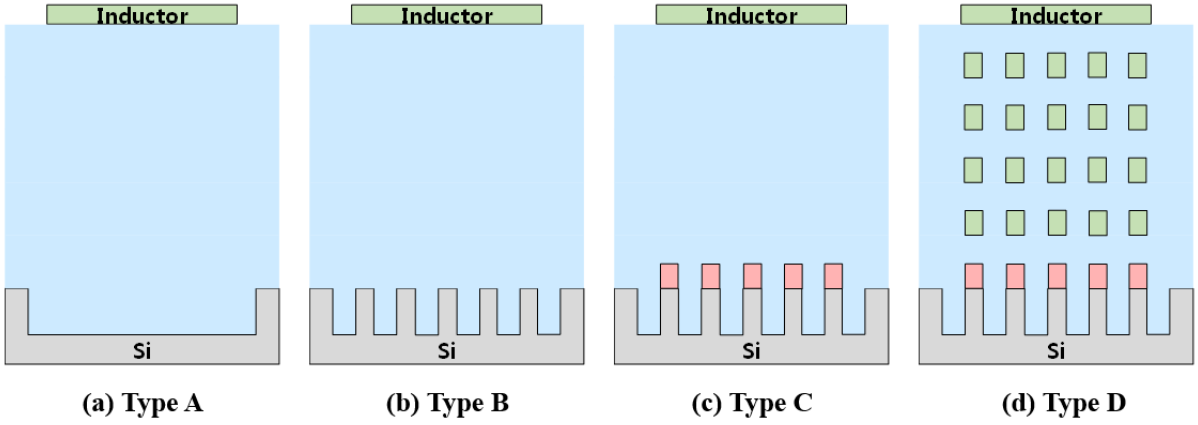

Fig 1. The vertical structure of inductor & dummy layout (a) Type A (all dummy blocking) (b) Type B (ISO dummy only) (c) Type C (ISO&Poly dummy) (d) Type D (ISO&poly&Metal dummy)

[1] H. Sugawara, Y. Yoshihara "Wide-Range RF Variable Inductor on Si CMOS chip with MEMs Actuator", 34th European Microwave Conference pp701-704, (2004)

Cost-Effective Approach using Deep N-type Well Junction in 180nm BCDMOS Technology

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In this paper, we propose 180nm 35V high-side LDNMOS (Lateral Diffused N-type MOSFETs) with optimized Deep N-type Well (DNW) junction in order to achieve low cost BCDMOS technology. High-side LDNMOS fundamentally processes N+ Buried Layer (NBL) implant and grows EPI layer in order to prevent punch-through of parasitic BJT in device [1]. However, In particular PMIC such as Micro USB IC, High-side characteristic is not a major consideration if substrate and device are isolated. Therefore, it is necessary to develop a device having basic high-side characteristic with optimized DNW, instead of NBL and EPI process, to reduce process unit cost. First of all, we set DNW conditions which prevent causing punch-through and enlarging design rules employing TCAD simulation. Then the optimized N-type DrifT layer (NDT) condition in device characteristic is determined by analyzing degree of overlapping STI under gate electrode and NDT concentration. Based on the above results, we obtain BV = 32.4V and $R_{on.sp}$ = 17.4mΩ·mm^2 in 24V operation voltage LDNMOS-HS. Since over 70V BV_{ces} is proved in parasitic BJT of device, we conclude that DNW condition is performed to prevent punch-through (Figure 1). Furthermore, the proposed devices have stable E-SOA (Electrical Safe operating Area) characteristic higher than 1.1 times of operation voltage (Figure 2).

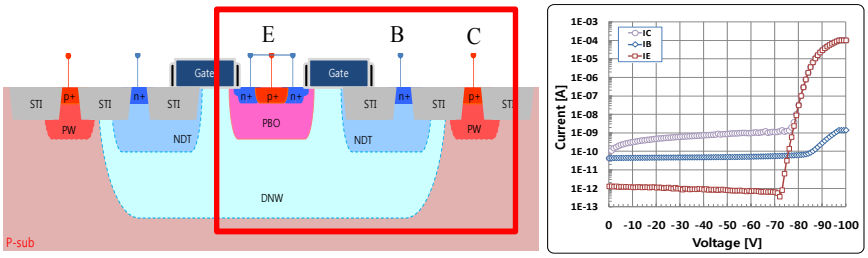

Figure 1. BV_{ces} measured parasitic BJT in the proposed device

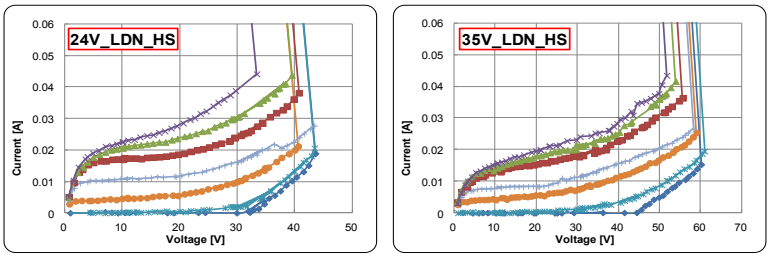

Figure 2. E-SOA characteristic of 24V/35V LDNMOS-HS

[1] Kunsik Sung, “High-side N-channel LDMOS for a High Breakdown Voltage”, JKPS, Vol. 58, No. 5, 2011

Origin of Kink Phenomenon in S_{11}-Parameter of Standard RF MOSFETs

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It has been reported that the kink phenomenon or anomalous dip in S_{11}-parameter occurs with increasing the gate-drain spacer offset [1] and source- body spacing [2] in nonstandard MOSFETs. However, because of degraded RF performance due to the increase of the gate-drain resistance [1] and bulk resistance [2], these nonstandard devices are inapplicable to practical RF IC applications. In this study, for the first time, the kink phenomenon of S_{11}-parameter is observed in 0.18μm standard multi-finger N-MOSFETs with optimized RF performance for the use of practical RF ICs and its physical origin is analyzed in detail. In Fig. 1, the S_{11} for the gate finger number (Nf) of 16 follows a constant r circle with increasing frequency, but the S_{11} for Nf = 64 exhibits the kink phenomenon with a large deviation from the constant r circle. In Fig. 2, the magnitude of S_{11} for Nf=16 is consistently reduced with increasing frequency, but the Mag[S_{11}] of Nf=64 rather increases largely from 2GHz to 6GHz in Fig 2, thus resulting in the kink phenomenon. In Fig 3, RF input resistanc R_{IN} converted from S_{11} of Nf=16 and 64 are decreased by pole and gradually flatted by zero with the frequency, but the decreasing rate of R_{IN} for Nf=64 is even higher than that for Nf=16. This higher rate of Nf=64 inducing the kink phenomenon is generated by the increasing difference between pole and zero frequency of R_{IN} at larger Nf. In Fig 1, the change rate of Mag[S_{11}] with respect to R_{IN} increases with increasing the S_{11} phase at the same frequency. Thus, more noticeable kink phenomenon occurs at larger Nf because the S_{11} phase increases due to higher input capacitance.

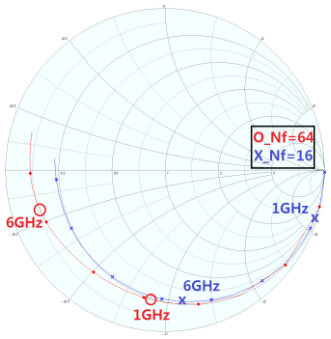

Fig. 1. Smith chart of S_{11}

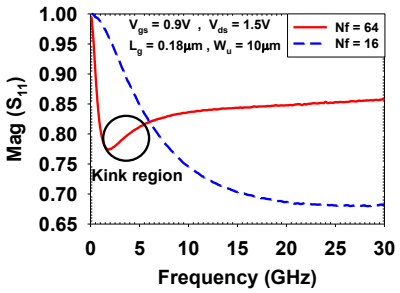

Fig. 2. Mag[S_{11}] vs. frequency

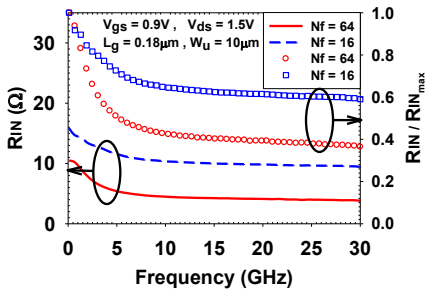

Fig. 3. R_{IN} and R_{IN}/R_{INmax} vs. frequency

[1] Y. Lin and S. Lu, IEEE Trans. Electron Devices, vol. 50, no. 2, pp. 525-528, 2003.
[2] Y. Lin, IEEE Trans. Electron Devices, vol. 52, no. 7, pp. 1442-1451, 2005.

A Characteristic Method of Extracting Intrinsic Threshold Voltage Fluctuation from Depletion Charge Variation

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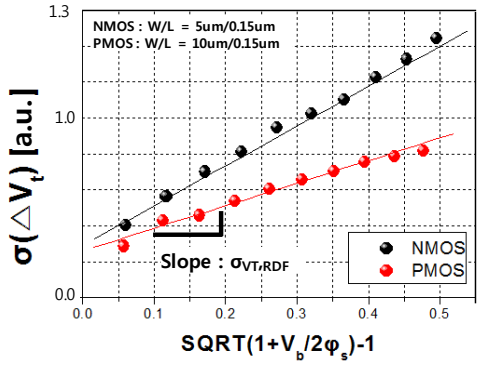
In order to have reliable operation in large scale integrated circuit, it is necessary to reduce the fluctuation of threshold voltage in field effect transistor. To reduce V_T fluctuation, above all, we have to analyze it into all constituent components. Among them are wafer level variation caused by process non-uniformity, random dopant fluctuation(RDF), oxide interface states (Nit), and so on. The RDF is regarded as a major source of V_T fluctuation and the degree to which RDF influences on the flucuation of scaled field effect transistor is getting worse [1]. In this study, we breaks down V_T fluctuation into component by component via the evaluation of back-bias effect in single device. As the body bias increases in absolute value, the standard deviation of V_T difference between body-biased and reference device also increases. From this analysis, we can extract the componet of RDF. Additionally, it is possible to obtain Nit-related factor among V_T fluctuation in V_T mismatch configuration.



$$V_T = V_{FB} + 2\varphi_S + \frac{\sqrt{2\varepsilon_{si} q N_a (2\varphi_S)}}{C_{OX}} - \frac{qD_{it}}{C_{OX}}$$

$$\Delta V_T = V_{T@Vb=Vbs} - V_{T@Vb=0V} = \frac{\sqrt{2\varepsilon_{si} q N_a (2\varphi_S + |V_{bs}|)}}{C_{OX}} - \frac{\sqrt{2\varepsilon_{si} q N_a (2\varphi_S)}}{C_{OX}}$$

$$STD[\Delta V_T] = STD\left[\frac{\sqrt{2\varepsilon_{si} q N_a (2\varphi_S)}}{C_{OX}}\left(\sqrt{1+\frac{|V_{bs}|}{2\varphi_S}} - 1\right)\right]$$

$$\cong \sigma_{V_T,RDF} \cdot \left(\sqrt{1+\frac{|V_{bs}|}{2\varphi_S}} - 1\right)$$

Fig 1. Standard deviation of V_T difference from obtaining back-bias effect (left side) and related equation(right side). The slope means V_T fluctuation caused by channel random dopants.

[1] K. Takeuchi , A. Nishida and T. Hiramoto, Proc. SISPAD, 79-85 (2009).

Design of Robust High-Voltage MOSFETs for Source Driver Applications

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Robust and competitive high-voltage MOSFETs have been designed for modern source drivers and decoders of monitors, navigation, etc. The high-voltage NMOSFETs (operating voltages V_G=V_D=13.5V) meet all the targets of threshold voltage (V_T), drain saturation current (I_{Dsat}), off-state breakdown voltage (BVDSS) and hot-carrier injection immunity ($\Delta V_T \leq 3\%$). TCAD simulation was essentially used for designing the MOSFETs and providing physical insights into the device. Althouth the high-voltage well anneal is effective in improving the hot-carrier injection immunity, the dimension of the diffused-well HV NMOSFET is no longer larger than retrograde-well [1] HV MOSFETs. The 2nd peak of a substrate current vs. gate voltage characteristic of the HV NMOSFETs can effect the channel or substrate hot-carrier injection immunity negatively. A methodology to remove the 2nd peak is proposed and its effectiveness is explained by TCAD. TCAD statstical process conrol (SPC) techniques are used to efficiently produce sensitivity analysis charts and to construct a viable design space [2] in which robust devices are located. From the TCAD results, we can recognize promptly devices vulnerable to process and critical dimension variations.

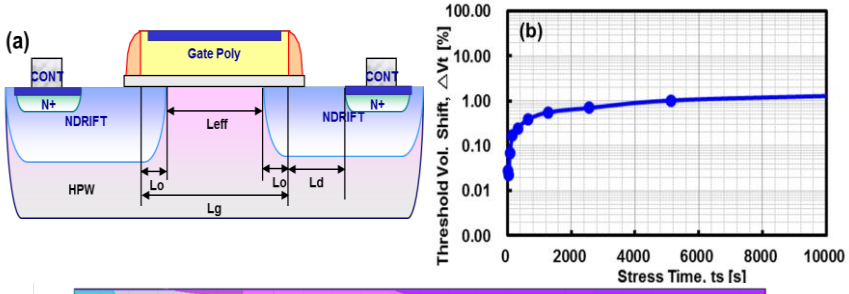

Fig. 1. (a) Cross-sectional view of V_G=V_D=13.5 V high-voltage NMOSFET and (b) ΔV_T vs. stress time at V_G = V_D = 13.5 V, V_S=6.75V and T = 125°C of substrate HCI characteristic of HV NMOS

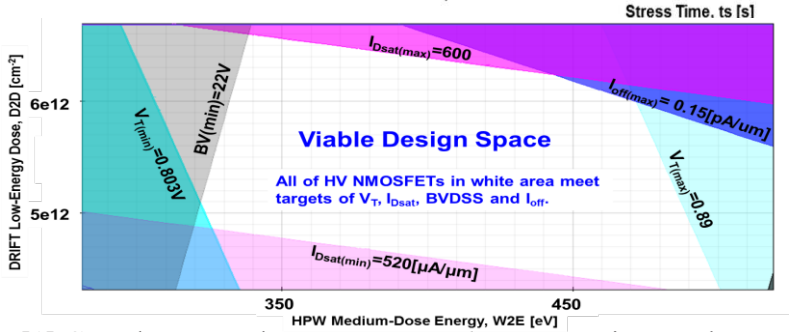

Fig. 2. Robust HV NMOSFETs are located at the center of the viable design space and meet all of the device design targets.

[1] C. Bulucea, et al., IEEE Trans. Electron Devices, Vol. 57, No. 10, (2010), p.2363–2380.
[2] Y.-S. Pang, et al., Solid-State Electronics, Vol. 46, No. 12, (2002), p.2315–2322.

Device characterizations on the performance and stabilities of InGaZnO thin film transistors fabricated on flexible polyethylene naphthalate

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[2] *Electronics & Telecommunication Research Institute. Daejeon, 305-730, Korea*

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Recently, there have been enormous studies on the fabrication of oxide thin-film transistors (TFTs) on the flexible substrates for flat-panel displays. The polyimide has been mainly employed as a flexible substrate due to its high-temperature compatibility. However, from the viewpoint of lower fabrication cost, the use of an alternative flexible substrate such as polyethylene naphthalate (PEN) would be preferred. In order to guarantee the performances of the oxide TFTs fabricated on PEN, the optimization of the buffer layer stucture is very important for reducing the surface roughness and moisture permeability. Therefore, the main object of this work was to investigate on the suitable configuration of buffer layer for the PEN to fabricate the InGaZnO TFTs, in which organic and inorganic thin films were prepared with varing the process conditions. For the optimized device, the field-effect mobility, subthreshold swing, and on/off ratio were estimated to be 13.5 $cm^2V^{-1}s^{-1}$, 0.16 V/dec, and 1.2×10^9, respectively, even when the device was bent with various curvature radius (2.4 cm ~ 9.1 cm), as shown in Fig. 1(a). The negative and positive-bias stress stabilities were examined, in which V_{GS} of -20 V or +20 V was continuously applied for 10,000 s, as shown in Figs. 1(b) and (c), respectively. The IGZO TFTs fabricated on the PEN exhibited excellent device characteristics including bias stability and bending performance thanks to the optimized buffer layer structure. At presentation, the detailed effects of organic and inorganic buffer layers and other process conditions on the flexible device behaviors will be fully discussed.

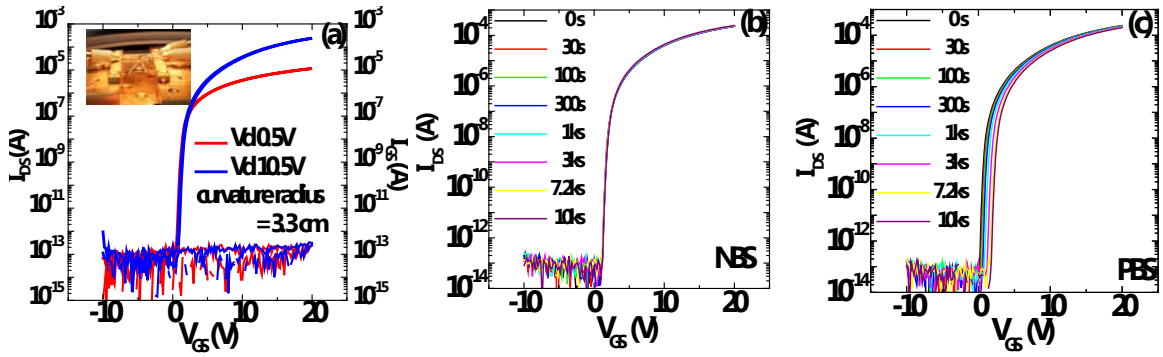

Fig. 1 (a) Transfer characteristics and gate leakage currents of a-IGZO TFT when the curvature radius was 3.3 cm. The variations in transfer curves of the a-IGZO TFT under the (b) negative and (c) positive bias-stress conditions.

Fully-Transparent Nonvolatile Memory Thin-Film Transistors Using Organic/Inorganic Hybrid Gate-Stack with Double-Gate Configuration

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Nonvolatile memory thin-film transistors (M-TFTs) have actively been researched as one of the most important device elements for realizing large-area next-generation consumer electronics, with which such functions as a power saving as well as an information storage can effectively be accomplished [1]. Optical transparency to the visible range can also be an important benefit in this technology field. In this work, we proposed and fabricated the transparent M-TFTs with double-gate (DG) structure, in which an InGaZnO and an In-Sn-O were employed as channel and electrodes, respectively, as shown in Figs. 1(a) and 1(b). Top-gate (TG) and bottom-gate (BG) insulators were formed with poly(vinylidene fluoride-trifluoroethylene) and Al_2O_3 thin films, respectively. BG and TG devices in DG configuration exhibited sound electrical characteristics. The DG configuration provides us a higher degree of freedom in designing the operation schemes because of an additionally prepared gate terminal. The transfer characteristics including the memory windows could be modulated when the fixed biases applied to BG were varied, as shown in Fig. 1(c) [2]. As transparent devices, illumination-bias instabilities affecting on the memory behaviors will be extensively evaluated and the related feasible mechanisms will be discussed.

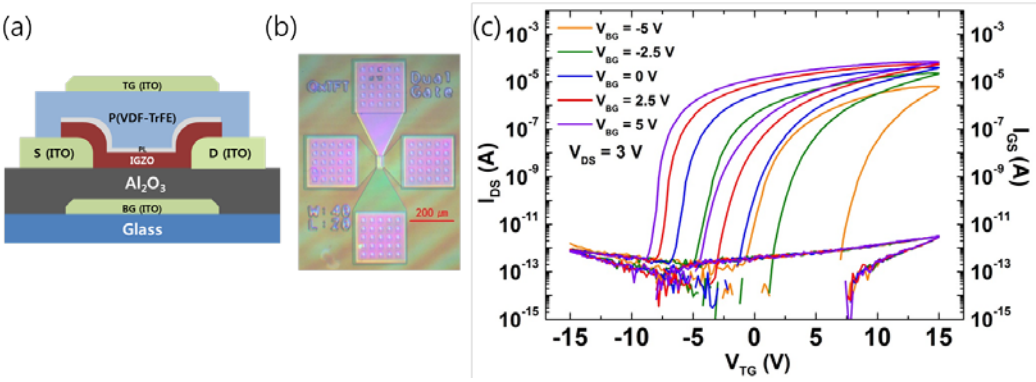

Fig. 1. (a) Schematic cross-sectional view and (b) microscopic image of the fabricated DG M-TFT. (c) Variations in transfer characteristics of the DG M-TFTs at various fixed BG biases.

[1] S.-M. Yoon et al, Semicond. Sci. Technol., 26, 034007 (2011).
[2] K. Abe et al, IEEE Trans. Electron Devices, 49, 1928-1935 (2012).

Nonvolatile Memory Performances of Transparent Memory Thin-Film Transistors Using IGZO Channel and ZnO Charge-Trap Layers

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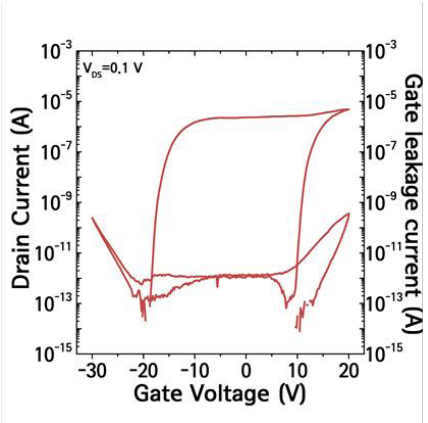
High-performance transparent electronics have emerged as one of the most promising applications for new paradigm in electronics industry. In order to realize these systems, nonvolatile memory device would be highly required for saving the power consumptions as well as for storing the information. In this work, we proposed oxide-based transparent charge-trap memory transistors (CTMs) for the first time. We fabricated fully transparent CTMs in glass substrate, as shown in Fig. 1, in which the gate-stack was uniquely designed to be ITO gate/block oxide Al_2O_3/charge-trap ZnO/tunneling oxide Al_2O_3/In-Ga-Zn-O channel/ITO source-drain. Fig. 2 demonstrated that the memory window in the transfer characteristics was successfully obtained as wide as 28.2 V at the sweep of gate voltage from -30 to 20 V, which was contributed by the charge trap/detrap process. It was also very impressive to note that the memory on/off ratio of higher than 3-orders-of-magnitude even with 500-ns-wide programming pulse, as shown in Fig. 3. It was concluded from these obtained results that the fabricated transparent nonvolatile memory TFTs would be significantly promising for the next-generation transparent electronics. The light-illumination stability of the memory behaviors will be investigated as future works and be fully discussed at presentation.



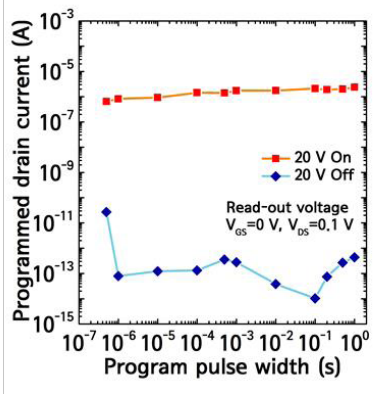


Fig. 1. Photo image of the fabricated transparent charge-trap-type nonvolatile memory TFT.

Fig. 2. I_{DS}-V_{GS} transfer characteristics of the fabricated CTM device.

Fig. 3. Variations in memory on/off ratio as a function of program pulse width.

Growth of MoS_2 Thin Films by Atomic layer deposition

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[1)] *KU-KIST Graduate school of Converging Science and Technology*

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대표적인 이차원 물질 중 MoS_2는 그래핀과 달리 밴드 갭이 존재하고, 전자이동도가 매우 높아 트랜지스터, LED, 반도체 센서 같은 소자들에 적용하기가 용이하여 최근 많은 관심을 받고 있다. MoS_2의 소자 응용을 위해서는 대면적에서의 균일한 증착과 박막의 두께 조절 등이 필수적이다. 그러나 기존의 MoS_2 연구에서 주로 이용되는 물리적인 전사 방법과 화학기상증착법을 이용한 증착 방법들은 박막의 두께, 결정립 크기 등을 정밀하게 조절하기 어려우며, 대면적 균일성을 확보하기 어렵다는 단점을 갖고 있다. 그에 비해 Atomic Layer Deposition(ALD) 방법은 표면 반응을 이용하여 원자 층 단위로 박막을 성장시키기 때문에 박막의 두께 조절이 용이하고 대면적에서 균일한 두께의 박막도 얻을 수 있다는 장점을 갖고 있다. 따라서 우리는 ALD 방법을 이용하여 MoS_2 박막을 Si, SiO_2 기판 위에 증착하였다. 반응 원료로는 $Mo(CO)_6$ 와 H_2S 를 이용하였고, 전구체들의 공급 시간과 유량, 증착 온도, cycle 수 등을 바꾸어가며 실험하였다. 전구체들의 self-limiting 거동을 확인하였으며, 이를 통해 MoS_2 의 박막이 대면적으로 균일하게 증착 가능함을 보여주었다. 타원계측법을 통해 측정한 밴드 갭은 약 1.3 eV 으로 bulk MoS_2 와 유사함을 확인하였다. AES, XPS 등의 분석 방법들을 통하여 증 Mo 와 S 의 구성 성분비 등을 분석하였다.

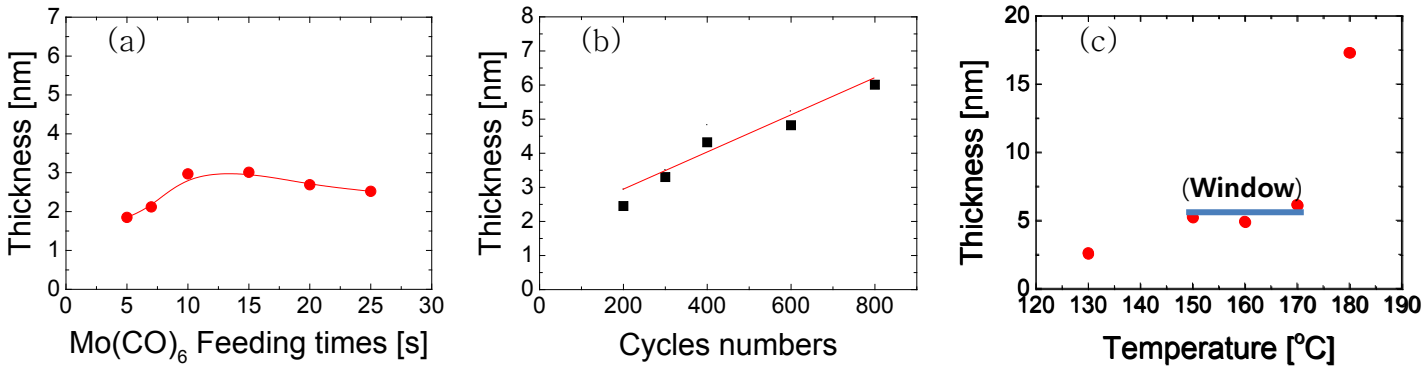

Fig 1. Variation in the thickness of MoS2 films as a function of (a) Mo(CO)6 feeding time, (b) number of ALD cycles, and (c) growth temperature, respectively.

Synthesis of Wafer-Scale Layer Controlled Molybdenum Disulfide using Atomic Layer Deposition

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The synthesis of atomically thin molybdenum disulfides (MoS_2) with layer controllability and wafer-scale uniformity is an essential for their application in electronic and optical devices. In this regards, several studies have been reported to prepare atomically thin MoS_2 nanosheets, including exfoliation, sulfurization of Mo and MoO_3 thin films and chemical vapor deposition (CVD) using MoO_3 and S powder. However, these methods have insufficient uniformity in large area and lack in layer controllability. Therefore, an improved synthesis process for atomically thin MoS_2 nanosheets with exact number of layers controllability and large area uniformity is required.

In this work, we describe a process for the synthesis of MoS_2 nanosheets using atomic layer deposition (ALD). ALD MoS_2 nanosheets show wafer scale area (1.5x9 cm^2) uniformity (up to 95%) and layer controllability from mono- to tri-layer. The X-ray photoemission spectroscopy, Raman, photoluminescence and transmission electron microscopy measurements exhibit that the ALD MoS_2 nanosheets have good stoichiometry, clear Raman shift and bandgap dependence as a function of the layer numbers, and honeycomb-like structure. The electrical properties of the monolayer ALD MoS_2 nanosheet are measured using a field-effect transistor (FET) with a bottom SiO_2 gate insulator. The electron mobility and on/off current ratio of monolayer ALD MoS_2 are comparable to that of CVD grown MoS_2.

MoS_2 전계효과 트랜지스터의 컨택 저항 개선 방법

박우진, 김용훈, 이상경, 정욱진, 양진호, 조천흠, 김윤지, 임성관, 이병훈*
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최근 실리콘을 대체할 2 차원 구조의 반도체 물질에 대한 연구가 활발히 진행되어 왔다. 그 중 높은 전하 이동도를 가진 그래핀에 대한 연구가 진행되어왔지만, 밴드갭이 없어 전계효과 트랜지스터로 활용하기 어렵다는 단점이 있다. 반면에 2 차원 전이 금속 반도체의 한 종류인 MoS_2 는 다층과 단층 구조에서 각각 1.3 eV 와 1.8 eV 의 밴드갭을 가지기 때문에, 차세대 전자 소자에 적용 가능할 것으로 기대되고 있다, [1]. 그러나 MoS_2 전계효과 트랜지스터를 실제로 활용하기 위해서 해결해야 할 몇 가지 문제가 있는데, 그 중 하나가 높은 컨택 저항이다 [2].

이 연구에서는 컨택 전극과 반도체 사이에 얇은 절연체 층를 삽입하여, Fermi level pinning 문제를 감소시킴으로써, 컨택 부분의 Schottky barrier height 를 줄여 컨택 저항을 줄이는 방법에 대한 실험을 진행했다. 절연체층 삽입결과, 전류는 2.51 μA/μm 까지 증가했고, 컨택 저항은 5.4 kΩ· μm 까지 감소했으며, 이 결과는 절연체를 사용하지 않은 MoS_2 전계효과 트랜지스터의 성능대비 2~5 배까지 개선된 결과이다. 이 방법을 이용하면, 고성능 MoS_2 전계효과 트랜지스터를 구현하는 데, 큰 도움이 될 것으로 기대된다.

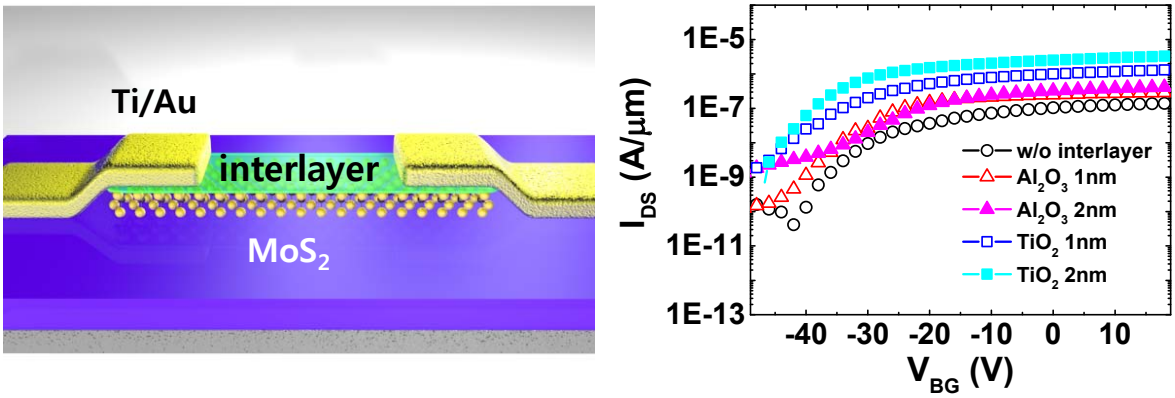

Figure 1 Schematic of MoS2 FET and electrical data

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Nonvolatile Memory Application of Tunneling Field-Effect Transistors

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Recently, non-volatile memory (NVM) application is developing toward low-voltage and low-power operation. Also, tunneling field-effect transistor (TFET), promising device to achieve extremely low off leakage and low sub-threshold slope (*SS*) [1], has been adapted for NVMs to reduce standby power [2]. However, these applications meet sensing voltage scaling limit due to large sub-threshold slope (*SS*) because the dielectric layer must be thick to operate as a NVM. Also, many researches have focused on adapting asymmetric-gate structures on TFETs to achieve lower *SS* [3], [4]. Dual gate work-function operation principles are feasible to TFET-based NVM for extremely low *SS* since locally trapped charge can control the asymmetric-gate effect.

In this study, we proposed noble NVM structure with localized charge trapping layer as shown in Fig. 1. This leads to *SS* and onset voltage (V_{onset}) deviation of charged cell from fresh cell. Charged cell shows steep on/off transition with *SS* = 40.3 mV/decade when trapped hole concentration is 10^{20} cm^{-3}. Hence, 10 order of sensing current ratio between positively and negatively charged cell is achieved at V_G = 0.59 V. The result suggests breakthrough of limits of MOSFET-based NVMs. This simulation work will be helpful for understanding sub-threshold behavior of TFET-based NVM applications.

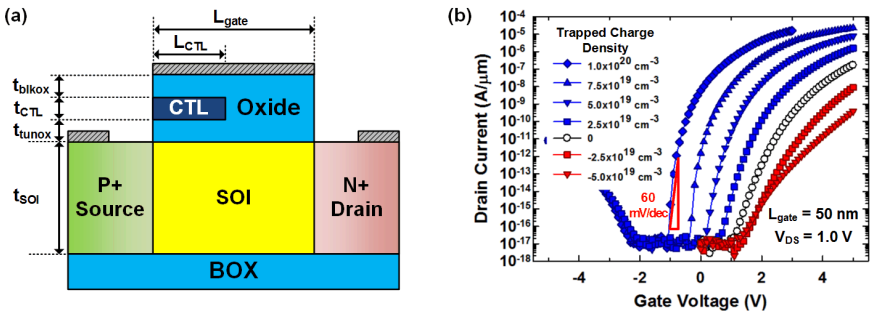

Fig 1. (a) Structure of TFET-based NVM and (b) transfer characteristic

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New Efficient Error Control Technique for 3D-Integrated SRAM

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3D integration of transistors has been a growing technology to enlarge the capacity of integrated circuits. In a perspective of reliability, highly integrated memory devices should confront the temporal bit-flip errors called as soft errors. Using bit partitioned 3D SRAM design [1], we proposed new efficient error detection and correction structure to reduce size of parity bits by applying two-dimensional *N*-way interleaving technique in bit-partitioned 3D SRAM. The 2D *N*-way interleaving scheme [2] can reduce the significant size of parity bits. However, it is hard to directly apply this technique into a planar SRAM design without a significant overheads of additional interconnection networks and logic circuits.

In this paper, we propose an efficient 2D bit-interleaving technique for 3D SRAM devices. Multiple data words are stored in an interleaved fashion along a single physical row of across all stacked dies. Proposed method uses only 1/*K* parity bits, compared with conventional bit-interleaving. Corresponding spatial error coverage is *K* times larger than the conventional bit-interleaving. According to simulation result, the difference between conventional and proposed detection probability is only 0.024% (when N=K=4).

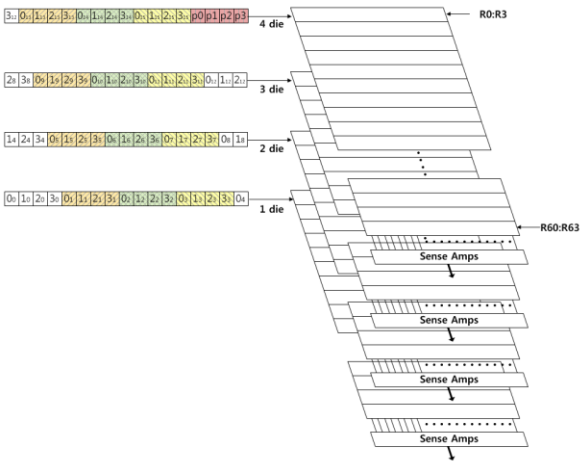

Fig. 1. 3D Bit-Partitioned SRAM with proposed method

EDC scheme (where N=K)	Parity bits (bit)	Detection probability (%)
Conventional 4-way interleaving	65,536	99.791
Proposed 4-way interleaving	16,384	99.767
Conventional 8-way interleaving	262,144	99.771
Proposed 8-way interleaving	32,768	99.735
Conventional 16-way interleaving	1,048,576	99.819
Proposed 16-way interleaving	65,536	99.786

Table 1. Simulation result (256KB)

[1] K. Puttaswamy and G.H. Loh, IEEE Trans. on Computers, 58, 10 (2009): 1369-1381.
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Modeling Statistics of Data Retention in PC-RAM by Phase-Field Method

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PC-RAM is the only memory whose full functionality has proven for a 7.5nm cell [1]. It is the closest to volume production among emerging memories. Hence, investigating the scalability in the reliability point of view is timely. The data retention of the PC-RAM is governed by crystallization kinetics. The Johnson-Mehl-Avrami-Kolmogorov (JMAK) equation describes crystallized fraction as a function of time, assuming constant nucleation and growth (NG) parameters and infinite sample size [2]. However, both assumptions are false for current nanoscale cells. Moreover, the JMAK equation is deterministic, implying no statistical variation, which is false in reality as well. We adopted phase-field method (PFM) with Poisson seeding to model NG correctly. Our PFM was calibrated to the Samsung's 58nm chip data. Then, many simulation runs for different cell sizes and temperatures were performed. Distributions of retention times are lognormal, and upon decreasing cell size the median increases while the spread becomes wider [3]. Recently, we found a general rule for the median and the spread as a function of cell size and material properties. Finally, we suggest a direction of material engineering to optimize the retention statistics.

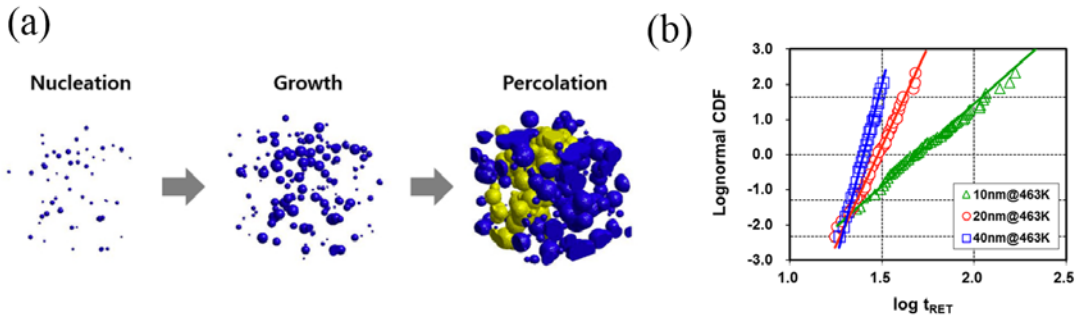

Fig. 1. (a) Modeling of NG by PFM (b) Lognormal distribution of data retention times

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Phase Change Analysis of $Ge_2Sb_2Te_5$ Nanowires with Joule Heating WN Electrodes

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We analyze a switching mechanism of nanoscale phase change memory (PCM) devices with Joule heating electrodes. Single crystal phase change nanowire (NW) structures are used as the PCM device geometry [1]. $Ge_2Sb_2Te_5$ (GST) nanowires are grown by using a vapor-liquid-solid (VLS) method in a chemical vapor deposition system [2]. W-rich WN electrodes are formed with varying concentration of nitrogen [3] on a dispersed PCM nanowire. WN electrodes are sub-micro patterned using a maskless lithography and a focused ion beam (FIB). Current-voltage characteristics and corresponding resistances at set and reset states are measured using a PRAM characterization system in a pulse-mode probe station. Contact resistance is determined as a function of nitrogen concentration of Joule heating electrodes and the gap between electrodes. In the case of W-rich electrode and narrow NW, resistance ratio between set and reset state is maximized to ~600. The amorphous or crystalline regions from the phase change are analyzed. This result indicates that the joule heat from contact region can change the phase of GST nanostructures and nitrogen content in the electrode is a main factor for switching behavior. The result can be applied to improve understanding of nanoscale PCM devices with joule heating electrode.

This research was supported by the National Research Project for Next Generation MLC PRAM Development by the Ministry of Knowledge Economy (MKE) of Korea.

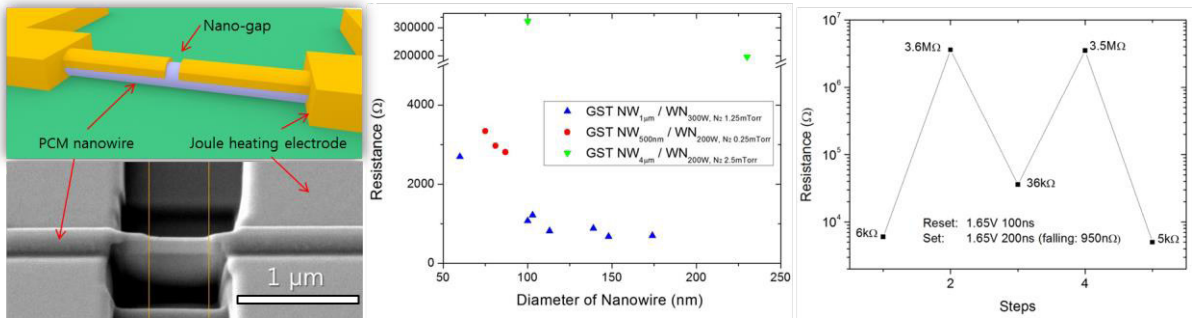

Fig 1. Schematic and SEM images of a nano-PCM device and its electrical characteristics.

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Bipolar resistive switching of amorphous $Ge_2Sb_2Te_5$ thin film without involving phase change

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Among the chalcogenide materials, alloys and compounds of Ge, Sb and Te are one of the major materials for phase change memory (PCRAM.) The applications such as a non-volatile memory depend on the electrical resistivity difference between crystalline and amorphous phase. This phase change effect and consequent resistivity change by polarity-independent electric pulse require high current density, which leads to high power consumption issue that has been an obstacle for commercialization of PCRAM. In this study, polarity-dependent resistive switching in amorphous $Ge_2Sb_2Te_5$ (GST) thin film was examined, which does not involve any phase change and thus can overcome such demerits of conventional PCRAM.

The crossbar type devices with Ti/GST/Pt and Pt/GST/Pt stack with various active area (from 16 to 100 μm^2) were fabricated. Two different type electrode materials (Ti, Pt), which are known to be electrochemically inert, were chosen to make sure that the RS effect in these memory cells is not related with the electrochemical metallization (ECM) effect. Typical bipolar resistive switching with $R_{HRS}/R_{LRS} \sim 100$ was observed. Stable reliability characteristics (endurance > 100 cycles and 10 years of data retention at 85°C) were also verified. The electrode area dependence of LRS current showed that the current path is localized, which implies the filamentary nature of switching. High resolution transmission electron microscopy revealed the presence of the conducting filament, composed of crystalline tellurium, surrounded by amorphous GST. The conduction mechanism analysis confirmed the HRTEM results. The polarity-dependent resistive switching behavior thus can be attributed to the formation and rupture of Te conductive bridge in the amorphous GST matrix by migration of Te anion under high electric field.

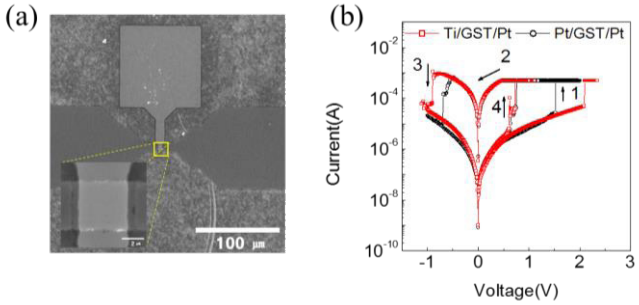

Figure 1. (a) SEM image of the crossbar structure device and (b) current-voltage characteristics for Ti/GST/Pt and Pt/GST/Pt.

Zigzag Multi-Bit Nano-Electromechanical Memory Cells

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Recently, the demand for high speed, low power consumption and high density of nonvolatile memory is increased due to the growing of portable device market. In order to fill the demand, the nano-electromechanical (NEM) memory cells which have high program/erase speed, low operation voltage, large sensing margin are researched as a replacement of flash memory that has scaling limits [1]. Also, the multi-bit NEM memory cells which enable multi-bit storage per bit such as T cell are researched for high density [2]. However, as the multiple bits share a same bit line (BL), the bit-to-bit interference (BI) where the operation voltage of one bit is increased when the other bit sharing BL is erased is occurred. The BI should be suppressed because it causes data disturbance.

In this study, the zigzag T cell structure is proposed to alleviate the BI without cell area increase. Fig. 1 (a) shows the variation of zigzag T cell structure. While structure 1 has overlapped area ($W_{overlap}$), structure 2 has perfectly split bits and zigzag patterned assist word line (AWL) for preventing the cell area increase due to increase of width of AWL (W_{AWL}). Structure 3 is the same as the structure 2 except that a distance between neighboring cells is removed for the cell area reduction. Fig. 1 (b) shows the BI of each structure by using pull-in voltage variation ($\Delta V_{pull\text{-}in}$). The $\Delta V_{pull\text{-}in}$ decrease while $W_{overlap}$ decrease bacause the degree of raised victim cell due to erased aggressor bit is reduced. Structure 2 is most immune to the BI and the BI effect of structure 3 is larger than structure 2 because the aggressor bit of neighboring cell affects victim bit.

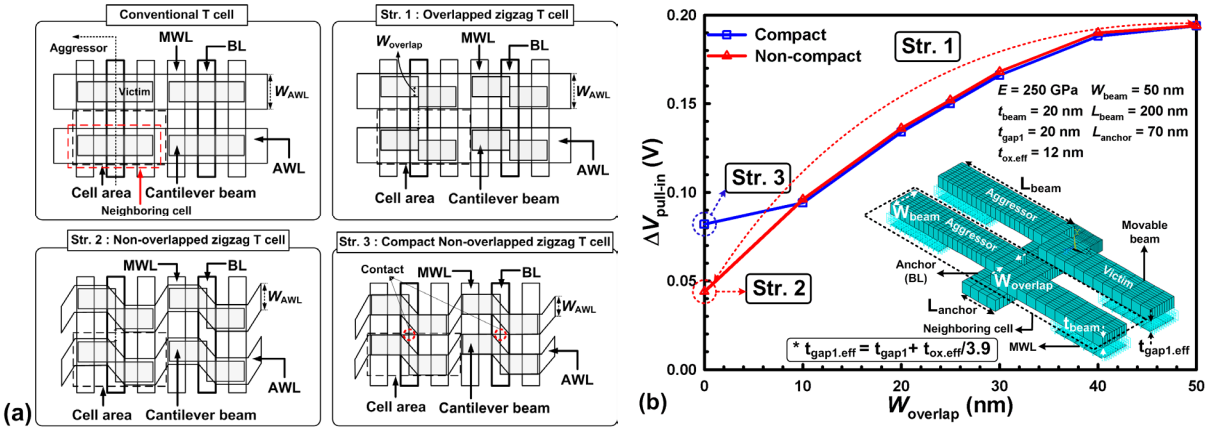

Fig. 1. (a) Schematics of conventional and zigzag T cell structures. (b) BI of each structure.

Acknowledgments: This work was supported in part by the NRF of Korea funded by the MSIP under Grant NRF-2012R1A2A2A01006159 (Mid-Career Researcher Program), in part by the NIPA funded by the MSIP under Grant 1711014140 (Information Technology Research Center), in part by the KEIT funded by the MOTIE under Grant 10039174 (IT R&D Program) and in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program).

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Effect of Double Patterning on Performance Variation Induced by Gate Line-Edge-Roughness (LER) in Germanium FinFET

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193-nm immersion lithography with single patterning and resolution enhnacment techniques was faced with its resolution limit to satisfy the minimal pitch requirements for sub-32/28-nm CMOS technology nodes. To address the technical challenge, multiple patterning technique such as double-patterning and double-etching (2P2E) is currently being adopted in 22-/20-nm CMOS technology and below. In this work, the effect of 2P2E technique [*versus* single-patterning and single-etching (1P1E) technique] on gate line-edge-roughness (LER)-induced performance variation in Germanium (Ge) FinFET device with or without metal-insulation layer on source/drain regions is investigated: It is concluded that the 2P2E technique (*versus* the 1P1E technique) can better suppress the gate LER-induced performance variations by ~ 10% [*i.e.,* threshold voltage, sub-threshold slope (SS), I_{OFF}, I_{ON} and R_{ON}] in Ge FinFET with or without metal-interfacial layer (IL) on source/drain (S/D) regions. This study will help to understand the LER-induced random variation in Ge FinFET when double patterning technique and Metal-IL-Semiconductor (MIS) structure on S/D contacts are used together.

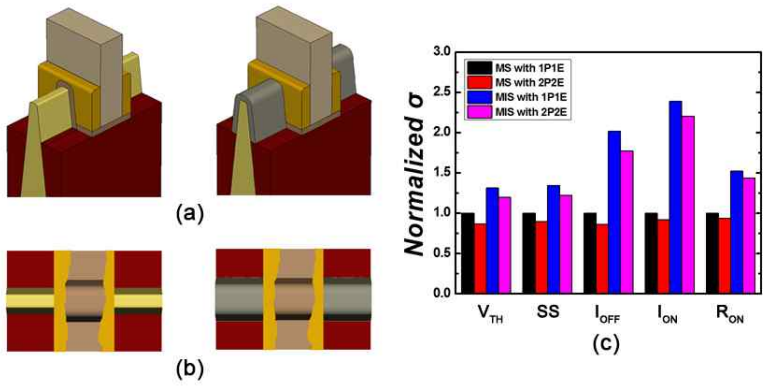

Fig. 1. (a) Isometric views of Ge FinFETs without IL on S/D (left) or with IL on S/D (right), **(b)** plan views with 2P2E-induced LER in Ge FinFETs without IL on S/D (left) or with IL on S/D (right), **(c)** LER-induced performance variation of MS or MIS S/D structure in Ge FinFETs with 1P1E or 2P2E technique. **M(I)S** refers to **M**etal-(**I**nterfacial layer)-**S**emiconductor on S/D regions.

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637)

Heterojunction Symmetric Tunnel Field-Effect Transistor (S-TFET)

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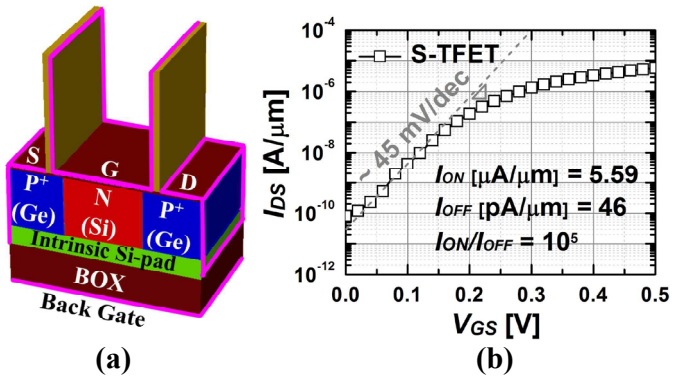
Ever-increasing power density has become one of the most significant barriers for scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs). In an effort to lower the power consumption, the tunnel field-effect transistors (TFETs) have been proposed as one of the promising alternatives to MOSFETs, since the generation of conduction carriers via band-to-band tunneling process can overcome the physical limit of the subthreshold slope (SS) (*i.e.*, SS steeper than 60 mV/decade at room temperature) [1-3]. However, a conventional TFET is a gated p-i-n diode that operates in reverse-bias mode, so that the current can only flow in one way. In this work, a novel heterojunction symmetric tunnel field-effect transistor (S-TFET) has been suggested and investigated in order to address the inborn technical challenges of the conventional p-i-n TFET. The bidirectional current flow in the S-TFET is implemented with a p-n-p structure, and better performance in the S-TFET is achieved with a thin silicon-pad layer below the source/drain regions.



(a) **(b)**

Fig. 1. (a) Three-dimensional (3-D) bird's-eye view and (b) input characteristic curve of symmetric tunnel FET (S-TFET).

[1] W. Y. Choi *et al*., "Tunneling Field-Effect Transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.,* vol.28, no.8, pp.743-745, August 2007.

[2] S. H. Kim *et al*., "Germanium-source tunnel field effect transistors with record high I_{ON}/I_{OFF}," *2009 Symposium on VLSI Technology,* pp.178-179, June 2009.

[3] P. Matheu *et al*., "Planar GeOI TFET Performance Improvement With Back Biasing," *IEEE Trans. Electron Devices,* vol.59, no.6, pp.1629-1635, June 2012.

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637)

Optimal design of an electrically self-isolated GaN-on-Si junctionless field-effect transistor for beyond-CMOS low-power applications

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Junctionless field-effect transistor (JLFET) is regarded as one of the most promising electron devices owing to simpler fabrication, cost-effectiveness, and higher device reliability [1, 2]. Also, GaN is gaining popularity as a versatile material for logic, optical, and power devices due to its high electron mobility, wide energy bandgap, and higher breakdown voltage [3]. In this work, a GaN-on-Si JLFET with an electrically self-isolated n-channel is optimally designed by device simulations for low-power (LP) applications toward beyond-CMOS technology [4, 5]. The task was focused on lower I_{off} and higher I_{on}/I_{off} ratio to make use of the merit of GaN as a wide-bandgap material, and the device variables included physical gate length (L_g), GaN channel thickness (T_{ch}), channel doping concentration (N_{ch}), Si substrate doping concentration (N_{sub}), and gate workfunction (ϕ_g). L_g needs to be kept near 50 nm for an I_{off} below 50 pA/μm at T_{ch} = 20 nm (Fig. 1) and N_{ch} (n-type) = 1×10^{18} cm^{-3} and N_{sub} (p-type) 1×10^{17} cm^{-3} are permissible for minimizing I_{off} and maximizing I_{on}/I_{off} (Fig. 2). Also, it was confirmed that I_{off} could drop below 10 fA by adjusting ϕ_g. Further structural design would enhance I_{on} to meet the high-performance (HP) requirements simultaneously [5].

Acknowledgement This research was supported by Nano·Material Technology Development Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning (2009-0082580).

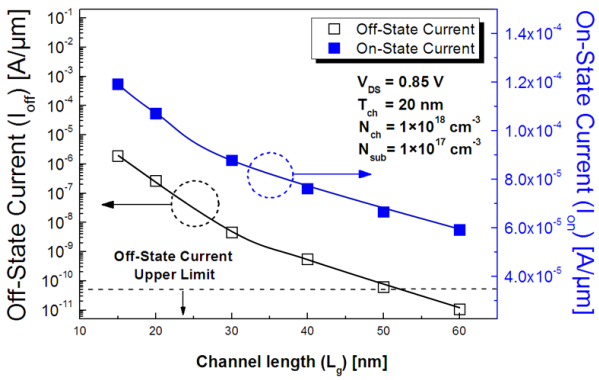

Fig. 1. Current characteristics as a function of L_g.

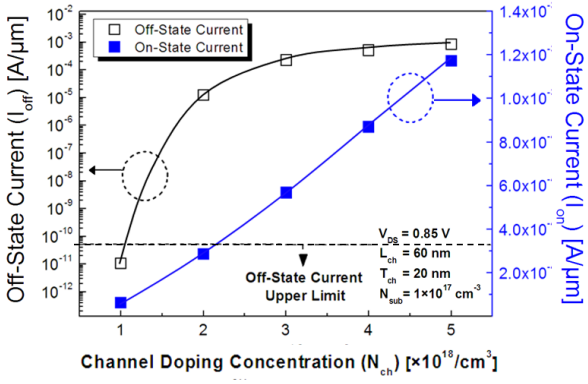

Fig. 2. Current characteristics as a function of N_{ch}.

[1] J. P. Colinge, *et al.*, *Nat. Nanotechnol.* **5** 225 (2010). [2] S. Cho, *et al.*, *IEEE Trans. Electron Devices* **58** 1388 (2011). [3] B. J. Baliga, ISBN 978-0-387-47313-0. [4] Atlas User's Manual (2014). [5] ITRS (2013).

A Novel Sampling Method Using Confidence Ellipse Concept to Estimate the Impact of Random Variation on Static Random Access Memory (SRAM)

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The read/write failures in static random access memory (SRAM) caused by random variation sources (*e.g.*, line-edge roughness, random dopant fluctuation, and work-function variation) become one of the critical issues in developing new CMOS technology [1]. The read/write failures in SRAM bit cells should be correctly, quickly and efficiently anticipated in order to better estimate the yield of large scale SRAM cells; Therefore, extensive simulations with stochastic sampling based on Monte Carlo (MC) methods should be performed with the large amount of computation time [2]. To considerably reduce the computation time, we proposed a novel sampling method with confidence ellipse concept. By using this manner, SRAM margin matrics such as word-line read retention voltage (WRRV), and word-line write trip voltage (WWTV) [3] in high sigma regimes can be more efficiently detected than the standard MC simulation.

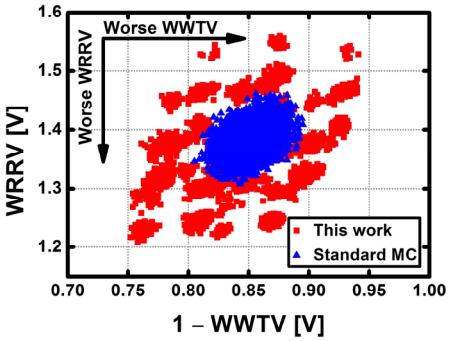

Fig 1. WRRV *versus* [1 – WWTV] for proposed method (red-colored squares) and standard MC method (blue-colored triangles). Note that 10,000 samples are generated for each method.

References

[1] X. Wang *et al*., "Impact of statistical variability and charge trapping on 14 nm SOI FinFET SRAM cell stability," in *Proc. 43rd ESSDERC*, Sep. 2013.

[2] R. Kanj *et al.,* "Mixture importance sampling and its application to the analysis of SRAM designs in the presence of rare failure events," in *Proc. Des. Autom. Conf.*, Jul. 2006, pp. 69–72.

[3] Z. Guo *et al*., "Large-scale SRAM variability characterization in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3174–3192, Nov. 2009.

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637).

Negative Capacitance Field-Effect Transistor for Sub-60-mV/decade Steep Switching Device

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By the Moore's Law, complemetary metal oxide semiconductor (CMOS) devices has successfully been scaled down "in size". However, V_{DD} (power supply voltage) scaling has not been as successful over the past five decades as channel length and/or gate-to-gate pitch scaling has been, because of the fundamental limits dictated by Boltzmann statistics that imposes a minimal gate voltage of 60 mV to obtain a tenfold drain-to-source current. The slowed scaling of V_{DD} leads to ever-increasing power density in CMOS devices, especially in transistors for low-power applications. To surmount the technical difficulty, negative capacitance (NC) [1] has recently come to the fore.

In this study, in order to experimentally demonstrate the effects of negative capacitance (*i.e.,* effects of surface potential amplification implemented by the phase transition of ferroelectric materials) in MOS transistor, a ferroelectric capacitor which consists of a P($VDF_{0.75}$–$TrFE_{0.25}$) insulation layer sandwiched by metal contacts is fabricated. Then, the ferroelectric capacitor is connected in series to the gate electrode of MOS transistor. The negative capacitance effects in the MOS transistor with the ferroelectric capacitor are observed, resulting in steep switching subthreshold slope (*i.e.,* sub-threshold slope < 60 mV/decade): 18 mV/decade subthreshold slope as shown in **Fig. 1b**.

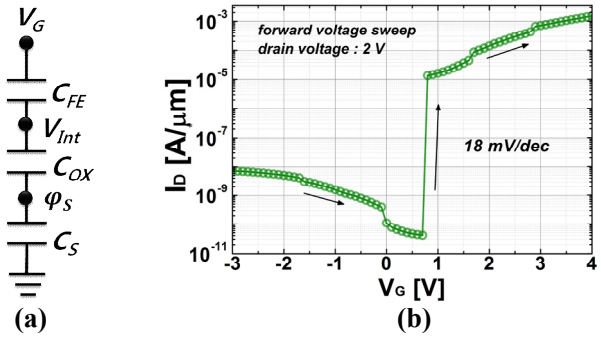

Fig. 1. (a) Capacitor divider of the negative capacitance FET, **(b)** Drain current *versus* gate current.

[1] S. Salahuddin and S. Datta, *Nano Lett*., **8**, 405-410 (2008).

Acknowledgments: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637). This work was supported in part by the KEIT funded by the MOTIE under Grant 10039174 (IT R&D Program) and in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program).

Germanium-Source Vertical Tunnel Field-Effect Transistor

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A novel tunnel field-effect transistor, germanium-source vertical tunnel field-effect transistor (Ge-source V-TFET), is newly proposed (**Fig. 1a**). Using two-dimensional TCAD device simulations, the performance of the Ge-source V-TFET is optimized. The V-TFET takes advantages of two types of tunneling (*i.e.,* "point tunneling" and "line tunneling" [1]) to improve its performance, resulting in both I_{ON}/I_{OFF} ratio of > 10^6 at power supply voltage (V_{DD}) of 0.5 V and steep subthreshold swing (SS) of sub-60-mV/decade at 300 K (**Fig. 1b**). Another feature in designing the V-TFET is that the total region for band-to-band tunneling is aggressively widened in-between the source/gate region for performance enhancement. Lastly but not least, the band-to-band tunneling, particularly within the source region, is very dependent of the equivalent oxide thickness and gate biasing for the V-TFET. For ultra-low power application (*i.e.,* V_{DD} < 0.5 V), the Ge-source V-TFET would be one of the promising future CMOS device structures.

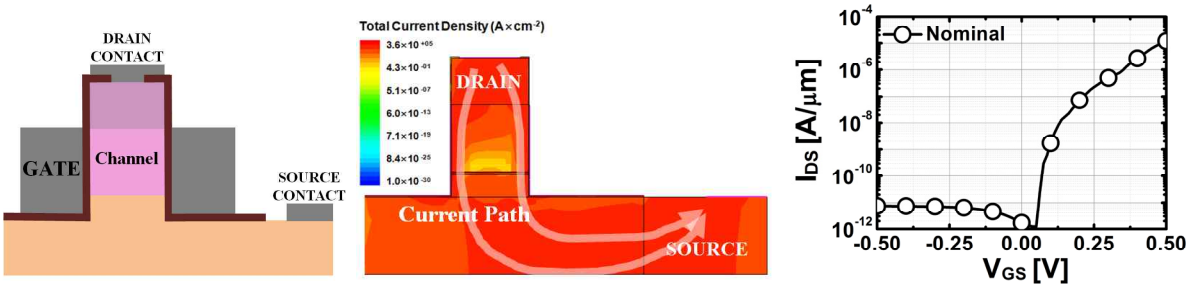

Fig. 1. (a) Cross-sectional view of Ge-source V-TFET (left) and contour map of total current density (right), **(b)** simulated I_{DS} *vs.* V_{GS} plot for the Ge-source V-TFET.

Reference

[1] W. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree and W. Magnus, in *Proc. SISPAD*, 137-140 (2008).

Acknowledgement: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2014R1A2A1A11050637).

Selective area growth of high quality InP layers on Si (001) by MOCVD

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High-quality epitaxial growth of InP on silicon substrates has been of great interest for many years because of the potential for monolithic integration of InP-based devices with Si metal-oxide semiconductor (MOS) integrated circuits and high performance and low power logic devices[1]. We report on the selective area growth (SAG) of high quality InP layers on patterned (001) Si substrates at various growth temperatures by metal organic chemical vapor deposition (MOCVD). Thin InP and GaP layers were used as intermediate buffer layers between patterned Si surface and high temperature (HT) InP layer. The InP layers grown by SAG at 650°C and 550°C exhibited the typical {111} facets and the smooth (100) top surface, respectively. Anti-phase domain boundaries (APBs) and defects were trapped by lateral sidewalls of the etched Si substrate.

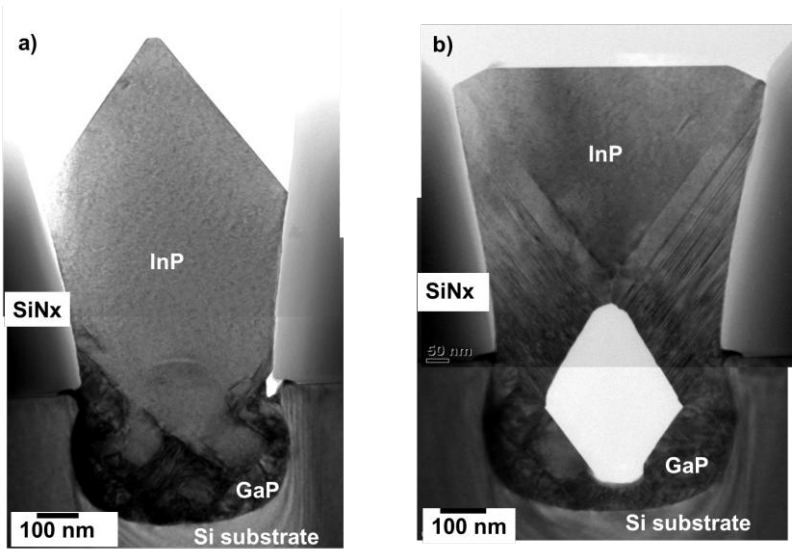

Fig 1. Cross-section TEM images of InP layers grown on patterned Si (001) substrate at (a) 550 ^{o}C and (b) 650 ^{o}C

[1] H. Ito et al., IEEE J. Selected Topics in Quantum Electronics, **10**, 709 (2004).

Reduction of dark current in InSb photodiode through band alignment engineering of barrier layer

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InSb photodiodes are widely used for mid wavelength infrared(MWIR) detectors. In order to obtain a high resolution image of IR, the reduction of dark current is one of the major challenges as the dark current deteriorates device performance. The use of electron blocking layer of an AlInSb alloy to reduce the surface leakage current and the diffusion current has been widely investigated.[1][2] The schematic of the device and band structure are represented in Fig. 1(a).
In this experiment, the growth conditions of the AlInSb layer for high performance device are modelled by SILVACO ATLAS software. It was observed that increasing p-type doping concentration in AlInSb is effective for the reduction of dark current due to the band alignment of AlInSb. The simulation result, shown in Fig. 1(b), indicated that in the invetigated range, the lowest dark current of 1 x 10^{-12} A appeared at 5 x 10^{18} cm^{-3}. In addition, the thickness of the AlInSb layer was varied in the range from 5 nm to 50 nm to reduce the dark current. The results showed that the lowest dark current value of 9 x 10^{-12} A was obrained at 50 nm thickness. More experimental results and discussion will be given in the presentation.

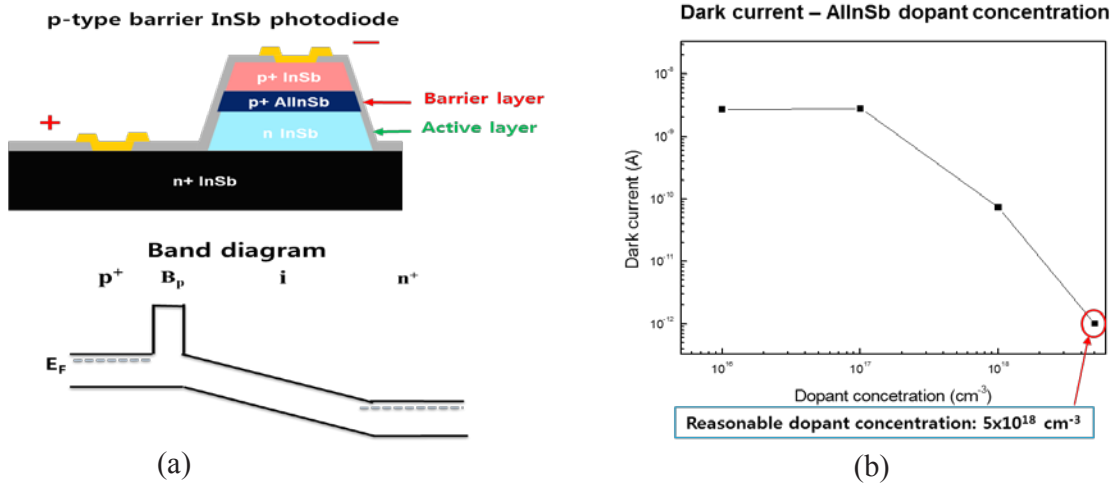

Fig 1. p-type barrier InSb photodiode and its dark current data

[1] S. Mailmon and G. W. Wicks, Applied Physics Letters, Vol. 89, No. 151109 (2006).
[2] J.R. pedrazzani. et al., Electron Letters, Vol. 44, No. 25 (2008).

Strain measurement in MOSFET structures with $Si_{1-x}C_x$ S/D upon thermal annealing process

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Mechanical stresses induced by the lattice mismatch at hetero-junction effectively enhance the carrier mobility of CMOSFETs [1]. For n-channel transistors, embedded epitaxial $Si_{1-x}C_x$ source/drain (S/D) structure induces tensile strain in the Si channel region. The tensile strain induced by the smaller lattice constant of $Si_{1-x}C_x$ than that of Si improve the electron mobility of n-channel transistors [2]. More recently, the formation of silicide on $Si_{1-x}C_x$ S/D in the n channel MOSFETs has been studied in order to reduce the contact resistivity at the interfaces between metal/ $Si_{1-x}C_x$. A new challenge, therefore, is to cautiously assess any possible influence of scaling on the channel strain or other steps in the process flow by using a reliable characterization method. For this purpose, it is essential to precisely measure the strain changes in the transistor. In this study, we experimentally evaluated effects of scaling and thermal annealing process on the channel strain. We used transistor arrays incorporating $Si_{1-x}C_x$ as a stressor with systematically varying gate and S/D lengths, and employed the nano beam diffraction (NBD) method to measure the channel strain. We also carried out simulation to check the validity of the NBD data.

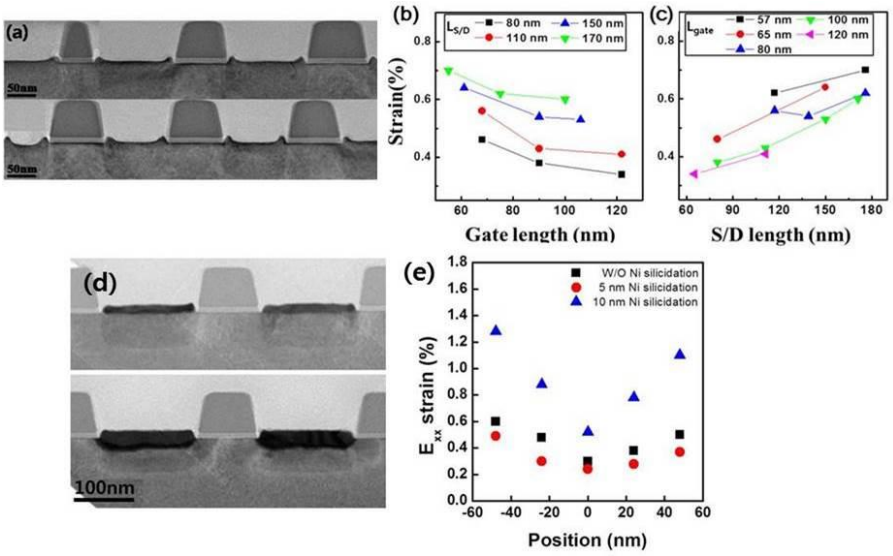

Fig 1. TEM images of MOSEFT structure with $Si_{1-x}C_x$ S/D and NBD data.

[1] Y.-C. Yeo, Semicond. Sci. Technol. 22, S177 (2007).

[2] S. S. Chung et al., Symp. VLSI Technology Dig. Tech. Pap. pp. 158 (2009).

MBE growth of III-V based materials and its applications to 2D/1D/0D structures

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In KIST, 5 (+3) MBE systems are installed for the study of low dimensional structures. With the MBEs, we are in the middle of studying; As/P/Sb-based materials with new properties, High speed 3-5 2DEGs/2DHG for physics (mesoscopic physics, Topo. Insul. etc), high speed, and low power consumption electronics, Digital-alloyed 2D structures for QCL, QWIP, LD, PDs, Catalyst free/Au-assisted GaAs/InAs/InP/InSb nano-rod 1D structures for SPS or Nano TR etc., Various kind of semi-conductor QDs grown by SK, MEE, and Droplet methods. With these MBE systems, the researcher in KIST published more than 200 SCI articles include Nature (2013) and Science (2009).

In this presentation, I will show MBE systems & activities with them in KIST and discuss probable co-works.

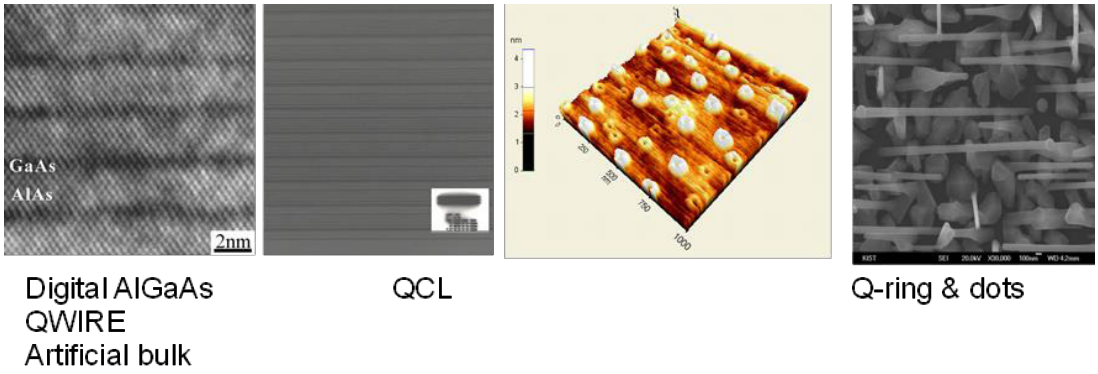

Figure. Examples of nanostructure grown by KIST MBE

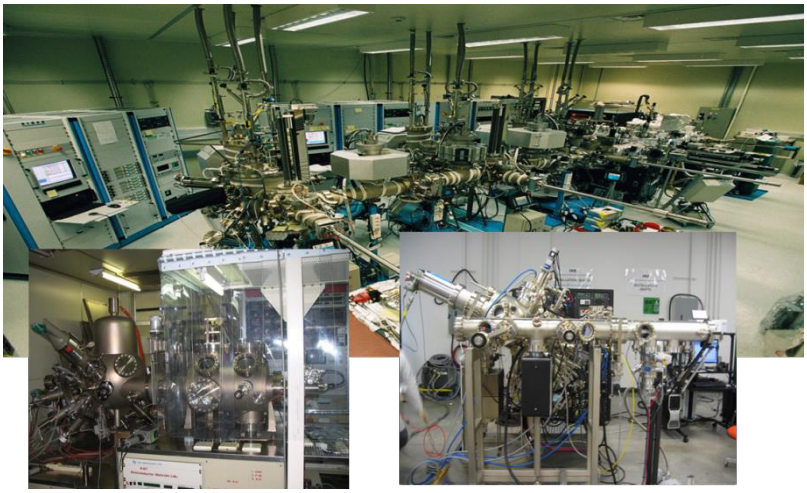

Figure. Images of KIST MBE systems.

Magnetic-field-controlled reconfigurable semiconductor logic

Jin Dong Song

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Logic devices based on magnetism show promise for increasing computational efficiency while decreasing consumed power. They offer zero quiescent power and yet combine novel functions such as programmable logic operation and non-volatile built-in memory. However, practical efforts to adapt a magnetic device to logic suffer from a low signal-to-noise ratio and other performance attributes that are not adequate for logic gates. Rather than exploiting magnetoresistive effects that result from spin-dependent transport of carriers, we have approached the development of a magnetic logic device in a different way: we use the phenomenon of large magnetoresistance found in non-magnetic semiconductors in high electric fields. Here we report a device showing a strong diode characteristic that is highly sensitive to both the sign and the magnitude of an external magnetic field, offering a reversible change between two different characteristic states by the application of a magnetic field. This feature results from magnetic control of carrier generation and recombination in an InSb p–n bilayer channel. Simple circuits combining such elementary devices are fabricated and tested, and Boolean logic functions including AND, OR, NAND and NOR are performed. They are programmed dynamically by external electric or magnetic signals, demonstrating magnetic-field-controlled semiconductor reconfigurable logic at room temperature. This magnetic technology permits a new kind of spintronic device, characterized as a current switch rather than a voltage switch, and provides a simple and compact platform for non-volatile reconfigurable logic devices.

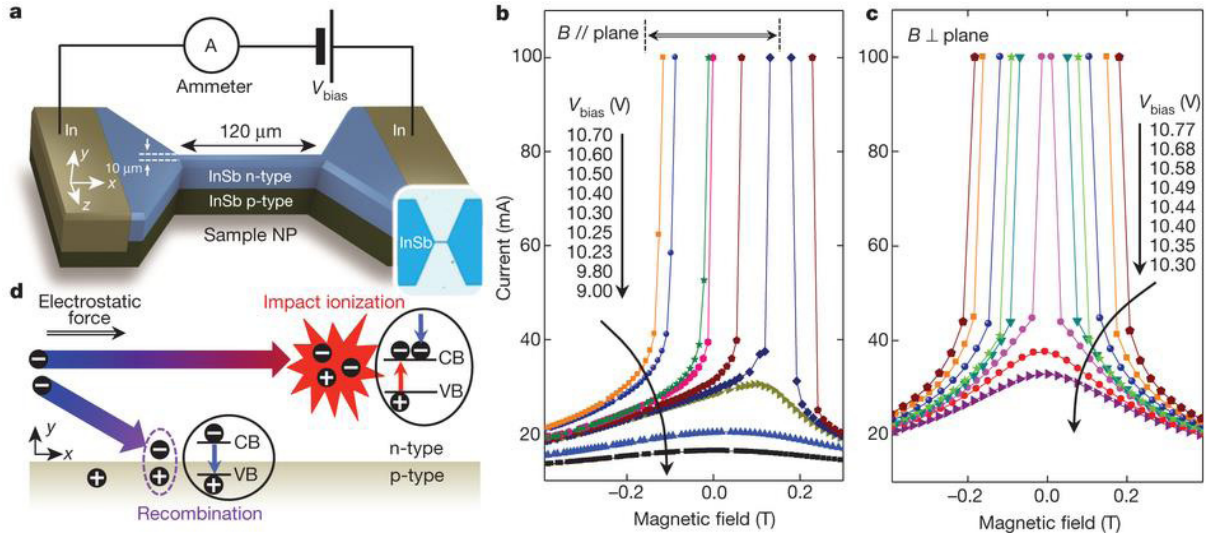

Figure. Magnetoconductance tunable by external voltage.

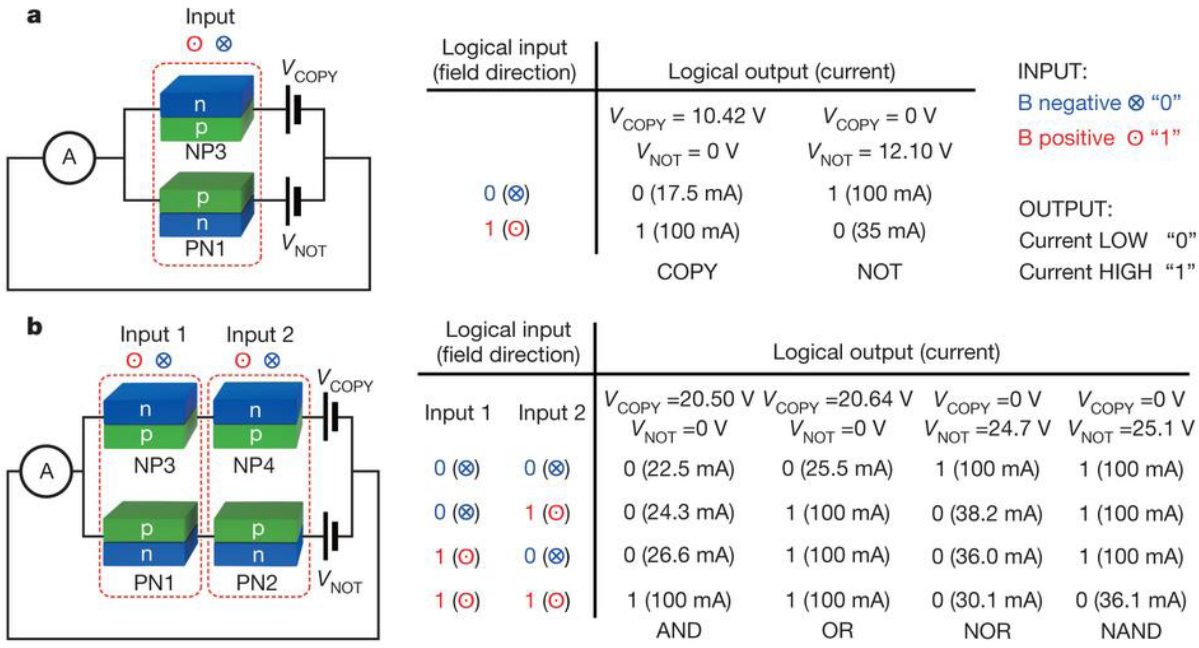

Figure. Demonstration of various Boolean operations.

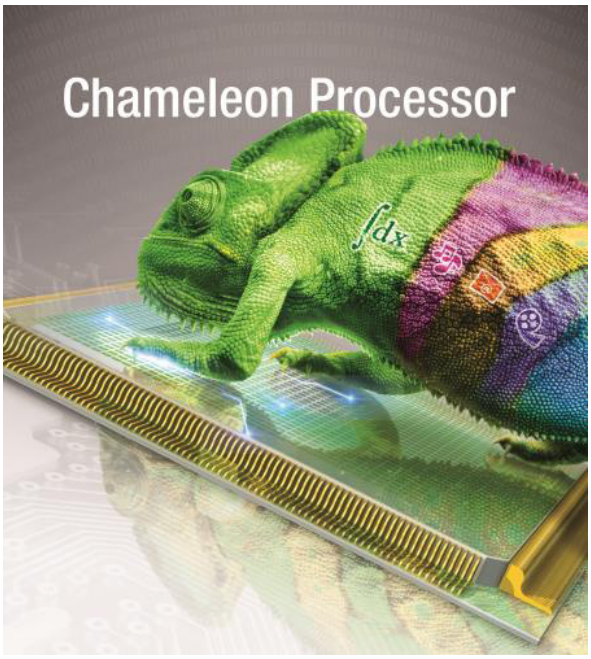

Figure. images of chameleon process; Goal of this research

[REF] Sungjung Joo, Taeyueb Kim, Sang Hoon Shin, Ju Young Lim, Jinki Hong, Jin Dong Song, Joonyeon Chang, Hyun-Woo Lee, Kungwon Rhie, Suk Hee Han, Kyung-Ho Shin & Mark Johnson, Nature v. 494, pp. 72–7, 2013.

Interfacial layer control by dry cleaning technology for polycrystalline and single crystalline silicon growth

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Native oxide removal prior to poly-Si contact and epitaxial growth of Si is the most critical technology to ensure process and device performances of poly-Si plugs and selective epitaxial growth (SEG) layers for DRAM, Flash and Logic application. Recently, dry cleaning process for interfacial oxide removal has attracted a world-wide attention due to its superior passivation properties to conventional wet cleaning processes [1,2]. In this study, we investigated the surface states of silicon substrate during and after dry cleaning processes, and the role of atomic elements including flourine and hygrogen on the properties of subsequent amorphous silicon layer using SIMS, XPS, and TEM analysis. Residual element on the Si surface, as well as bonding nature on the silicon surface after dry cleaning is the key factor for interface control. We also observed epitaxial growth of silicon islands at low temperature by the decrease of residual F and the perfect termination of H on Si surface after dry cleaning.

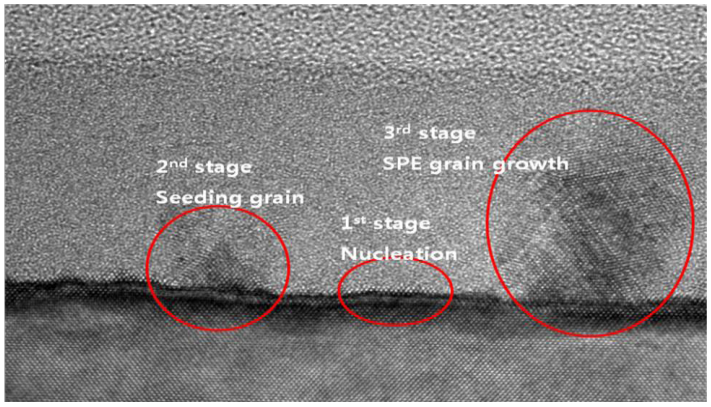

Fig 1. TEM observation of interface and crystal growth of amorphous Si using dry cleaning

[1] H. Ogawa, *et al.*, Jpn. J. Appl. Phys., Vol.41, 5349 (2002).
[2] J. Kikuchi, *et al.*, Jpn. J. Appl. Phys., Vol.33, 2207 (1994).

Two-Dimensional Layered Materials for Advanced Electronics

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Two-dimensional (2D) materials have brought a great deal of excitement to researchers and nanoscience community with its attractive and unique properties. Such outstanding electrical, optical, and mechanical properties of various 2D materials can be utilized for advanced electronics, which are transparent and flexible form along with multifunctions. Here we present our recent achievements in the van der Waals heterostructure devices consisting entirely of 2D materials. By stacking and combining diverse 2D materials, we fabricate high performance switching devices, memories, and p-n junction diodes [1,2,3]. These van der Waals heterostructure devices operate in a flexible form with high stability and transparency [2]. Strong light-matter interaction in 2D heterostructures shows that 2D materials are one of the most promising candidates for advanced optoelectronics, such as photodetectors, solar cells, and light-emitters [3]. Our demonstration of 2D heterostructure devices shows a new way toward fabrication of novel electronic devices, which employ new physics occuring only in 2D materials.

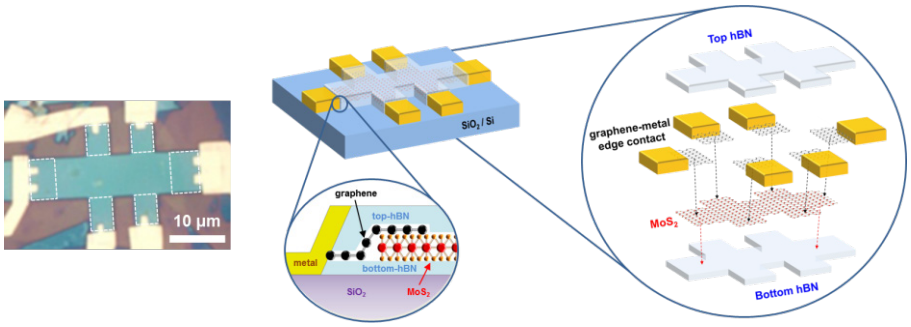

Fig 1. van der Waals heterostructure devices consisting of 2D materials.

[1] M. S. Choi, G. H. Lee, Y. J. Yu, D. Y. Lee, S. H. Lee, P. Kim, J. Hone, and W. J. Yoo, Nature Commun. 4, 1624 (2013).
[2] G. H. Lee, Y. J. Yu, X. Cui, N. Petrone, C. H. Lee, M. S. Choi, D. Y. Lee, C. Lee, W. J. Yoo, K. Watanabe, T. Taniguchi, C. Nuckolls, P. Kim, and J. Hone, ACS Nano, 7, 7931–7936 (2013).
[3] C. H. Lee, G. H. Lee, A. van der Zande, W. Chen, Y. Li, M. Han, X. Cui, G. Arefe, C. Nuckolls, T. F. Heinz, J. Guo, J. Hone, and P. Kim, Nature Nanotechnol. 9, 676-681 (2014).

Polymorphous Two-Dimensional van der Waals system of Tin-Sulfides: Controllable Synthesis and Electrical Characteristics

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In recent years there has been an explosive interest in research on two-dimensional (2-D) van der Waals (vdWs) materials due to their unique physical properties and great potential in the application of emerging devices. In aspect of device application, it is very important to achieve the directly grown single crystal on substrate with a large area, and many researchers have focused on the synthesis method and device characterization of the versatile vdWs materials with hexagonal symmetry such as graphene, h-BN and transition metal chalcogenide compounds [1]. However, there are only a few reports on layered crystal of orthorhombic symmetry, which is another type of 2-D vdWs materials, and the 2-D growth on substrate has not been realized based on orthorhombic symmetry. Here, we present a controlled growth of the polymorphous 2-D structures of tin sulfide compounds directly on substrate via control of the growth atmosphere. The SnS_2 crystal with hexagonal symmetry and the SnS crystal with orthorhombic symmetry could be grown in an inert ambient and a hydrogen ambient, respectively, and the growth behavior is supported by the thermodynamic study. Our layered crystals shows n-type characteristics with band gap of 2.69 eV for SnS2, and p-type characteristics with band gap of 1.26 eV for SnS, respectively. In addition to this, we demonstrate p-n heterojunction devices. The SnS2-SnS heterojunction devices show the gate tunable rectifying characteristics and obvious photovoltaic effect across the p-n junction.

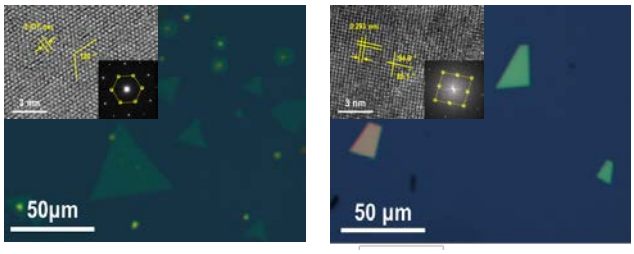

Fig 1. 2-D grown SnS2 and SnS crystal

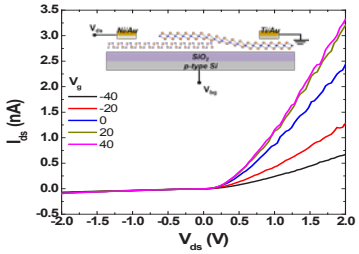

Fig 2 SnS2-SnS heterojunction

[1] M. Xu, T. Liang, M. Shi, and H. Chen, Chem. Rev. 113, 3766 (2013).

The suppression of electron transport by ion-beam irradiation on multilayer WSe_2

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Transition metal dichalcogenides(TMDs) have garnered much attention in the recent years because it overcomes the shortcomings of zero-bandgap graphene, while it is still sharing many of graphene's advantages for electrical device applications.
Current advances in Molybdenum disulfide(MoS_2), one of the TMD semiconductors with a large band gap of ~1.8eV in monolayer, have shown the potential use of layered semiconductors for high performance n-type field effect transistor(FET). However, studies about p-type TMD are still very limited in spite of various efforts to get enhanced performance transistors. At the same time, the research for an p-type FET becomes urgent for realizing complementary digital logic applications.
In this work, we demonstrate the suppression of ambipolar property as demoting the electron conduction in ion-bombarded multilayer Tungsten diselenide(WSe_2). We investigate the effect of implanted ion beam with ion beam energy, power and post annealing temperature performed in N_2 ambient. After rapid thermal annealing(RTA), we could observe stable transfer curves and rises of the channel currents. In addition, the result presents increases of hole mobilities in comparison to pristine WSe_2. Therefore, this doping technique provides a highly viable route to present p-channel transistors with TMDs, paving the way for a certain strategy to fabricate 2D nanoelectronic devices.

Irradiation effects of high energetic proton beams on MoS_2 and pentacene field effect transistors

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Recently, molybdenum disulphide (MoS_2) has gained a significant research interest due to their potential applications in atomic-film devices. With the motivation that we could tailor the electrical properties of field effect transistor (FET) devices made with semiconducting nanowires [1], we studied the irradiation effects of high energetic proton beams on MoS_2 FETs that were made with exfoliated multi-layer MoS_2 atomic films. We measured and compared the electrical characteristics of the MoS_2 FETs before and after the proton-beam irradiation with beam fluence conditions of 10^{12}, 10^{13}, and 10^{14} cm^{-2}. For high enough proton beam fluence conditions of 10^{13} or 10^{14} cm^{-2}, the current level and conductance of the devices significantly decreased after the proton irradiation compared with those prior to the proton irradiation, which was originated from the proton-irradiation-induced traps such as positive oxide-charge traps in the SiO_2 layer and the trap states at the interface between the MoS_2 channel and the SiO_2 layer [2]. Also, we studied similar proton-beam irradiation effects on organic pentacene FETs. Interestingly, the conductance of the pentacene FETs increased after the proton beam irradiation with low fluence condition, however, decreased after the proton beam irradiation with high fluence condition. These electrical changes are due to the negative trap charges at the pentacene/SiO_2 interface. Our studies will enhance the understanding of the influence by the high energetic particles on various types of electronic devices.

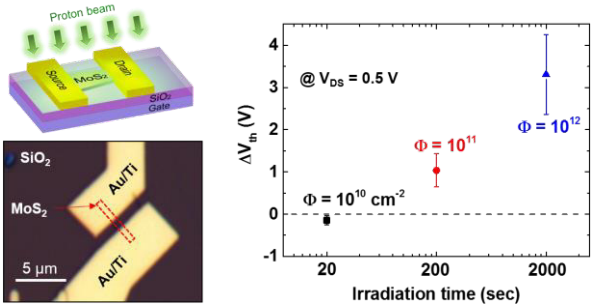

Fig 1. MoS_2 FET devices and the threshold voltage change by proton-beam irradiation

[1] W.-K H, G. J, J. I. S, W. P, M. C, G. W, Y. H. K, M. E. W, and T. Lee, ACS Nano, 4, 818 (2010).
[2] T.-Y. Kim, K. Cho, W. Park, J. Park, Y. Song, S. Hong, and T. Lee, ACS Nano, 8, 2774 (2014).
[3] T.-Y. Kim et al. manuscript in preparation (2014).

Efficient Virtual Machine Live Migration through Discarding Unnecessary Data Transmission

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가상화 환경에서 물리서버의 효율적인 운용을 위하여 부하가 많은 물리서버로부터 부하가 적은 물리서버로 가상머신을 이주시키는 Live Migration[1]이 사용된다. Xen[2]에서는 가상머신에게 할당한 전체 메모리를 네트워크를 통해 전송하는 방식으로 동작한다. 하지만 전송되는 데이터의 양이 많기 때문에 물리 서버의 가용 네트워크 대역폭 감소를 불러일으키게 되고, 이로 인하여 동일한 물리서버 내 다른 가상머신들의 네트워크 성능저하가 일어나는 문제점을 가지고 있다. 이주되는 가상머신이 사용하고 있는 메모리의 크기가 클수록, 이주시간은 증가하고 가상머신들이 제공하는 서비스들의 QOS(Quality of Service)를 보장하지 못하는 문제도 발생할 수 있다. 이러한 문제를 해결하고자 Xen 을 기반으로, 전송되는 페이지들의 값들을 대조군과 비교하여 특정 값으로만 이루어진 페이지들을 전송하지 않는 Live Migration 기법을 제안한다. 이 기법에서는 위 페이지들을 전송하는 대신, 각각의 페이지 주소와 메타데이터를 전송하여 가상머신을 받는 물리서버에서 페이지들을 재구성한다. 가상머신의 모든 페이지에 대한 검사 비용을 줄이기 위하여 특정 크기의 바이트만 먼저 검사 한 후, 결과에 따라 전체 페이지 크기에 대한 검사 수행 여부를 확정하는 Sampling 방식을 적용하였다.

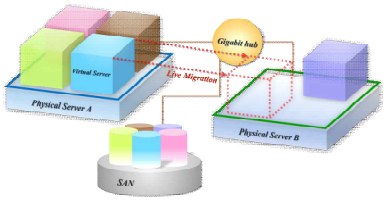

Fig 1
Experimental environment

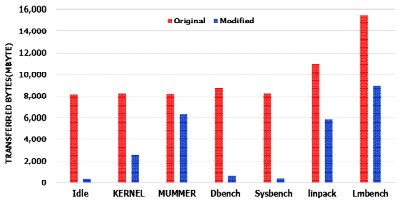

Fig 2
Transferred data size comparison

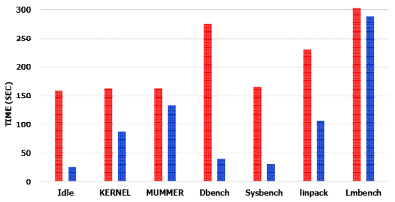

Fig 3
Virtual machine migration time

[1] C. Clark, K. Fraser, S. Hand, J. G. Hansen, E. Jul, C. Limpach, I. Pratt, and A. Warfield. Live migration of virtual machines. In Proceedings of the 2nd Conference on Symposium on Networked Systems Design & Implementation, pages 273–286, 2005.
[2] P. Barham, B. Dragovic, K. Fraser, S. Hand, T. Harris, A. Ho, R. Neugebauer, I. Pratt, and A. Warfield. Xen and the art of virtualization. In Proceedings of the Nineteenth ACM Symposium on Operating Systems Principles, pages 164–177, 2003.

Exploring the Performance of PCM-Swap Systems*

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This paper explores the performance of PCM-swap systems and discusses how this system can be managed efficiently. We assume PCM to be attached on DIMM slots thereby eliminating block I/O overhead and removing context switches while handling page faults. We show that an optimal page size is relatively small in PCM-swap as shown in Fig. 1. This is different to HDD-swap where the best performance is obtained when the page size is 4KB or more. Though reducing the page size is not a simple issue as the number of page table entries should be increased, we argue that this overhead can be relieved by reducing the total DRAM capacity of the system. Through our experiments, we show that a "small memory – fast swap" system exhibits a competitive performance. Fig. 2 shows the total elapsed time under PCM-swap as the DRAM capacity is varied from 5% to 100% of the footprint. For each configuration, we also vary the page size. As shown in the figure, the performance is not degraded even with the 5-10% DRAM capacity when a small page size is used. This is because only the necessary part is loaded into DRAM. As we eliminate block I/O and context switch overheads, reducing the transfer size is important in minimizing the total cost of a page fault. Based on these preliminary results, we set the DRAM capacity to 10% of the footprint hereinafter. Fig. 3 compares the performance of various PCM-swap configurations. The "baseline" uses the 4KB page with the default read-ahead option and the CLOCK algorithm, "small page" shrinks the page size to 256B, "RA-OFF" turns off the read-ahead, and "W-CLOCK" employs a new page replacement policy by changing the original CLOCK such that the dirty bit is used to capture the recency of write references. The result shows that the cost of loading unnecessary pages through read-ahead is relatively expensive in PCM-swap, and predicting future write accesses and maintaining pages likely to be re-written in memory is effective. Fig. 4 shows the total elapsed time and the energy consumption of our PCM-swap under 10% DRAM size in comparison with disk-swap under 100% DRAM size. PCM-swap exhibits 64.1% better performance but consumes 90.2% less energy. We expect that our result will lead to the transition of legacy swap systems of "large memory – slow swap" to a new paradigm of "small memory – fast swap."

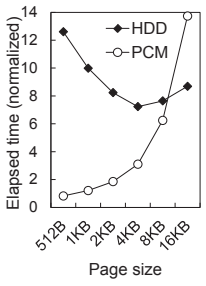

Fig. 1 HDD vs PCM.

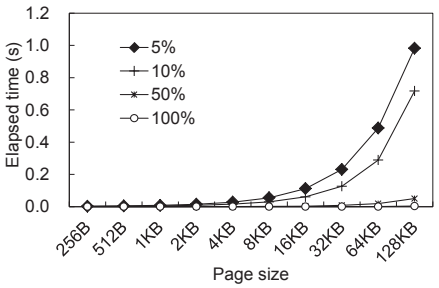

Fig.2 PCM-swap as DRAM size changes.

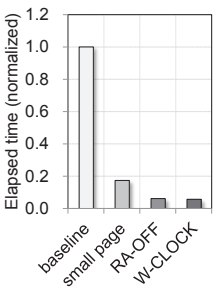

Fig. 3 PCM-swap configs.

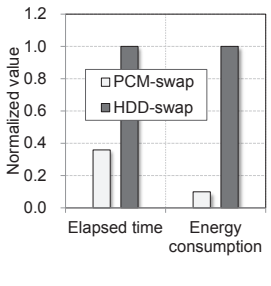

Fig. 4 PCM-swap with small DRAM

* This work was supported by the IT R&D program MKE/KEIT (No.10041608, Embedded System Software for New-memory based Smart Devices) and the National Research Foundation (NRF) grant funded by the Korea government (MEST) (No. 2011-0028825).

플래시 기반 저장장치에서 무작위 선택을 활용한 마모 평준화 기법

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단국대학교 컴퓨터학과 컴퓨터공학
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플래시 메모리 기반 저장장치는 빠른 임의 접근 시간, 높은 데이터 처리량, 저전력 등의 장점을 가지고 있어 스마트 폰, PC 뿐만 아니라 대용량의 서버와 데이터 센터에도 활발히 도입되고 있다. 그러나 플래시 메모리의 제한된 삭제 횟수 문제로 인해 저장장치의 신뢰성 문제가 야기되어 왔다. 이에 따라 플래시 메모리 내의 각 블록 간에 삭제 연산을 균등하게 수행함으로써 신뢰성을 향상시키는 마모 평준화 기법(wear-leveling)이 제안되었다. 대표적인 마모 평준화 기법은 블록 전수검사를 통한 교체(greedy policy) 기법이다. 그러나, 플래시 저장장치의 용량이 증가됨에 따라 정적 마모 평준화 기법에 소모되는 부하(load)가 점점 증가하고 있다. 이에 따라, 본 논문에서는 마모 평준화 작업의 부하를 줄이기 위한 무작위 선택 기법(randomized block select)을 제안한다. 구체적으로, 제안된 기법에서는 무작위로 삭제대상 블록을 선택함으로써 삭제 대상 블록 선정에 따르는 부하를 최소화 한다. 이 때 무작위로 2 개의 블록을 선택하여 삭제 횟수를 비교함으로써 단일 블록 선정을 통한 마모 평준화 기법 대비 높은 신뢰성을 제공한다 [1]. 제안된 기법은 OpenNFM 플래시 메모리 시뮬레이터 상에 구현되었으며, MSR Cambridge trace 를 사용한 실험 결과 제안된 기법이 기존기법 대비 적은 부하 만으로도 최적 평준화에 근접하는 마모 평준화가 가능함을 확인하였다.

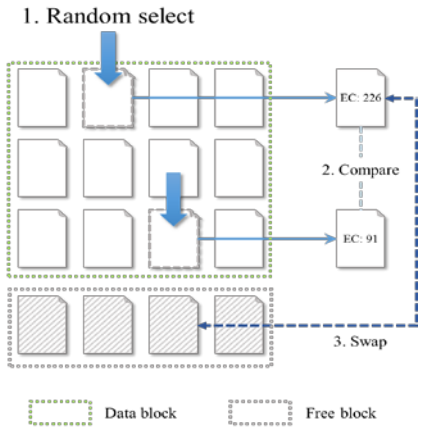

Fig 1. Random select replacement policy

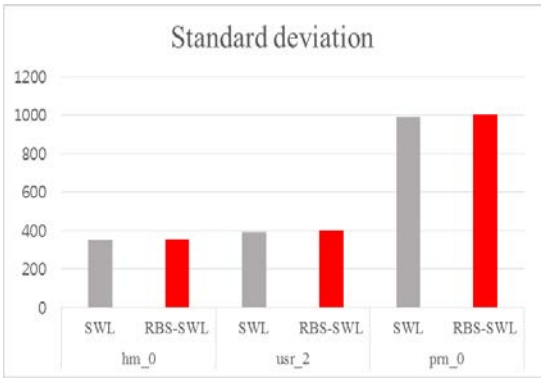

Fig 2. Standard deviation of erase count

[1] M. Mitzenmacher, "The Power of Two Choices in Randomized Load Balancing", IEEE Transactions on Parallel and Distributed Systems, 12(10), 2001

Preventing Fast Wear-out of Flash Cache with Admission Control*

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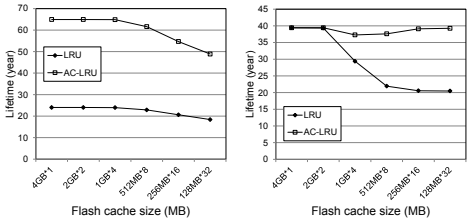
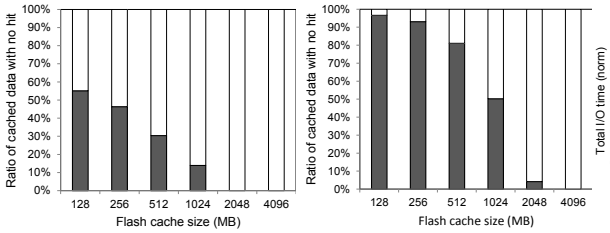
[1]*Chungbuk National University* [2]*Ewha University*
http://oslab.cbnu.ac.kr

Recently, flash cache is widely adopted as the performance accelerator of legacy storage systems. Unlike other cache media, flash cache should be carefully managed as it has peculiar characteristics such as long write latency and limited P/E cycles. In particular, when the working-set of a system is beyond the capacity of flash cache, it encounters a serious worn-out problem caused by excessively frequent cache replacement. To quantify this effect, we investigate the lifetime of different flash cache configurations under the same cost. Specifically, we set the initial cache size to 4GB and investigate the lifetime of this cache first. Then, we split the 4GB cache into two 2GB caches and use one 2GB first, and the other 2GB after the first one is worn out. Similarily, we measure the lifetime of subsequent cache configurations reducing the cache size in half. As shown in Fig. 1, the lifetime of using many small caches repeatedly is not longer than the lifetime of adopting a large cache once. This is because a small cache incurs much more frequent replacement. We can also observe the reason of this phenomenon in Fig. 2, which shows the ratio of non-accessed data during the cache residence as the cache size is varied. As shown in the figure, 67% of data on average has no hit when the cache is smaller than 1GB. To address this problem, we propose a cache admission control (AC) policy that detects data unlikely to be re-referenced soon and prevents them from being loaded into the flash cache. The proposed polisy does not cache data when it is first accessed, and inserts it in the cache only after its second access occurs within a certain time window. This allows the filtering of data disruptive to flash cache in terms of endurance and performance. With this policy, we prolong the lifetime of flash cache 2.3 times (Fig. 1) compared to original LRU, without any performance degradations (Fig. 3).



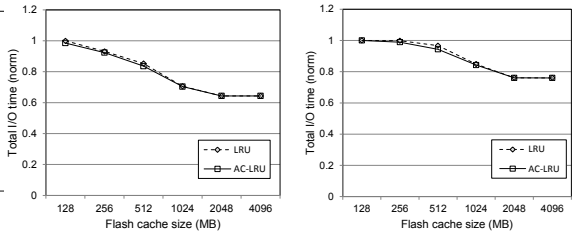
(a) Financial W/L (b) Websearch W/L

Fig. 1. Flash cache lifetime



(a) Financial W/L (b) Websearch W/L

Fig. 2. Ratio of non-hit data in Flash cache



(a) Financial W/L (b) Websearch W/L

Fig. 3. I/O performance with/without AC.

* This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (No. 2011-0025633) and the Ministry of Science, ICT & Future Planning (No. 2014R1A1A3053505).

An Analytical Approach to Evaluation of SSD Effects under MapReduce Workloads

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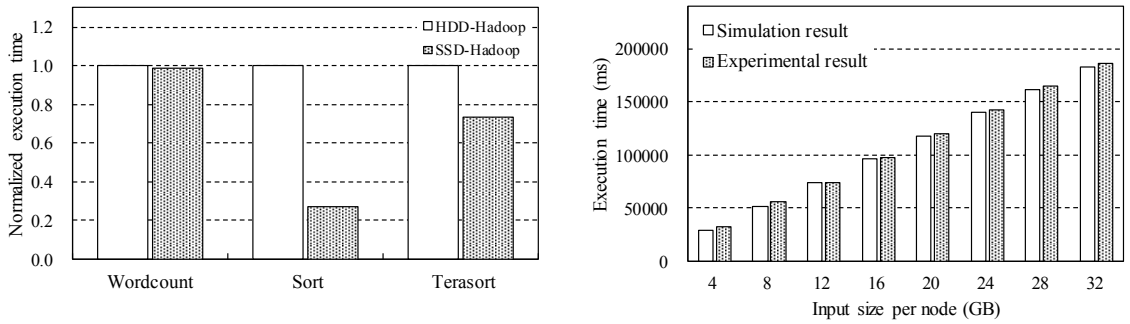
As the cost-per-byte of SSDs dramatically decreases and real-time BigData processing emerges, the introduction of SSDs becomes an unavoidable choice in the BigData industry, especially to reduce I/O overhead. Although there are many studies to evaluate the influence of SSDs in Hadoop, the most of them depend on experimental evaluation results [1]. In this paper, we propose a simplified performance model, as well as experimental evaluation results, for investigating the implication of SSDs in MapReduce workloads. First, we evaluate the effect of SSDs in Hadoop clusters. The evaluation results indicate that SSDs improve network throughput and CPU utilization because the adoption of SSDs removes the I/O bottleneck incurred by HDDs. As a result, it reduces the execution time of MapReduce jobs by up to 73%. Second, to build the performance model of MapReduce jobs, they are divided into three different phases: Map, Shuffle and Reduce, and each of them is carefully profiled while running Hadoop benchmarks. The profiling results show that the latency of each task is not deterministic but dispersed over a wide range, unlike the assumption of previous studies such as [2]. Therefore, we build a queuing network based on our profiling results to simulate MapReduce jobs. In conclusion, the simulation results show that our performance model can predict the execution time of MapReduce jobs within 10% error rate.



(a) Comparison of Hadoop benchmark results (HDD vs SSD) (b) Correlation of MapReduce performance model

Fig 1. Performance evaluation results

[1] S. Moon, J. Lee and Y. Kee, “Introducing SSDs to the Hadoop MapReduce Framework,” In the proceeding of International Conference on Cloud Computing, 272, (2014).
[2] E. Vianna, et al. “Analytical Performance Models for MapReduce Workloads,” Int. Journal Parallel Programming, vol. 41, issue 4, 495-525, (2013).

Circuit-Level Modeling of 10-Gbps Si-Photonic Transceiver

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Recently, there are growing interests in Si-photonics for optical interconnect applications as it can provide high-performance integrated photonic devices in a cost-effective manner [1]. For successful design of integrated Si-photonic and electronic circuits for the target interconnect applications, it is very important to co-simulate photonic devices and electonic circuits on a single simulation platform. In this paper, we present a behaviour model of Si micro-ring modulator implemented in Verilog-A, a hardware description language often used for high-level behavioral modeling of electronic systems, and circuit-level simulation of this behaviour model with other electronic circuits for 10-Gbps transceiver realization. Fig. 1(a) shows the block diagram for the target transceiver. The electronic circuit block is composed of PRBS generator and error-rate tester that allow on-chip self-testing, for serializer and deserializer, modulator driver and transimpedance amplifier. The optical block consists of Si micro-ring resonator and Ge photodetector. Fig. 1(b) and (c) are trasmitted and received eye diagrams, respectively, obained from the simulation done entirely in Spice. With such co-simulation of photonic devices and electronic circuits, design optimization of the entire Si-photonic transceiver can be easily performed allowing more successful implementation of the target optical interconnects in a more cost-effective manner.

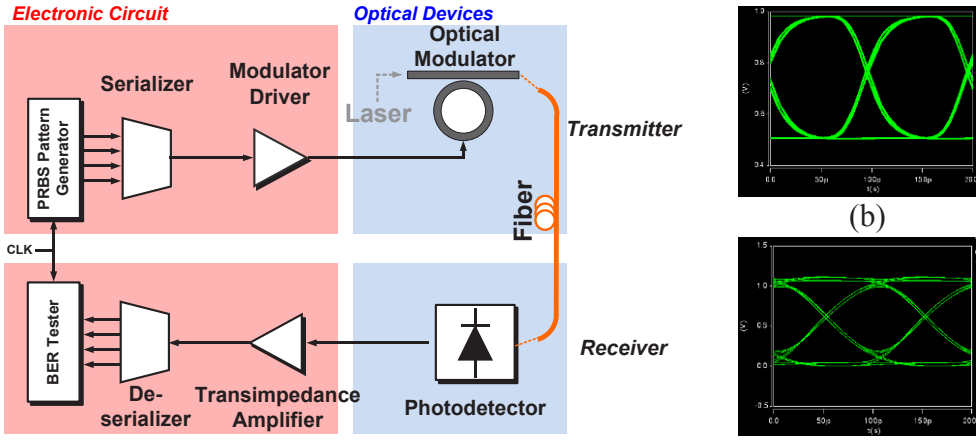

Fig 1. (a) Block diagram of Si-photonic transceiver and eye-diagram of (b) transmitted data and (c) received data

[1] X. Zheng *et al.,* Optics Express(2011), Vol. 19, No. 6

The conducted radiation modeling method for automotive IC

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최근 복잡한 전자 통신 시스템의 가파르게 성장하게 되면서 시스템에 영향을 주는 전자파 방해에 대한 관심이 높아졌다. 특히 자동차와 관련된 전자 장비의 경우 EMI에 의한 자동차 전자 장비의 오작동은 운전자에게 치명적인 영향을 줄 수 있다. 따라서 EMI에 대한 영향을 알아보기 위해서는 conducted radiation 모델링이 필요하다.[1]

본 논문에서는 IC의 conducted radiations을 모델링하는 방법을 제안하고 그 모델링을 통해 ASIC에 인가되는 power를 알아내고, 이를 외부포트로 인가하여 자기장에 대한 영향을 확인 하였다.

RFI 에서 인가되는 sin파의 20Vpp에 주파수 400MHz를 인가하였고 modeling을 통해 ASIC에 전달되는 power가 1.7dBm인 것을 알았다. 모델링을 의해 알아낸 power를 외부 포트를 통해 ASIC에 인가 하였을 때 회로의 동장에 영향을 주는 것을 확인 하였다.

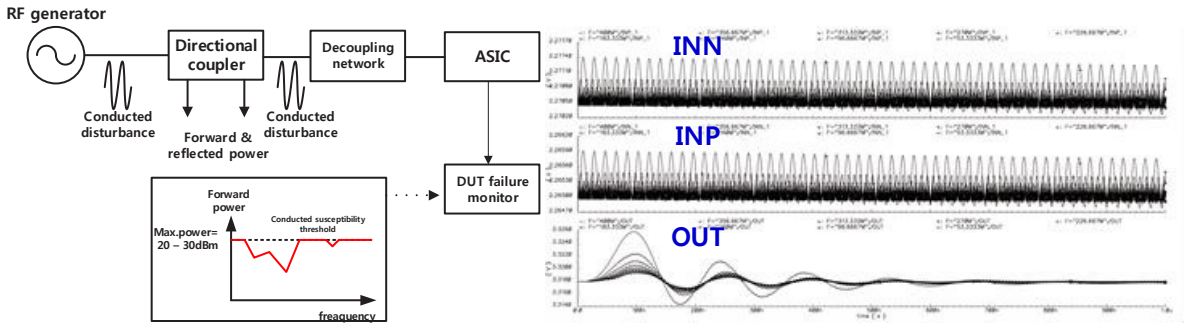

Fig 1. Modeling diagram and results

[1] Ali Alaeldine, Richard Perdriaou, Mohamed Ramdani, Jean-Luc Levant, and M'hamed Drissi, "A Direct Power Injection Model for Immunity Prediction in Integrated Circuits," IEEE TRANSATION ON ELECTRO MAGNETIC COMPATIBILITY, VOL.50, NO.1, FEBRUARY 2008

[2] 박상현, 이동수, 이강윤, “자동차 IC 용 Direct Power Injection 모델링 기법”, 2014 년도 대한전자공학회 SoC 학술대회, pp.226-227, May, 2014

Performance Improvement of On-Chip Inductor Using Novel Patterned Ground Shield Structure and Thick Metal Layer

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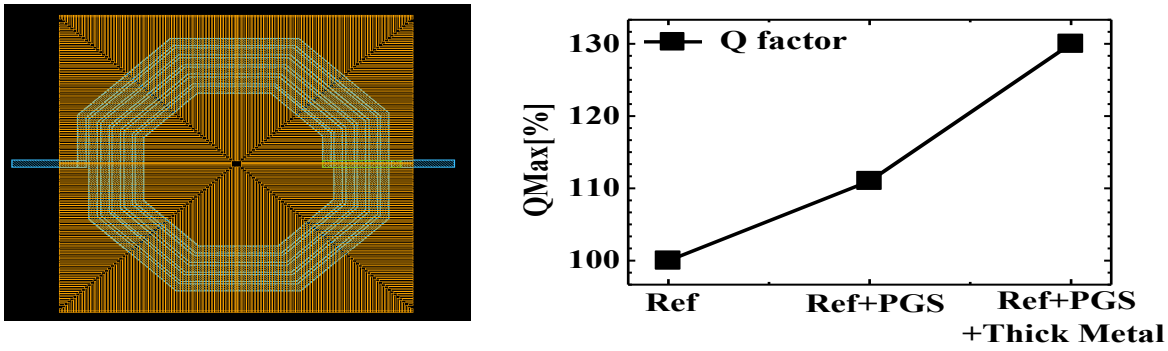
On-chip high-Q inductor is one of the key components in radio frequency integrated circuits(RFIC) design. However, Q factor of on-chip inductor is lower than that of off-chip stand-alone inductor due to the lossy silicon substrate. In order to reduce substrate losses, patterned ground shield (PGS) structure has been proposed [1], since it can prevent the capacitive coupling to the substrate.
In this paper, several PGS structures were proposed to improve the performance of on-chip inductor and one of the structure is shown in Fig. 1(a) We obtained accurate Q-factor through 'open-short-thru' three-step de-embedding method[2]. Experimental results show that Q factor of the spiral inductor increaseed about 11 % using the PSG as shown in Fig. 1(b). In addition, we increased the thinckness of the metal layer for further improvement of Q-factor as in Fig. 1(b).



(a) (b)

Fig. 1. (a) Spiral inductor with a PGS structure and (b) improvement of Q factor.

ACKNOWLEDGEMENTS

This research was financially supported by the IT R&D program of MKE/KEIT (10041855, Development of e-NVM [embedded Non-Volatile Memory] analog mixed signal-based convergence process technology & IP).

[1] C. P. Yue, and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si_Based RF IC's." IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, pp. 743-752, May 1998.

[2] M.H Cho and Y.M Teng "A Cascade Open-Short-Thru (COST) De-Embedding Method for Microwave On-Wafer Characterization and Automatic Measurement," IEICE Trans. Electron., Vol.E88−C, No.5, pp.845-850, May 2005.

Low Power, Wide Range, High Speed Digitally Controlled Ring Oscillator

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고속, 대용량의 데이터 처리를 위한 RF 대역의 송수신기의 설계에서 클럭 데이터 복원기(CDR : Clock and Data Recovery)는 필수적으로 필요한 시스템이다. 전체 시스템의 동작속도를 낮추고, 데이터 복원의 정확성을 높이기 위해선 오버샘플링 기법을 적용하게 되는데, 면적 측면에서 이득이 있기 때문에 보통 LC 발진기 보다 링 발진기 설계를 통하여 구현하게 된다[1]. 기존의 링 발진기의 경우 PVT 변화에 따른 주파수 보상을 위하여 일반적으로 커패시터 뱅크를 사용하였고 그에 따른 면적 또한 크게 늘어났다. 또한 단위 지연셀이 늘어남에 따라 전류 소모 또한 크게 늘어났다. 나아가 기존의 링 발진기는 기본적인 인버터 타입으로 구성되어 그 동작 속도가 제한적이었다. 본 논문에서는 부 스큐 지연 방식을 통하여 PMOS 의 동작 속도를 향상시키고[2], PMOS 를 통한 전류 어레이를 이용하여 전류소모량 및 면적을 크게 감소시킬 수 있는 링 DCO 를 제안한다.

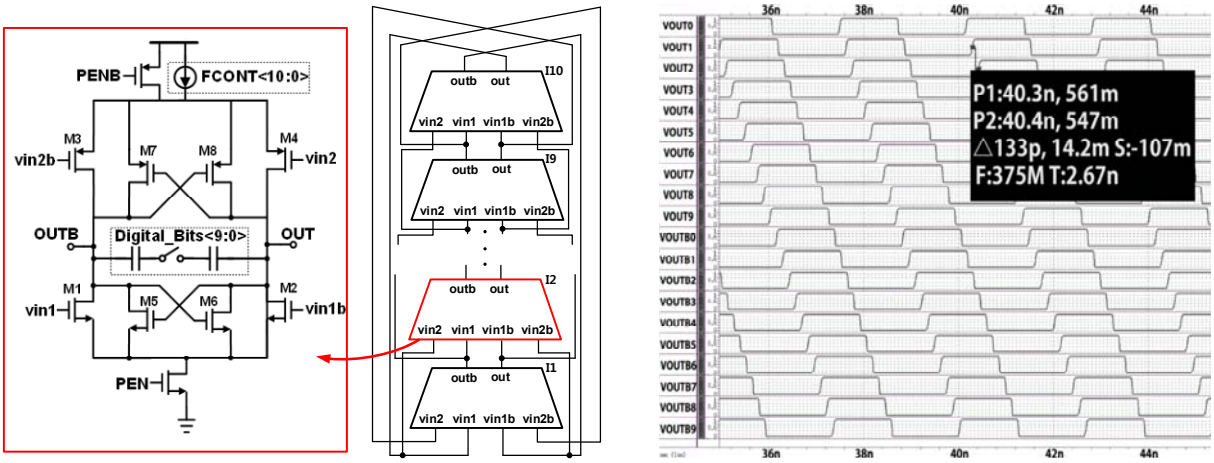

Fig 1. Schematic of proposed Ring DCO and its output waveform simulation result

[1] Marcus van Ierssel, Ali Sheikholeslami, Hirotaka Tamura and William W. Walker, "A 3.2 Gb/s CDR Using Semi-Blind Oversampling to Achieve High Jitter Tolerance," IEEE Journal of Solid-State Circuits, Vol. 42, no. 10, pp. 2224-2234, October 2007.
[2] Chan-Hong Park and Beomsup Kim, "A Low-Noise, 900-MHz VCO in 0.6um CMOS," IEEE Journal of Solid-State Circuits, Vol. 34, no. 5, pp. 586-591, May 1999.

10bit low power SAR ADC design for Multi-channel sensing

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Device 내에 사용되는 ADC 는 주로 아날로그 신호를 Sensing 하여 디지털 신호로 컨트롤하기 위하여 사용된다. Device 가 복잡해 질수록 ADC 에서 처리해야 될 신호가 많아지게 되므로, 계속 동작을 시켜야 되고 Device 내의 큰 전력 손실로 이어지게 된다. 이런 손실을 막기 위해서는 저전력 회로로 구현해야 하는데, SAR 구조의 ADC 는 저전력 구조가 가능하다. 본 논문은 듀얼 샘플링 구조와 APC 를 이용한 저전력 비교기, Multiplexer 을 통해 다채널 Sensing 이 가능한 저전력 ADC 를 구현하였다.

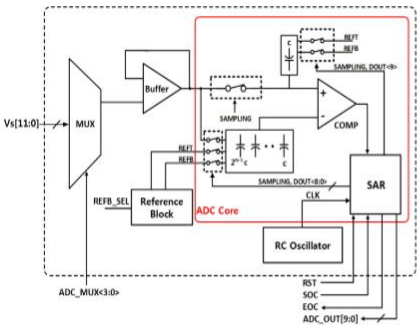

Figure 1. Block diagram of the SAR ADC

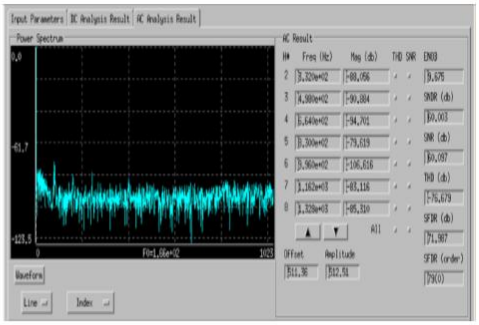

Figure 2. ADC ENOB and SNDR Simulation Result

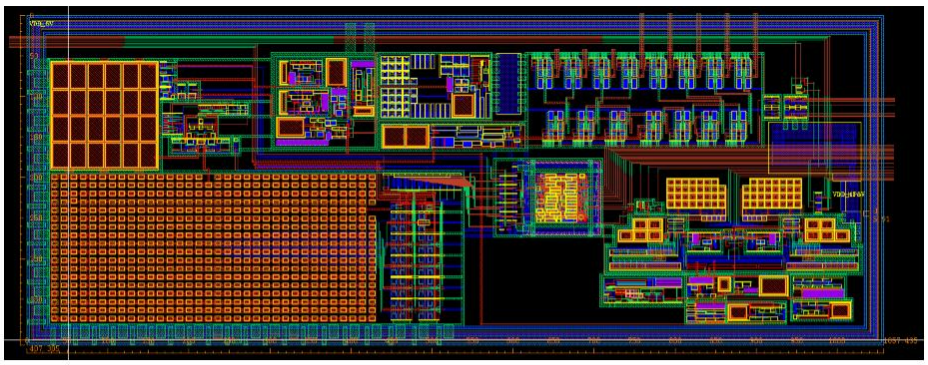

Figure 3. ADC TOP Layout

[1] Binhee Kim, Long Yan, Jerald Yoo, Namjun Cho, and Hoi-Jun Yoo, “An Energy-Efficient Dual Sampling SAR ADC with Reduced Capacitive DAC,” Circuits and Sysyems, pp. 345-357, Taipei, May 2009.

[1] Song Lan, Chao Yuan, Yvonne Y.H. Lam and Liter Siek, “An Ultra Low-Power Rail-to-Rail Comparator for ADC Designs,” Circuits and Sysyems, pp. 1-4, Taipei, Aug. 2011.

A Third Order Active Notch Filter with Process Compensation and Tunable Frequency Range for Suppressing Spurious Emission

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The industrial, scientific and medical(ISM) radio bands are radio bands reserved internationally for the use of radio frequency energy for industrial, scientific and medical purposes other than telecommunications.[1] It might makes some problem because LTE telecommunication use 1.8GHz bands, which can be second harmonic of 900MHz, industrial radio bands already reserved. Hence, it needs additional circuit for suppressing the second harmonic tone of 900MHz.

In this paper, it supposes a third order active notch filter to solve this problem. Especially, it applies compensation of varying process.

It shows the schematic of the supposed third order active notch filter in Fig. 1. If attaching inductor and capacitor series at the main signal path of pre-driver amplifier located in power amplifier. Those determine the wanted frequency for filtering. For improvement bandwidth of filter, it supplement negative transconductance to enhance Q-factor of filter. Additionally, it use varator to make the filtered frequency tuned little by little.

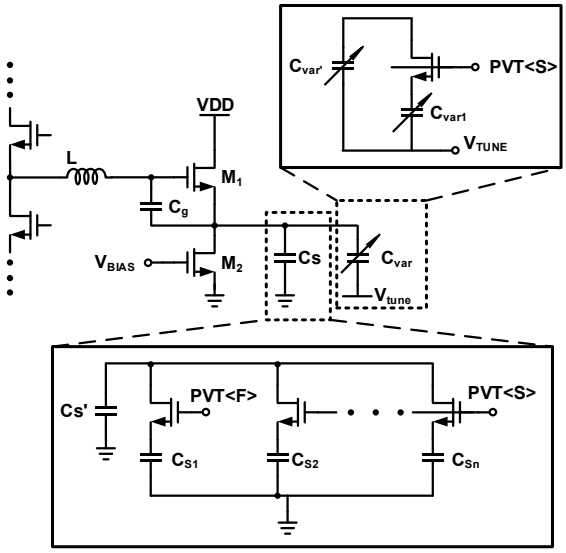

Fig 1. The Schematic of Proposed Active Notch Filter with Process Variation Compensated

[1] "ARTICLE 1 - Terms and Definitions". *life.itu.ch*. International Telecommunication Union. 19 October 2009. 1.15. "Industrial, scientific and medical (ISM) applications

Electromigration Reliability of Silver Interconnect Fabricated by Reverse Offset Printing

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Wearable devices have drawn a great attention with rising of a new era of innovation. From health monitors and fitness trackers to temperature-adjusting jackets and flying dresses, wearable technology is revolutionizing how we use our everyday electronics. These wearable devices are placed in contact with the human skin, therefore mechanical flexibility is needed. In this view, printing technology is suitable for making wearable devices. There are several printing methods such as inkjet, gravure, flexo, screen printing, offset. Among them, reverse offset printing is one of good methods that have high resolution (< 20 um) and layer thickness (< 1 um). Recently many researches are focused how to make organic products fabricated by reverse offset printing, however, research of electrical reliability have been rarely investigated. In pure metal such as Al, Cu and Ag, the ions move due to the momentum transfer between conducting electrons and diffusing metal atoms when current inducing. This transport of material is called Electromigration (EM). EM which is a current induced mass transport phenomena in the atomic level, has been identified to be one of the major causes of premature failure of interconnects in integrated circuits. It can also be a cause of reliability degradation in organic devices. Shrinkage in organic device dimensions has led to EM problems, therefore it is important to understand electrical stability of organic materials for reliability.

In this study, we investigated failure mechanism induced by electric current in organic Ag interconnect on a polyimide (PI) substrate fabricated by reverse offset printing. DC current densities of range from 1 X 10^3 to 1 X 10^6 A/cm^2 at 150 ºC were applied to a dog born shaped organic Ag samples during 96 hours. The electrical resistance was measured during the test. Microstructure changes were observed using SEM and FIB analysis.

Organic Ag samples were fabricated organic Ag ink on PI substrate with dog born shaped pattern by reverse offset printing. The sample size is approximately 20 μm x 1 mm x 0.5 μm. Samples annealed at 250℃ for 30 min in air condition.

In case of pure Ag metal sample, failure by resistance increasing usually occurred instantly at specific time under current stressing condition, however in our study organic Ag sample has an

abnormal failure mode interestingly. Gradual resistance increasing phenomenon and microstructure change were observed for the current stressing test of organic Ag samples. The changes in surface roughness measured using AFM every 24 hour from the staring of current stressing. For Ag interconnects at 1 X 10^5 A/cm^2 current stressing, arithmetic average of absolute values (R_a) of surface roughness were 6.7, 7.2, 9.4, and 11.6 pm for 24, 48, 72, and 96 hrs-tested samples, respectively. In same condition, change (%) of resistances were 5, 10, 30 and 50 % for 9, 15, 23 and 24 hrs-tested samples, respectively. For microstructure change analysis in current stressing sample, SEM observation was used. As time passed, agglomeration of Ag nano particles were accelerated with time and local deficient region were formed. Although the degree of surface roughness and microstructure change depend on current density range (10^4~10^6 A/cm^2 at 50 ºC), as a result Ag deficient regions were locally formed and they resulted in gradual changes of resistance.

EM reliability issue of organic electronic materials will be more important according to interconnect shrinkage. However there are no guidelines of EM reliability in organic electronic products. Our study is meaningful about gaining ground in this organic electronic material part.

Interconnect filling improvement by reduction of CuOx before electroplating

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The damascene process for forming copper interconnects employs physical vapor deposition (PVD) to form a diffusion barrier layer (typically a metal nitride), an adhesion layer (usually Ta), and then a conductive seed layer (Cu). A problem that arises in this process is that the Cu seed layer after PVD can readily react with oxygen in the air to form CuO and Cu_2O.[1] Subsequently, the Ta adhesion layer can rapidly oxidize. As Cu interconnect feature sizes continue to scale downwards the deposited PVD seed becomes very thin (<30 Å) along the sidewall of trenches and vias. Wafer processing queue times between PVD and electroplating can result in significant oxidation of the sidewall. Oxide formation on the sidewall can lead to void formation due to CuO_x dissolution at the start of plating processes, leading to areas of missing Cu, poor adhesion in finished interconnects resulting in voiding during thermal stress tests, and a loss of EM life associated with poor Cu adhesion to the sidewall.[2] Here, a process for reducing CuO_x to metallic Cu before electroplating on full 300 mm wafers is described.

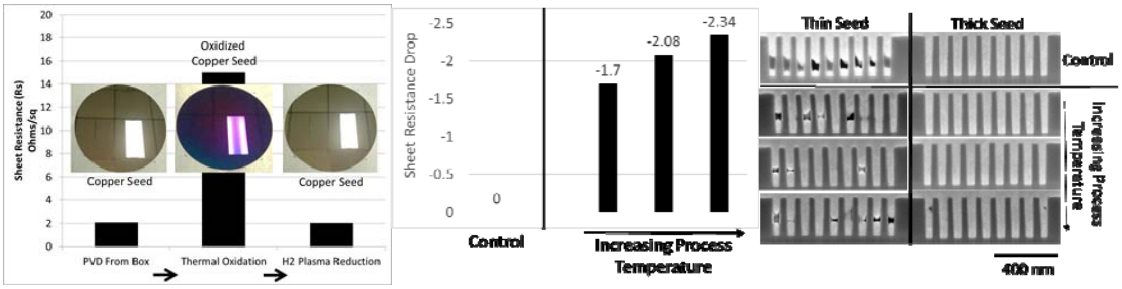

Fig.1. Remote plasma treatment impact on oxidized Cu seed appearance, sheet resistance, and fill performance.

[1] E. Apen, B.R. Rogers, and J.A. Sellers, J. Vac. Sci. Technol. A 16, 1227, 1998.
[2] H. Inui, K. Takeda, H. Kondo, K. Ishikawa, M. Sekine, H. Kano, N. Yoshida, and M. Hori, Appl. Phys. Expr. 3, 126101, 2010.
[3] Y. Sawada, H. Tamaru, M. Kogoma, M. Kawase, and K. Hashimoto, J. Phys. D: Appl. Phys. 29, 2539, 1996.

메모리 소자용 금속배선의 배선간 접합 변화가 일렉트로마이그레이션 신뢰성에 미치는 영향

장경태 [a], 박용진 [a], 정민우 [a], 임승민 [a], 연한울 [a], 조주영 [a], 신진섭 [b], 우병욱 [b], 배장용 [b], 황유철 [b], 주영창 [a,*]

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반도체 소자의 고집적화로 배선 폭이 미세화 되고, 소자의 작동 전류 밀도는 점차 가혹한 환경으로 증가하게 된다. 이에 따라서 높은 전류밀도에 의해 배선이 파괴되는 일렉트로마이그레이션(EM) 현상이 중요한 신뢰성 문제로 대두 되고 있다. 현재 메모리 배선에서는 Al, Cu, 및 W 물질이 동시에 사용 되고 있고, 배선 구조에 따라 금속물질의 접합관계도 다양하다. 그러므로 금속배선간 접합 변화에 따른 EM 현상을 관찰하고 메커니즘 분석을 통해서 EM 신뢰성에 가장 취약한 부위를 찾아내는 연구가 필수적으로 요구된다. 본 연구에서는 Al, Cu 및 W 으로 구성된 다양한 배선 접합구조에서 EM 현상을 관찰하였다 [Fig. 1(a)]. Figure 2(b)는 metal 1: Cu, metal 2: Al, 및 W via 로 구성된 배선에서 전류방향 차이에 따른 EM 결과를 나타낸다. 전류방향이 donwstream 인 경우 upstream 조건보다 더 가혹한 스트레스 환경에서도 EM 수명이 비슷했다. 또한 저항증가추이도 upstream 의 경우에는 급격히 증가하는 반면, downstream 의 경우에는 계단식으로 저항이 증가함을 보였다. 이는 upstream 의 경우에는 Al 배선에서 EM 이 발생하고, downstream 의 경우에는 EM 저항성이 Al 보다 상대적으로 큰 Cu 배선에서 일어나기 때문이다. 또한 Cu 배선의 Ta/TaN 배리어 효과로 인해서 저항이 급격히 변화하지 않는다고 판단할 수 있다. 본 연구에서는 Al/W/Cu 배선 뿐만 아니라 Cu 로만 이뤄진 배선, Cu/W/W 구조의 배선에서의 EM 거동에 대해서 논의할 예정이다.

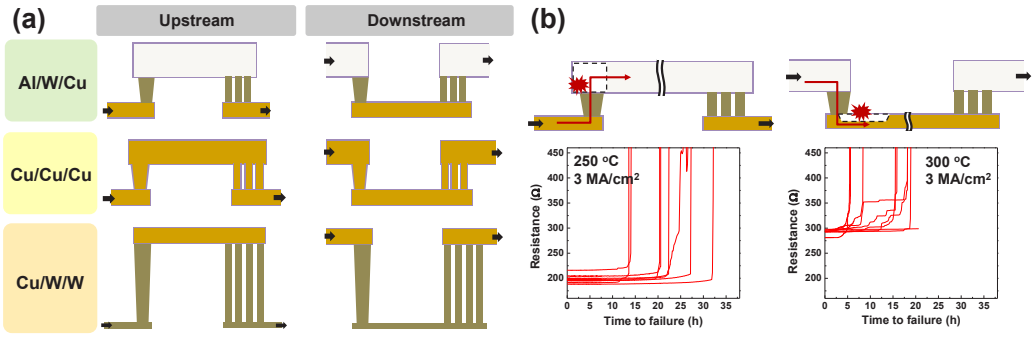

Fig 1. (a) Schematics of interconnects for EM test, (b) EM failures at Al/W/Cu interconnects

The effects on the formation process and Schottky barrier height of ytterbium silicide by alloying with molybdenum

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As the scale-down of complementary metal-oxide-semiconductor field-effect-transistors (CMOSFETs) continues, the contribution of the source/drain resistance becomes significant, which makes it a critical issue to find a novel contact formation scheme with low source/drain series/contact resistances [1]. Rare-earth metal (Er, Yb, etc) silicides have been noticed as a promising candidate for n-type channel transistors owing their low Schottky barrier heights on n-type Si (0.27-0.4eV) [2]. First, we studied the ytterbium silicide as a contact material. The ytterbium was deposited using RF magnetron sputtering system and annealed using RTA to form ytterbium silicide. The materials reactions have been studied by transmission electron microscopy (TEM), X-ray diffraction (XRD). In addition, the electrical characteristics of the diodes were measured using an HP semiconductor parameter analyzer (HP4145B). For Yb/Si sample, the epitaxial Yb silicide layer formed as a flat layer of a uniform thickness with epitaxial relation with the underlying Si lattice. This epitaxial silicide layer led to low Schottky barrier height (SBH). However, oxidation of Yb silicide degraded the contact properties at high temperatures. To mitigate the oxidation problem, we examined further the possibility of using Yb alloyed with Mo. For Mo-alloyed Yb/Si sample, epitaxial Yb layer remained up to 800°C because Mo-segregated region above Yb silicide fended off the oxygen diffusion. Also, SBH was kept low up to a temperature as high as 800°C.

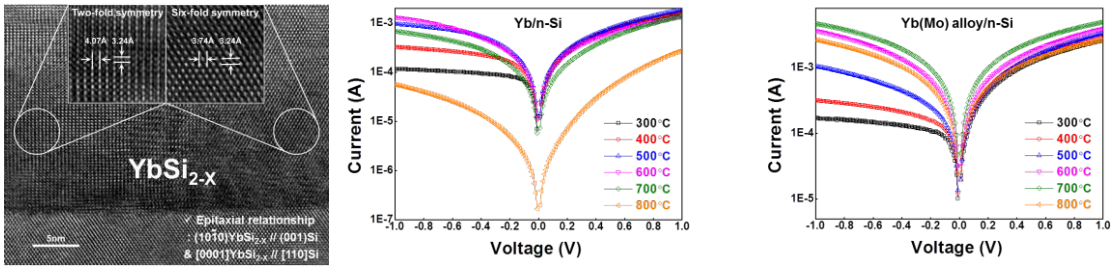

Fig 1. HRTEM image of epitaxial $YbSi_{2-X}$, I-V curves of Yb/Si and Yb(Mo) alloy/Si

[1] Z.-W. Zheng, T.-C. Ku, M. Liu, and A. Chin, Appl. Phys. Lett., 101, 223501 (2012).
[2] S. Zhu, J. Chen, M.-F. Li, S. J. Lee, J. Singh, C. X. Zhu, A. Du, C. H. Tung, A. Chin, and D. L. Kwong, IEEE Electron Device Lett., vol. 25, No. 8, pp.565-567 (2004).

Schottky Barrier Engineering in Ti/TiO_2 Metal-Insulator-Silicon Contact

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Contact resistance (R_{co}) becomes a dominant component in a whole transistor resistance, therefore R_{co} reduction becomes crucial for transistor performance. Recently, a metal insulator semiconductor (MIS) contact attracts much attention, because MIS contact can decrease Schottky barrier height (SBH), hence providing a low contact resistivity [1]. Among insulators, TiO_2 is considered promising due to the low conduction band offset of TiO_2 to Si or Ge [2]. In this study, we demonstrated nearly zero of n-SBH and low contact resistivity by Ti/TiO_2 MIS contact on n-Si.

Fig.1 (a) shows n-SBH dependence on annealing temperature (H < I < J) at 3 different TiO_2 thicknesses, A < B < C. From Fig.1 (a), thicker TiO_2 and lower thermal budget are preferable for attaining low n-SBH. From Fig.1 (b), Ti thickness F without annealing or with temperature H gives nearly zero n-SBH, however, n-SBH increases as increasing annealing temperature. We consider that intermixing Ti and TiO_2 degrades n-SBH of Ti/TiO_2 MIS contact. Therefore, thicker TiO_2, thinner Ti and lower annealing temperature are preferable for achieving low n-SBH. However, in the case of G as Ti thickness, Ti thickness is too thin to protect TiO_2 from nitridation of TiN deposition. Finally, a contact resistivity of Ti/TiO_2 MIS contact is measured by four terminal Kelvin structure, which provides high reliable measurement value. From our experiments, we achieved contact resistivity of Ti/TiO_2 MIS as low as $1.5x10^{-8}$ Ω-cm^2, which is the lowest value of MIS contact on n-Si with Kelvin structure.

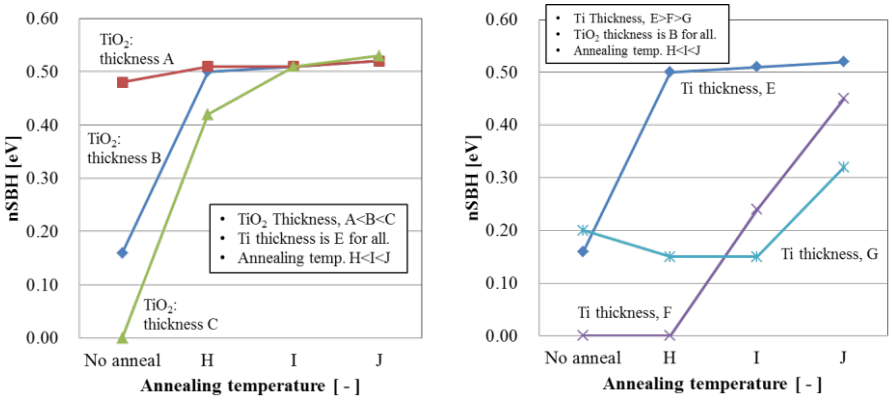

Fig. 1 n-SBH dependence on annealing temperature with different (a) TiO_2 or (b) Ti thicknesses.

[1]M. Kobayashi et al. *J. Appl. Phys.* 105, p. 023702 (2009)
[2] A. M. Roy *Ph.D thesis* Stanford University (2012)

Improvement in mechanical properties and reliability of porous low-k through novel UV cure process

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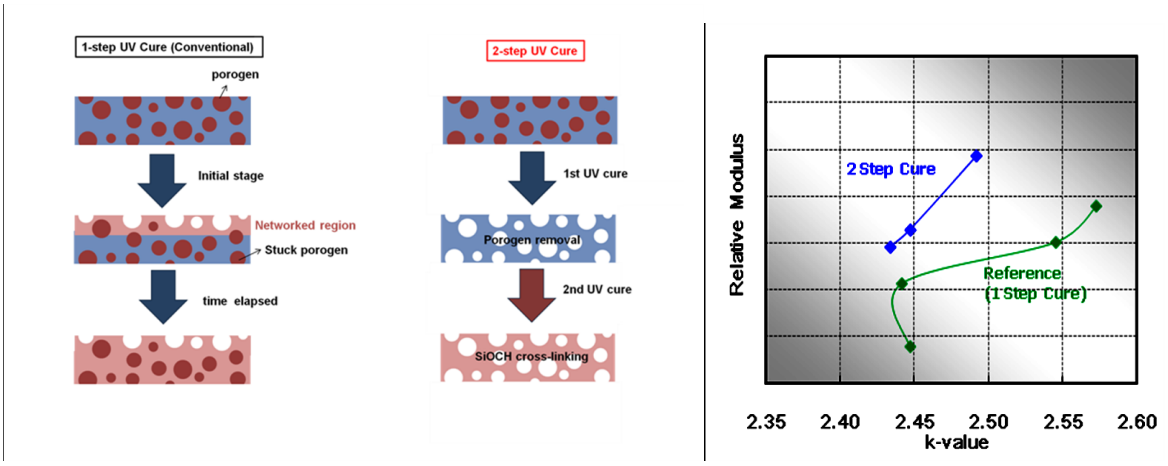
As the RC delay and crosstalk of the interconnects emerge as the prime limiting factors for further scaling of logic devices to 20 nm and beyond, porous low-k dielectrics has been introduced as inter-metal dielectrics. However, poor mechanical properties of porous low-k materials have raised significant reliability concerns such as electromigration and time-dependent dielectric breakdown (TDDB). In this study, a novel UV cure process was developed to remove porogen from ULK and cross-link ULK sequentially. This 2-step UV process enhanced the elastic modulus more than 30% without compromising the dielectric constant. The resultant improvements of TDDB and EM lifetime, evaluated using the 80 nm-pitch metal lines, were attributed to efficient porogen removal and high degree of cross-linking of porous low-k.



(a) (b)

Fig 1. Comparison of conventional UV Cure and 2step UV cure process: (a) schematic description of processes and (b) dielectric constant and mechanical property (elastic modulus).

Multi-Channel Incremental Delta-Sigma ADC for Multi-Sensor Application

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This paper presents a multi-channel incremental delta-sigma (IΔΣ) analog-to-digital converter (ADC) for multi-sensor application. In the conventional ΔΣ ADC, it is impossible to multiplex the input, because output is the serial bit-stream. Thus, multi-channel ADC cannot be designed by using the conventional ΔΣ ADC. The proposed IΔΣ is operating only clock period of N cycle, which was already determined, and then give a reset pulse to initialize the each integrator and decimation filter so that erase the stored data and quantization error component. As the result, it can convert a new sample for every reset period, and it means that the input multiplexing is possible. In this paper, design is aiming for the sensor applications, IΔΣ ADC target is focused on low-power consumption. For these reason, the order of ΔΣ loop filter is chosen to 2nd order and to satisfy its linearity, 1-bit quantizer is the most suitable. Due to the integrator output dynamic range, this paper proposed the single-loop feed-forward structure so that reduce the output swing of integrator. The proposed IΔΣ was fabricated in a standard 0.13 um CMOS process and it has an active area of 0.22 mm^2. The ADC draws 70.8 uA from a 1.2 V supply. This work achieves the peak SNDR of 87.3 dB at the maximum sampling rate of 512 kHz.

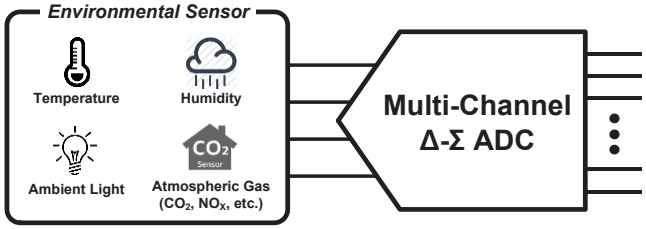
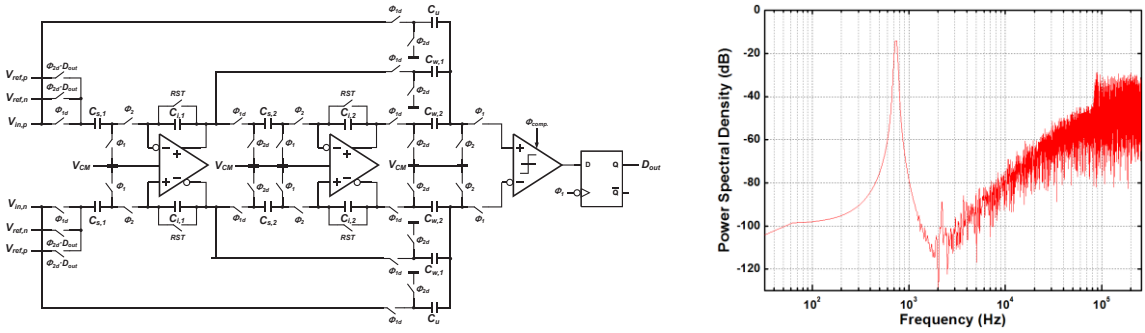


Fig 1. Multi-input sensing scheme by using single ADC.



(a) (b)

Fig 2. (a) Overall schematic and (b) output spectrum of IΔΣ modulator.

A 10-bit single-ended SAR ADC for multiple-channel neural recording system

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Concurrent neural recording without data loss across a large cortical area is an important step in analysing the functioning of the brain (EEG), the heart (ECG) and the muscles (EMG). This requires the developments of multiple-channel neural recording system which performing concurrent recording of neuropotentials over a large number of electrodes from the brain and the body [1]. In these systems, low-power operation is required to prolong the battery life and to avoid tissue damage by overheating. Furthermore, the small-area design is also essential for the large number of channels. A new multiple-channel 10-bit SAR ADC is proposed to promote multiplexing between channels, thus eliminates the disadvantages of offset mismatch owing to multiple comparators and load mismatch between comparator inputs in digital multiplexing scheme. It is composed of multiple S/H and a capacitive-DAC (CDAC), single comparator, a SAR logic as shown in Fig. 1. The proposed ADC reduces the total capacitance and switching energy of capacitive-array by 85.1% compared with the digital multiplexing scheme [2] without offset mismatch between multiple comparators.

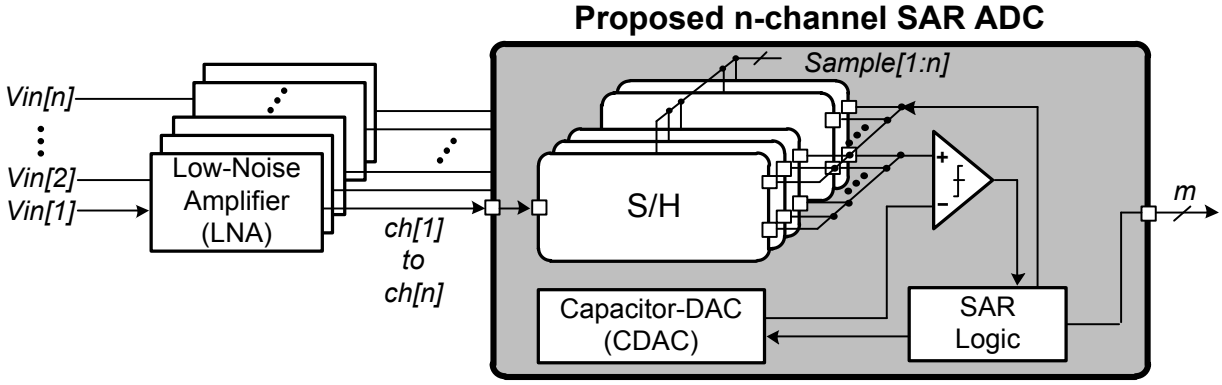

Fig 1: Block diagram of multiple-channel system with the proposed n-channel SAR ADC

[1] T. Roh, K. Song, H. Cho, D. Shin, U. Ha, K. Lee, H.-J. Yoo, ISSCC Dig. Tech. Papers, pp. 318-319 (2014).
[2] W.-S. Liew, X. Zou and Y. Lian, in proceedings of the ESSCIRC, pp. 219-222 (2011).

A 3.8 MHz Wien-Bridge Oscillator with Capacitive Automatic Amplitude Control in 0.35μm CMOS

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One of key requirements of the wireless sensor network(WSN) is ultra low power(ULP) operation with small size and extremely low cost. To satisfy these requirements, Bulky off-chip components need to be removed[1]. As an effort for this, there is a growing interest in implementing on-chip reference clock generators operating at a few MHZ with low power consumptions.

In this paper, 3.8 MHz Wien-bridge oscillator with capacitive automatic amplitude control (AAC) is presented. In deep-submicron processes, passive device are much more predictable and controllable than active device. Wien-bridge oscillator for which the oscillation frequency is determined by resistor and capacitor is suitable candidate to generate such reference clocks. However, with PVT variation, the fabricated oscillator would not oscillate ever or carry a highly distorted waveform with off-target output frequency.

In this work, the non-inverting gain of the opamp stage is controlled by using a linear MOS capacitor instead of a more conventional but less linear MOS variable resistor. And the capacitance is controlled by AAC. According to control closed –loop gain, nonlinearity of oscillator is increased. Fabricated in 0.35 μm CMOS, the oscillator draws 170 μA from 2 V supply. The oscillation frequency and amplitude is 3.8 MHz and 450 mV, respectively. Second harmonic distortion is as low as -20.2 dBc.

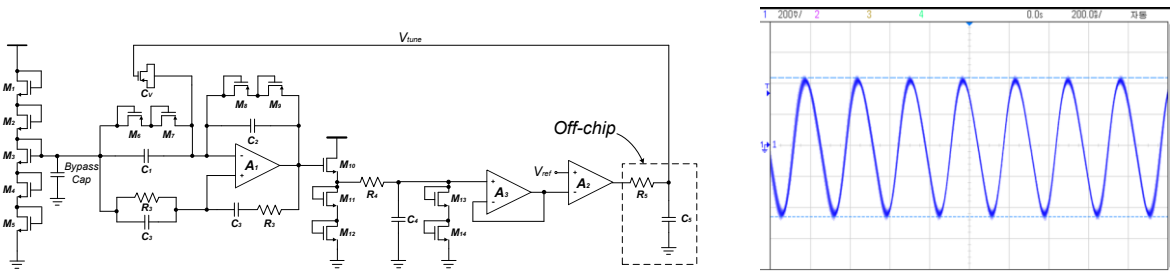

Fig 1. Proposed Wien-bridge oscillator and its measured data

[1] S. Drago, F. Sebastiano, and L. J. Breems, D. Leenaerts, K. Makinwa, and B. Nauta, “Impulse-based scheme for crystal-less ULP radios,”IEEE Tran. Circuits and System-I, pp. 1041-1052, May 2009.

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A 12b 1.25MS/s SAR ADC Using Dual Sampling Technique and Low Switching Energy Technique

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This paper describes a successive approximation register (SAR) type 12-b analog-to-digital converter (ADC) for DMPPT control in photovoltaic (PV) system in a 0.35μm BCDMOS technology**.** A dual sampling technique and a new low switching-energy technique are used for the digital-to-analog converter (DAC). With these techniques, we can implement a 12-b SAR ADC with 10-b DAC. The proposed ADC implemented with the differential DAC by receiving the single input PV signal. Figure 1-(a) shows the single-to-differential DAC which adopts dual sampling technique. Since only one switch is activated in each conversion, switching energy is reduced. Figure 1-(b) shows conceptual diagram of this low switching-energy technique with 3b DAC that uses just one quarter of capacitors compared to conventional 3b DAC. The simulation results show that the proposed ADC achieved the SNDR of 70.75 dB, the SFDR of 83.28dB, and the ENOB (effective number of bits) of 11.46 bits. The power consumption including all the circuits is 115μW at the sampling frequency of 1.25MHz under 3.3V supply voltage and the FoM (figure of merit) is 32.68fJ/conv. The chip area is 600μm×935.5μm excluding pads.

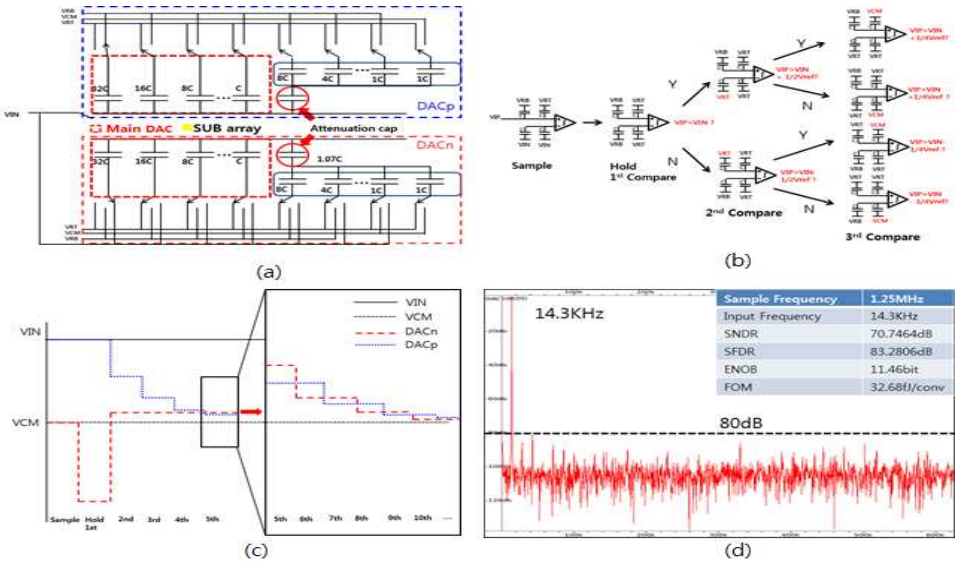

Fig. 1 (a) Proposed DAC Schematic, (b) Switching process of 3b SAR ADC
(c) Conversion Process (d) FFT Simulation Results

A 0.6V 1.17ps PVT Tolerant and Synthesizable Time-to-Digital Converter using a Stochastic Phase Interpolation in 14nm FinFET Technology

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A time-to-digital converter (TDC) is a key element for the digitalization of timing information in modern mixed-signal circuits such as digital PLLs, DLLs, and ADCs. For the purpose of achieving a high resolution TDC, many researches have usually focused on minimizing unit delay of the quantization [1][2]. However, its performance, however, is limited by delay variation and random mismatch among delay cells unless additional calibration circuits or external controls are accompanied. Hence it not only tends to be power hungry but also requires very sophisticated layout.

We presented a very simple, low power and synthesizable TDC architecture without any calibrations using a stochastic phase interpolation technique with 16x spatial redundancy. The measured time resolution of the TDC is 1.17ps with 0.8 LSB of DNL and 2.3 LSB of INL even under severely varying PVT conditions. It consumes only 0.78mW of power under 0.6V supply for 100MS/s input. The proposed TDC achieves the most competitive performance in FoM point of view [3] (4-fold improvement over state of the art level).

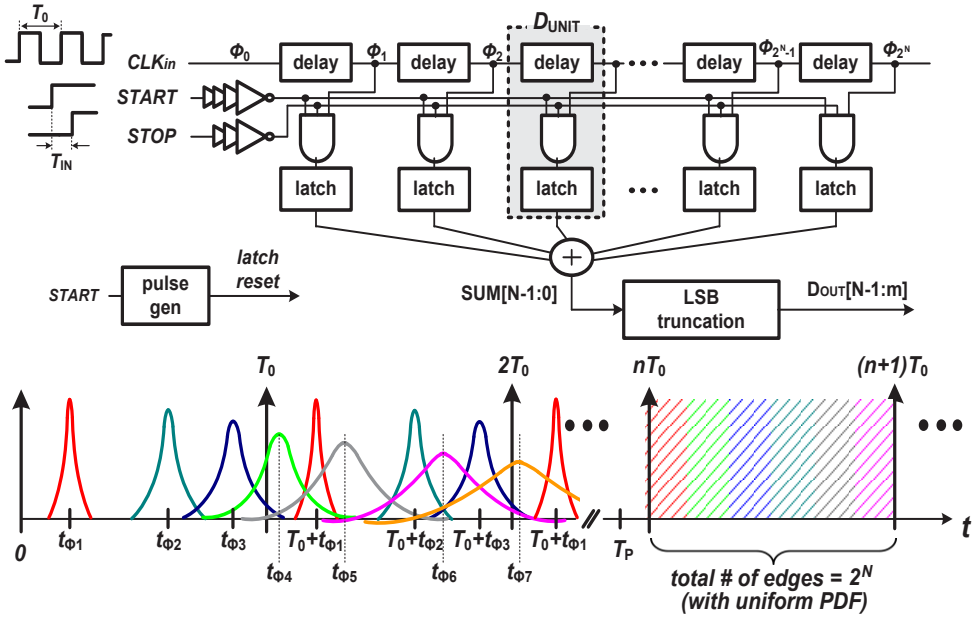

Fig. 1. The proposed synthesizable TDC using stochastic phase interpolation.

[1] L. Vercesi, A. Liscidini, and et al, *IEEE J. Solid-State Circuits,"* Vol. 45, no. 8, pp. 1504-1512, Aug 2010.

[2] S.-J. Kim, T. Kim, and et al, *IEEE Int. Symp. VLSI Circuits Dig.*, 2014.

변이 적응성과 에너지 효율성을 갖는 NEM(Nano ElectroMechanical) 릴레이 전하펌프

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본 논문에서는 무선 센서에 사용하기 위한 NEM 릴레이를 사용한 전하 펌프 회로를 제안하였다. 이 회로는 전하 펌프의 스위칭 전압을 감소시켜 전력 효율을 증가시켰다. NEM 릴레이의 동작 전압은 공정변수에 민감하기 때문에 정확한 동작을 보장하는 것이 어렵다[1]. 일반적인 NEM 릴레이로 만든 전하 펌프 회로는 정확한 동작을 보장하기 위해서 동작전압보다 높은 전압을 사용하여 불필요한 전력 손실을 야기한다[2]. NEM 릴레이의 정확한 pull out 전압을 생성하는 회로를 사용하여 스위칭 전압의 크기를 줄여 스위칭 전력 손실을 줄이도록 구현하였다. 이를 입증하기 위해, 동작전압에 큰 영향을 주는 공정변수를 ±10%의 변화를 주어 몬테카를로 시뮬레이션을 하였다. 그 결과, 스위칭 전력손실은 평균 112.5uW(일반적인 회로), 평균 40uW(제안한 회로) 이다. 스위칭 전력 손실은 평균 64.4%로 감소하였다. 전체 전력 효율을 비교한 결과 62.8%(일반적인 회로), 73.8%(제안한 회로)로 평균 11% 증가하였다

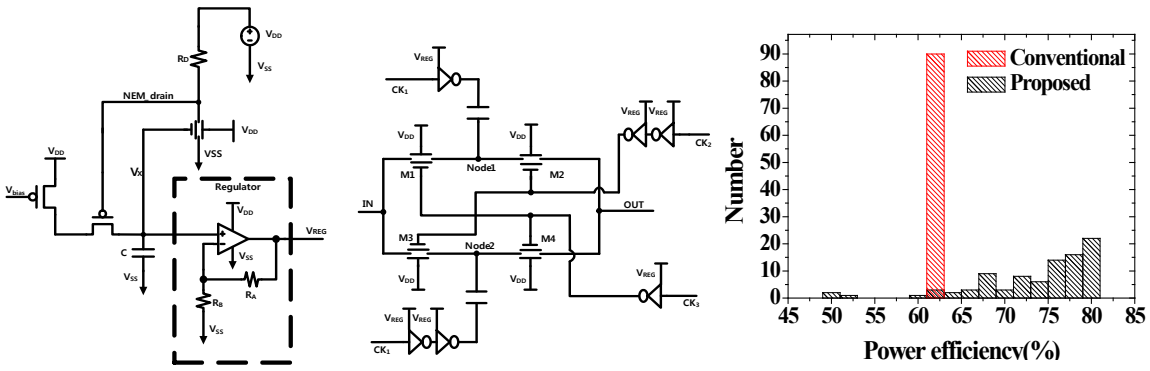

Fig 1. Proposed circuit and power efficiency result

The work was financially supported by NRF-2011-220-D00089, NRD-2011-0030228, NRF-2013K1A3A1A25038533, NRF-2013R1A1A2A10064812, and BK Plus with the Educational Research Team for Creative Engineers on Material-Device-Circuit Co-Design (Grant No: 22A20130000042), funded by the National Research Foundation of Korea(NRF), and by Global Scholarship Program for Foreign Graduate Students at Kookmin Univ. The CAD tools were supported by IC Design Education Center(IDEC), Daejeon, Korea.

[1] M. Spencer et al., IEEE Journal of Solid-State Circuits, 46, 1 (2011).

[2] Venkatasubramanian, R et al., IEEE transaction on Nanotechnology, 12, 386 (2009).

Large-signal simulation of plasma instability in 2-dimensional electron gas

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For the simulation of the plasma instability in 2-dimensional electron gas [1], long simulation time required to obtain the large-signal (LS) solution is one of the serious practical difficulties. Since the velocity of the plasmonic wave inside the 2-dimensional channel is very high, the time step in a transient simulation cannot be increased without sacrificing the simulation accuracy. Inspired by the previous works on the LS simulation of the LC oscillator [2], the LS solution of the oscillating variables in the 2-dimensional channel is obtained. In this work, a simplified channel model of the high electron mobility transistor (HEMT) [1] is numerically implemented. After an initial transient simulation, the oscillation period is estimated. Starting from the estimated value, the finite difference method is adopted in order to find the actual oscillation period. When compared to the conventional transient simulation, the perfect periodicity of the solution variables was obtained. Fig. 1(a) shows the LS drain voltage oscillation in THz frequency range for the HEMT with channel length of 100nm, for various Mach numbers. The Mach number is given as the ratio of the electron drift velocity to the plasma velocity. Fig.1(b) shows the peak-to-peak amplitude and the oscillation frequency of the drain voltage as a function of the Mach number.

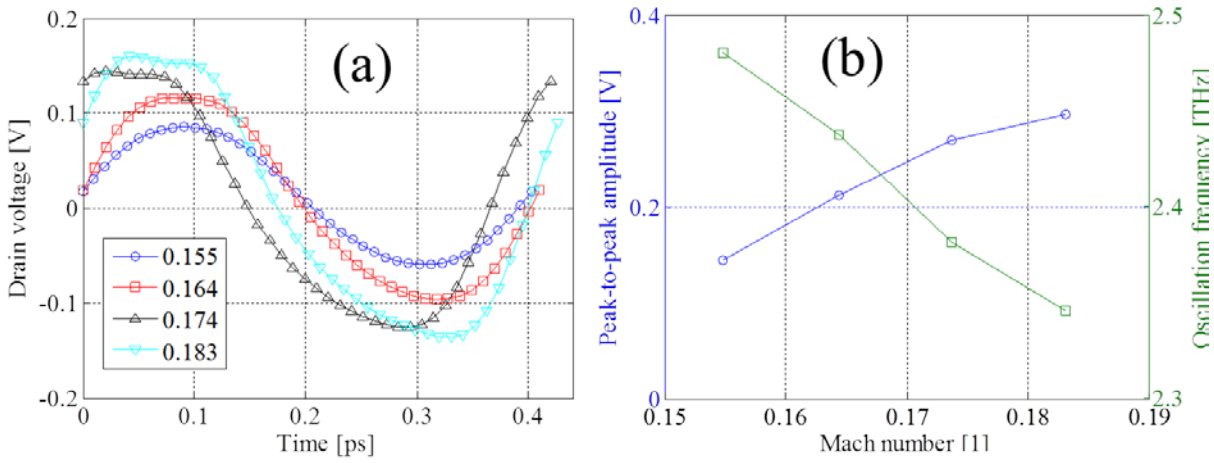

Figure 1. (a) Simulated LS drain voltage oscillation for various Mach numbers (0.155~0.183)

(b) Peak-to-peak amplitude and the oscillation frequency of the drain voltage as a function of the Mach number

Acknowledgment: This research was supported by the Samsung Research Funding Center for Future Technology.

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[2] S.-M Hong et al., IEEE TED, **53**, 2195-2201 (2006)

Voltage-Dependent SPICE Modeling for Gate-Drain Overlap Capacitance in RF MOSFETs

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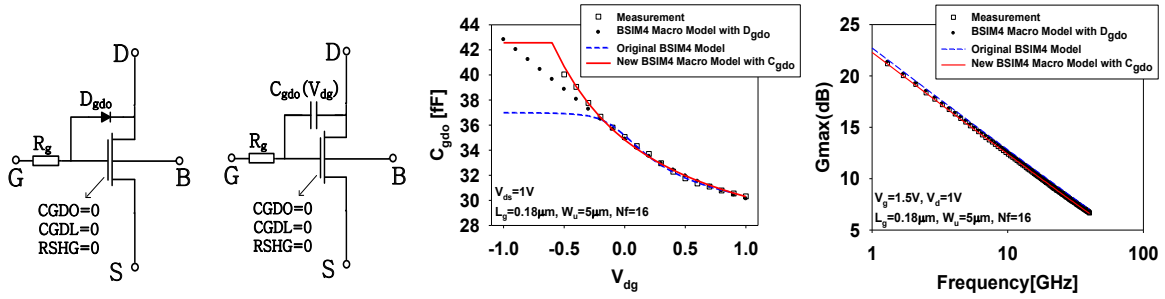
For accurate SPICE compact modeling of RF MOSFETs, the gate-drain overlap capacitance C_{gdo} is a very important parameter. In the original BSIM4 [1], C_{gdo} is unable to be modeled at $V_{dg}(=V_{ds}-V_{gs}) < 0V$. In order to improve the BSIM4, the macro model adding the junction diode D_{gdo} [2] has been used for N-MOSFET in Fig. 1(a), but it does not work in the linear region of $V_{dg} < -V_{th}$ because D_{gdo} turns on. In this study, to remove the problems of the conventional models, a new macro BSIM4 model with the voltage-dependent capacitance of $C_{gdo}=[(C_{OLD}C_{de})/(C_{OLD}+C_{de})]+C_{pgd}$ for the parasitic MOS structure in the gate-drain overlap LDD region is proposed in Fig. 1(b). The surface depletion capacitance C_{de} in the drain LDD region is modeled as $C_O[1-(V_{dg}/V_{fbo})]^{-M}$ for $V_{dg} > V_{fbo}$, where C_O, M and the flat-band voltage V_{fbo} are extracted by fitting C_{gdo} data at $V_{dg} > V_{fbo}$. The parasitic gate-drain capacitance C_{pgd} occuring to the exterior of LDD region is extracted by fitting C_{gdo} data at very high V_{dg}. The oxide capacitance C_{OLD} over the drain overlap region is directly determined by extracting the oxide capacitance per unit area and drain overlap length. Unlike the conventional models, the new C_{gdo} equation is able to accurately model C-V characteristics at full bias region in Fig. 1(c). This new model is verified by observing the better agreement to the measured power gain vs. frequency than that of the original BSIM4 in Fig. 1(d).



(a) (b) (c) (d)

Fig. 1. (a) Conventional macro BSIM4 with D_{gdo}, (b) New macro BSIM4 model with C_{gdo}, (c) Measured and modeled C_{gdo} vs. V_{dg} curves, (d) Measured and modeled power gain vs. frequency.

[1] BSIM4.6.0 MOSFET Model Manual, U. C. Berkeley, 2006.
[2] S. Lee, C. S. Kim, H.-K. Yu, Telecommunication Review, vol. 12, no. 1, pp. 130-137, 2002.

Physical Modeling and Analysis for Performance Enhancement of Terahertz Wave Detector based on Silicon Field-Effect Transistor

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Recently, terahertz (THz) wave detection has been attracted for various applications such as real-time imaging system for security and remote sensing [1]. However, many researches with the simplified device structure show a lack of physical models for the advanced field-effect transistor (FET) behaviors with the structural design variations. In this work, we present the modeling and simulation results for the physical analysis of the photoresponse (Δu) enhancement according to the gate oxide (t_{ox}) scaling in silicon (Si) FETs by using our technology computer-aided design (TCAD)-based simulation platform with quasi-plasma 2-dimensional electron gas (2DEG) model (Fig. 1) [2]. Figure 2 shows the electron density contour plots for extracting the quasi-plasma 2DEG length (l_{QP}) and density (N_{QP}), which are key parameters for investigating effects about Δu, by using Synopsys^{TM} *Sentaurus* TCAD framework. In order to compare the Δu by increased N_{QP} and fixed l_{QP} as t_{ox} scaling down, Fig. 3 shows simulation results of the Δu, which have been normalized by maximum value near $V_g = V_{th}$ with arbitrary unit, as a function of V_g with various t_{ox}. In terms of N_{QP} as electron density of average (l_{QP}= 80 nm) in channel surface, In accordance with the simplified theory of the non-resonant plasmonic wave THz detector, as t_{ox} scaled down from 4 to 1.1 nm, the higher Δu (about 63.4 percent) has been obtained in the sub-threshold region.

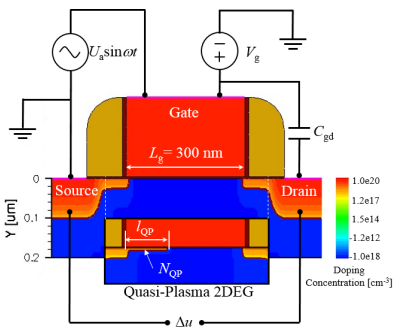

Fig. 1. THz detector structure and simulation framework based on Si FET. Inset shows the quasi-plasma 2DEG modeling by N_{QP} and l_{QP}.

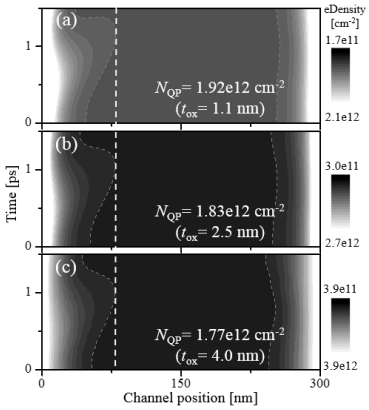

Fig. 2. Contour plots of the channel electron density modulation along with the channel position at the same gate overdrive voltage V_g- V_{th}= 0.

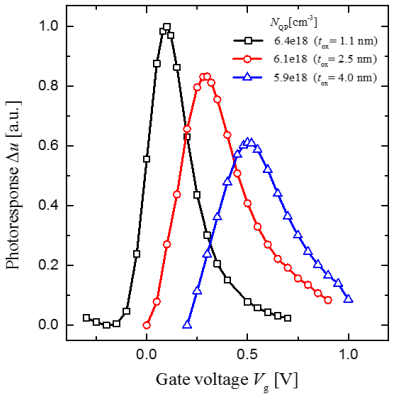

Fig. 3. The simulation results as a function of V_g according to the variation t_{ox} (= 1.1, 2.5, and 4 nm) by incorporating the quasi-plasma 2DEG into channel region.

[1] P. H. Siegel, *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 3, pp. 910-928, (2002)
[2] M. W. Ryu, *et. al, J. Semicond. Technol. Sci.* vol. 13, no. 6, pp. 576-580, (2013)

Intrinsic Output Equivalent Circuit Modeling for RF MOSFETs

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The intrinsic output equivalent circuit of most MOSFET models [1-3] used in general has only one resistance r_{ds} that is the DC drain-source resistance due to the channel length modulation in the saturation region. Thus, it is unable to model the frequency-dependent characteristics of intrinsic effective drain-source capacitance $(1/\omega)\mathrm{Im}(Y^i_{22}+Y^i_{12})$ and drain-source conductance $\mathrm{Re}(Y^i_{22}+Y^i_{12})$ exhibiting a larger variation with decreasing L_g in Figs. 1 and 2. Therefore, in this study, the physically acceptable intrinsic output equivalent circuit is proposed to model the frequency dependent characteristics accurately. In order to simulate the decrease of $(1/\omega)\mathrm{Im}(Y^i_{22}+Y^i_{12})$ as well as the increase of $\mathrm{Re}(Y^i_{22}+Y^i_{12})$ with the frequency simultaneously, the new resistance of r_{ch} should be connected in series with C_{ds} as shown in Fig. 3. According to a device structure in Fig. 4, r_{ch} clearly indicates the channel resistance existing in the inversion layer in the saturation region. The r_{ch} is physically verified by observing the linear dependence with L_g in Fig. 5. In Fig. 6, the new model in Fig. 3 has been demonstrated by observing the much better agreement upto 40GHz between the measured and modeled data of Y_{22}-parameter than the conventional one without r_{ch}.

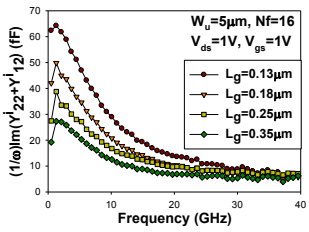

Fig. 1. $(1/\omega)\mathrm{Im}(Y^i_{22}+Y^i_{12})$ data.

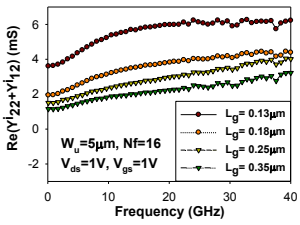

Fig. 2. $\mathrm{Re}(Y^i_{22}+Y^i_{12})$ data

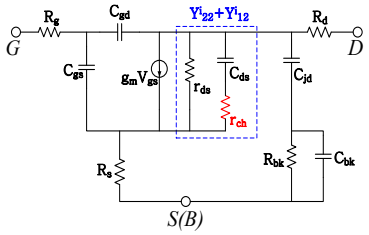

Fig. 3. New MOSFET model

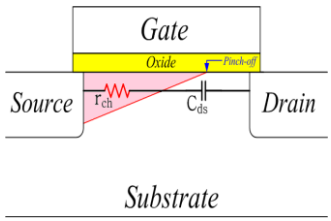

Fig. 4. MOSFET cross-section

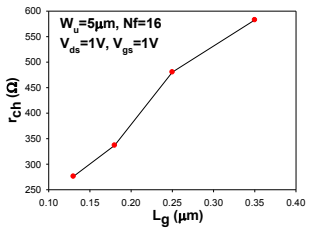

Fig. 5. Extracted r_{ch} values

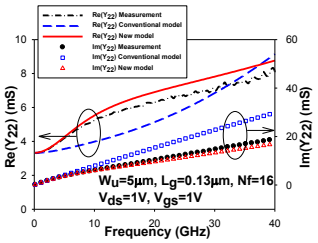

Fig. 6. Modeled & measured data

[1] Y. J. Chan et al., IEEE Trans. Electron Devices, vol. 46, pp. 611-615, (1998).
[2] S. Lee, Microwave and Optical Technology Lett., vol. 39, pp. 344-347, (2003).
[3] S. Lee, Electron. Lett., vol. 41 no. 24, pp. 1325-1327, (2005).

Amplification of electromagnetic waves in InAlN/AlN/GaN grating structures

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There are growing interests in terahertz emitters to bridge the terahertz gap (0.1-10 THz) that lies between infrared and microwave bands. Medical imaging, security, and non-destructive product -defects detection are new application areas for terahertz emitters.[1-4] Previously, there were works on grating structures on top of devices to realize terahertz emitters. Due to the large difference of resonance peaks between a metal grating structure and a two dimensional electron gas (2DEG) in the high-electron mobility transistor (HEMT), it was shown that the quantum-wire grating is more suitable for the emitter application. [5] In this work, we propose quantum-wire grating structure with 2DEG based on double-channel GaN HEMTs and numerically investigate a semiconductor-based grating, which consists of the InAlN/AlN/GaN heterostructure. The sheet carrier density in the grating can be modulated by changing the thickness of the InAlN layer (Fig. 1(a)). The transmission coefficient of the electromagnetic wave is also calculated following the model in [5], when the grating is placed on top of a 2DEG (Fig. 1(b)). The proposed grating can reduce the difference of resonance peaks between the grating and the underlying 2DEG, to enable the amplification of the incident electromagnetic wave.

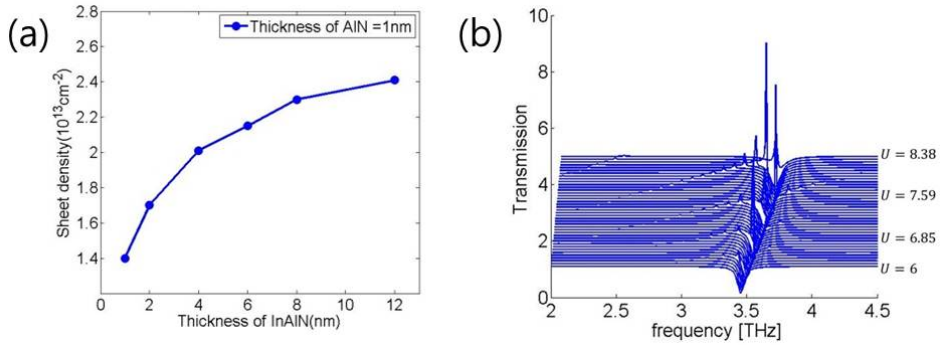

Figure 1. (a) Calculated sheet density as a function of the InAlN barrier thickness (AlN thickness is 1 nm.) (b) Calculated transmission coefficient of the proposed structure as a function of frequency

Acknowledgment
The research was supported by the Pioneer Research Center Program through the NRF of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009594).

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[3] W. Chan et al., Rep. Prog. Phys. **70**, 1325–1379 (2007)
[4] C. Jansen et al., Applied Optics, **49**, E48-E57 (2010)
[5] S. A. Mikhailov, Physical Review B, **58**, 1517-1532 (1998)

The DRC-based check tool for new ESD failure mechanism

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In general, a direct current path among ESD discharge paths accounts for the major cause of ESD failure. Differently from a general failure mechanism by such a direct current path, however, the ESD failure mechanism presented in this paper represents low impedance paths formed by parasitic capacitances on chip layout construct indirect current paths and result in ESD damage when ESD pulses are flowed into.

It is identified that switch devices directly connected to IOs suffer from ESD damage by parasitic capacitances built between metal layers, which is verified with a new ESD failure mechanism we have developed.

There is an increasing number of cases where a DRC-based check tool is used to detect and analyze various types of ESD failure mechanisms including the existing ones [1]. This method enables an intuitive analysis on diverse ESD issues, in particular, easier approach to the identification and enhancement of ESD weak points. Furthermore, it is possible to predict accurate capacitance in a simple and fast manner using the DRC-based check tool, without using complicated LPE (Layout Parasitic Extraction) tools such as Star-RCXT. As a result, it minimizes the loss of development cost and time to improve ESD failure by optimizing the weak points where ESD failure is expected to occur.

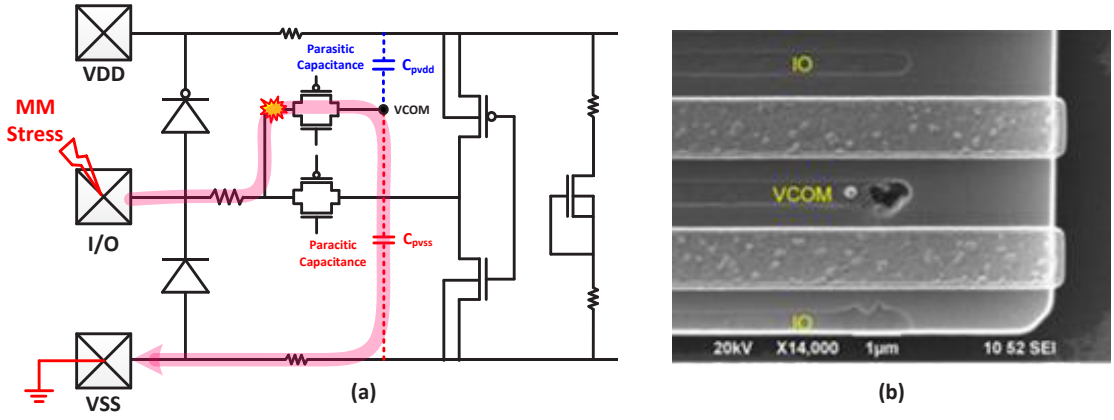

Fig 1. (a) Indirect ESD Current Paths and (b) Physical Damage of ESD Failure

[1] T. Smedes, N et al.," A DRC-based check tool for ESD layout verification," EOS/ESD Symposium, pp.1-9, 2009.

Effective work function modulation of nanoscale FinFET devices by plasma treatment method

Moonkyu Park,[1] Hoonjoo Na,[1] Ohseong Kwon,[1] Jinkyu Jang,[1] Sangjin Hyun,[1] Jahum Ku[1]
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As scale down the gate length of transistor to the nanoscale, 3 dimensional (3-D) FinFET has been essentially introduced for the high performance LOGIC devices. Consequently, precise effective work function (eWF) control is significantly important for the performance boosting of Fin structure.[1] In this study, we showed the precise eWF modulation for the 3-D FinFET devices using plasma treatment method. From the X-ray reflectometry (XRR) analysis, we found that the plasma treatment changed the density of metal gate. In addition, we also found that the plasma treatment process could control the surface potential of metal gate. Finally, using the plasma treatment, we could accurately modulate the eWF of the FinFET devices by the precise control of the physical properties (such as density and surface potential) of metal gate. We believe that this study is very useful to develop the next generation 3-D FinFET devices.

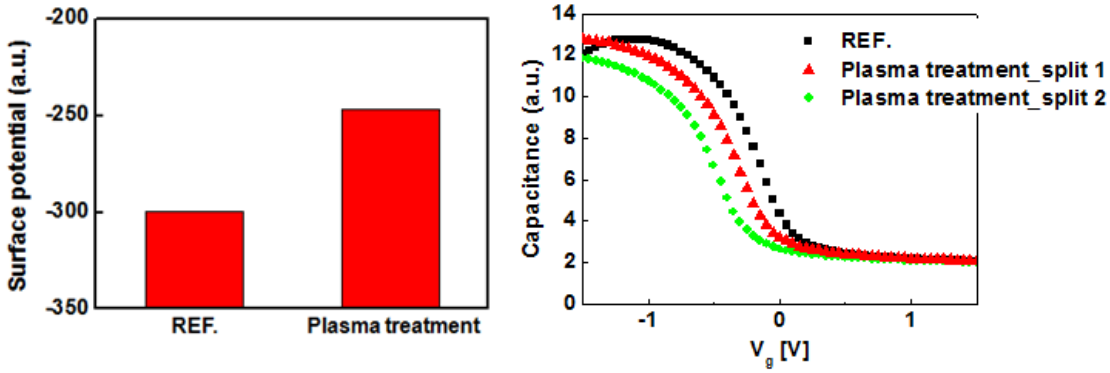

Fig 1. Surface potential data (left) and C-V graph (right) for the plasma treatment process

[1] Indranil De, Deepak Johri, Anadi Srivastava and C.M. Osburn, Solid-State Electronics. 44, 1077 (2000)

A Facile Interface Passivation to Reduce Interface State (N_{it}) in Tunneling Field Effect Transistor (TFET) with ALD HfO_2 and TiN Gate Stack

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Tunnel field-effect-transistor (TFET) is one of the promising devices for low power applications due to improved subthreshold (S.S) characteristics and lower I_{off}. It is a crucial to modulate interface between gate dielectric and substrate for better S.S characteristics. Hydrogen based passivation is reported to suppress interface state by passivating the dangling bonds with H in MOSFET. However, to our best knowledge, the effects of hydrogen passivation have not been reported with TFET. In this study, we demonstrated the effective interface passivation with hydrogen based annealing as H_2 and D_2. Compared to pristine TEFT, H_2 and D_2 treated TFETs show improved transistor characteristics such as higher I_{ds}, lower S.S, lower V_{TH}, and higher $I_{on/off}$. D_2 treatment is more effective to improve S.S characteristics. From charge pumping analysis, it turns out that H_2 and D_2 significantly reduced N_{it} and D_2 is still more effective, which well correlated with transistor characteristics. Similar to MOSFET, hydrogen passivation is still effective method to suppress interface state in TFET.

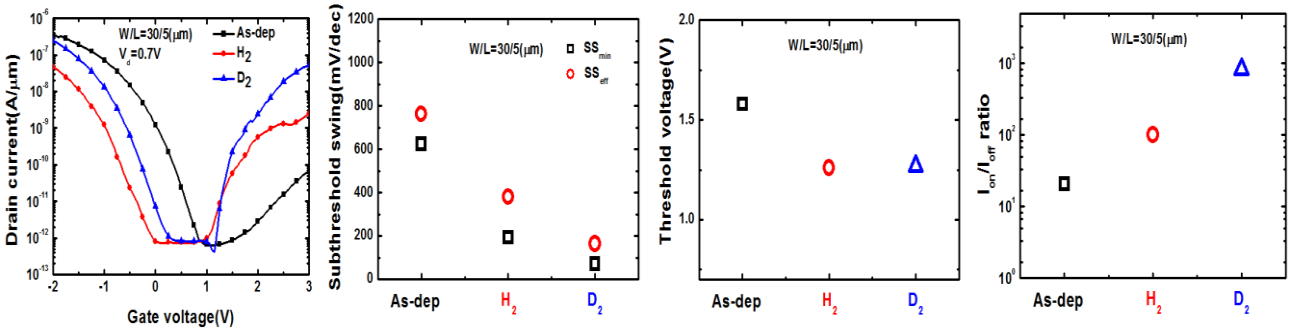

Fig 1. Electrical characterization of HKMG TFET

[1] A. Vandooren, A. M. Walke, A. S. Verhulst, R. Rooyackers, N. Collaert, and A. V. Y. Thean, IEEE Trans. on electon devices (2014).

[2] Q. T. Zhao, J. M. Hartmann, and S. Mantl, IEEE Electron Devices Letter (2011).

This work was supported by the Future Semiconductor Device Technology Development Program (10044842) funded By MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium).

Post-Cleaning Effect on the HfO_2 Gate Stack using NF_3/NH_3 Plasma

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Kyu Dong Kim[c], and Dae Hong Ko[a,b]

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Recently, the fluorinated HfO_2 gate stack has been suggested on the purpose of defect passivation of the gate stack. Furthermore, fluorinated gate dielectrics have been shown to improve the electrical characteristics [1]. However, the interfacial layer (IL) regrowth between HfO_2/Si and the change of chemical bonding state with a reduced k-value is still a critical issue during the fluorine plasma treatment [2]. In this paper, we have investigated the effects of dry cleaning for HfO_2 gate stack engineering using NF_3 only and NF_3/NH_3 gas mixture plasma. The plasma dry cleaning process was carried out after HfO_2 deposition using an indirect down-flow CCP system. As shown in Fig.1, the analysis of chemical composition of HfO_2 gate stacks by XPS has revealed that fluorine was incorporated into the HfO_2 films by plasma dry cleaning. The significant changes in HfO_2 chemical composition were observed in NF_3 dry cleaning, while they were not observed from NF_3/NH_3 dry cleaning. TEM results showed that the IL thickness was increased by plasma dry cleaning. However, in the case of NF_3/NH_3 dry cleaning with 150W, the IL thickness was suppressed significantly compared to the sample without dry cleaning. Also its electrical properties were improved, including the low gate leakage currents, and reduced EOT. Finally, we found that the IL thickness of the HfO_2 gate stack can be controlled with the novel NF_3/NH_3 dry cleaning process technique without any the change of chemical composition.

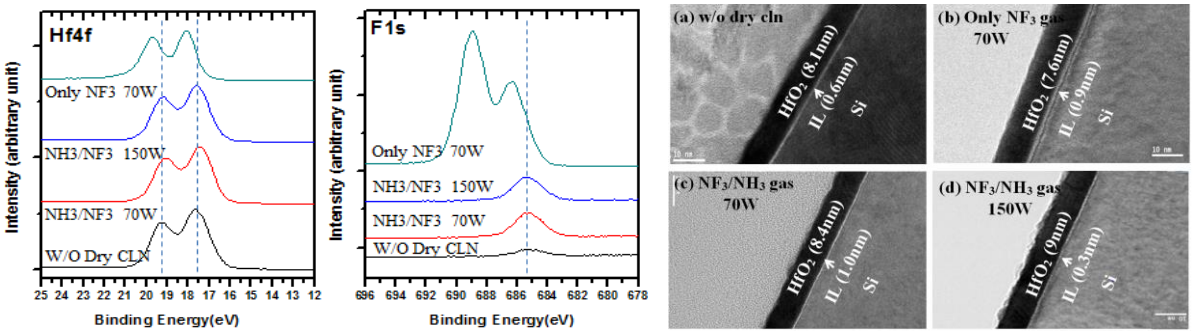

Fig 1. XPS Spectra of HfO2 film and its TEM image

[1] W. C. Wu, et al., *J. Electrochem. Soc*., **154**, H561 (2007).
[2] J. C. Lee, et al., *J. Microelectronic Engineering*, **88**, 1417 (2011).

Effect of thermal defects on C-V characteristics of MOS structure with SiO_2 passivation layer deposited on InSb substrate via Raman spectroscopy

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[2]*Memory Manufacturing Operation Center, Samsung Electronics, Suwon, Korea*
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Indium antimonide (InSb) has been widely used as mid-IR detectors for the wavelength of 3~5 μm since 1950s. To fabricate a high performance device using InSb, the optimization of surface passivation layer for suppressing the dark current is one of the key issues. As a result, the change of interfacial phases between SiO2 and InSb has attracted great interest over the last several decades, with the aim of improving the performance of InSb-based devices.

In this sense, C-V measurement is a very effective method to evaluate the bulk and interfacial trap density of the passivation layer which have a close relation with the dark current of devices. In this work, in order to find the optimized condition for the deposition of the SiO2 passivation layer, the effect of deposition temperature on the C-V characteristics of Au/Ti/SiO2/InSb was investigated.

The effect of interfacial phases on the electrical properties of Au/Ti/SiO2/InSb metal-insulator (oxide)-semiconductor (MIS or MOS) structures was investigated by capacitance-voltage (C-V) measurements. With increasing the deposition temperature of silicon oxide from 100 to 350oC using PECVD, the change in the interfacial phases between SiO2 and InSb were analyzed by resonant Raman spectroscopy to verify the relation between the breakdown of C-V characteristics and the change of interfacial phases. The shape of C-V characteristics was dramatically changed when the deposition temperature was above 300oC. The C-V measurements and Raman spectra represented that elemental Sb accumulation resulted from the chemical reaction of Sb oxide with InSb substrate was responsible for the failure in the C-V characteristics of MIS structure.

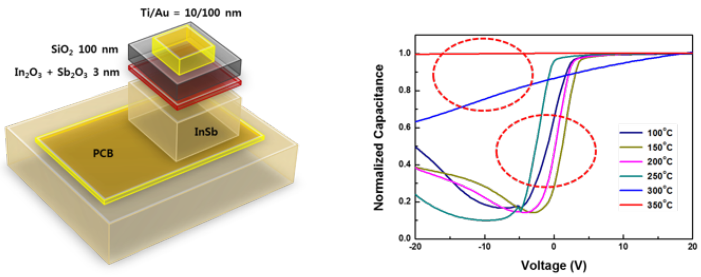

Fig 1. MOS structure and its C-V characteristics

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films with Al_2O_3 interlayer as a serial resistor on ferroelectric switching

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Recently, it was reported that HfO_2 can show ferroelectric (FE) properties when doped with various dopants such as Zr, Si, Y, Al, Gd, La, and Sr. It is generally accepted that the ferroelectricity within these materials originates from the formation of non-centrosymmetric $Pca2_1$ orthorhombic phase [1]. The feasible ferroelectricity (remanent polarization >20μC/cm^2) with extremely small thickness (<10nm) is considered highly promising for various applications. However, the ferroelectricity of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films is significantly degraded when the thickness of the thin films increases over 20nm. The reason is that the FE orthorhombic phase transforms into monoclinic phase alongside with the grain growth (increase in grain size). In our previous report, 1nm-thick Al_2O_3 inter-layer was inserted in the middle of HZO layer, which controls grain size of HZO thin films. [2] It was found that the transformation into the monoclinic phase and grain growth could be suppressed effectively, thus the FE property of $Hf_{0.5}Zr_{0.5}O_2/Al_2O_3/Hf_{0.5}Zr_{0.5}O_2$ (HZAHZ) film was not degraded with increasing thickness up to ~40nm. Surprisingly, the upper and lower HZO layers in HZAHZ films involves almost identical FE performances. In general, dielectric Al_2O_3 deposited on FE films plays a role to degrade ferroelectricity with a dead layer effect. In our result, however, the role of Al_2O_3 layer as a series resistor during ferroelectric switching could be clearly confirmed by transient switching current analysis. The effect of Al_2O_3 layer on total resistance (R_L) and interfacial capacitance (C_i) could be examined by comparing those of 10nm-thick HZO and 20nm-thick HZAHZ films. From the analysis, calculated R_L of 20nm-thick HZAHZ film was larger than that of 10nm-thick HZO film by ~18Ω, whereas C_i values of 10nm-thick HZO film and 20nm-thick HZAHZ film are ~33nF and ~32nF, respectively. Since these values are much larger than the theoretical capacitance of 1nm-thick Al_2O_3 (~8nF with ε_r of 9), the Al_2O_3 layer did not work as a series capacitor. Thus, these results suggest that the Al_2O_3 interlayer works as a series resistor during ferroelectric switching, not as a dielectric layer.

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Adaptive-Learning Synaptic Device Using Organic Ferroelectric Thin Films at Low-Process Temperature

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To improve the adaptive-learning capability for the conventional artificial neuromorphic systems demanding the complex circuit and long-time learning algorithm, new types of synaptic devices have actively been researched. In synapatic device operations, the gradual modulation in synaptic weight is essential for mimicking human synapse. Ferroelectric materials can be promising for controlling the synaptic weights by exploiting partial polarization. However, conventional oxide ferroelectrics need to be crystallized at high temperautre[1]. In this study, we proposed a thin-film transistor using organic ferroelectric poly(vinylidenefluoride-trifluoroethylene) gate insulator as a adaptive-learning synaptic device fabricated at low temperaure below than 200 ºC. The device structure was shown in Fig. 1(a). Channel conductance could be modulated by controlling the partial polarization caused by the applied excitatory and inhibitory pulses. For evaluating the adaptive-learning feasibility, the pulse amplitude and width were set as 10 V and from 10 to 500 ms, which corresponded to smaller and shorter pulses for full-switching memory behaviors. As shown in Fig. 1(b), the programmed current was linearly increased and decreased with increasing the number of excitatory and inhibitory pulses, respectively. It was also found that the saturated current values and learning linearity sensitively depends on the applied pulses widths. At presentation, the detailed behaviors including the stability of partial polarization of ferroelectric synaptic devices and the feasibility for flexible applications realized with low-temperatue compatibility will be discussed.

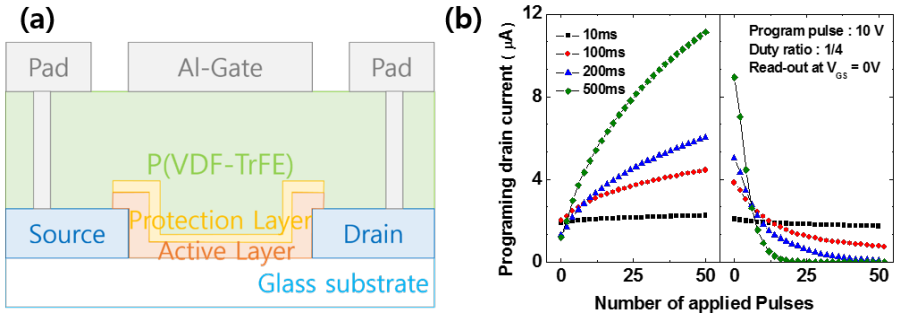

Figure 1. (a) A Cross-section of the fabricated device. (b) Demonstrations on gradual increase in the drain current for the fabricated synaptic device when excitatory and inhibitory pulses with various pulse widths were applied.

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A Monte Carlo simulation model for an anomalous ISPP behavior in NAND flash memory

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A Monte Carlo simulation model for describing an anomalous ISPP (Incremental-Step Pulse Programming) behavior in NAND cell has been proposed as shown in Fig. 1(a). The simulation model is based on a physical model of current-crowding effect at the active edge of planar NAND cell. In the planar NAND cell, the active edge is a sensitive portion regarding the cell operation because it is relatively prone to have a sharp corner as in Fig. 1(b) due to the different oxidation rate at the corner. The increase of the electric field at the sharp edge leads to the crowding of current at the corner. Then, the charge trapping and de-trapping rates increase at the corner and it randomly disturbs the FN current flow [1]. The random fluctuation of FN current has been simulated by a Monte Carlo simulator that has been built as shown in Fig. 1(a) with anomalous cells having a portion of $1/10^5$. The current fluctuation of anomalous cell has been modeled by the fluctuation of B_{FN} parameter in FN equation (1) with a standard variation of 8 times larger than the normal cells. Fig. 1(c) shows the simulation can exactly regenerate the experimental result.

$$J_{FN} = A_{FN} E_{Ox} Exp(-B_{FN} / E_{ox}) \quad (1)$$

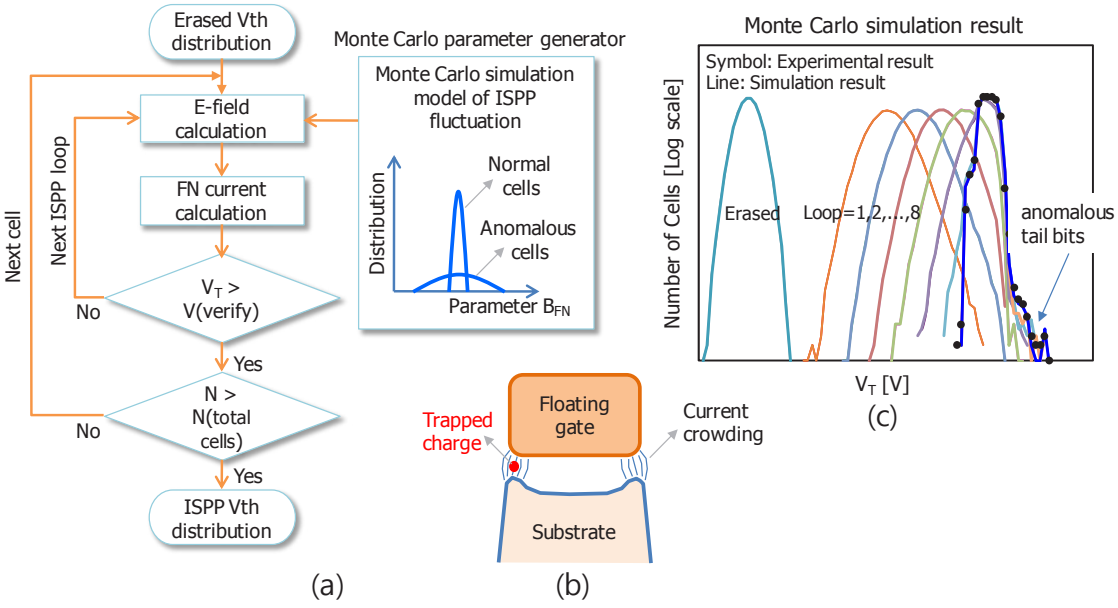

Fig. 1. (a) Monte Carlo simulation algorithm, (b) physical model, and (c) simulation result.

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3차원 플래시 메모리를 위한 채널 두께와 고체화 결정법에 의한 결정 크기 효과에 관한 연구

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최근 3 차원 구조의 플래시 메모리에 대한 연구가 많이 진행되고 있다. [1-2] 2 차원 평판 구조의 플래시 메모리와 달리 3 차원 구조의 플래시 메모리를 만들기 위해서는 다결정 실리콘을 채널영역으로 사용해야 한다. [3] 다결정 실리콘의 결정크기는 소자의 전기적인 특성 및 그 분포는 물론 산화막 과의 계면 상태에도 큰 영향을 미친다. 채널영역으로 사용되는 다결정 실리콘은 고체화 결정법을 통해 먼저 증착한 비정질 실리콘으로 만들어진다. 이에 따라 다결정 실리콘의 결정 크기는 고체화 결정법의 온도와 처음 증착된 비정질 실리콘의 두께에 큰 영향을 받는다. [4] 본 논문에서는 3 차원 플래시 메모리를 제작하는 방식과 동일한 순서로 게이트, 산화막, 채널영역을 구현하였다. 채널영역의 실리콘 두께와 고체화 결정법의 온도를 조절함으로써 증착된 실리콘의 두께와 고체화 결정법의 온도가 transfer curve 특성 및 program/erase, endurance 와 같은 메모리 특성에 어떠한 영향을 미치는지 확인하였다. 결과를 보면 채널 영역의 두께가 두꺼울수록, 적당한 수의 nucleation site를 형성하는 온도일수록 큰 결정 크기로 인해 포화 전류가 높은 것을 확인하였다. 또한 큰 결정크기로 인한 채널과 산화막 계면의 표면 거칠기 차이로 인해 달라진 메모리 특성도 살펴보았고, charge pumping method 를 통해 채널영역의 두께 별, 고체화 결정법의 온도 별로 trap density 를 추출하여 외삽법을 통해 각 고체화 결정법의 온도에 따른 계면 상태 밀도(interface state density)를 정량적으로 분석하였다.

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Multi-state resistance controllability and variability analysis of binary oxide RRAM for ultra-high density memory applications

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Multi-level per cell (MLC) storage will be required in future in order to achieve ultra-high density memory with low cost [1]. RRAM is particularly attractive for MLC applications due to its simplicity of obtaining such characteristics even in scaled sub-10 nm device. Although, MLC characteristics in filamentary RRAM are reported [2-4], the resistance variability during switching is the most important concern for its successful operation and hence need to be studied more to enhance the understating. In this study, we have investigated the MLC characteristics of two most promising and extensively studied binary oxides; TaO_x and HfO_x based RRAM stack by varying the switching current. In both the stacks, 3 different levels of low resistance states (LRS) with same high resistance state (HRS) were obtained which can be used in 2-bit per cell storage [Fig. 1(a) and (c)]. The switching variability decreases with increasing the current compliance (I_C) due to the presence of more defined conduction path with higher number of vacancies [Fig. 1(b) and (c)]. The TaO_x based device shows resistance saturation [fig. 1(a)] due to unavailability of vacancy source needed for filament to grow whereas HfO_x device show self-compliance behavior which degraded the margin among the MLC levels [Fig. 1(c)]. With this analysis, an engineered stack with W/Ta/TaO_x/Pt structure was designed which exhibit 3-bit MLC characteristics at smaller switching current range of 30 to 300 μA.

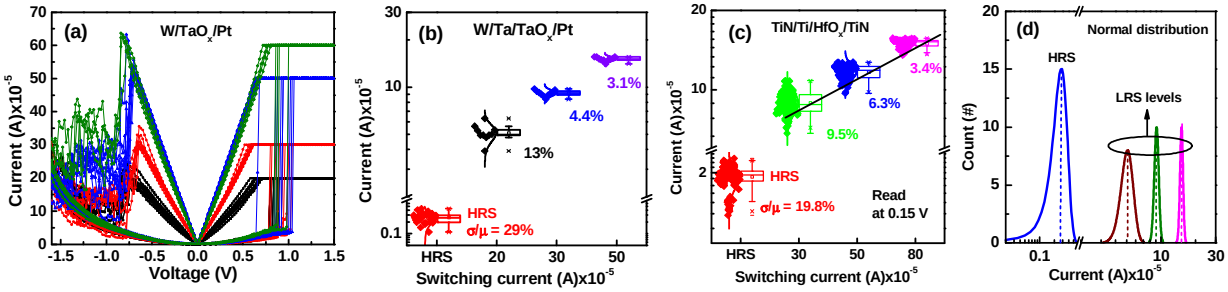

Fig 1. (a) MLC characteristics of W/TaO_x/Pt device. Distribution of LRS/HRS of (b) W/TaO_x/Pt and (c) TiN/Ti/HfO_x/TiN devices. (d) Normal distribution of HRS and LRS levels.

Acknowledgment: This work was supported by the POSTECH-Samsung Electronics ReRAM Cluster Research project.

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Sub-Oxide Dependence of Insulator Metal Transition Characteristics on 3-D Structural Niobium Oxide Selector

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Recently, niobium oxide thin film is highlighted because of its unique characteristics as an insulator metal transition (IMT) material. Moreover, NbO_2 thin film is studied as selector devices for cross-point array memory structure by using IMT characteristic. Generally, it is known that the near-stoichiometry of NbO_2 has IMT characteristic in a bulk, which can be controlled by changing oxygen-content [1,2]. However, it is very difficult to obtain control the composition in thin film for cross-point array memory structure. For finding optimal composition that exhibits IMT characteristic suited for selector devices, we demonstrated the large range of oxygen composition NbO_x film by using a combinatorial sputtering tool on 3-D structure substrate (Fig. 1-(a)). Moreover, we revealed the operating mechanism during voltage sweep at each composition. In our experiment, the film, with a gradient in oxygen content, shown slightly different IMT characteristic depending on the oxygen content. To understand the correlation between the IMT characteristics and oxygen content of NbO_x film, we conducted electrical analyses and various physical analyses such as atomic force microscopy (AFM) and electron diffraction spectroscopy (EDS). These results show that the film in position y = 0.6 has near stochiometry NbO_2 phase and it has superior characteristic including over one-order on-off ratio, very good cycle variation, and up to 10^6 cycles pulse-endurance. In addition, we discovered the role of sub-phases such as insulating NbO_{2+x} (Nb_3O_7, Nb_2O_5 etc) and metallic NbO_{2-x} (NbO,Nb_2O_3 etc) which incur unstable characteristic and leakier characteristic, respectively.

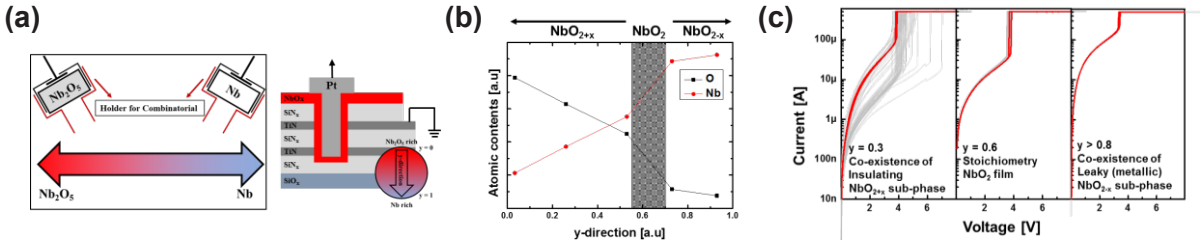

Fig 1. (a) Combinatorial tool for gradual composition, sample structure, (b) EDS analysis for composition confirmation and (c) I-V characteristic at each composition

Acknowledgement. This work was supported by the POSTECH-Samsung Electronics ReRAM Cluster Research.

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Improvement in reliability characteristics (retention and endurance) of RRAM by using high-pressure hydrogen annealing

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Recently, transition metal oxide based resistive switching memory (RRAM) is emerging as one of the most promising candidates for next-generation non-volatile memories [1]. However, one of the critical reliability issues is the trade-off between retention and endurance [2]. It is highly desired to find out the solutions for both retention and endurance improvement. In this study, we confirmed the trade-off between retention and endurance by using the various top electrode thickness conditions which in turn have different degree of oxygen scavenging property. The thicker Ta TE cells have worse retention because the large amount of oxygen in scavenging layer (Ta) can diffuse back into HfO_2 and recombine with V_O in the filament [3]. However, it has longer endurance because the large amount of V_O in switching layer (HfO_2) can be a source of the filament [4]. Hence, there exists a trade-off relation between retention and endurance under the various Ta TE thickness conditions [Fig. 1(a)]. To improve both retention and endurance characteristics, we proposed a new method by using high-pressure hydrogen annealing (HPHA). The thinner Ta TE cells have longer retention and worse endurance because it has small amount of both oxygen in Ta TE and V_O in HfO_2. Therefore, to generate more V_O in HfO_2, we treated the samples by HPHA before TE deposition [Fig. 1(b)]. The decreased forming voltage was observed after HPHA treatment [Fig. 1(c)], indicating the reduction effect caused by hydrogen atom impurities [5]. Finally, we obtained both improved retention and endurance characteristics in HfO_2 based RRAM devices after HPHA treatment as shown in Fig . 1(d).

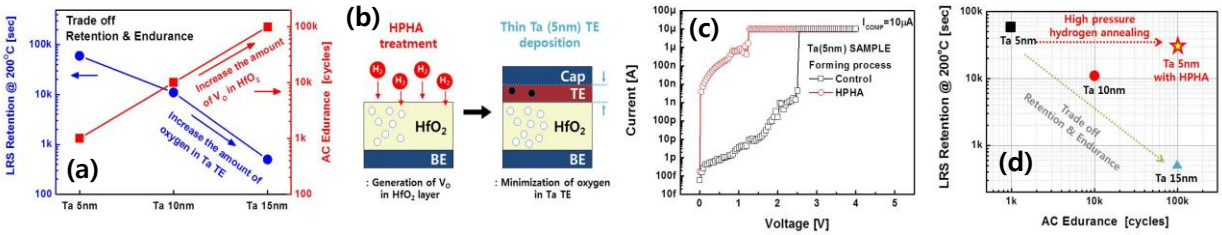

Fig 1. (a) Trade-off between retention and endurance (b), (c) High-pressure hydrogen annealing and its electrical data (d) Retention and endurance characteristics

Acknowledgement This work was supported by the Future Semiconductor Device Technology Development Program (10045085) funded By MOTIE(Ministry of Trade, Industry & Energy) and KSRC(Korea Semiconductor Research Consortium)

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Selector-less ReRAM with an Excellent Selectivity by the Tunnel Barrier Engineered Multi-layer Titanium Oxide and Triangular Shaped AC Pulse

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The effect of oxygen profile control of a multi-layer. TiO_x on tunnel barrier characteristics has been extensively investigated to achieve high selectivity and endurance of selector-less ReRAM. By optimizing oxygen profile of TiO_x layer in the selector-less ReRAM, readout margin of cross-point array has been significantly improved compared with previous 1S1R-type devices. In addition, AC operations of the device have been investigated with various AC pulse shapes to obtain high selectivity and endurance.

The resistive switching random access memory (ReRAM) has been considered as next generation NVMs to solve the scaling limit and for low power operation of the conventional Flash memory [1]. However, ReRAM suffers from leakage current (I_{LKG}) of reading operation in cross-point array owing to low-resistance state (LRS) of on-state [2]. It occurs reading failure in high-resistance state (HRS) reading because most current flows LRS cells during HRS reading. To prevent above reading failure, I_{LRS} of ReRAMs should be reduced at low voltage ($½V_{Read}$). Furthermore, ReRAM should maintain sufficient I_{LRS} at high voltage (V_{Read}) for high selectivity. Therefore, various selectors have been introduced with compositional and structural complexity to obtain reduced I_{LRS} at $½V_{Read}$ [3]. To implement excellent selectivity and cost-effective device, selector-less ReRAMs haven been recently investigated. However, their selectivity values were quite insufficient for high-density cross-point array applications.

In this research, tunnel barrier engineering of the multi-layer TiO_x has been extensively investigated to improve selectivity with modulating tunnel barrier characteristics by TiO_x thickness and oxygen profile control. Tunnel barrier engineering determines selectivity and its yield. In addition, we have investigated the effect of AC pulse shape on the selectivity and switching endurance of selector-less ReRAM. We observed that current overshoot removal can exhibit suppressed I_{LKG} (~800 nA) and high endurance (~10^8 cycles) in AC pulse mode. Fig. 1a shows the DC I-V curve comparison between general ReRAM and selector-less ReRAM in 250 nm cell and 1kb-cross-point array. The selector-less ReRAM shows high selectivity for the suppressed I_{LKG} at $½V_{Read}$. It is attributed to TiOx tunnel barrier in selector-less ReRAM. Fig. 1b shows the TEM image of the Pt/Ti/HfO_2/ TiO_x/Pt selector-less ReRAM with multi-layer TiO_x tunnel barrier. The TiO_x layer of the TEM image confirms that TiO_y has higher oxygen profile than that of TiO_x owing to thermal oxidation of the TiO_x top surface. In addition, XPS binding energy analysis shows that the top surface of the TiO_y layer has more Ti^{4+} valence of insulating state. This multi-layer TiO_x is the key factor for high selectivity of the device. Finally, the selector-less ReRAM exhibited 10^8 programming and erasing cycles in the triangular pulsed pulse by current overshoot removal. Furthermore, the device could exhibit sufficiently suppressed I_{LKG} in even AC pulse mode without any degradation.

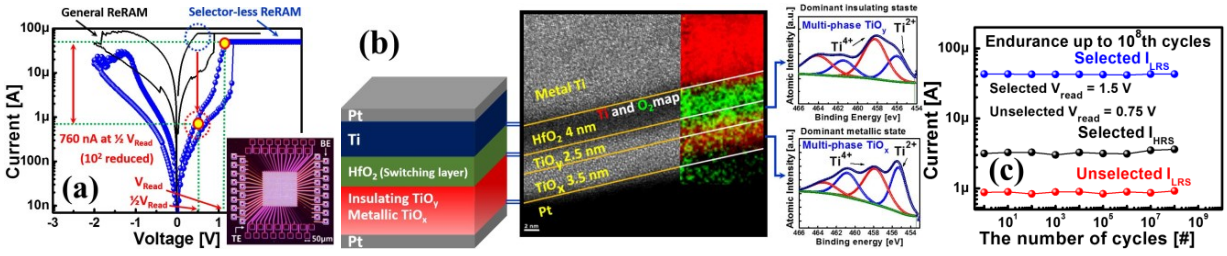

Fig 1. (a) The highly suppressed I_{LKG} of the selector-less ReRAM compared to the linear ReRAM in 250 nm via-hole structure (b) It describes device structure and a TEM image and XPS binding energy results show the multi-layer TiO_y/TiO_x of the TiO_x tunnel barrier for low I_{LKG} of high selectivity (c) By applied triangular AC pulse for continuous switching, 10^8 switching endurance was successfully exhibited without degradation (In rectangular AC pulse, it showed up to 10^6 switching endurance).

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TDR 분석법을 이용한 미세전계효과소자의 Effective Mobility 추출 방법

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Metal-oxide-semiconductor field-effect transistors (MOSFETs) 의 effective mobility 는 소자의 성능을 평가하는 데 있어서 가장 중요한 지표 중에 하나이다. 반도체 소자의 effective mobility 는 실리콘 채널의 inversion charge 를 측정하는 split capacitance-voltage (C-V) 방법을 이용하여 평가를 하게 된다. 하지만, 반도체 소자가 미세화됨에 따라 C-V 측정시 누설전류의 영향이 점점 더 커지게 되어, 정확하고 신뢰성 있는 mobility 추출이 어려워 지고 있다. 또한 series resistance (R_{sd}) 가 total resistance (R_{tot}) 에서 차지하는 비중이 커지게 되어, R_{sd} 에 의한 effective mobility 의 오차가 커지게 되었다. Time domain reflectometry (TDR) 분석법을 이용하면. 누설전류가 큰 MIS 나 MIM capacitor 소자의 capacitance 와 series resistance 를 안정적으로 측정할 수 있다. [1, 2]

본 연구에서는 매우 간단한 소자 패턴에서도 활용할 수 있도록 특수제작된 RF probe 를 TDR 에 적용하여, 누설전류가 매우 큰 일반 MOSFET 소자 (EOT<10 Å) 의 gate-to-channel capacitance (C_{gc}), gate-to-bulk capacitance (C_{gb}), total gate capacitance (C_g)를 성공적으로 추출하였고, 동시에 series resistance (R_{sd}) 를 추출하여, 신뢰성 있는 effective mobility 추출이 가능함을 보였다. 결과를 요약하면, J_g= 30A/cm^2 (EOT=0.85nm) 의 상태에서 $\mu_{eff,peak}$ ~ 180 (cm^2/Vs), R_{sd}~13 Ω 가 추출되었고, 추출된 R_{sd} 값을 이용, effective mobility 를 보정하게 되면 실제 mobility 는 종래의 방법에 대해 약 15% 정도 증가된 값을 얻게 되었다. 이 측정은 매우 간단한 소자 패턴에도 적용할 수 있기때문에, TDR 분석법을 이용한 effective mobility 추출방법은 in-line test 에도 적용 가능한 매우 유용한 측정법임을 검증하였다.[3]

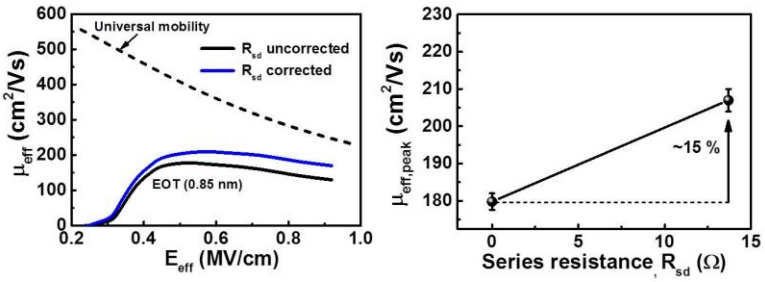

Figure 1 R_{sd} corrected effective mobility using TDR split C-V method

[1] Y. H. Kim et al., IEEE Electron Device Lett., vol. 33, 1303 (2012) [2] Y. H. Kim et al., Jpn. J. of Appl. Phys., vol. 53, 08LC02 (2014), [3] Byoung Hun Lee, Yong Hun Kim, Young Gon Lee, "반도체 장치의 검사방법및 이에 사용되는 프로빙 어셈블리", US patent application No. 2013-0120988 , 2014.
This work was supported by the IT R&D program of MOTIE/KEIT. [10039174, Technology development of 22nm level foundry devices and PDK]

In-situ thermal annealing and ALD SiO_2 interfacial layer as an interface passivation for Ge pMOSFETs

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Ge channel MOSFETs are being intensively researched as a performance booster for the mobility enhancement and drive current improvement beyond the device scaling limits of Si channel MOSFETs [1]. In order to realize high performance Ge channel MOSFETs, it is absolutely necessary to control the thermodynamic instability of Ge native oxides and Ge indiffusion into the high-k dielectric layer, which can result in degraded carrier mobility, high gate leakage current, and large flatband voltage (V_{fb}) shift [2]. However, Ge passivation techniques for superior high-k/Ge interfaces have not yet been fully established. In this study, we investigated two passivation methods to control the high-k HfO_2/Ge interface qualities prior to high-k HfO_2 deposition: in-situ thermal annealing without any ambient gas and an insertion of ultra-thin SiO_2 interfacial layer by ALD process. TEM and XPS analyses reveal that in-situ thermal annealing and ultra-thin SiO_2 interlayer can effectively suppress the GeO_2/Ge interfacial reaction and the formation of defective Ge suboxide (GeO_x) compared to sample without passivation as shown in Fig.1. As a result, the improved interface qualities exhibit smaller capacitance-voltage (C-V) hysteresis.

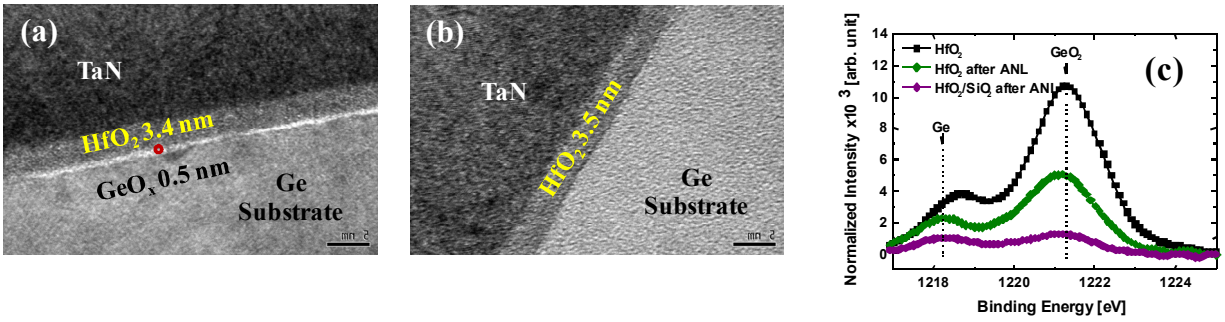

Fig 1. Cross-sectional TEM images taken from (a) HfO_2 on Ge, and (b) HfO_2 on Ge with annealing at 550℃. (c) Corresponding XPS Ge 2p core-level spectra.

Acknowledgment : This work was supported in part by the MOTIE(Ministry of Trade, Industry & Energy (G01201406010774) and KSRC(Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device. This research was also supported in part by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education(2012003567).

[1] S. Takagi, N. Taoka, and M. Takenaka, ESC Transactions. 19, 67 (2009).

[2] Y. Kamata, Materials Today. 11, 30 (2008).

Electrical Characteristics of MOSCAP with High-κ/Metal Gate using an Oxygen Scavenging Process

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Recently, high- κ gate dielectrics have been extensively studied and are considered to become one of solutions for providing high capacitance without increasing leakage current. It has high permittivity in comparison with SiO_2. Thus gate dielectric of low equivalent oxide thickness (EOT) can be obtained. HfO_2 films exhibit high permittivity (~22) and band gap is 5 eV. Whereas many traps in HfO_2 induce hysteresis characteristic leading to threshold voltage shift and decrease of carrier mobility. For the purpose of getting better interface quailty, we insert very thin SiO_2 film (< 2 nm) which is very compatible with Si substrate. However this SiO_2 layer results in increasing of EOT. In order to reduce the thickness of SiO2 layer, scavenging technology is one approaches[1-2] . From Fig. 1 (a), TiN/Ti/TiN stacks are used as metal gate electrode and susequent annealing process can reduce the thickness of HfO_2/SiO_2 stack. Also the electrical characteristics of samples are investigated using capacitance-voltage measurement as shown in Fig. 2. As a result, it is observed that EOT can be decreased dramatically.

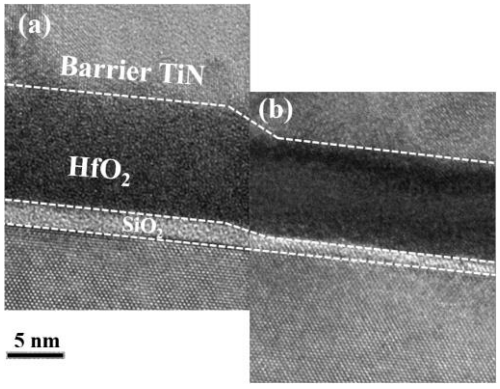

Fig. 1. Cross-sectional view of stack (a) before and (b) after annealing

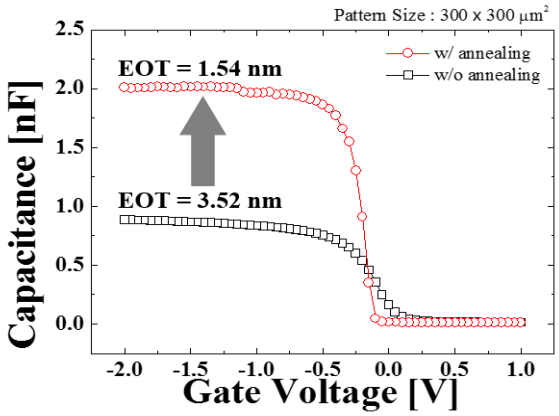

Fig. 2. Measured Capcitance of each samples

This work was supported by the Future Semiconductor Device Technology Development Program (10044842) funded By MOTIE(Ministry of Trade, Industry & Energy) and KSRC(Korea Semiconductor Research Consortium).

[1] T. Ando, M. M. Frank, K. Choi, J. Bruley, M. Hopstaken, M. Copel, E. Cartier, A. Kerber, A. Callegari, D. Lacey, S. Brown, Q. Yang, and V. Narayanan, International Electron Devices Meeting, (2009)

[2] M. Xueli, H. Kai, and W. Wenwu, Journal of Semiconductors, Vol. 34, No. 7 (2013).

A novel processing technique for reducing contact resistance of n^+ Si junctions by a high-κ dielectric prepared by atomic layer deposition

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In these days, low-power operation capability of electron devices is regarded as one of the most crucial requirements in both high-performance (HP) and low-power (LP) applications, and further, it is notable that pursuing a unified operating voltage (V_{DD}) for both has begun as demonstrated in the most recent technology roadmap [1]. As the CMOS device is aggresively scaled down, the resistances in ultra-shallow junctions take a larger portion in total series resistance, which causes degradation in current drivability and fast swtich. In this work, a novel low-temperature processing technique for reducing the contact resistances of n^+ Si junctions by an insertion of HfO_2, a high-κ dielectric, prepared by an atomic layer deposition (ALD), which effectively screens the metal-induced gap states (MIGS) [2], and helps securing higher ohmicness (Fig. 1). The electrode metal Ni was prepared, by an e-beam evaporation, for a study of the extreme Schottky contact to n^+ Si (Fig. 2) and post-metal annealing (PMA) was performed to further reduce the interface states (D_{it}'s). Higher linearity and symmetry in the *I-V* curves have been obtained at an optimal HfO_2 thickness (Fig. 3).

Acknowledgements This research was supported by the National Research Foundation of Korea (NRF) funded by the Korean Ministry of Science, ICT & Future Planning (MSIP) (NRF-2014R1A1A1003644) and also supported by Nano·Material Technology Development Program through NRF funded by MSIP (2009-0082580).

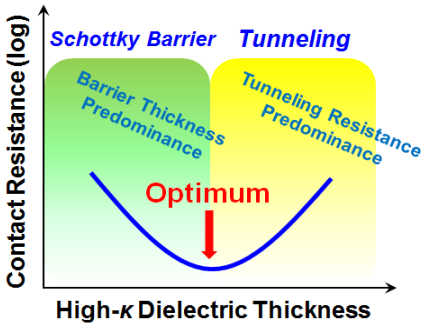

Fig. 1. MIGS and tunneling predominences control by ALD.

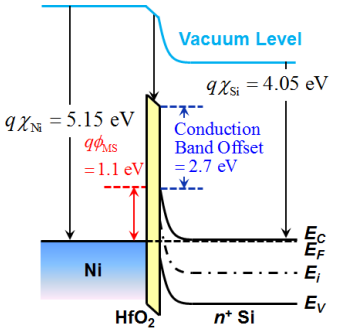

Fig. 2. Energy-band diagram of Ni/HfO_2 (ε_r=18 [3])/n^+ Si junction.

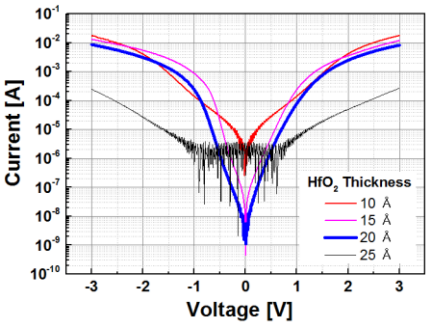

Fig. 3. Measured *I-V* curves. Optimized at 2-nm-thick HfO_2.

[1] ITRS 2013 Edition. [2] T. Nishimura, *et al.*, *Appl. Phys. Lett.*, vol. 91, no. 12, pp. 123123-1–123123-3, Sep. 2007. [3] D. W. McNeill, *et al.*, *J. Mater. Sci. - Mater. Electron.*, vol. 19, no. 2, pp. 119–123, Feb. 2008.

Ni-Al alloy silicide to reduce the electron Schottky barrier height in source/drain junction for high performance nano-scale NMOSFET

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Recently, the contact resistance (R_c) at the interface between silicide and source/drain junction has become a major contributor in parasitic resistance as MOSFET has been scaled down to improve the device performance [1]. It has been reported that R_c is closely related to the Schottky barrier height (Φ_B) of silicide to source/drain region [2]. Hence, reduction of Φ_B is highly necessary to improve the device performance. In this paper, Ni-Al silicide using Al/Ni/TiN structure is proposed to reduce the electron Schottky barrier height (Φ_{Bn}) to n-type source/drain region. Ni-Al alloy silicide was formed by Al/Ni/TiN structures with a split of Al interlayer thickness (2 and 4 nm) as shown in Fig. 1(a). Fig. 1(b) shows the schematic diagram of the fabricated Schottky diodes. As the Al interlayer becomes thicker, the current level of the fabricated Schottky diode increases and the differences between the forward and reverse currents are reduced. These results show that Φ_{Bn} becomes significantly lower than the control sample without Al interlayer. The Φ_{Bn} reduction is due to changes in the work function caused by the formation of Ni-Al alloy silicide, which will be proven by X-ray diffraction and secondary ion mass spectroscopy analysis. This study will be helpful for high performance n-channel MOSFET.

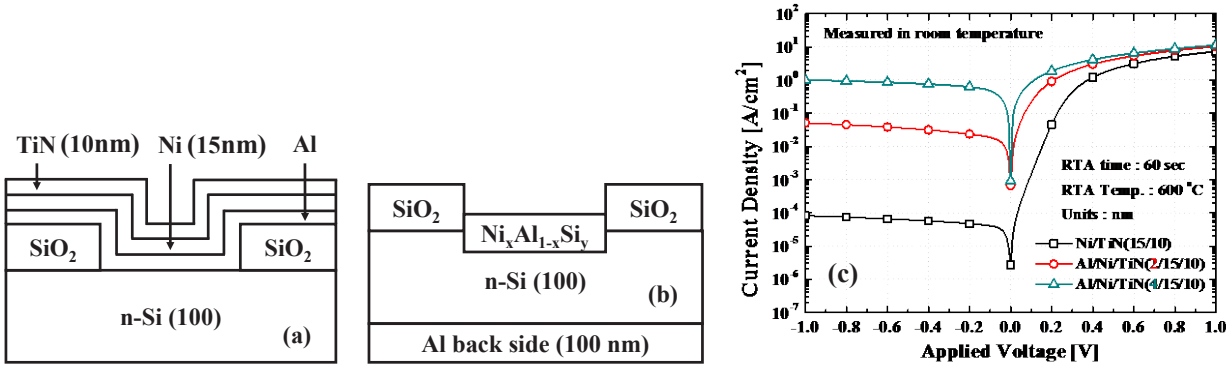

Fig 1. (a) As-deposited layer structure before silicidation, (b) expected layer structure after silicidation and selective wet etching, followed by aluminum deposition on the back side, and (c) I-V characteristics of the fabricated Schottky diodes.

Acknowledgment : This work was supported in part by the MOTIE(Ministry of Trade, Industry & Energy (G01201406010774) and KSRC(Korea Semiconductor Research Consortium) support program for the development of the future semiconductor device. This work was also supported in part by research fund of Chungnam National University.

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[2] S. D. Kim, et al, IEEE Transactions on Electron Devices, **49**, 3 (2002)

2-Dimentional Defect Monitoring Array with Series Testing

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Yield in current Semiconductor industry is one of the most import parameter as it is directly correlated to the profit of the technology. As a result, monitoring possible defects throughout process development becomes essential where feedback from monitoring process can point to the issues hindering from improving yield of the technology.[1] Addressable array has been appealed to many designers as it enables to pinpoint defect location as well as reduces silicon area by using less number of pads.[2] However, when array size grow larger test time also rises, becoming a drawback when used as process monitoring. In this study, a novel 2-dimentional array design with series testing is introduced. Array design preseneted below enables addressing whole row in addition to conventional row-column addressing. Defect monitoring array could be programmed to perform row testing first, then locate cells with defect by stepping through columns of failed rows. For 64x64 array with one defect in every other row at the last column, about 48% of test time reduction is expected. Depending on the size of array, location and frequency of defect in the array, the test time reduction would be more significant.

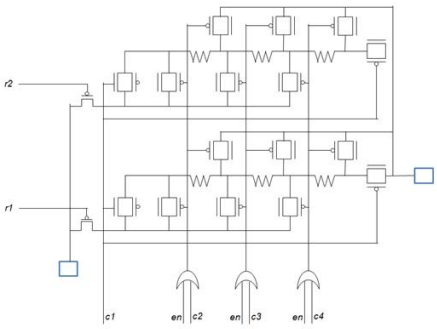

Fig1. Schematic of array

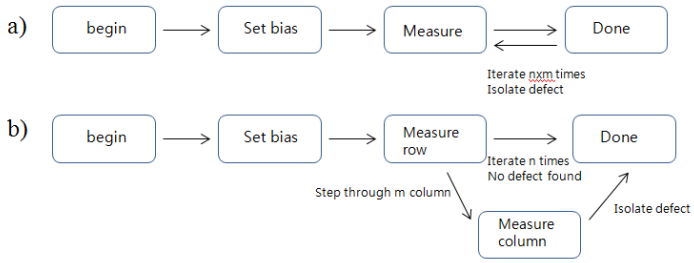

Fig2. Test flow of typical (a) and presented (b)

[1] Karthikeyan M, Gasasira A, Fox S, Yeric G, Hall M, Garcia J et al in IEEE Int'l Conf. Microelectronic Test Structure(ICMTS 2006), pp 104-109
[2] Bushan M, Ketchen M; Microelectronic Test structures for CMOS Technology, Springer NY 2011

Thermoreflectance microscopy and applications for thermal characterization of semiconductor devices

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To find out from where the local self-heat emerges, how it distributes, and how it affects the performance of the semiconductor devices, several thermal imaging techniques, such as scanning thermal microscopy [1], micro-Raman thermography [2], and infrared micro-thermography [3], have been developed. Thermoreflectance microscopy (TRM) is a contactless optical imaging technique that provides a two-dimensional thermal image of semiconductor devices with high spatial and thermal resolution [4, 5]. TRM measures temperature-dependent changes in reflection using the thermo-optic response of a thermally modulated sample. Spatially resolved surface temperature changes (ΔT) of the sample can be obtained from the variation of the optical reflectivity (ΔR) and a linear approximation of the relationship between the temperature change and the reflectivity variation: $\Delta T = \kappa^{-1}(\Delta R/R)$, where R and κ are the optical reflectivity and the thermoreflectance coefficient, respectively.

In this presentation, we demonstrate a CCD-based thermoreflectance microscopy system and their applications, such as quantitative surface temperature measurement of semiconductor devices, hot spot detection for failure analysis of semiconductor integrated circuits.

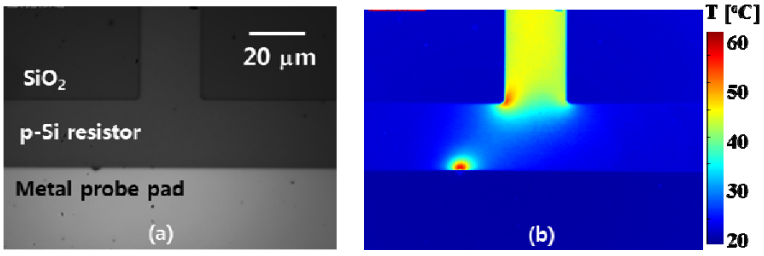

Fig 1. (a) Optical microscope image (b) Temperature image measured by TRM

[1] I. Jo et al., *Nano Lett*. 11, 85 (2011).
[2] D. Chae et al., *Nano Lett*. 9, 1883 (2009).
[3] K. S. Chang et al., *Sensors* 12, 4648 (2012).
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[5] W. J. Choi et al., *Opt. Lett*. 38, 3581 (2013).

Quantifying precision limit for multichannel spectroscopic ellipsometers

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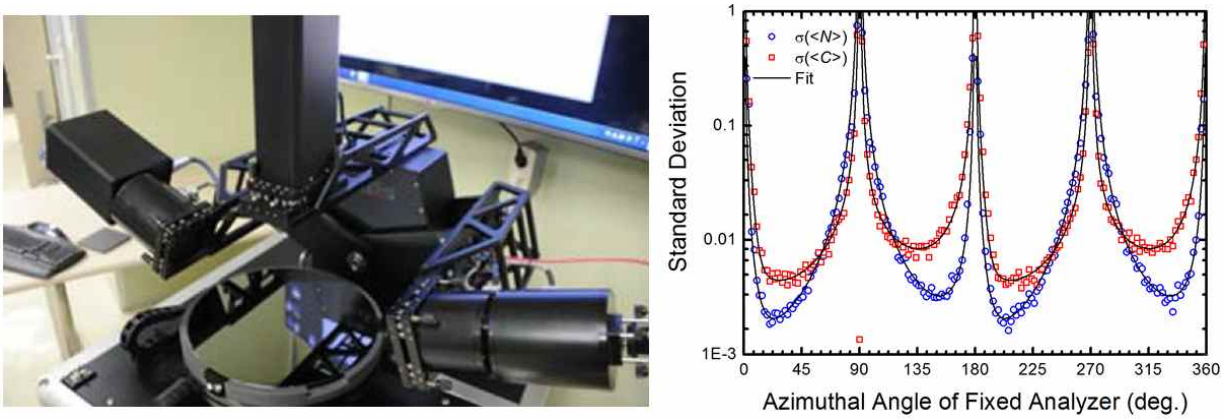
The requirements for enhancing ellipsometric accuracy become more stringent especially in the semiconductor industries but there is no generally accepted method for characterizing or quantifying ellipsometric data accuracy [1]. For the acual spectroscopic ellipsometers, there are temporal random noises due to stochastic fluctuation in the exposures measured during a given integration time by a CCD arrays. Using a novel ellipsometric data acquisition method [2], we analyzed experimentally the error propagation from the measured Fourier coefficients of the irradiance waveform to the ellipsometric sample parameters [3]. In this presentation, we show that the closed-form expressions of ellipsometric sample parameters can be evaluated from the Fourier coefficients using the method of least squares. To quantify the ellipsometric data uncertainties due to the random noises, we obtain the standard deviations and correlation coefficients of the unnormalized Fourier coefficients formulated analytically for the novel data acquisition method and then analyze the error propagation from the measured exposures to the ellipsometric sample parameters [4].



Home-made multichannel spectroscopic ellipsometer (left) and measured precision limits (right)

[1] M. Losurdo, Thin Solid Films **519**, 2575 (2011).
[2] Y. J. Cho, W. Chegal, and H. M. Cho, Opt. Lett. **36**, 118 (2011).
[3] W. Chegal, J. P. Lee, H. M. Cho, S. W. Han, and Y. J. Cho, J. Opt. Soc. Am. **A 30**, 1310 (2013).
[4] Y. J. Cho, W. Chegal, J. P. Lee, H. M. Cho, to be submitted (2014).

2D-strain measurement in transistor by scanning moiré fringe imaging

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Strain enginnering is a key technology that can improve the electrical performance in semiconductor devices, and strain measurement is required in order to optimize the strain engineering. We report on the development of scanning moiré fringe (SMF) imaging that can measure strain field in a transistor with nanometer scale spatial resolution [1]. The SMF is appeared due to harmonic interference between scanning spacing and crystal lattice in high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image, as can be seen in Fig. 1(a). The SMF image is applied to the strain measurement of a transistor with SiGe embedded in a source and drain region [2]. The result of an example is presented in Fig. 1(b). The SMF imaging is a powerful method that can reveal the strain field, thus it allows for developing the strain engineering in modern devices.

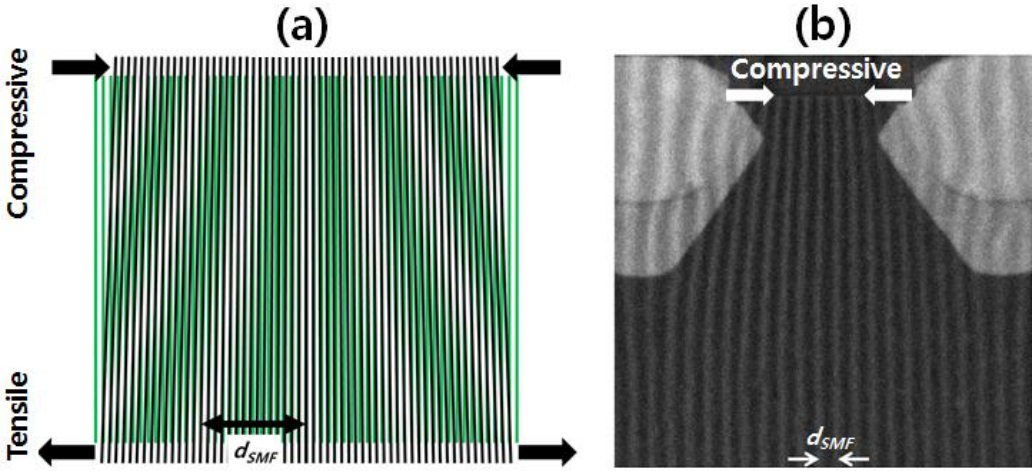

Fig. 1(a) Schematic view of SMF method. The SMFs are formed due to harmonic interference between scanning grating (green lines) and crystal lattice (black lines). (b) SMF image of a strained-channel-transistor. The compressive strain field in the channel region is revealed by SMFs.

[1] S. Kim, S. Lee, Y. Oshima, Y. Kondo, E. Okunishi, N. Endo, J. Jung, G. Byun, S. Lee, and K. Lee. **102**, 161604 (2013).
[2] S. Kim, Y. Kondo, K. Lee, G. Byun, J. Kim, S. Lee, and K. Lee. **103**, 033523 (2013).

XPS 를 이용한 Atomic Layer Deposition 된 Hafnium Oxide 박막과 Aluminum Oxide 박막의 전자 구조 측정

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Device 의 Design Rule 이 낮아질수록 그 전자 구조 특성을 개선하기 위하여, 많은 종류의 물질들이 사용되고 있다. 특히 Hafnium Oxide 및 Aluminum Oxide 막의 경우, DRAM Device 에서 Capacitance 물질로 이용[1]할 뿐만 아니라, 근래에는 EOT 를 줄이면서 실제 두께는 낮추지 않아도 되는 특성 때문에 MOS(Metal Oxide Semiconductor)구조의 Gate Oxide[2]로도 사용되어 반도체 전반에 사용되고 있다. 따라서 두 막에 대하여 전자 구조를 측정하는 것은 반도체 동작 특성을 이해하는데 필요한 요소이다.

이 Paper 에서는 Hafnium Oxide 와 Aluminum Oxide 막의 전자구조를 측정하기 위하여, 조성 및 화학구조측정에 많이 사용하는 XPS 를 이용하여 전자구조를 구성하는 인자(Band Gap[3], Work Function[4], Valence Band Offset[5])를 실제 측정하였다. 또한 측정된 결과를 통하여 Hafnium Oxide 와 Aluminum Oxide 막의 전자 Band 구조를 확인하였으며, 두 막이 접합 되었을 때의 예상과 실제 접합된 시료간의 차이를 밝히는 연구를 진행하였다.

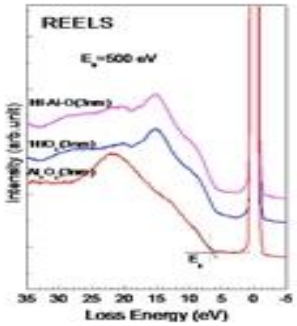

Fig1. HfO2 & AlO REELS Data[3]

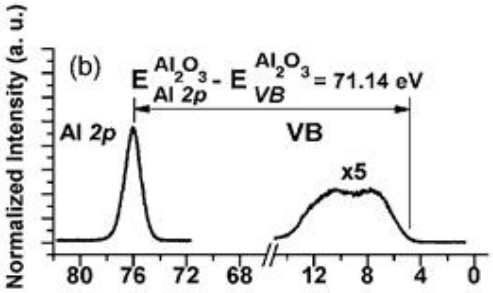

Fig2. A2lO3 Valence Band Data[5]

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고분해능 TEM 과 암시야 전자홀로그래피를 이용한 $In_xGa_{1-x}N$ MQWs 내 In 조성 및 격자변형의 정량적 분석

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$In_xGa_{1-x}N$ MQW 에 대한 정밀한 분석과 In 조성 및 격자변형에 대한 평가는 고효율 LED 발광소자의 특성향상을 위해서 매우 중요하다. 보통 수 나노미터 정도의 얇은 두께인 $In_xGa_{1-x}N$ MQW 의 분석에 있어서 미세 구조 관찰이 가능한 TEM 은 매우 유용한 분석 도구이다. 특히 고분해능 TEM(High resolution TEM; HRTEM)은 원자 단위의 분해능을 가짐으로써 In 조성에 따른 격자변형을 관찰할 수 있으며, 암시야 전자홀로그래피(Dark-field electron holography; DFEH) 기법은 시편 내부의 변형에 민감하기 때문에 LED 내부의 In 조성에 따른 격자변형 관찰에 유용하다. 본 연구에서는 GaN LED 의 MQWs 영역에서 In 조성 변화에 따른 격자변형 및 조성의 정량적 평가를 HRTEM 및 DFEH 를 이용하여 정밀하게 분석하고자 한다.

조성이 다른 single $In_xGa_{1-x}N$ layer 샘플 A 와 B 의 HRXRD 측정 및 시뮬레이션 결과, 각 샘플의 In 조성은 각각 8%와 14%로 RBS 결과인 8%, 14.4%와 거의 비슷했다. HRTEM 영상에서 *a* 면 격자간격의 변화는 없었으나 *c* 면 격자간격의 경우 각각 5.26 Å, 5.3 Å으로 In 조성이 늘어날수록 격자변형이 커졌다. 이 결과는 임계두께 이하에서의 후크의 법칙(Hooke's law)에 의한 것이며, In 조성에 따른 격자상수의 변화를 나타낸 그래프에 대입해 보았을 때 RBS 와 HRXRD 결과와 거의 일치하는 것을 알 수 있었다. LED 시편의 Low-In MQWs 와 High-In MQWs 의 영역에서 촬영한 HRTEM 영상에서 *c* 면 격자에 대한 간격을 측정해본 결과, 각각 5.26 Å, 5.31 Å였고 이것으로 MQWs 의 In 조성을 계산하였을 때 Low-In 영역과 High-In 영역의 In 조성은 각각 8±1%, 14.5±1%였다. 이 결과는 HRTEM 기법을 이용하여 복잡한 MQWs 구조에서 In 조성을 구할 수 있음을 보여준다. 마지막으로 HRTEM 과 DFEH 기법을 이용하여 격자변형을 측정해보았다. $In_xGa_{1-x}N$ layer 의 HRTEM 영상에서 격자상수를 바탕으로 격자변형을 계산했을 때 약 2.8%였다. DFEH 기법을 이용하여 구한 격자변형 매핑 영상에서 격자변형은 약 2.5% ~ 4%로 이는 HRTEM 으로 측정한 결과와 비슷하다. 따라서 본 연구에서 수행한 분석기법들은 복잡한 나노구조의 조성 및 격자변형을 정량적으로 분석하는데 유용하게 활용될 수 있을 것으로 기대된다.

감사의 글: This research was supported by the Technology Innovation Program, 10048393, Core Technology Development of the Measurement and Analysis Techniques for the Promotion of Nanotechnology Commercialization funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

2D strain measurement in sub-10 nm SiGe layer with dark-field electron holography

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Dark-field electron holography (DFEH) is a powerful transmission electron microscopy technique for strain measurement [1]. The two-dimensional (2D) strain mapping in sub-10 nm SiGe layer was carried out using this technique. The dark-field electron hologram was obtained from the (400) spot with bias of voltage of +25 V. From the results, we could successfully analyze the 2D strain mapping along the [100] growth direction. The obtained dark-field electron hologram was interpreted and the strain distribution in the very thin SiGe layer was visualized. The strain was measured in the range of 1.8-2.4 %. The strain precision was evaluated about ~2.5 × 10^{-3}. As a result, the DFEH technique is useful for measuring the 2D strain mapping in the sub-10 nm SiGe layer with nanometer resolution and high precision [2].

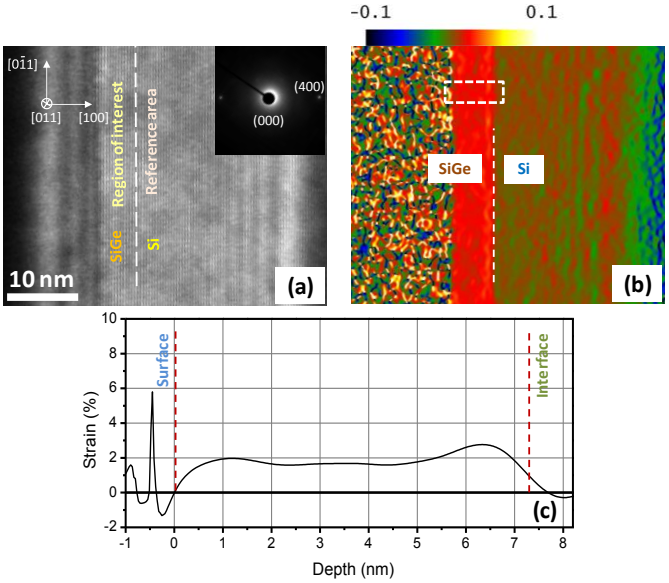

Fig. 1. (a) Dark-field hologram from the (400) diffracted beam, and the two beam condition inset. (b) Reconstructed phase image. (c) Strain map along the [100] direction. (d) Strain profile extracted from the strain map indicated by the white dashed box in (c).

Acknowledgement
This research was supported by the Technology Innovation Program, 10048393, Core Technology Development of the Measurement and Analysis Techniques for the Promotion of Nanotechnology Commercialization funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

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Highly Conformal Graphene Devices on Uneven Substrate

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Recently, conformal device on uneven surface have received great attention because of its multifaceted applications such as healthcare monitoring system [1], and wearable electronics which are difficult to achieve with planar layout. Graphene can be an ideal choice as a constituent material for conformal device because it combines an atomically thin thickness, resulting extraordinary mechanical flexibility and optical transmittance [2]. In this work, we demonstrate graphene based conformal devices that can be conformally integrated onto uneven surface of animal hide. The graphene field effect transistors have ultrathin, device thickness less than 70 nm, by direct applying a polymer medium film used for transfer process of graphene sheets to a gate insulator, which results in much lower bending stiffness (EI ~1.24 GPa·μm^4) than any reported values and excellent conformal coverage over the uneven surface without any adhesive layer. Another notable advantage of the conformal UT-GFETs was the good mechanical stretchability across three-dimensionally curved surfaces.

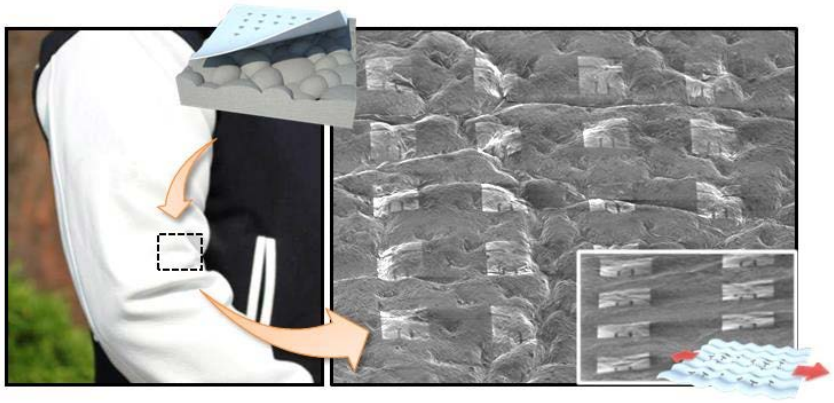

Fig 1. SEM images of the UT-GFETs on the animal hide substrate. The inset image shows mechanically stretched UT-GFETs under a 5% extension.

[1] Dae-Hyung Kim, J. Viventi, J.J. Amsden et al., Nat. Mater. 9, 511 (2010)
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Nanotube-on-Graphene Heterostructures for Smart Nano/Bio-Interface

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Living biological systems communicate with their external environment via pore-forming membrane proteins. These membrane proteins, or ion channels, regulate intracellular ion concentrations, and are fundamental to the physiology of living cells and tissues. However, conventional electrophysiology techniques that are used to study such ion channel activities [1, 2], such as voltage/current clamp and patch clamp methods, tend to be invasive or even destructive. Consequently, non-invasive and high-resolution electrical detection of ion channel activities in living cells and tissues is critical to the next phase of electrophysiology. We fabricate the nanotube-on-graphene biosensors as a high performing, mechanically robust and minimally invasive sensor platform to study biomaterials and biosystems. Nanotubes are utilized as an artificial nanofluidic channel which connects the graphene field effect sensor with the intracellular medium of cells/tissues. We also check the transfer curve of the graphene field effect sensor shifts to higher gate voltage with the increase of pH. The nanoscale nature of the nanotubes may ensures high resolution sensing and noninvasive interface with biosystems.

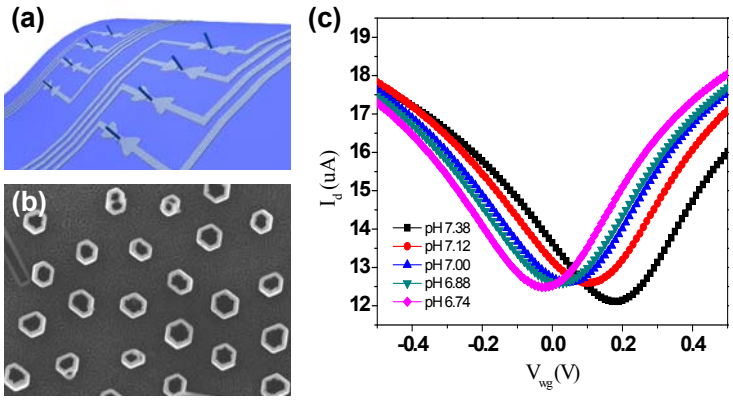

Fig 1. (a) Schematic image of sensor array, (b) SEM image of vertical nanotube array on graphene, and (c) I_d-V_g curves of the Graphene field effect sensor at different pH

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Buried gate Graphene FET 의 게이트 절연막 scaling 연구

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Graphene 과 같은 2D 물질을 이용한 새로운 논리 소자를 개발하기 위해서는 local gate 를 가지는 FET 소자를 제작하고 이를 연결하여 회로를 구성하여야 하는데, graphene 고유의 특성으로 인하여 graphene 상에 얇고 균일한 유전체를 증착하는 것이 쉽지 않다. 이를 해결하기 위해 금속을 얇게 증착한 후 산화시켜 유전체를 형성하거나, Atomic layer depposition (ALD) 공정 상의 변화를 주어 유전체를 증착하는 시도가 계속 되고 있다. 그럼에도 불구하고, 얇은 유전체를 이용하여 제작된 소자들의 균일한 동작 특성을 확보하는 것은 여전히 큰 도전 과제로 남아 있다. 이번 연구는 buried gate 구조를 이용하여 graphene 을 전사하기 전에 ALD 공정을 이용하여 저온에서 균일하고 안정적인 유전체를 gate 금속 위에 먼저 증착함으로써, graphene 상에 불균일한 유전체가 증착되는 문제를 근본적으로 해결하고, 소자들 간의 균일한 성능을 확보하여, 게이트 절연막이 scaling 된 상태에서의 소자특성을 분석하고자 하였다.

Fig.1 에 소자의 단면구조를 보였는데, buried metal gate 위에 ALD 공정을 이용하여, 7.5nm(50cycle), 12.9nm(100cycle), 24.6nm(200cycle)의 Al_2O_3 절연막을 증착 했다. 이후 graphene 을 전사하고 patterning 하여, buried gate 소자를 제작하였으며, 마지막으로 소자 안정성을 확보하기 위해, passivation 용 Al_2O_3 를 30nm 를 증착 했다. 7.5nm 절연막의 경우, Fig.2 에 보인 것과 같이 동일한 V_g-V_{Dirac} 에서 7.5nm 절연막의 경우, 24.6nm 절연막과 비교하여 전류가 67% 증가하여 소자 특성이 대폭 향상되었으며, 소자의 특성도 상당히 균일한 것을 알 수 있었다. 이로써, graphene 소자의 불안정성이 기판과 graphene 의 계면에 크게 영향을 받는 다는 것을 확인할 수 있었으며, top gate graphene 소자와의 특성비교를 통해, top gate graphene 소자를 최적화하는 데 필요한 정보를 얻을 수 있을 것으로 예상된다.

Acknowledgments: This work was supported by the Global Frontier R&D Program (2013M3A6B1078873) on Center for Hybrid Interface Materials (HIM) funded by the Ministry of Science, ICT & Future Planning.

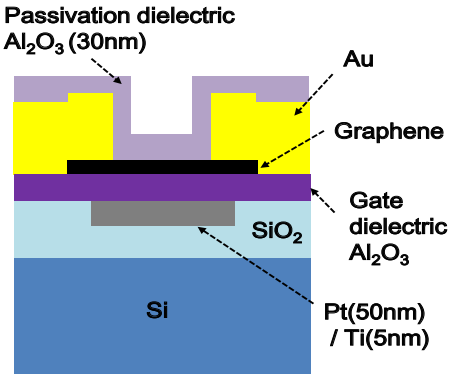

Fig.1. Buried gate 소자 단면도

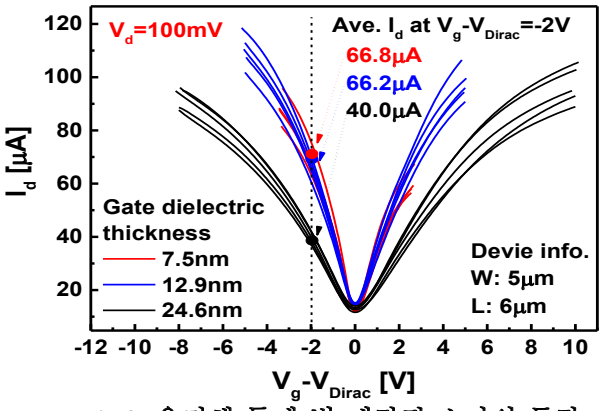

Fig.2. 유전체 두께 별 제작된 소자의 동작 특성 비교

Electrical Characteristics of Graphene Field Effect Transistors on Stainless Steel (STS) Substrate

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Top-gated Graphene transistors with Al_2O_3 gate-dielectric on the flexible stainless steel substrate have been fabricated and characterized. Graphene was synthesized on copper foil using a chemical vapor deposition method and transferred onto the STS substrate by wet transfer technique [1]. The stainless steel substrate was polished by chemical mechanical polishing method and the spin-on-glass layer was coated on the surface to improve the surface roughness. The average surface roughness Ra was as low as 5.9 nm from the AFM measurement. The meausred hole and electron mobilities were 310 and 43 cm^2/Vs, respectively. In order to evaluate the device performances with flexible situation, the device was put under the bending test with a bending radius 1.5 cm~5 cm. It turns out that the mobility was degraded down to 40% of its initial value. One of the advantage of using the STS is to apply higher surrounding temperature. Norminal plastic substrate showed a poor performances with thermal stress. Here we increse the temperature up to 355 K. The mobility was inversely proportional to the temperature with little hysterisis, compared to a plastic substrate. [2].

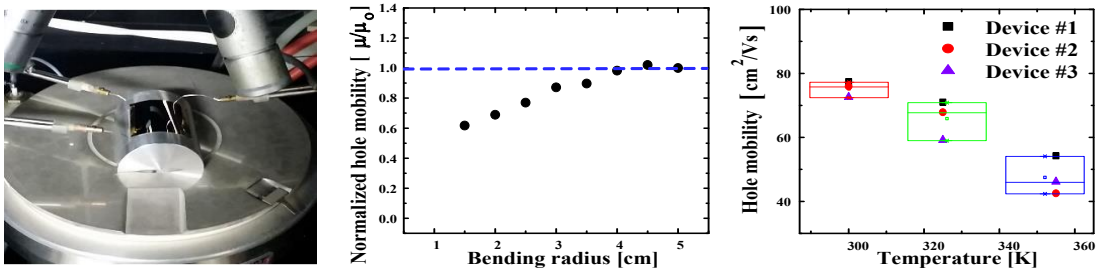

Fig 1. (a) graphene FET on the STS substrate under measurements, (b) Mobility behavior vs. mechanical stress, and (c) Mobility degradation vs. ambient temperature

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Addressing Bathtub Failure Curve of SSD by FS-RAID Scheme

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The advent of MLC (Multi-Level Cell) and TLC (Triple-Level Cell) flash memory leads to increased capacity along with decreased reliability of SSDs. Generally, failure rate of a storage device follows the bathtub curve shown in Fig. 1 [1]. The curve can be divided into three regions according to lifetime stage, namely EFP, CFP, and WFP. In early stage of lifetime denoted as EFP in Fig. 1, a device shows high failure rate. Then, the device shows low and stable error rate in CFP region. Finally, device error rate increases again in WFP region as its lifetime expires. Specifically, SSDs suffers from high bit error rate as flash memory undergoes P/E (Program/Erase) cycles. Though error rate of SSDs has this bathtub curve, most SSDs use the ECC scheme with fixed strength against failures. Hence we propose *Flexible Strength RAID (FS-RAID)* scheme that employs RAID configuration and dynamically adjusts its strength against failures according to the typical failure rate of the device lifetime. Specifically, to face high failure rate of the EFP region, FS-RAID employs RAID-6 configuration that writes two parties in a stripe. In CFP region, it uses RAID-5 configuration that writes one parity in a stipe. In WFP region, it again employs RAID-6 configuration to cope with high failure rate. With analytic models derived in [2] and parameters obtained from simulation results of 128GB SSD with TLC chips under Financial workload, we calculate error rate of a SSD employing FS-RAID scheme and compare them with SSDs using three different schemes, namely, ECC-only, RAID-5, and eSAP. Particularly, eSAP scheme employs log-structured style RAID-5 configuration but does not change its configuration according to the error rate variation [2]. Fig. 2 shows Uncorrectable Page Error Rate (UPER) and P/E cycles of four schemes, where X-axis denotes total amount of data written to the SSD in TB (Tera Byte) unit and names in the parentheses represent lifetime stage of the device shown in Fig. 1. In Fig. 2(a), FS-RAID shows the lowest UPER in both EFP and WFP regions as it increases redundancy to cope with high failure rate in those regions. Also, though FS-RAID writes two parities in EFP and WFP regions, it shows longer lifetime than conventional RAID-5 due to its log-structured style RAID configuration and reduced number of parity updates as seen in Fig. 2(b) that presents average P/E cycles of flash memory.

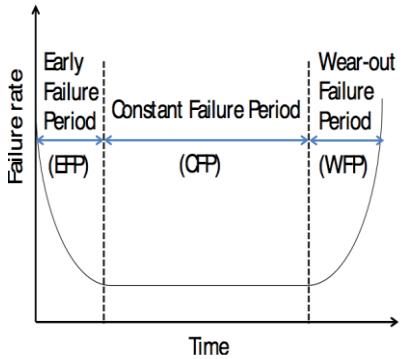

Fig 1. Bathtub Failure Curve

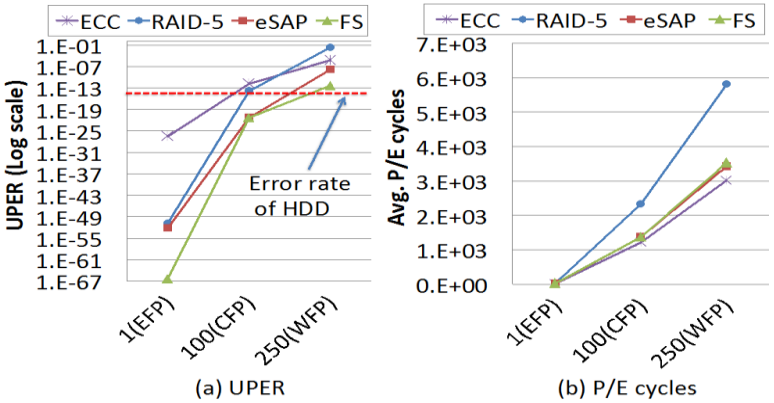

Fig 2. Comparison of UPER and P/E cycles with TLC SSD

[1] Guoqiao Tao, Bisschop J., Som Nath, "On intrinsic failure rate of products with error correction," IEEE Integrated Reliability Workshop Final Report, 2005
[2] Jaeho Kim, Jongmin Lee, Jongmoo Choi, Donghee Lee, S. H. Noh, "Improving SSD reliability with RAID via Elastic Striping and Anywhere Parity," IEEE DSN, 2013

Aggressively Exploiting Parity of RAID for Reliable Flash SSD

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2Xnm 이하의 미세공정과 MLC/TLC 방식의 기술로 인해 플래시 메모리의 용량은 증가했지만 신뢰성이 크게 하락하는 문제가 있다. 대부분의 상용 SSD 는 ECC 를 통해 에러율을 크게 낮출 수 있지만 교정 가능한 비트수가 제한되어 있으며 페이지 또는 칩단위의 오류에 대해서는 대처할 수가 없다. 이러한 한계를 극복하기 위해 SSD 내의 여러 칩을 RAID-5 형태로 구성하는 기법이 제안되었다[1]. RAID-5 기법을 도입하는 경우, 스트라이프당 하나의 페이지를 패리티용도로 사용하지만 활용도는 극히 제한적이다. RAID 패리티는 ECC 가 페이지내의 오류를 검출한 경우에만 오류 복구용도로 사용된다. 본 논문에서는 RAID 의 패리티를 보다 적극적으로 활용하여 SSD 의 신뢰성을 향상시킬 수 있는 방안을 다음 두 가지 방법으로 제안한다. 첫째, CRC (Cyclic Redundancy Check)와 같은 해시함수로 오류검출범위를 증가시키고 패리티를 이용해 복구하는 방법이다. 대부분의 상용 SSD 에서 사용하는 ECC 는 페이지당 오류 비트를 n 개까지 교정할 수 있고, 2n 개까지 검출할 수 있다. n+1 ~ 2n 개의 검출된 오류는 패리티를 통해 복구할 수 있지만, 2n 개 초과된 오류는 검출할 수 없으므로 시스템이나 응용소프트웨어가 오작동할 때까지 발견되지 않으므로, 치명적인 문제를 야기시킬 수 있다[2]. 이에 대한 해결방안으로, 그림 1 과 같이 각 페이지의 OOB 공간에 에러 검출용 CRC 코드를 m 비트(1.E-16 에러율을 보장하기 위해서 54 비트 필요) 저장하여 검출 가능 비트수를 증가시키고 검출된 에러는 패리티를 이용하여 교정한다. 둘째, ECC 를 이용한 오류 교정 시 발생하는 페이지 쓰기를 패리티를 이용해서 최소화하는 것이다. 기존 방식은 오류 검출 시 ECC 로 교정 후 즉시 새로운 페이지에 기록한다. 이때 발생하는 추가적인 쓰기를 줄이기 위해서, 그림 2 와 같이 n 비트 이하만큼 오류가 누적될 때까지 쓰기를 미루는 방법이 제안되었다[3]. 본 논문에서는 그림 3 과 같은 절차의 에러 교정 방법을 제안한다. 그림 3 의 "Decision" 단계에서 대상 페이지의 오류 비트수, P/E 횟수, 데이터 쓰인 시간, 에러율을 기준으로 3 가지 경우로 구분하여 처리한다. Case #1 은 P/E 횟수나 데이터 쓰인 시간이 오래되지 않고 오류 비트수가 적은 경우로 교정 후 쓰기를 미룬다. Case #2 는 P/E 횟수나 에러율이 높은 경우로 ECC 를 이용해 교정 후 페이지 쓰기를 한다. Case #3 은 ECC 로 교정가능한 범위를 초과한 오류가 발생한 경우로 패리티를 이용해 교정 후 페이지 쓰기를 한다. "Decision" 은 페이지 상태에 따라서 동적인 결정이 가능하므로 오류에 대한 유연한 대처가 가능하고 페이지 쓰기를 최소화할 수 있다. 제안하는 두 가지 방법을 통해 신뢰성 향상이 가능하며 성능 향상 또한 기대할 수 있다.

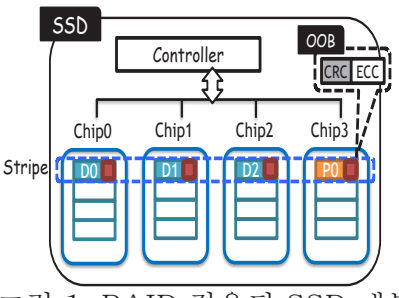

그림 1. RAID 적용된 SSD 내부

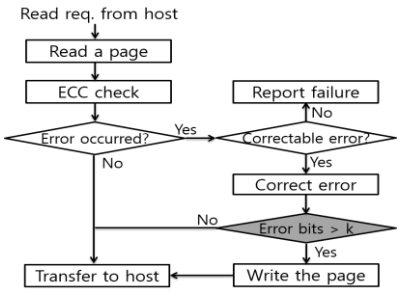

그림 2. ECC 이용한 오류교정

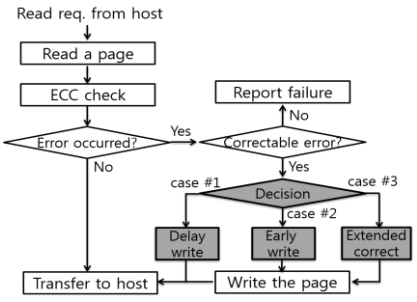

그림 3. 제안하는 방법

[1] J. Kim, J. Lee, J. Choi, D. Lee and S. H. Noh, "Improving SSD Reliability with RAID via Elastic Striping and Anywhere Parity," IEEE DSN, 2013
[2] J. L. Hafner, et al. "Undetected disk errors in RAID arrays," IBM Journal, 2008
[3] S. Moon and A.L.N. Reddy, "Write Amplification due to ECC on Flash Memory or Leave those Bit Errors alone," IEEE MSST, 2012

Model and its Implication for PIM (Processing in Memory)

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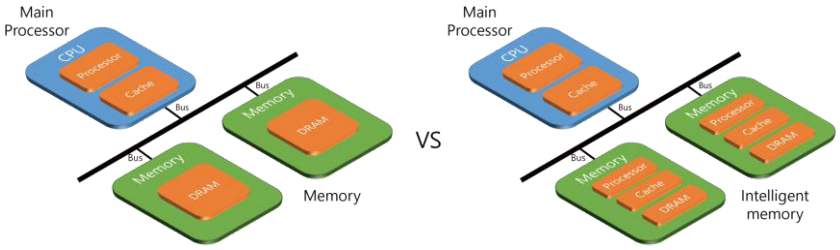
CPU, 메인 메모리, 디스크 등 컴퓨터 시스템을 구성하는 컴포넌트의 성능은 지속적으로 향상되고 있다. 그러나 SDRAM 으로 대변되는 메인 메모리와 CPU 의 데이터 처리 속도에는 상당한 격차가 존재하며, 이는 컴퓨터 시스템 성능의 주된 병목 지점으로 작용된다. 따라서 최근 발표되는 CPU 는 고속/대용량의 캐쉬 메모리를 장착하고 있으며, 선 반입(pre-fetching) 등의 다양한 최적화 기법이 사용되고 있다. 최근 활발히 연구되고 있는 PIM(Processing In-memory) 기법은 컴퓨터 시스템의 성능 향상을 위한 새로운 방향을 제시한다[1]. PIM 은 메모리 접근 량이 많은 메모리 중심 작업을(memory-bound job) CPU 개입 없이 메모리 장치 내에서 직접 처리함으로써 컴퓨터 시스템의 성능 향상을 도모한다. 즉, PIM 은 메모리 접근을 수반하는 작업을 메모리 장치 내에서 처리하는 일종의 분산 처리 기법이다[2,3]. 이에 따라 본 논문에서는 PIM 이 도입된 시스템의 성능 모델을 제안한다. 제안된 모델은 CPU 와 PIM 이 가지고 있는 데이터 처리 능력과 메모리 접근 시간을 고려하여, 프로그램 실행 시 얻을 수 있는 성능 향상에 대한 객관적인 평가를 가능케 한다. 본 논문에서는 다양한 워크로드를 사용한 모델링 결과를 분석하며, 메모리 중심 작업을 분산시킴으로써 PIM 이 적용된 메모리를 사용하여 얻을 수 있는 성능 향상에 대한 정량적 평가결과를 보인다.



$$I_{total} = I_{cpu} + I_{memory}$$
$$ET_{cpu} = (1 - ER_{memory}) \times I_{total} \times (CPT_{computing} + CPT_{memory})$$
$$ET_{pim} = ER_{memory} \times I_{total} \times (MPT_{computing} + MPT_{memory})$$
$$ET_{total} = ET_{cpu} + ET_{pim}$$
$$(0 \le ER_{memory} < 1,\ CPT_{computing} < MPT_{computing},\ CPT_{memory} > MPT_{memory})$$

그림 1. PIM 구조 및 성능 측정 모델

[1] Gabriel H. Loh, Nuwan Jayasena, Mark H. Oskin, Mark Nutter, David Roberts, Mitesh Meswani, Dong Ping Zhang, and Mike Ignatowski, "A Processing-in-Memory Taxonomy and a Case for Studying Fixed-function PIM", WoNDP (2013).
[2] David Patterson, Thomas Anderson, Neal Cardwell, Richard Fromm, Kimberly Keeton, Christofors Kozyrakis, Randi Thomas, and Katherine Yelick, "A Case for Intelligent RAM: IRAM", Micro, IEEE (1997).
[3] Mark Oskin, Frederic T. Chong, and Timothy Sherwood, "Active Pages: A Computation Model for Intelligent Memory", IEEE Computer Society (1998)

Virtual Fence for controlling for animals using Flash Memory Storage

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Virtual fence is a way to control animals by placing a visually unseen boundary around animals or landscapes such as conventional fencing. The boundary can be any shape, rectangle or polygon, and is constructed with embedded computer systems [1]. The embedded computer systems use flash memory based storage system for the protection from external impact. Flash memory is now an indispensable storage component for embedded devices. The performance improvement of the flash memory based storage is the important factor of embedded systems [2]. By using the virtual fence, the cost is cut down and the movement of the animal is controlled or the invasion of animal from outside of virtual fence can be detected. In this paper, we present virtual fence structure that uses embedded system using GPS device. The proposed a virtual fence can detect the animals for going out the virtual fence and send a warning signal such as sound or vibration to the animals.

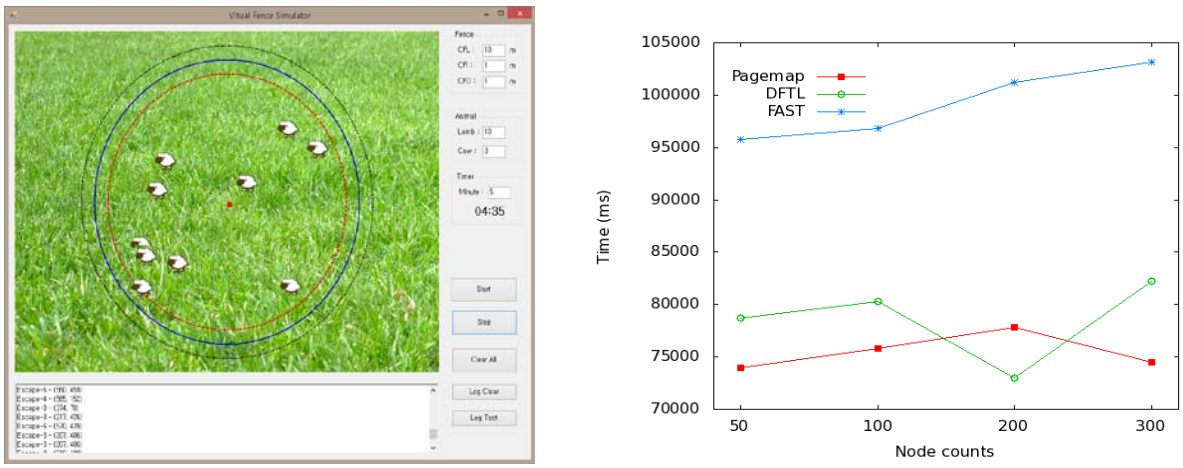

Fig 1. Simulation program and result data

[1] J. Chen, T. Tseng, C Lai and S. Hsieh Xu, "An Intelligent Virtual Fence Security System For the Detection Of People Invading," International Conference on Ubiquitous Intelligence & Computing, pp.786 - 791, 2012
[2] Seungjae Baek, Jongmoo Choi, Donghee Lee and S. H. Noh, “Energy Efficient and High Performance Software Architecture for Storage Class Memory," ACM Transactions on Embedded Computing Systems (TECS), Vol. 12, Issue 3, Article No. 81, Mar, 2013
* Corresponding Author : Heung Suk Jeon

An Implementation of a Module for Retaining Legacy File System Compatibility while Improving I/O Performance for New Memory based Systems

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New memory technologies represented by PRAM and STT-MRAM are suitable mediums for high performance storage systems as they are non-volatile and yet, provide random byte addressability and latency similar to DRAM [1]. In this study, we present an architecture of a novel I/O processing module for new memory storage that we call NTL (New memory Translation Layer). NTL allows for file systems to retain the use of legacy file systems providing compatibility and maturity, while transparently attaining high I/O performance through new memory. We implement our approach on the Linux v3.10.4 kernel. As shown in Figure 1, for compatibility, the NTL is added in the I/O stack as a module allowing the rest of the operating system to remain untouched. For high I/O performance, NTL is implemented to directly absorb I/O data without going through the traditional block I/O software layer. Then, block level requests are translated to byte-addressable requests to exploit the beneficial traits of new memory. Preliminary results show that we can attain bandwidth of over 700MB/sec, which is well over the performance observed in high-end SSDs.

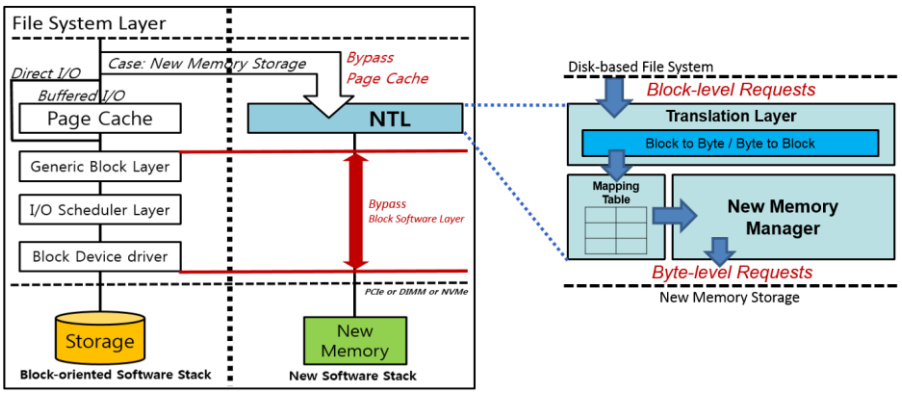

Figure 1. Architecture of new OS stack apply NTL

[1] S. Eilert, et al, "Phase Change Memory: A new memory technology to enable new memory usage models," In Memory Workshop, IEEE International, (IMW'09), 2009.

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반도체소자 배선을 위해 직접전해도금에 의한 구리-은 합금 박막 형성 연구

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Keywords: Cu-Ag alloy, seedless electrodeposition, interconnect

현대시대에 접어들어 전자소자가 소형화, 고성능화되면서 내부배선도 점점 축소되고 복잡한 구조를 가지게 된다. 이처럼 내부배선의 크기가 줄어드는 것에 반비례하여 단면적 당 큰 전기에너지를 전달하기 때문에 배선의 신뢰도를 떨어뜨리는 현상인 electromigration과 stress induced voids에 대한 저항을 높일 수 있는 방법이 중요시 되고 있다. 기존배선의 재료로서 알루미늄을 대체하여 더 우수한 전기 전도도와 이동현상에 대한 저항성을 가진 구리를 사용한 것도 같은 맥락이다. 그러나 구리도 소형화, 복잡화 되는 배선에서 한계를 가지기 때문에 은, CNT와 같은 차세대 재료를 연구 및 개발하려는 시도가 많다. 하지만 경제적, 실용적인 측면에서 아직은 미흡하기 때문에 구리-은, 구리-팔라듐, 그리고 구리-주석 등과 같은 구리합금을 사용하여 배선을 형성하는 연구활동 역시 다양하다. 본 연구에서는 구리보다 전기 전도도와 기계적 성질이 우수한 은을 구리와 합금해 구리-은 합금 박막을 확산방지막 상에 직접 전해도금하는 공정을 진행하였다. 이 공정은 건식/진공 증착 공정에 비해 상대적으로 공정의 설비 및 과정이 간단하여 경제적이고, 증착 속도가 높아 생산적인 장점이 있다. 높은 종횡비로 된 패턴을 결함 없이 채우기 위해 확산방지막 위에 씨앗층을 형성하는 기존의 공정을 사용하지 않고 확산방지막 상에 직접 전해도금을 실시하는 공정을 채택하였다. 또한 $CuSO_4$, $AgNO_3$으로 구성한 전해질에 밀도가 높고 조도가 우수한 구리-은 합금층을 형성하기 위해서 첨가제와 착화제를 사용하였다. 상대전극은 그물 형태의 백금을 사용하였으며, 작업전극은 100 nm 텅스텐 확산방지막을 증착한 실리콘 웨이퍼 시편을 테플론 하우징에 장착하여서 사용하였다. 순환전압전류법과 정전위 증착법 등과 같은 전기화학적 분석법을 기본적으로 사용하여 환원전위, 농도, pH와 같은 변수에 따른 구리-은 도금막질의 물성 변화를 분석하였다.

Characterization of Mn-based self-forming barriers on low-k samples with or without UV curing treatment

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In the present work, we report a Cu-Mn alloy as a material for the self-forming barrier process, and we investigated the diffusion barrier properties of the self-formed layer on low-k dielectrics with or without UV curing treatment. Cu alloy films with 3.8 at.% Mn were directly deposited onto low-k dielectrics by co-sputtering followed by annealing at various temperatures. The self-formed layers were investigated by transmission electron microscopy (TEM) and energy-dispersive X-ray spectroscopy (EDS). In order to compare barrier properties between the Mn-based self-formed layer on low-k dielectric with UV curing and the interlayer on low-k dielectric without UV curing, thermal stability was measured at various thermal stress temperatures. Our results indicated that the formation of the barrier at the interface of Cu-Mn alloy/low-k dielectric was enhanced by UV curing due to changes in the porosity and C concentration in the dielectric layer.

Keywords: Copper interconnect, self-forming barrier, copper-manganese alloy, low-k dielectric

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Atomic layer deposition of Mo_2N thin film as a diffusion barrier against Cu

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The technological applicantions of Mo-based thin films such as its nitrides, oxides, sulfides are many including diffusion barrier for semiconductor matallication, hard coating, superconductor, sensor, channel layers, catalyst and etc. Among them Mo_2N are particulaarly interesting because it is a potential material as a diffusion barrier against Cu due to its high thermal and chemcal stability, reatively low resistivity, and excellent diffusion barrier performance [1, 2]. The device size will continue to shrink and novel 3D structure with high aspect ratio trench or hole structure with excellent thickness uniformity and prosess comtrollability is essential. In thes respects, atomic layer depsotion (ALD) for these materials have been drawn much attention bacause ALD uses a self-limiting film growth made by surface-saturated reartions, which enables atomic-scale control of the lack of suitable presurcur. In this study, Mo_2N thin films were deposited by ALD techniques using a novel nitrogen and sulfur containing Mo metallorganic precursor. By using H_2 plsma as a reactant, we could succesful grow the Mo_2N thin film (360 μΩ-cm) by ALD. For example, figure 1 show the grazing incidence angle ($\theta = 3°$) XRD pattern of typical ALD Mo_2N film deposited on SiO_2 substrate. Three peaks from cubic-structured Mo_2N crystal were clearly shown. And the inset figures (cross-sectional view SEM image) showed the successful growth of very smooth ALD-Mo_2N film. We applied the deposited Mo_2N thin film as a diffusion barrier between Cu and Si. The results showed that 4-nm-thick ALD Mo_2N (effectively prevented the diffusion of Cu up to 600°C. Finally, it should be emphasized that a performance of ALD-grown Mo_2N as a diffusion barrier in the device structures would superior to ones deposited by other processes because of its inherent excellent conformality and this advantage is becoming more significant as the device size shrinks.

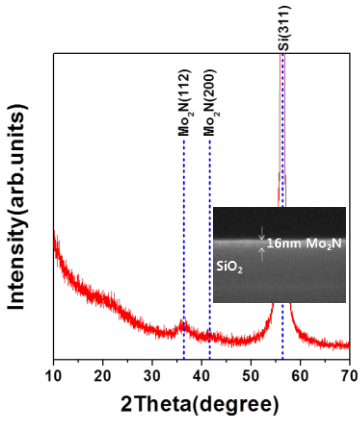

Figure 1. Typical XRD patterns of ALD-Mo_2N films deposited on SiO_2 substrate. The inset figure shows the cross-sectional view SEM image of ~16-nm-thick ALD-Mo_2N film.

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Acknowledgements

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Atomic layer deposition of Ru thin films using new zero valent Ru precursors

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Ruthenium(Ru) thin films are widely used as an electrode for the DRAM capacitor, a seed layer for Cu metallization, and a gate electrode due to its advantages including low resistivity(7.1 μΩ-㎝ for bulk), large work function (4.7eV), thermal, chemical stability and feasibility for the dry etch process. Due to the continuous scaling-down of the devices, atomic layer deposition can be a potential solution for preparing Ru thin films because ALD enables atomic-scale control of the film thickness with an excellent conformality. Recent investigations by us reported that Ru film nucleation was enhanced considerably using zero metal valence precursors, (1-methyl-4-isopropylbenzene) (1,3-cyclohexadiene) Ru(0) ($C_{16}H_{22}Ru$), (ethylbenzene)(1-ethyl-1,4-cyclohexadiene)Ru(0) ($C_{16}H_{22}Ru$), (ethylbenzene) (1,3-cyclohexadiene)Ru(0) ($C_{14}H_{18}Ru$), (EthylBenzene)(1,3-butadiene)Ru(0) (EBBDRu, $C_{13}H_{16}Ru$) [1~5] and molecular oxygen (O_2), compared to the utilization of precursors with higher metal valences, such as cyclopentadienyl-based Ru precursors, which have a metal valence of 2, or beta-diketonate Ru precursors, which have a metal valence of 3. In addition, the use of zero valence precursors has another advantages such as high growth rate and relatively low deposition temperature. In this study, we report Ru ALD processes using new zero metal-valence Ru precursors containing a η^6-arene ligand and the second η^4-butadiene derivative ligand instead of closed ring cyclohexadiene. Ru films were deposited using a traveling wave-type ALD reactor (Lucida D100, NCD Technology) using a sequential supply of new zero metal valence precursors and O_2 molecules at the deposition temperature ranging from 180 to 310°C and chamber pressure of 1 Torr. The representative results using a new Ru precursor showed short incubation cycle (~ 7 cycles) with a relative high growth rate of ~ 0.106 nm/cycle as shown by Fig. 1. The step coverage of ALD-Ru film deposited into ultra-small trench with an aspect ratio of ~ 4.5 (top-opening diameter: ~25 nm) was excellent, around 100% [Fig. 2]. The ALD-Ru films were evaluated as a seed layer for Cu electroplating and bottom electrode of high-*k* MIM capacitor with ALD-ZrO_2 as a dielectric.

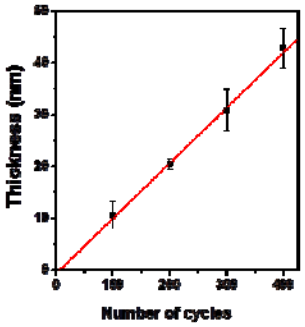

Figure 1.
Growth rate as a deposition temperature

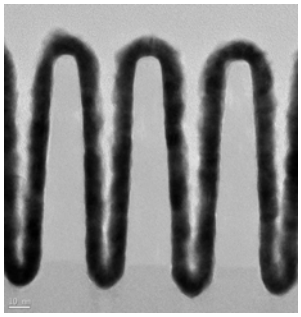

Figure 2.
Step coverage of ALD-Ru film

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Acknowledgements

This work was supported by BK21+ program and also partially supported by a KBSI Grant (T33524) to T.E. Hong.

Ultralow Interlayer Dielectrics for the Next Generation System LSI

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The next generation microchips call for ultralow dielectric materials (k < 2.2) to insulate the Cu interconnect or wires in BEOL shrinked by Moore's law. In order to reduce dielectric constant, pores (k = 1.0) have been introduced by decomposing sacrificial organic materials (porogens) in low dielectric materials. Although many types of porogens have been developed [1-2], it is difficult to satisfy the CMP-processibility of nanoporous ultralow dielectrics (ULKs) due to large and interconnected pore morphologies above certian porosity. This phenomenon has been very well known due to aggregation of porogens into large nano- or microphase domain by nucleation and growth mechanism during sol-gel condensation of low dielectric organosilicate. In order to solve this problem, we applied completely defferent concept of porogens called reactive porogens with trialkoxysilyl propyl end groups, which can participate in the sol-gel reaction of organosilicate. We designed several kinds of reactive porogens based on reducing sugars and organic polyols. These reactive porogens were very effective in prohibiting their aggregation, which led to closed nanopores with r < 2 nm even at k = 1.94. Also, they were possible to develope the nanoporous ULKs with superb mechanical properteis (E = 7.2 GPa and H = 1.0 GPa) at the porosity of 34.3%. These results indicate that the developed ultralow dielectrics are world-best in terms of both mechanical and dielectric properties, which may be applicable to ≤ 8 nm devices in the year of 2027.

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다층그래핀 성장과 EM 특성분석

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탄소 원자 한층으로 이루어진 2D물질인 그래핀은 원자간의 결합이 매우 강하며 전자 이동도가 굉장히 높은 물질이다. 이러한 그래핀의 저 저항 특성과 강한 본딩 특성으로 인해 그래핀은 차세대 배선 물질로 고려되고 있다. 그래핀을 반도체의 배선으로 사용하기 위해서는 단층 그래핀이 아닌 다층 그래핀이 필요하다. 본 논문에서는 다층 그래핀을 손쉽게 얻을 수 있도록 단층 그래핀 위에 적층 성장할 수 있는 다층 그래핀 성장법을 연구하였고, 이러한 다층 그래핀의 EM특성을 평가하였다.

먼저 다층 그래핀을 적층 성장하기 위해서 그래핀을 구리호일 위에 성장한 후 이러한 성장된 그래핀 위에 얇은 금속 박막을 추가 성장하여 그래핀 위에 성공적으로 다층 그래핀을 성장하였다.

우선 그래핀 성장은 화학기상증착법(CVD)을 이용하여 메탄과 수소 분위기에서 CMP 구리호일 위에 성장하였다. 이러한 성장된 그래핀 위에 열증착기를 이용하여 니켈막을 증착하였다. 그 이후에 두번째 적층 그래핀 성장을 Furnace CVD에서 1시간 성장하였다. 구리보다 탄소 고용도가 높은 니켈로 2차 성장을 하였기 때문에 1차 성장한 단층 그래핀보다 훨씬 두꺼운 다층 그래핀을 얻을 수 있었다. 이러한 다층 그래핀은 니켈호일 위에 성장된 다층 그래핀보다도 훨씬 균일하였다. 이렇게 성장된 다층 그래핀에 패터닝을 진행하여 Electromigration(EM) 특성을 분석하였다. 최대 허용 전류밀도는 $>10^8/cm^2$ 으로서 매우 높은 값을 가짐을 확인할 수 있었다.

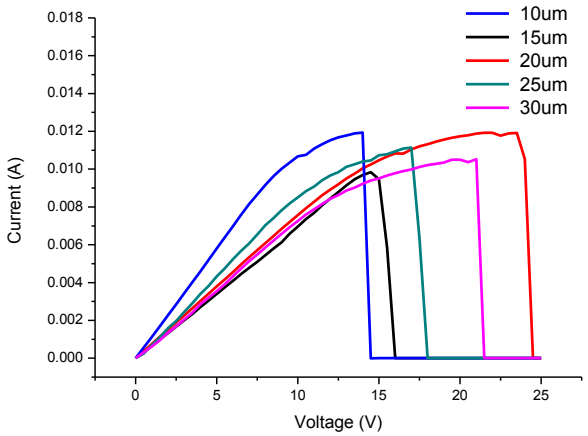

Figure 1 다층그래핀의 길이에 따른 Breakdown Voltage

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Cobalt-based Bi-functional Layer for Cu Interconnect by Atomic Layer Deposition

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As Si device structures become even more complex and smaller, the line width of Cu interconnect has been decreased accompanying with reduction of diffusion barrier and seed layer thicknesses. Since the diffusion barrier and seed layer cannot maintain their physical continuity as well as desired properties below several nanometers in thickness, other approaches are required, such as thickness reduction and process simplification by using a bi-functional layer. Cobalt and its alloy materials have been investigated for diffusion barrier or seed layer separately but not for a bi-functional layer.[1] The polycrystalline microstructure of Co is disadvantageous as a diffusion barrier due to the presence of grain boundaries which are potential diffusion paths.

In this research, we suggest alloying Co and TiN to form CoTiN which has amorphous microstructure for the bi-functional layer by using atomic layer deposition (ALD).[2] We developed the Co ALD and TiN ALD separately using Bis(N-tert-butyl-N′-ethylpropionamidinato)Cobalt(II) [$Co(AMD)_2$] as Co precursor and Tetrakis-(di-methylamino)-titanium [TDMAT] as TiN precursor. The NH_3 gas was used as a counter reactant and the substrate temperature was 200 °C in both Co ALD and TiN ALD. The alloying process was performed by supercycle of ALD Co and ALD TiN and the cycle ratio was controlled to change film composition. The microstructure, diffusion barrier property and seed layer property were investigated by changing film composition. In addition, the deposition conformality of ALD CoTiN film was examined in nanoscale interconnect patterns.

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TiO_2-SiO_2 Laminated Films grown by Plasma Enhanced Atomic Layer Deposition.

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TiO_2-SiO_2 laminated films were grown on the Si substrate by plasma enhanced atomic layer deposition (PEALD) method. The cycles of lamination between TiO_2 layer and SiO_2 layer have been controlled respectively to observe TiO_2 crystalline structure change. Several nano-sized crystalline seeds of anatase phase were observed at pure TiO_2 film in TEM analysis. Both pure TiO_2 film and 20:1 cycle ratio of films have anatase crystalline phase in XRD pattern after post-annealing process at 400°C and N_2 environment. However, films less than 10:1 lamination cycles were kept the amorphous phase even after post-annealing process. And also particles assumed by crystal induced were not observed on the film surface less than 10:1 cycle ratio. It is considered that SiO_2 layers inside TiO_2 laminated film played a role as disrupter for crystallization of TiO_2 films. Therefore, the lamination method of TiO_2-SiO_2 has been proved as an effective method to keep the film in amorphous phase and good surface morphology at required process condition.

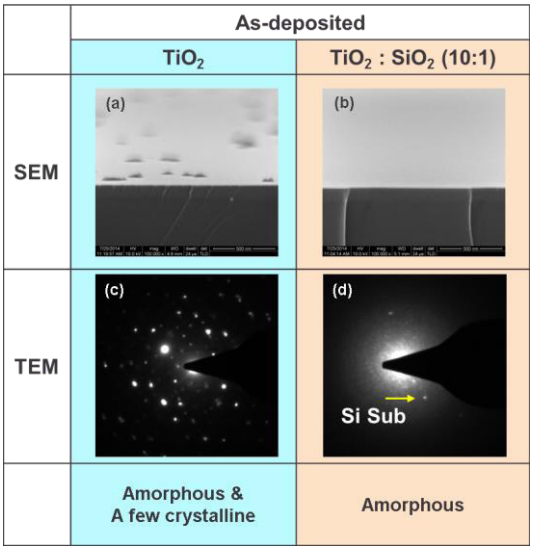

Fig. 1 (a), (c) SEM and TEM image of TiO_2 film and
(b), (d) SEM and TEM image of laminated TiO_2 film (10:1)

A study of current crowding and its effects on the carrier spill-over in InGaN/GaN Blue Light Emitting Diodes.

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Since conventional GaN-based light-emitting diodes (LEDs) grown on the sapphire substrates are using mesa structure for current injection, the current flows have both vertical and horizontal components. In these LEDs, the distribution of current density in horizontal direction cannot be totally uniform. The non-uniform current flows may cause non-uniform light emission and degradation in the external quantum efficiency. This effect is called the current crowding effect[1-2]. In this study, we analyzed the degree of current crowding and its effects on the carrier spill-over and resultant external quantum efficiency in InGaN/GaN blue LEDs. We further show that the non-uniform distribution of carrier resulted in different external quantum efficiency (EQE) as a function of the distance from p-contact edge, which can make a significant effect on the efficiency droop at high current. In this study, we analyzed the degree of current crowding and its effects on the carrier spill-over and resultant external quantum efficiency in InGaN/GaN blue LEDs. 1.7 times larger carrier spill-over was observed where the current crowding was measured to be 3.1 times lager, which means the current crowding enhance current overflow. Increasing current 2.5 times was shown a 2.42 times increases loss of light. These results suggest that current crowding is a important factor of efficiency droop at high current. Although several mechanisms have been suggested to explain the droop, including electron leakage at heterointerfaces, poor hole injection efficiency, indium-rich regions, we show that the current crowding effect that increases with the current density is one of the major causes of the efficiency droop.

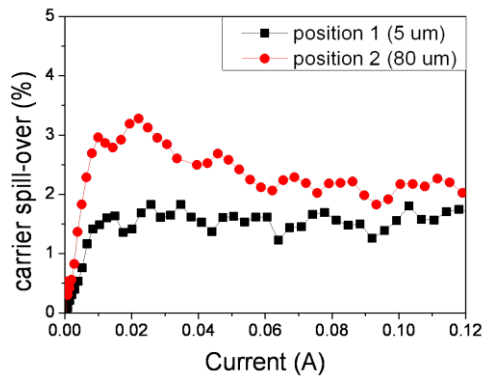

Fig. 1. Experimental result of carrier spill-over as a function of injection current on a position 1 and position 2

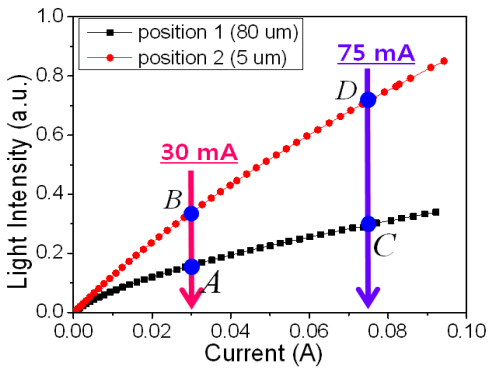

Fig. 2. Experimental result of emission intensity as a function of injection current on a position 1 and position 2

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Effect of p-AlGaN electron blocking layer on efficiency droop and identification of the dominant mechanism for the droop in InGaN/GaN MQW LEDs

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GaN-based light emitting diodes (LEDs) have attracted extensive attention for their potential applications in energy saving solid-state lightning. However, LEDs in the InGaN/GaN material system suffer from a loss of external quantum efficiency at high current densities, a phenomenon known as efficiency droop. To date the mechanisms that have been suggested to be responsible for efficiency droop are carrier overflow, current crowding, poor efficiency of hole injection, Auger recombination, carrier loss mechanisms associated with the effects of reduced carrier localization or saturation of localized state.

Electron leakage from active layers to the p-GaN layer assisted by internal polalization fields has been a common problem. In fact, the electron leakage has been a common problem in GaN-based devices, and it is a reason for the implementation of an AlGaN electron blocking layer(EBL) with high Al composition between the QW active layers and the p-GaN layer.

However, looking at the several reports, the insertion of AlGaN EBL causes new problems. It has been found that although the p-AlGaN EBL is able to reduce the overflow of the electrons from the active region to the p-GaN layer, it also retards the hole injection from the p-GaN layer to the active region.

Thus, we reported effect of p-AlGaN electron blocking layer on efficiency droop and identification of the dominant mechanism for the droop in InGaN/GaN MQW LEDs.

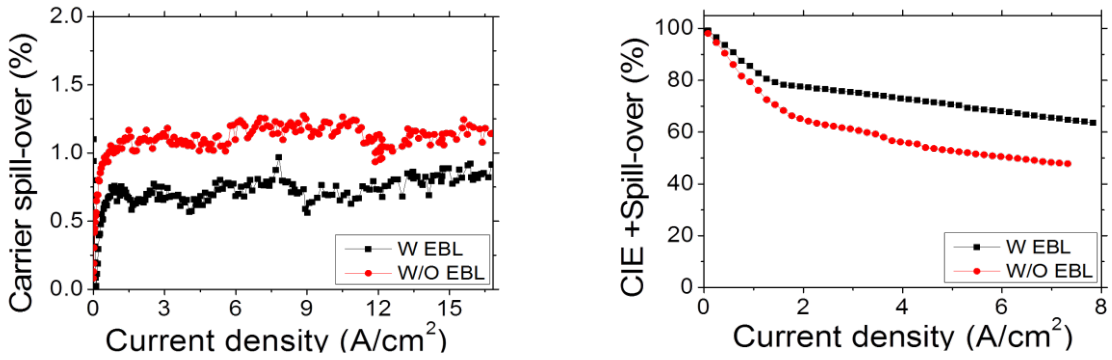

Fig. 1. Carrier spill-over, CIE + Spill-over at Room temperature(RT)

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Identification technique of grain boundaries in large-scale chemical vapor deposited graphene

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Pristine graphene, which is normally exfoliated mechanically from graphite, has attracted intensive attention because of its superior physical properties [1]. Development of graphene growth techniques enables us to grow large-scale graphene with high quality [2]. Among them, chemical vapor deposition (CVD) is one of the most promising methods for mass production of large-scale graphene. However, generation of defects, such as grain boundaries (GBs), impurities, vacancies, and wrinkles, is unavoidable during the process. Especially, GBs of graphene, which dominantly influence its characteristics, have been observed by transmission electron miscopy (TEM) [3]. Because of complicated sample preparation process for TEM, the more convenient method to identify GBs is required. Here we propose a new method that allows for locating the GBs of graphene on copper foil. By using thermal oxidation and plasma-treatment, GBs of graphene can be easily observed by optical microscope, allowing for measurement of grain size and unveiling the relation between graphene crystal shape and copper substrate. Our method provides a straightforward way toward analysis of defects of CVD-grown graphene for large-scale graphene electronics.

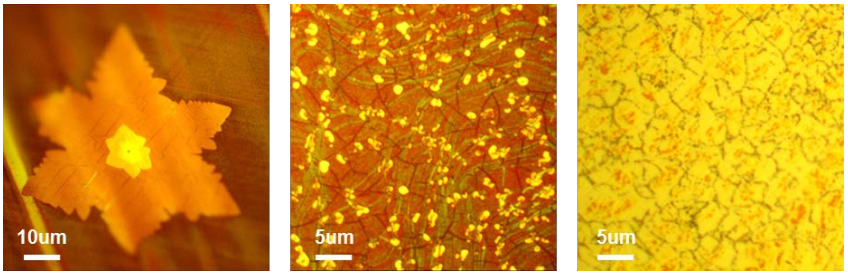

Figure 1. Optical images of plasma-treated or thermally-treated CVD-grown graphene on copper foil. Multilayer graphene island and grain boundaries can be clearly observed.

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Theoretical analysis of silica nanosphere effects on light extraction of light emitting diode by FDTD simulation

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We investigated effective SiO_2(silica) nanospheres on light extraction of GaN-based light emitting diode(LED) by using finite different time domain(FDTD) simulation. Silica nanopsheres are used to increase light exraction of GaN-based LED becasue of its proper refractive index and simple method to form on LED structrue [1]. To evaluate light extraction effects of silica nanopheres on LED epi structures, we made 3 types of FDTD simulation models: giving variety to diameter of nanosphere, coverage and shell thickness in hollow silica spheres. As change of diameters of silica spheres, FDTD results revealed that the coated LED by silica nanospheres of 700 nm diameters shows about 2.8 times increased electric field intensity(EFI) comparing to conventional LED strcuture [2]. In case of coverage dependent simulation results, the fully covered by 350 nm silica nanospheres shows 1.59 times increased EFI comparing other models. Finally, we find out that EFI is more increased as increase of silica shell-thickness in hollow silica model, but it is no longer increased until 70 nm-thickness. The diameter, coverage and shell-thickness of silica nanosphres are critical points to increase on light extraction of GaN-based LED because of its spheral geometry characteristics, transmittance and light scattering effects.

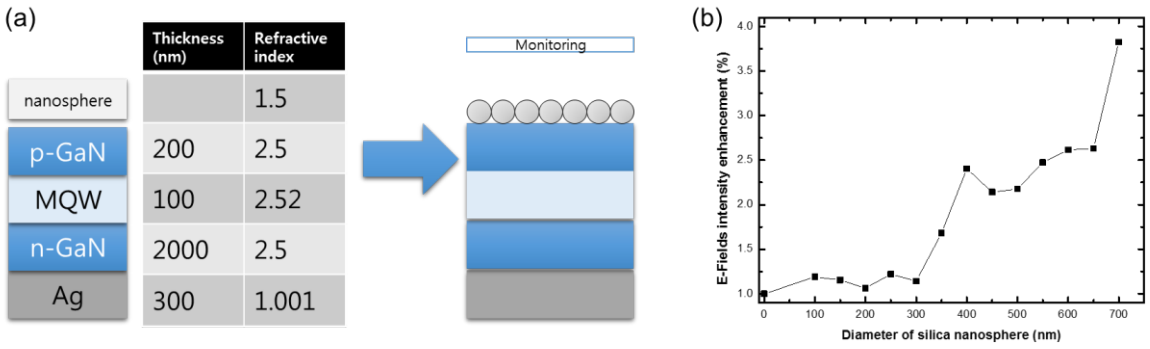

Fig 1. FDTD simulation : (a) Schematic simulated structure of LED and (b) Electric fields intensity as function of silica nanosphere diameters.

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[2] H. K. Lee, Y. H. Ko, G. S. R. Raju, and J. S. Yu, Opt. Express. 20, 25058 (2012).

Synthesized $ZnSnO_3$ nanoparticles by reflux condensation method and application to LEDs

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$ZnSnO_3$ (ZTO) materials are very attractive due to the numerous application fields such as solar cells, transparent conductor, sensor, and active layer for thin film transistor devices. They have high electron mobility, high electrical conductivity, and superior optical properties compared to other compound semiconductors[1-3]. We attempt cost effecitive synthesis method for obtain $ZnSnO_3$ by reflux condenstaion method which is very simple and easy. The generally synthesized materials in this study consist of mixture of $ZnSnO_3$ and ZnO. We can control the phase and morpholoyg of ZTO nanopartices through the change of process parameters. After characterization of ZTO materials,,synthesized materials were coated on the p-GaN surface of LED structure by drop-casting and spin coating method. In comparison with the reference sample without the nanoparticles, electroluminescence (EL) intensity of LED coated with solution consisting of ZnO and small amount of $ZnSnO_3$ was increased 1.34 times. Moreover, EL intensity of LED coated with solution consisting of ZnO and large amount of $ZnSnO_3$ was increased 1.85 times.

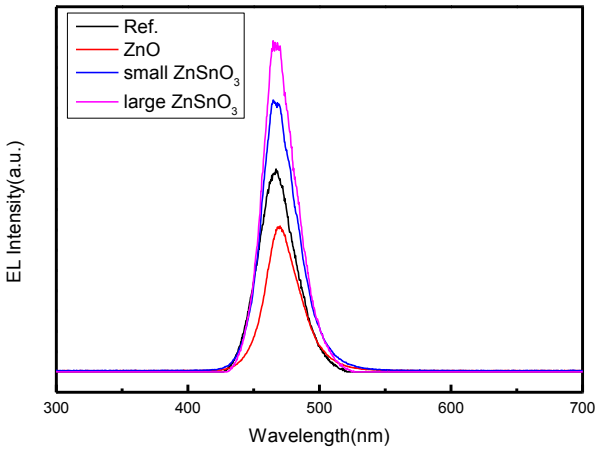

Fig 1. Comparison of EL intensity of LED coated with different nano materials.

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Variation of electrical characteristics in AlGaN/GaN Schottky diode with graphene/Ni/Au electrodes via plasma treatments

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AlGaN/GaN hetero-structures are very attractive material system to be used in high electron mobility transistors and Schottky diode due to their high sheet carrier density and high mobility of carriers in the channel of two-dimensional electron gas (2DEG) [1].

In this study, we investigated the effects of O_2 Plasma and H_2 annealing treatments of on degradation and recovery of plasma damaged graphenes resulting in, the recovery of degraded electrical characteristic in AlGaN/GaN structure with graphene based electrode. To analyze the effects of O_2 plasma treatments on electrical properties of graphene, the binding energy of carbon and oxygen is measured and analyzed with x-ray photoelectron spectroscopy. The measured current-voltage curves show the degraded electrical characteristic through the O_2 plasma treatments on graphene and the improved electrical characteristic with relatively low resistance for graphene/Ni/Au metals on AlGaN with hydrogen post annealing. In addition, the Raman spectroscopy results obtained from graphene with different thermal treatments showed that the H_2 annealing decrease the intensity of D-peak and increase of full width at half maximum of G-peak. The improvement of electrical properties of damaged graphene by H_2 post-annealing can be attributed to the elimination of native oxide.

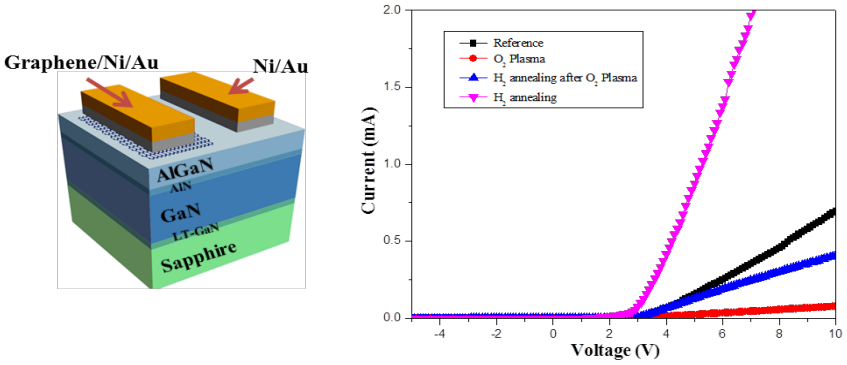

Fig 1. MoS_2 FET device and its electrical data

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Correlated visible-light absorption and intrinsic magnetism of SrTiO3 due to oxygen deficiency: Bulk or surface effect?

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Abstract:
The visible-light absorption and luminescence of wide band gap (3.25 eV) strontium titanate (SrTiO3) are well-known to originate from the existence of natural oxygen deficiency in the material. In this study based on density functional theory (DFT) calculations, to our knowledge, we provide the first report indicating that oxygen vacancies in the bulk and on the surfaces of SrTiO3 (STO) play different roles in the optical and magnetic properties. We found that the doubly charged state of oxygen vacancy (VO2+) is dominant in bulk SrTiO3 and does not contribute to the sub-band-gap photoexcitation or intrinsic magnetism of STO. Neutral oxygen vacancies (VO0) on (001) surfaces terminated with both TiO2- and SrO-layers induce magnetic moments, which are dependent on the charged state of VO. The calculated absorption spectra for the (100) surfaces exhibit mid-infrared absorption (~0.2 eV) and sub-band-gap absorption (2.5-3.1 eV) due to oxygen vacancies. In particular, VO0 on the TiO2-terminated surface has a relatively low formation energy and possesses half-metallicity, which can explain the recently observed spin-dependent photon absorptions of STO in an X-ray magnetic circular dichroism (XMCD) measurement [W. D. Rice, et al., Nat. Mater. 13, 481 (2014)]

Optimization of Silicon Doped InGaAs Grown by MOCVD for Source/Drain Contact of III-V n-MOSFET

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Since $In_{0.53}Ga_{0.47}As$ layers, which is exactly lattice matched on InP, have superior electron mobility compare with Si, it is a promising candidate for channel material of n-MOSFET in below 10 nm logic technology. To achieve this high performance device with an InGaAs channel, the doping concentration must highly doped in source/drain layer. However, it is difficult to achieve such a high carrier density using ion implantation technologies for III-V materials because these materials are not suitable for the high-temperature thermal annealing needed for dopant activation and recovery of implantation damage. Thus, one solution is using a regrown source/drain structure. [1, 2]. In this study, we report systematically investigated results on the variation of composition, surface morphology and dopant incorporation behavior of epitaxial InGaAs layers regrown on semi-insulating InP(001) substrate by MOCVD as a function of In/Ga ratio, growth temperature, and SiH_4 flow rate.

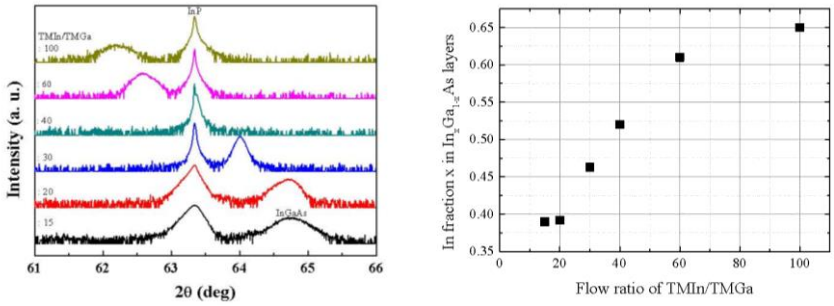

Fig 1. HR-XRD ω-2θ plots as a function of the flow ratio of TMIn/TMGa and its Indium fraction data from simulation.

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CVD Grown MoS2 Transistors with High-K Dielectrics

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최근, 뛰어난 전기적, 광학적 특성을 지닌 그래핀은 차세대 전자소재로서 많은 주목을 받았다. 그러나 이러한 그래핀은 밴드갭이 없는 전자구조로 인하여, 전자산업의 핵심소자인 트랜지스터로의 상용화에서 한계를 나타내고 있다[1]. 전이금속 다이칼코게나이드는 그래핀과 같이 이차원(2-dimensional) 물질이며, 밴드갭을 지녀 반도체적 특성과 함께 기타 다른 특성들 때문에 새로운 채널 물질로서 각광받고 있다. 그 중에서 몰리브덴 이황화물(MoS2)은 벌크 상태에서는 1.2eV의 간접 천이 밴드갭(indirect bandgap)을, 단일 층(monolayer)에서는 1.8eV의 직접 천이 밴드갭(direct bandgap)을 지니고 있어 전계-효과 트랜지스터(Field Effect Transistor)의 채널 물질로서 활발히 연구가 이루어지고 있다. 이 논문에서는 기상화학증착법(Chemical Vapor Deposition; CVD)으로 성장시킨 multilayer MoS2 박막을 기반으로 Top-gate 트랜지스터를 제작하였고, 게이트 절연막으로서 SiO2, HfO2, Al2O3의 세 가지 물질을 사용하여 각각의 특성을 비교 분석 하였다.

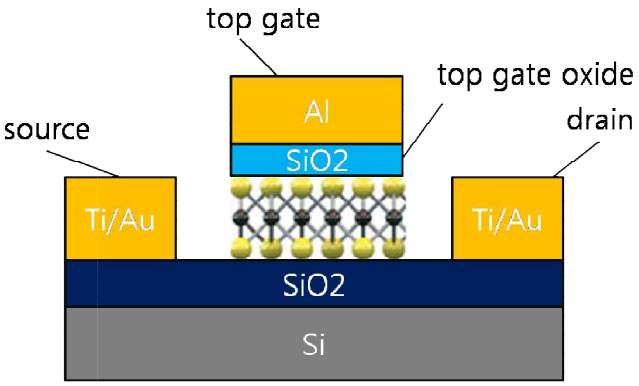

그림 1. Top-gate MoS2 트랜지스터 구조

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Effect of growth condition on carbon concentration of $Si_{1-y}C_y$ films by UHV-CVD

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Semiconductor heterojunctions and superlattices have recently shown tremendous potential for device applications because of their flexibility for tailoring the electronic band structure[1]. The introduction of epitaxy techniques have allowed heterostructure to be used in many different ways to improve electrical performance. Strain induced by lattice mismatch enhances carrier mobility. N-channel Si-MOSFETs(metal-oxide-semiconductor field effect transistors) use SiC as a stressor in source and drain regions to improve the electron mobility. The investigation on epitaxial growth of $Si_{1-y}C_y$ is important to apply strain in Si-based devices.

Epitaxial $Si_{1-y}C_y$ films were deposited on silicon substrates using ultrahigh vacuum chemical vapor deposition at 550, 600 and 650℃. Disilane(Si_2H_6) and monometylsilane(SiH_3CH_3) were used as Si and C source gas. SiH_3CH_3 flow rate were varied at a fixed Si_2H_6 flow rate of 20 sccm. $Si_{1-y}C_y$ films were characterized by means of atomic force microscopy (AFM), high resolution X-ray diffraction (HRXRD) and transmission electron microscopy (TEM). Substitutional carbon concentration was determined by HRXRD. Microstructures were examined by TEM. Surface roughness was measured by AFM. Epitaxial $Si_{1-y}C_y$ films with substitutional C composition of above 1% could be obtained by controlling SiH_3CH_3 flow rate over 6 sccm. C concentration in $Si_{1-y}C_y$ layer incresed with increasing SiH_3CH_3 flow rate, while growth rate decreased with increasing SiH_3CH_3 flow rate. We confirmed that growth temperature has an effect on root mean square roughness of $Si_{1-y}C_y$ films.

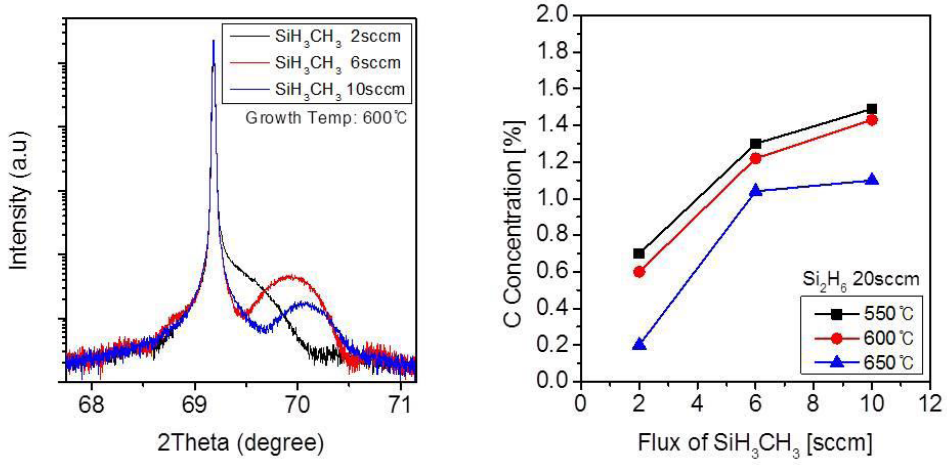

Fig 1. C concentration of $Si_{1-y}C_y$ films on Si

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The Growth of GaSb on Silicon (100) with AlGaSb/GaSb SPS buffer layers for Converting from Threading Dislocation to Misfit Dislocation

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Sb-based material semiconductors have attracted for high-speed and low power electric devices. Silicon substrate has a lot of advantages including growth of large area and cost effectiveness comparing to GaSb substrate. However, the lattice mismatch of silicon and GaSb is ~13%. Thermal expansion effect and the growth of polar compound on a non-polar substrate are also obstacles [1]. The large lattice mismatch could make threading dislocations (TDs) and exacerbate GaSb crystal quality on silicon (100) substrate. Therefore, it is important to minimize threading dislocation in AlSb buffer layer [2]. AlGaSb/GaSb shore-period lattice (SPS) layer is used to overcome problem of large lattice mismatch. TDs bent to misfit dislocations (MDs) at the interface of SPS layer for strain release [3]. MDs could not affect to upper GaSb layer and dissipated at the interface of SPS layer. The surface of AlSb buffer layer was measured by AFM measurement. The root mean square (RMS) value of SPS layer is about 2nm. In addition, AlSb buffer layer will be measured by dark-field (DF) XTEM to observe from TD to MD. GaSb/AlGaSb MQW PL spectra were obtained at room temperature and 10K with a fixed excitation power of 100mW. Emission peaks showed at 1761nm and 1623nm, respectively.

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Formation of InGaAs nanowires on (111) Si for antireflection

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Semiconductor nanowires have potential for light trapping and absorption to improve efficiency of optoelectronic devices such as solar cells or light emitting diodes due to their structural properties [1-2]. Long, dense, and tapered nanowires have shown better antireflection properties in a wide range of wavelength [3].

However, the fabrication of the antireflective nanowires is mostly including an etching process. The nanostructures formed by etching can reduce the light efficiency on optoelectronic devices, since light could be absorbed in their own structures due to the trap sites made by damage from etching [1]. Furthermore, since the self-assembly growth of nanowires has merit of hetero-epitaxial growth, combination of various materials is possible [1]. In particular, self-assembled nanowires formed on a Si substrate for antireflection would be applied to Si-based optoelectronic devices.

In this study, vertically-aligned, dense InGaAs nanowires were grown on the (111) Si substrates by Au-assisted molecular beam epitaxy. The structural properties of InGaAs nanowires were investigated by a scanning electron microscope and a transmission electron microscope. 18 μm- long nanowires showed excellent suppression of reflectance at various angles of incidence.

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High mobility InAs/AlSb 2DEG HEMT on GaAs for SPIN-FET and Effect of p-/n- doping on InSb/GaAs

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상온에서 30,000 cm2/Vs 이상의 전자 이동도를 보유한 InAs 는 GaAs 혹은 Si 등 기존의 반도체 물질보다 spin length 값이 크므로, SPINFET 을 위한 2DEG 을 구현하기 위한 최적의 물질로 인정받고 있다.

그러나 상기 InAs 는 0.606nm 의 격자상수를 가져 구득이 용이한 GaAs (0.565nm)및 InP (0.587nm)기판과 격자부정합이 심하여 고품질의 InAs 2DEG 을 구현하기위하여 특별한 기술이 요구된다. 이에 본 발표에서는 InAs 2DEG 을 구현하기 위하여 GaAs 기판을 AlSb 로 변환하여 forward 및 back-ward 형태의 HEMT 를 제작하였다. forward HEMT 구조는 기존에 SPIN-FET 의 연구를 위해 오랫동안 사용되어 왔고, back-ward HEMT 구조는 doping 층으로 인한 ion-scattering 이 적어 추후의 SPIN-FET 용 소자로 적절하다고 생각된다. 현재 forward HEMT 의 구조를 이용하여 상온 및 77K 전자이동도 21,690 및 56,890 cm2/V 의 전자 이동도를 얻었으며, back-ward HEMT 구조로 상온 및 77K 전자이동도 28,270 및 160,330 cm2/Vs 의 전자이동도를 얻었다. 상기 값은 모두 현재 SPIN-FET 실험용 HEMT 로 적절하거나 매우 우수한 품질이다.

InSb 는 상온에서 약 70,000 cm2/Vs 이상의 전자이동도를 보이고, 0.18eV 이하의 밴드갭을 가지므로 자성센서 및 적외선 센서로 크게 곽광받고 있다. 본 발표에서는 이를 자성 제어 디지털 소자에 응용하기위하여 n- 및 p- 도핑을 실험하고 이의 결과를 보고 한다.

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Novel methodology to fill nano-size trenches by VS growth of Te-rich SbTe nanowires for three-dimensional PCRAM devices

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In this paper, the growth of Te-rich SbTe nanowires inside the trench structure for phase change random access memory (PCRAM) was investigated using a modified atomic vapor deposition system. On the basis of understanding the film formation process and the kinetic parameters related to the boundary layer model, overall experimental conditions such as gas flow rate, working pressure, deposition temperature and precursor injection fraction were controlled and analyzed to grow nanowires instead of thin films [1]. The deposition behaviors were observed by top-view and cross-sectional SEM. Te-rich SbTe nanowires of well-ordered and even size were obtained on the trench structure as a template for growth despite not using any metallic catalysts. The crystallinity of the nanowires was confirmed by XRD and TEM. Deposition inside a nano-trench is the most important issue in the PCRAM process becauase the trench cell has a heat confinement effect to reduce thermal energy loss and cross talk between adjacent cell in the phase transition process comparing to the conventional planar cell [2]. We expect that this work will provide a way to overcome the difficulty of filling nano-scale trenches by a conventional film deposition method.

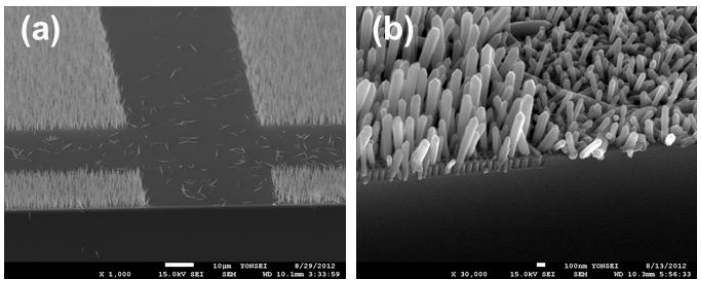

Fig 1. Cross-sectional SEM image of Sb-Te nanowires at the border between the trench and the planar surface with (a) 1,000 magnification and (b) 30,000 magnification.

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The effects of plasma frequency on high-k film properties in plasma enhanced atomic layer deposition

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Plasma-enhanced atomic layer deposition (PE-ALD) has been spotlighted because of its several benefits over conventional thermal ALD, such as wide process temperature and improved film properties by the reactive radicals of reactants. However, the use of plasma reactants negatively affects electrical properties of high-k films since ion bombardment of energetic radicals generates defects. Compared to radio frequency (RF) plasma usually used for plasma assisted processes, very high frequency (VHF) plasma could reduce negative effects of plasma on film properties since it has higher plasma density with lower ion kinetic energy than RF plamsa. However, there has been no report on PE-ALD using VHF plasma reactant.

For this study, PE-ALD Al_2O_3 was developed using Trimethylaluminum (TMA) precursor and O_2 plasma reactant on Si substrate. O_2 plasma reactant was generated using two different frequencies, 13.56 MHz and 60 MHz for RF and VHF, respectively. PE-ALD using VHF plasma showed higher growth rate, 2.7 Å/cycle, and higher film density, 3.26 g/cm^3, than PE-ALD using RF plasma, 2.3 Å/cycle and 3.11 g/cm^3. Also, the VHF PE-ALD showed improved electrical properties, such as low leakage current and low interface trap density, compared to the RF PE-ALD. The different growth characteristics and film properties were explained by plasma radical density and kinetic energies directly measured from the PE-ALD chamber. The VHF plasma reactant for PE-ALD has potentials for various applications which require very thin and dense films in nanoscale regime.

ALD-like Growth Behavior of Ru Thin Film with RuO_4 Precursor

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DRAM 소자의 집적화가 이루어짐에 따라 소형화된 구조의 소자에 Atomic Layer Deposition(ALD) 공정을 통해 차세대 전극물질인 Ru 박막을 균일하게 증착하는 공정이 많이 연구되고 있다. 다양한 Ru 전구체 중 RuO_4 전구체는 분자의 크기가 작고 탄소를 포함하지 않아, 유기금속전구체와 달리 Ru 박막 내 탄소 불순물을 거의 포함하지 않는다. 또한 RuO_4 와 수소를 이용한 환원반응이므로, MO 전구체의 산화반응과 달리 하부 막이 산화되는 문제점도 나타나지 않는다.

RuO_4 전구체는 열분해 온도 이하의 온도에서는 ALD 증착 거동을 보이고 그보다 높은 온도에서는 Chemical Vapor Deposition(CVD) 와 같은 거동을 보인다[1]. CVD Ru 박막의 특성에 대한 연구는 이미 보고되어 있으나[2], 보다 낮은 온도에서 ALD 거동을 통해 증착된 박막에 대한 자세한 분석은 아직 진행된 바가 없다. 본 연구에서는 Ta_2O_5 기판에서 RuO_4 전구체와 N_2/H_2 환원제를 이용하여 Ru 박막을 증착하였다. 공정 온도는 170° C 이며, 전구체 주입/퍼지 시간에 따라 self-limited saturation 거동을 보였으나 환원제 주입 시간에 대해서는 이상적인 ALD 거동과 다르게 2 step saturation 거동을 보였다. 또한 증착속도 역시 일반적인 ALD(~1 monolayer/cy) 보다 높은 값(>3A/cy)을 나타내었다. 본 연구에서는 증착 거동이 단순한 전구체의 흡착과 환원에 의한 과정이 아니라, 증착된 Ru 막과 RuO_4 전구체와의 역불균화 반응도 포함하는 메커니즘을 가짐을 확인하였으며, ALD Ru 박막의 우수한 단차피복성(~95%)을 확인하였다. 또한 Ru 박막의 전기적, 구조적 특성에 대한 분석도 진행하였다.

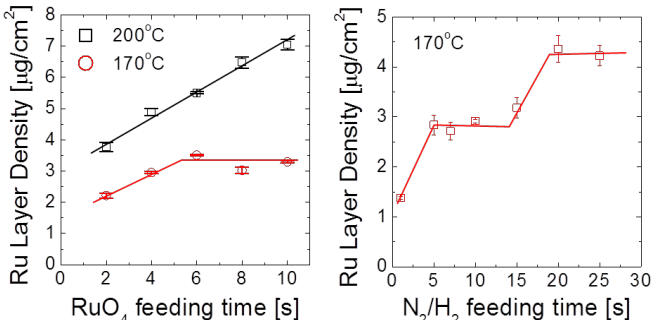

그림 1 전구체/환원제 주입 시간에 따른 saturation curve

[1] J.Gatineau et al., Microelectron Eng. 83, 2248-2252 (2006).
[2] J.H.Han et al., Chem.Mater. 21, 207-209 (2009).

Comparison of H_2O and O_3 as Oxidant in Atomic Layer Deposition of STO Films

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DRAM 의 집적화로 인해 capacitor 의 차세대 유전물질로 결정화되었을 때 bulk 유전상수 300 정도의 매우 큰 값을 갖는 perovskite 구조의 $SrTiO_3$ (STO)가 각광받고 있다[1] [2]. 본 연구에서는 Ru 전극 위에서 STO 박막을 단차피복특성이 우수한 원자층증착방법 (Atomic Layer Deposition, ALD)을 이용하여 성장시키고, 그 특성을 분석하였다. $[Sr(demamp)(tmhd)]_2$ 와 H_2O 를 각각 Sr 전구체와 산화제로 사용하여 SrO 박막을 증착하였으며, Sr 전구체 주입시간 5 초, 산화제 주입시간은 2 초, Ar purge 시간은 모두 5 초 이상에서 self-saturated 거동을 보이는 SrO ALD 공정 조건을 확보하였고, SEM 과 AFM 을 통해 박막의 표면 특성을 확인하였다. 이렇게 확보한 SrO 공정조건과 Ti 전구체는 $Ti(Me_5Cp)(OMe)_3$ 를 산화제는 250g/m^3 의 고농도 O_3 을 이용하는 TiO_2 공정 조건을 병합하여 STO 박막을 증착하였다. 새롭게 개발된 STO 박막 증착 공정은 TiO_2 와 SrO 의 증착비를 변화시킴에 따라 Sr:Ti=1:1 을 포함하여 원하는 조성의 박막을 성장시킬 수 있었으며, 화학량론적인 STO 박막은 결정화된 STO seed 층을 이용하여 별다른 후열처리 없이도 perovskite 구조로 in-situ 로 결정화 된 것을 확인하였다. 새롭게 개발된 STO 박막 공정은 기존의 SrO 증착 cycle 에서 O_3 을 산화제로 사용하였을 때 나타났던 Ru 하부 전극막의 열화 현상이 훨씬 완화되었으며, 이외에 박막의 화학적, 전기적 특성 역시 비교되었다.

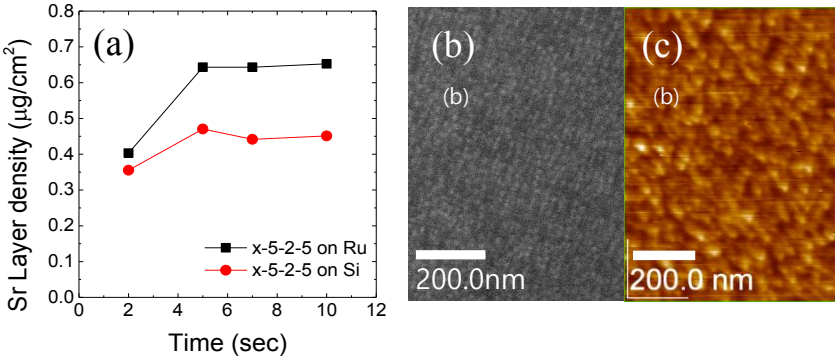

그림 1. (a) Sr 전구체 주입시간에 따른 SrO 박막 성장에 관한 saturation curve (b)Ru 기판에 증착된 SrO 박막의 SEM image (c)AFM image

[1] Seong Keun Kim et al., Adv. Fuct. Mater. 20, 2989 (2010).
[2] Sang Woon Lee et al., Appl. Phys. Lett. 92, 222903 (2008).

Stretchable thin-film transistors fabricated on elastomer substrate

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The increasing need for stretchable circuitries, wearable displays, soft and human-friendly devices, has increased the industrial importance [1-4]. As a result, the future development of electronics is expected to incorporate multifunctional electronic systems on the human body or clothing, requiring stable device performance under conditions of high strain and extreme body motion. One of the key technologies towards the realization of these ultimate goals is the development of transistors and circuits. Silicon integrated circuits are made of stiff active device films that fracture under a tensile strain of 1%. Single-crystal gold films also rupture under a tensile strain of 1–1.5%. To solve these problems, a few studies have focused on the fabrication of a stiff platform on elastomer substrates [1, 4].

In this paper, we propose stiff-island structures that act as a platform for stretchable electronic devices with high strain. The stiff islands are defined by conventional photolithography on an elastomeric substrate. Thin-film islands within a stiff region are fabricated on an elastomeric substrate, and electronic devices are fabricated on these stiff islands. When the substrate is stretched, the deformation is mainly accommodated by the substrate, and the stiff islands and electronic devices experience relatively small strains.

[1] J.-S. Choi, C. W. Park, B. S. Na, S. C. Lim, S. S. Lee, K.-I. Cho, H. Y. Chu, J. B. Koo, S.-W. Jung, and S.-M. Yoon, IEEE Electron Dev. Lett. 35, 762 (2014)
[2] S.-W. Jung, J.-S. Choi, J. B. Koo, C. W. Park, B. S. Na, J.-Y. Oh, S. C. Lim, S. S. Lee, H. Y.g C. and S.-M. Yoon, Org. Elect. inpress.
[3] S.-W. Jung, J.-S. Choi, J. H. Park, J. B. Koo, C. W. Park, B. S. Na, J.-Y. Oh, S. S. Lee, and H. Y. Chu, J. Nanosci. Nanotechnol. accepted.
[4] S.-W. Jung, J.-S. Choi, J. B. Koo, C. W. Park, B. S. Na, J.-Y. Oh, S. S. Lee, and H. Y. Chu, ECS Solis State Lett. inpress.

Simple Control of V_{TH} in *a*-IGZO TFTs by Rapid Thermal annealing

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최근, *a*-IGZO (amorphous In-Ga-Zn-O)를 사용한 전자 소자는 투명하고 유연하다는 장점으로 인해 다양한 방면에서 연구되고 있다. 특히, *a*-IGZO TFT(Thin Film Transiotor)는 비정질 상태에서도 높은 mobility(~10 $cm^2 V^{-1}s^{-1}$)와 subthreshold slope을 가지며, 가시광 영역에서도 높은 투과도(> 90%)를 가지기 때문에 기존의 a-Si TFT나 organic TFT보다 전기적, 광학적 특성도 우수하다. 또한 대면적화가 가능하기에 대면적의 liquid crystal displays나 organic light-emitting diode panel와 같은 future flat-panel display의 소자로 사용될 수 있고, glass 또는 flexible 기판 상에서 HF 또는 UHF-RFCPU에 응용될 것으로 기대된다 [2]. 그러나, display의 픽셀 및 CPU 설계와 같은 다양한 응용을 위해서는 TFT의 문턱치 전압(V_{TH}) 조절이 필수적이다. 지금까지의 연구결과에 의하면 *a*-IGZO TFT channel 두께 조절, 게이트 절연막 두께 조절, 게이트 전극의 일함수 조절, channel 불순물 도핑, 그리고 IGZO channel의 조성비 변화를 통해서 V_{TH}를 조절하는 방법 등이 보고되어 있다. 그러나 이와 같은 방법들은 고비용의 추가 공정을 필요로 하거나 소자구조가 복잡해질 수 있고, channel에 결함을 유발하여 소자 성능의 저하를 초래한다 [3]. 본 연구에서는 소자구조 및 공정이 복잡해지지 않고 결정 결함을 유발하지 않으면서도 저비용으로 목적을 달성할 수 있는 새로운 방법으로써, RTA (Rapid Thermal Annealing) 처리에 의한 간단한 V_{TH} 조절 방법을 개발하였다. RTA의 급속한 온도 상승 및 하강에 의하여 IGZO channel 내의 oxygen vacancy가 발생되는 원리를 이용하여 전자 농도를 조절할 수 있었다. RTA 열처리 온도에 따라서 oxygen vacancy 농도가 변화하는 것을 XPS 분석으로 확인하였고, 이에 따라서 Hall 측정을 이용하여 전자 농도가 변화하는 것을 측정하였다. 또한, TFTs를 제작하여 RTA온도에 따라서 전기적 특성을 확인한 결과, 아래와 같이 RTA 온도에 따라서 V_{TH}가 변화되는 것을 확인하였다. 따라서 RTA 처리에 의한 V_{TH} 조절은 산화물 기반의 다양한 전자소자 구현에 매우 유용할 것으로 기대된다.

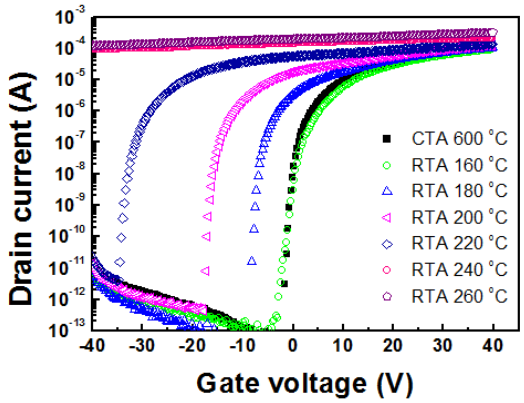

Fig 1. Transfer curves of *a*-IGZO TFTs as a function of RTA temperature.

[1] K. Nomura et al., Nat. 432, 488 (2004).
[2] J. Koyama et al., ECS Transactions, 8 (1) 57-62 (2007).
[3] T. Mizuono et al., IEEE Trans. Elec. Dev., 41, 11 (1994)

저전력 Barristor 소자 집적 공정 개발과 특성

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그래핀 FET 의 낮은 on-off 비는 전자 소자로서의 활용에 결정적인 단점이 되어 왔다. 그 대안으로 그래핀/실리콘 schottky junction 의 barrier 조절을 통해 on-off 비를 증가시킬 수 있는 Barristor 소자가 제안되었다. [1] 이 소자는 매우 높은 구동전류, on-off 비를 얻을 수 있지만, 실리콘기판과 그래핀간의 계면이 매우 깨끗해야하고, 그래핀의 결함이 적어야만 정상적인 barrier 조절특성을 얻을 수 있기 때문에, 소자특성의 재현이 쉽지 않다는 단점이 있다.
이 연구에서는 Fig.1 에 보인 것과 같이 그래핀 캔틸레버 제작공정을 응용하여 그래핀/실리콘 접촉 계면을 개선함으로써, uniformity 가 좋은 barristor 를 제작하였다. Fig.2 는 소자의 I_d-V_d 특성으로, 역방향 bias 영역에서 V_g 에 비례해 포화 전류가 증가한다. 이는 그래핀/n 형 실리콘의 barrier height 과 V_g 가 반비례하기 때문에 나타나는 특성이다. 또한 기본 소자특성으로부터 semi-empirical device model 을 개발하여, barristor 의 EOT 를 1nm 까지 낮출 경우, 약 10^5 (Vg=0~1V) 의 on-off 비를 얻을 수 있음을 예측할 수 있었으며(Fig. 3), 이 결과는 barristor 가 저전압영역에서 높은 전류를 얻을 수 있는 매우 유망한 소자임을 보여준 결과이다.

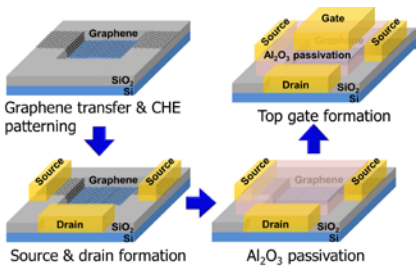

Figure 1. Fabrication process of barristor device.

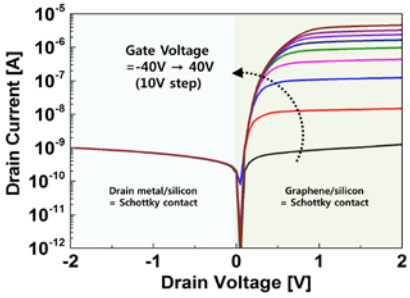

Figure 2. The measured I_d-V_d curves.

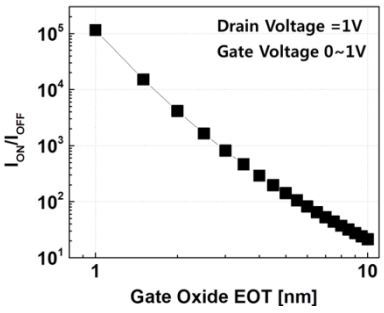

Figure 3. The I_{ON}/I_{OFF} ratio controlled by gate oxide thickness with semi-empirical device model.

[1] H. Yang et al., Science, 336, p1140-1143, (2012).
This research was supported by Basic Science Research Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (grant number).

Investigation on the effect of post deposition annealing on the Sn-doped In_2O_3 thin film transistor

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On the road to the next generation display devices, amorphous oxide semiconductors (AOSs) have been attracting great attention due to material's high mobility, stability, and relatively easy fabrication process. Among these AOSs, the indium oxide based materials (i.e. InZnO, $InGaZnO_7$ and Sn-doped In_2O_3) have been intensively studied due to materials' highest mobility.[1] One of the known problem of Sn-doped In_2O_3 (ITO) when it is used as the channel layer of the thin film transistor (TFT), was device's large hysteresis, which makes device unsuitable. Park et al. has tried to solve such problem through their oxygen high pressure annealing system, where almost no hysteresis was observed after annealing at 150°C, low enough for the application on the flexible substrate [2]. However, despite the already expansive high vacuum sputtering system, such method involves additional high vacuum system where the alternative solution with relatively simple process is desired. For such purpose, we demonstrate the effect of post deposition annealing (PDA) of ITO TFT at atmosphere (atm). Although atm PDA has shown to reduce hysteresis at 200°C, it cause the negative shift of the transfer curve in negative V_g direction. In this study, we will investigate on the effect of atm PDA on the ITO TFT and possible reasons for the negative shift of the transfer curve.

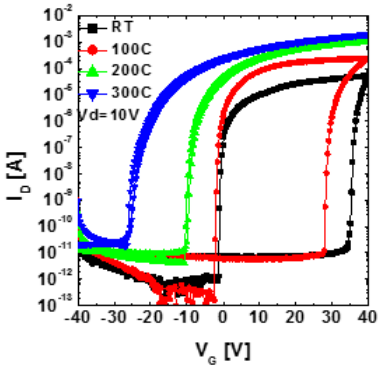

Figure 1. ITO TFT hysteresis behavior with respect to the PDA temperature

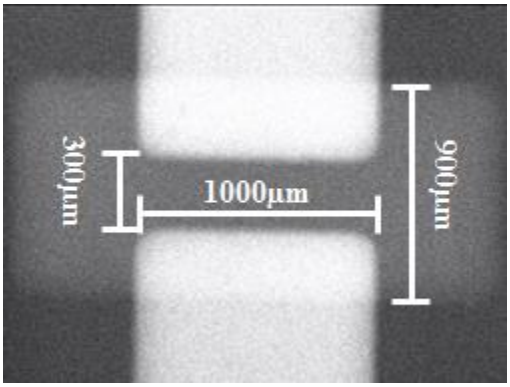

Figure 2 Picture of ITO TFT used for this experiment

[1] Chang Eun Kim and Ilgu Yun, Semiconductor Science and Technology, 27 (2012)

[2] Se Yeob Park, Kwang Hwan Ji, Hong Yoon Jung, Ji-In Kim, Rino Choi et al, Applied Physics Letters 100, 162108 (2012).

Atomic layer deposited WN_x thin films using a new F-free tungsten metallorganic precursor as a diffusion barrier against Cu

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One of the refractory metal nitrides, WN_x, has been used in many different applications because of their desirable material properties, including high melting temperatures, relatively low resistivities, chemical inertness, etc. Among those applications, the most interesting area nowadays is microelectronics, where these materials are being extensively studied as a diffusion barrier, a metal gate electrode, and a glue layer at ultra-high-aspect-ratio contact and via holes in ultra-large-scale-integrated (ULSI) devices. With the continuous scaling-down of the devices size requiring the excellent conformality, thickness uniformity, and large-area uniformity of the process, atomic layer deposition (ALD) can be a viable solution since ALD uses a self-limited film growth mode through surface-saturated reaction of precursors and enables an atomic-scale control of a film thickness and composition with excellent step coverage. ALD-WN_x films was generally deposited by inorganic precursor, WF_6 and NH_3 as a reactant though a few investigations were done using metallorganic precursors such as bis(tert-butylimido)bis(dimethylamido)tungsten(VI) [TBIDMW, $(N^tBu)_2(NMe_2)_2W$], and tungsten (III) precursor, $W_2(NMe_2)_6$ and NH_3 as a reactant at temperatures ranging from 150 to 400 ^oC [1]. In this study, we reported the ALD-WN_x process using a new F-free W metallorganic precursor at the low deposition temperature between 150 and 350 ^oC (Fig.1) and the developed ALD-WN_x film has been evaluated as a diffusion barrier for Cu metallization. The use of F-free precursor can give advantages by excluding many issues of the conventional WF_6: (i) WF_6 and its by-products such as HF are corrosive and can chemically attack many other materials exposed on substrate surfaces; (ii) F-containing species that are trapped inside the films may diffuse out, react with their adjacent materials such as Cu and dielectric layers, and finally degrade the device performances; and (iii) fluorine impurities residing on the surface of the films may impede the adhesion of Cu. The results showed that self-limited film growth with both precursor and reactant (NH_3 plasma) pulsing time, which is the typical characteristics of ideal ALD, could be obtained at 250 ^oC and its step coverage was good [~ 60 % at a very small-sized trench structure (bottom width: 15 nm and aspect ratio of ~ 3.5)]. 5-nm-thick ALD-W_2N effectively prevented the diffusion

of Cu upto 550 °C.

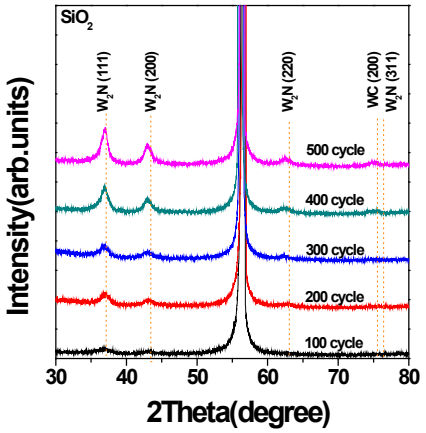

Fig.1. XRD results on the ALD-WN_x thin films deposited at 250 °C as a function of reaction cycles.

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[1] H. J. Kim, S. H. Kim and H. –B. –R. Lee, *Atomic Layer Deposition for Semiconductors,* Chapter 8, C. S. Hwang (Eds.), New York, Springer (2014).

Acknowledgements

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Scavenging of Native Oxide on Semiconductors in Metal-Oxide-Semiconductor with Metal Electrodes

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Metal-oxide-semiconductor (MOS) based devices have faced various challenges for continuous improvements of their performance. Especially, dielectrics in MOS capacitor is aimed to replace exist silicon dioxides dielectrics with new high-k materials. Native oxide in the high-k/semiconductor interface, playing a role of additional dielectric with high-k oxide, is a major cause decreasing the capacitance of MOS capacitor [1]. Thus, the native oxide should be reduced and qualified for higher device performance. Scavenging is one of phenomenon reducing the physical thickness of native oxide using oxygen-gettering metal electrodes such as Ti and Ta. Figure 1 shows general scheme of scavenging. In this study, several electrodes have been investigated whether such materials also have scavenging effect as well as Ti using Si-based MOS structures.

P-type (100) Si substrates were used as a channel and HfO_2 dielectric films were deposited in an ALD reactor at 350ºC. The thickness of native oxide of each sample is confirmed identically after cleaning by using a spectroscopic ellipsometry. The physical thickness of HfO_2 films on native oxide layer is the same 6nm. After then, Mo, Ti, and Al electrodes with 150nm thickness were deposited on HfO_2 film by a DC magnetron sputtering system at room temperature. The top electrodes were patterned with lithography and lift-off methods. These MOS capacitors were treated by forming gas anneal (FGA) for 30 min in N_2 ambient with 5% H_2 at 400ºC. C-V characteristics and transmission electron microscopy (TEM) analysis were measured to confirm the scavenging effect of native oxide with each metal electrode. Figure 2 shows C-V characteristics of MOS structures with Mo, Ti, and Al electrodes. The capacitance equivalent thickness (CET) of capacitors with Mo, Ti, and Al electrodes are respectively 3.2, 2.9, and 4.6nm. It is found that the values of capacitance are very different with electrode materials, even though all capacitors were processed identically with the same thicknesses of native oxide and HfO_2 layers. Figure 3 shows the TEM images of MOS capacitors with Mo, Ti, and Al. Native oxide thickness of Mo, Ti, and Al samples are respectively 2.0, 1.6, and 1.5nm. It also shows the decrease of native oxide thickness with metal electrode, meaning scavenging effect.

[1] Takashi Ando, Materials, 5, 478-500 (2012)

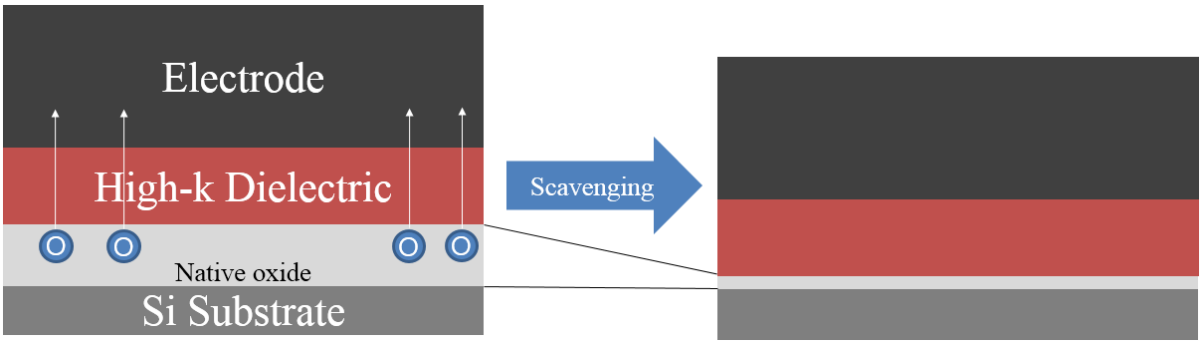

Figure 1. General scavenging scheme: oxygen transfer from native oxide.

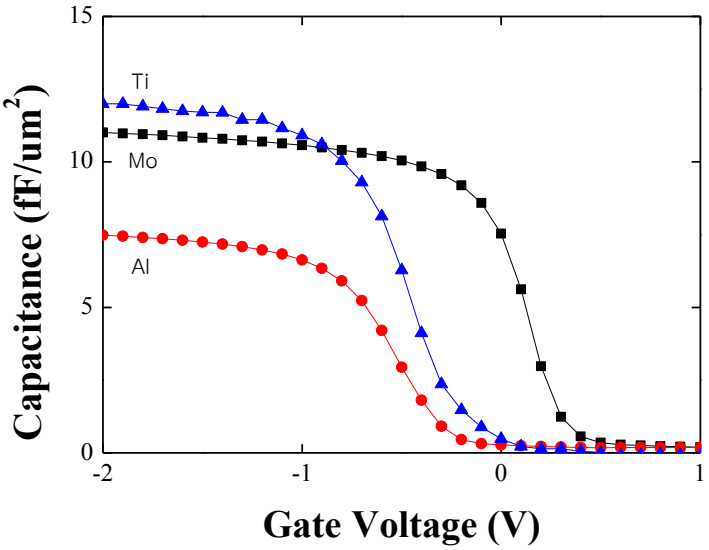

Figure 2. Electrode material dependent C-V characteristics of metal/HfO_2/Si MOS capacitors with Mo, Ti, and Al electrode, respectively. The high-k HfO_2 films are 6nm thick.

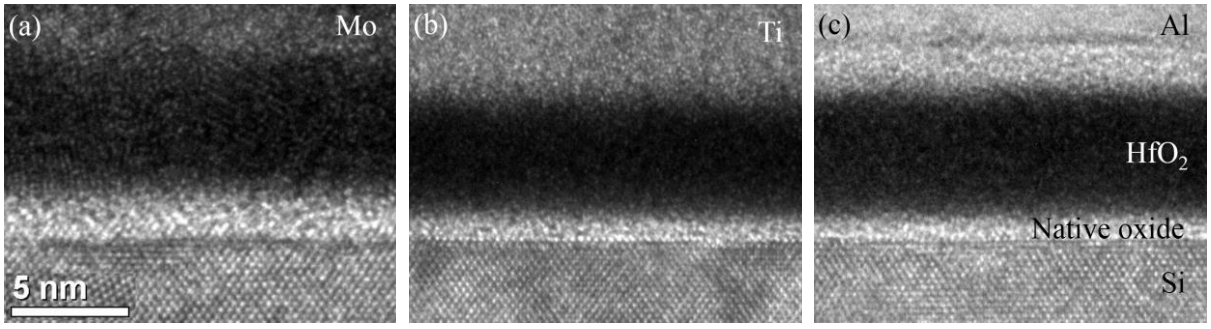

Figure 3. TEM images of MOS capacitors with (a) Mo, (b) Ti, and (c) Al electrodes.

The Study on Increment of Non-Lattice Oxygen Defects by O_2/Ar Ratio Variation in Sputtered HfO_2

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Recently, hafnium oxide (HfO_x) film has been researched for performance improvment of variable applications due to its high dielectric constant and diffective characterisitc. Especially, defective characteristic of HfO_x attract attention to study on Resistive Memory (ReRAM) and Charge Trap Device (CTD)[1, 2]. Typically, lots of oxygen vacancy is well known as major defect of HfO_x. We investigated the oxygen vacancy controllablity in sputtered HfO_x film by variable O_2/Ar ratio. The depostion rates of HfO_x are extremely increased above the 3.5 % of O_2/Ar ratio conditions. It is shown that Hf sputtering rate is increased in comparison with oxidation rate on Hf metal target surface[3]. X-ray Phtoemission Spectroscopy (XPS) results show that the low O_2/Ar ratio is affected to O_2 contents decrease in HfO_x films. Then, lots of "Non-Lattice oxygen" in low O_2/Ar ratio HfO_x films are observed from O1s peak deconvolution. It is indicated that oxygen vacancies in HfO_x is controllable by variable O_2/Ar ratios. From CV characteristics, low O_2/Ar ratio HfO_x show that flat band voltage is shifted to negative axis direction. It is meaning that oxygen vacancies in sputtered HfO_x play as positive charge.

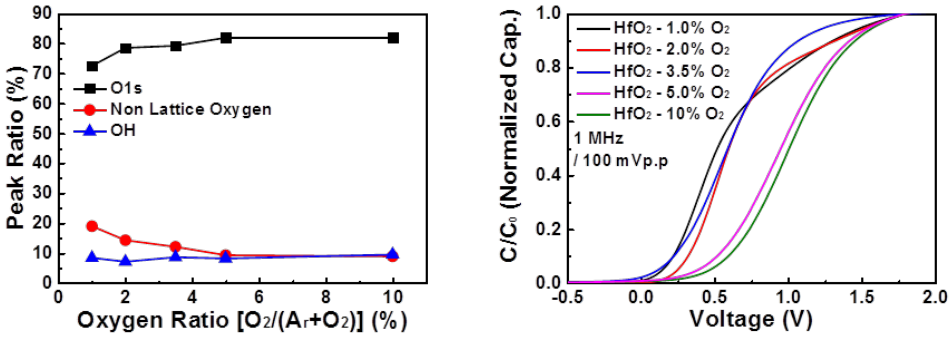

Fig 1. O, NLO, OH ratios in O1s peak and CV characteristics by O_2/Ar ratio

[1] L. Goux, P. Czarnecki, Y. Y. Chen, L. Pantisano, X. P. Wang, R. Degraeve, B. Govoreanu, M. Jurczak, D. J. Wouters, and L. Altimime, Appl. Phys. Lett. **97**, 243509 (2010)
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Improved Electrical Performance of Amorphous Oxide TFTs Using Solution-Processed Dual Active Layer Structure

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Soulution-processed amorphous oxide semiconductors (AOSs) thin-film transistors (TFTs) such as InZnO (IZO), InGaZnO (IGZO), InSnZnO (ITZO), have many merits in terms of the low cost, easy process, high mobility.[1] However, the high-mobility TFTs reported in many papers show bad characteristics of high off current, large negative shifted threshold voltage and large subthreshold swing. In this study, we reported solution-processed InGaZnO (IGZO)/InSnZnO (ITZO) dual-active layer (DAL) TFTs to overcome the trade-off between high mobility and other parameters. In our experiment, optimized DAL TFT showed a saturation mobility of 4.6 $cm^2/V{\cdot}s$, steep subthreshold swing of 0.21 V/dec and a high on/off ratio of $4x10^8$. Enhanced electrical performance is due to both the proper carrier concentration of the back channel and the adjustable carrier flow by the difference of the energy barrier height between front channel and back channel. (Fig. 1(b))

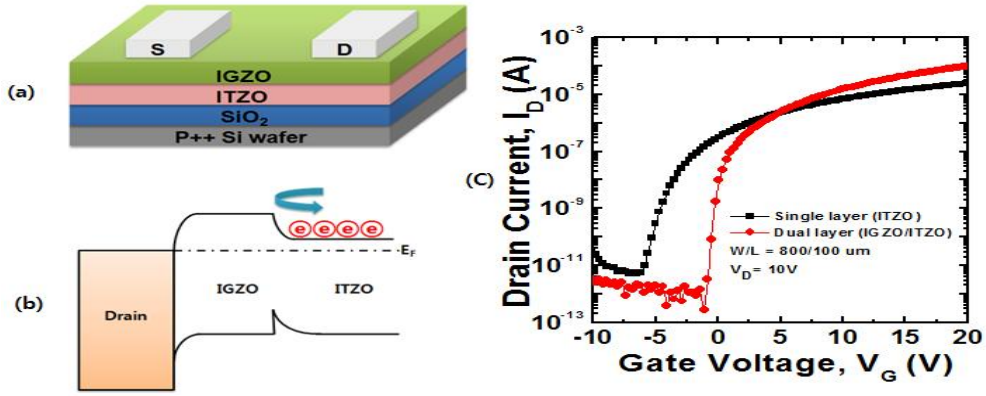

Fig 1. (a) Schematic of the DAL TFT. (b) Band structure of drain/IGZO/ITZO.

(c) Transfer characteristics of single and DAL TFT.

[1] E. Fortunato , P. Barquinha , R. Martins , Adv. Mater. 2012, 24, 2945 .

Effect of Ge doping on structural and electrical properties of Ge-doped ZrO_2 films by atomic layer deposition

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Recently, Dynamic Random Access Memory(DRAM) is required higher capacitance density and lower leakage current. Capacitance density is increased by using high-k material such as Al_2O_3(9), HfO_2(17~21), ZrO_2(19.7~46.6) and dielectric constant of ZrO_2 is depend on crystal structure (monoclinic=19.7, cubic=36.8, tetragonal=46.6).[1] It is reported that various dopant elements used to stabilize the tetragonal ZrO_2. In this study, the structural and dielectric properties including dielectric constant, leakage current and micro-sturucture of Ge-doped ZrO_2 (G-ZO) films with various Ge concentration. The G-ZO films were fabricated by atomic layer deposition and the composition of the G-ZO films was determined by controlling the number of cycles for ZrO_2 and GeO_2 deposition. XRD spectra shows that the ZrO_2 film has a tetragonal phase and phase transition occur from poly crystalline to amorphous with increasing Ge content. The G-ZO films show larger dielectric constant than ZrO_2 film when the cycle ratio ZrO_2 and GeO_2 was changed from 10 : 1 to 3 :1. However, the G-ZO film with the cycle ratio of ZrO_2 : GeO_2 = 1 :1 has a smaller dielectric constant. This implied that Ge dopant affects the dielectric constant of ZrO_2 film and critical concentration exists

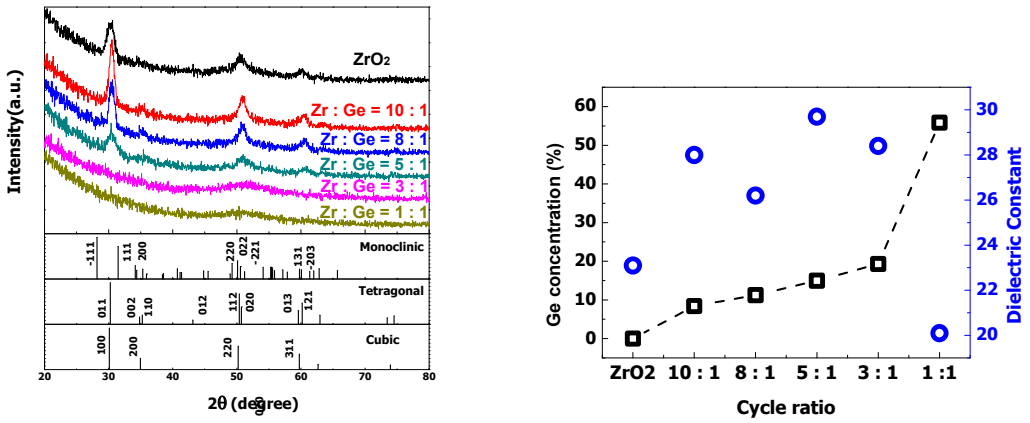

Fig 1. XRD spectra and dielectric constant of G-ZO with various compositions.

[1] J.Ferrand, V.Beugin, A.Crisci, S.Coindeau, S.Jeannot, M. Gros-Jean and E. Blanquet, ECS Transaction 58 (10)223-233(2013)

Comparison of contact resistance properties in solution processed IGZO TFTs with top-contact and bottom-contact S/D structures

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The amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) are generally fabricated with a bottom-gate staggerd structure on the SiO_2 or SiN_x gate insulator [1-2]. Bottom-gate TFTs are prone to degradation due to the exposed active layer. In this study, contact resistance of two types of top-gate TFTs were analyzed from transfer and the output characteristics. The two type of strucures are, top-gate top-contact (TGTC) where the source and drain (S/D) electrodes are on top of the active layer and top-gate bottom-contact (TGBC) where the S/D electrodes lie under the active layer. The TFTs were fabricated with spin-coating a-IGZO and PMMA film on Si_3N_4 which reduces the process steps and fabrication cost [2]. The PMMA layer has a dual role in this device. It works as a gate insulator, as well as acts as a channel passivation layer. The channel passivation layer suppress the electric-field-induced threshold voltage instability, which is caused by the adsorption of oxygen and water molecules in the ambient atmosphere. The electrical characteristics depends on the contact type. As per Fig. 1(a), the TGTC device showed stable perfomance. In TGBC device, due to poor contact resistance, the leakage current increased (Fig. 1(b)). In TGBC structured device, solution prcosseing of a-IGZO leads to side-wall coating of electrodes, which results in poor performance.

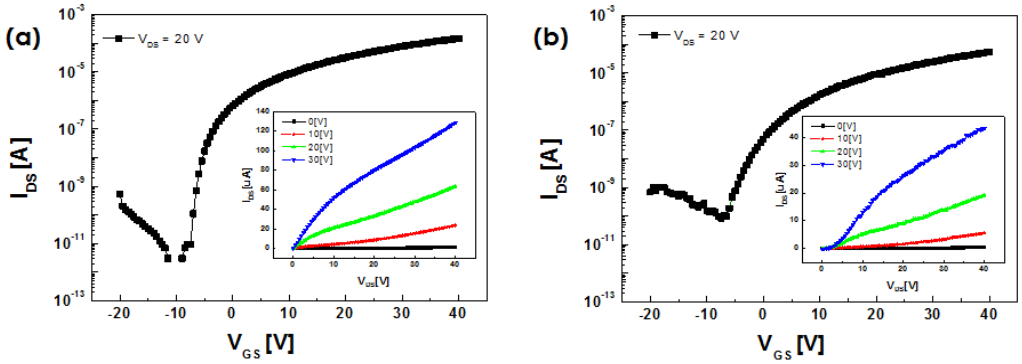

Fig 1. Transfer characteristics of (a) TGTC and (b) TGBC structured thin film transistors; (inset: output characteristics)

[1] M. Kim, J.-H. Jeong, H.-J. Lee, T.-K. Ahn, H.-S. Shin, J.-S. Park, J.-K. Jeong, Y.-G. Mo, and H.-D. Kim, Appl. Phys. Lett. 90, 212114 (2007).
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High quality LT-SiO2 Film Deposition Process on MAHA PECVD System

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The fabrication of electronic devices at relatively low deposition temperatures (100–150°C) becomes increasingly important. At low temperature, one can fabricate devices on glass or polymer substrates, or one can add extra functionalities to standard ICs by post-processing [1]. In order to realize good devices, high-electrical quality should be obtained, which is a challenge at such low temperature. In this paper, low-temperature (< 120℃) PECVD LTO-770 SiO_2 process on blanket film electrical performance and mechanical properties are investigated and compared with a traditional PECVD TEOS SiO_2 process at similar deposition temperatures. The LTO-770 SiO2 process provides > 1.4x hardness and modulus than the PE-TEOS based process and also exhibits superior electrical characteristics at these temperatures, with measured electrical leakage values < 1E-10 at 2 MV.cm-1 and electrical breakdown electric field > 8 MV.cm-1.

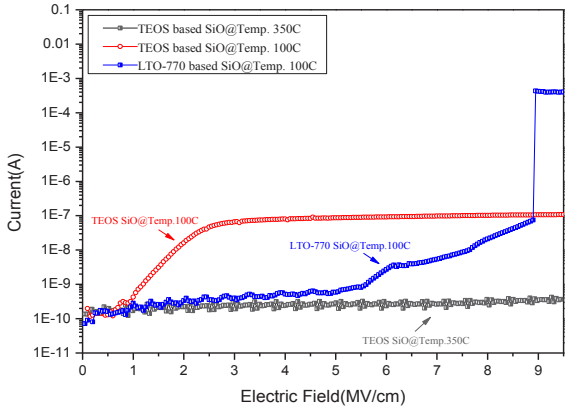

Fig 1. Electrical I-V Curve data

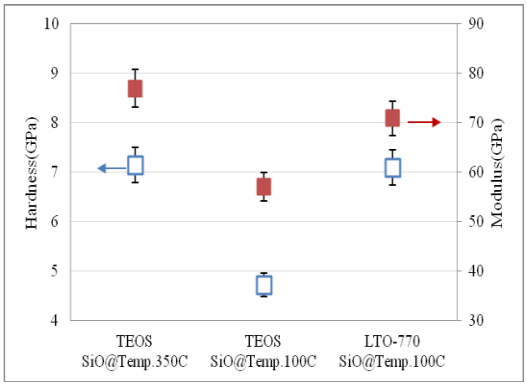

Fig 2. Mechanical Hardness & Modulus Properties

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Reaction Mechanism Study on Atomic Layer Deposition of Silicon Nitride Films Using Silicon Chlorides and Ammonia

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Atomic layer deposition (ALD) of a variety of materials has been being investigated owing to the precise control of thickness and composition and the conformality on complex three-dimensional structures. Recently, reaction mechanism of ALD has been studied by real-time process monitoring techniques, such as quartz crystal microbalance (QCM), Fourier transform infrared spectroscopy (FTIR), quardrupole mass spectrometer (QMS), or X-ray photoelectron spectroscopy (XPS). These methods are complementary because each of these has unique advantages and limations.

In this work, we utilized *in-situ* QCM and FTIR for real-time monitoring of ALD process. The deposition kinetics was investigated during ALD process of silicon nitride films, and the reaction mechanism of the ALD process was studied. Octachlorotrisilane (Si_3Cl_8) and ammonia (NH_3) were selected as the silicon precursor and the nitriding agent, respecticely. ALD temperature window was between 285°C and 520°C, and high-quality film was grown at 520°C with a relatively high growth rate of 0.22 nm/cycle. The results from *in-situ* QCM and FTIR show that $–SiCl_x$ (x=1 and/or 2) groups were generated by Si_3Cl_8 dose in the first half reaction and $–NH_2$ groups were generated by NH_3 dose in the second half reaction.

[1] K.-C. Park, W.-D. Yun, B.-J. Choi, H.-D. Kim, W.-J. Lee, S.-K. Rha, C.-O. Park, Thin Solid Films 571, 3975 (2009)

Nitride 막의 Anneal 전/후 Stress 변화 개선 연구

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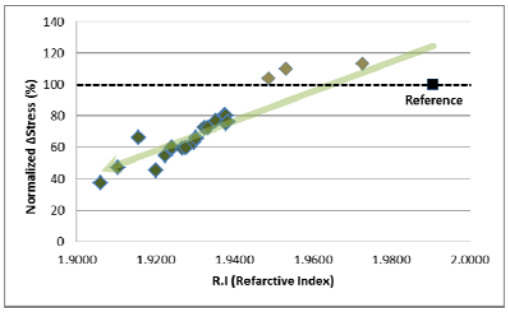
NAND Flash 가 3D Vertical 구조로 변경되면서 Oxide / Nitride 막을 연속적인 Deposition 공정을 진행하여 수직 구조를 형성하고 집적도 향상을 위하여 Stack 단수를 증가시키기 위한 연구가 활발히 이루어지고 있다. [1-3] 이 때, Oxide / Nitride Stack 에서 Oxide 는 층간 절연막으로 사용되고, Nitride 막은 수직으로 증착된 후 Gate 물질을 채우기 위한 희생막으로 사용되어 후속 공정에서 제거된다. 이 때 사용되는 막의 Stress 변화가 적을수록 Integration margin 을 가져오는 방향이다. Oxide 와 Nitride 막의 Factor 에 따른 Stress 변화를 확인하는 연구결과들도 있다. [4]

본 연구에서는 Nitride 막의 Anneal 전/후 Stress 변화 폭 개선을 위하여 원익 IPS 社의 MAHA-MLT PECVD 장비를 이용하여 Nitride 막을 증착 시, 공정 Factor 별 및 증착 온도 별 Anneal 전/후의 Stress 변화를 평가하였다. 그 결과, 공정 Factor 중 NH_3 : SiH_4 비율(R.I 변화)에 따른 Anneal 전/후 Delta Stress 변화폭과 증착 온도는 450 ~ 600 도까지 변화시켜 Anneal 전/후의 Stress 변화폭을 확인하였고, 최소한의 Anneal 전/후 Delta Stress 변화를 가져갈 수 있는 개선 조건을 확보하였다.



Temp(℃)	Δstress (%)
T_{Ref}	100
T_2	87
T_3	80

※ Process Temperature : T_{Ref} < T_2 < T_3
Anneal Temperature : 850℃

Fig 1. R.I 및 공정온도 변화에 따른 ΔStress 변화

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Controlling Structural and Electrical Properties by Dispersing Metallic Nanoparticle into Dielectric Thin Films for ReRAM application

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Nanocomposite thin film can be formed by an insulation oxide matrix with uniformly dispersed metallic particles < micro-meter-size. Recently, it is of great interest to apply nanocomposite thin films into nanoelectronics by using the oxide dielectric thin film by dispersing 1-10nm size of metallic particles likewise Au, Ni, Pt, Ir, Co or semi-conductor material likewise Si, Ge. CTF (Charge trap flash) memory and ReRAM (resistance random access memory) can be representative examples. This study was trying to figure out the relationship between the microstructure of composite thin material and its own electrical properties. Pt nanoparticle-dispersed SiO_2 (SOP) films were prepared by RF co-sputtering method using Pt and SiO_2 targets in Ar atmosphere. The growth rate and Pt content in the film were controlled by means of manipulating the RF power of Pt target while that of SiO_2 was fixed. This study revealed that the relationship between the microstructure of composite thin film and its own electrical properties by using TEM, AFM, SAXS (small angle X-ray scattering) and the electrical measurement (DC I-V and Hall effect measurement).

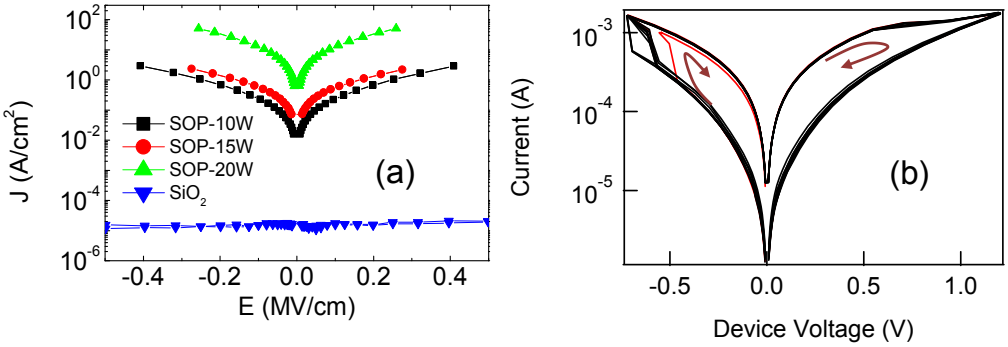

Fig 1. (a) J-E characteristics of various SOP and SiO_2 junction devices, (b) forming-free resistive switching behavior with SOP device

Interface sulfur passivation using H_2S pre-deposition annealing for atomic-layer-deposited HfO_2 film on Ge substrate

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Volatile desorption of thermodynamically unstable GeO induces a number of interface state defects between Ge substrate and dielectric layer,[1] which degrades the performance of Ge-based MOSFETs. Thus, there have been extensive efforts to prevent the performance degradation using interface passivation. Among them, Ge surface passivation with S has been known to be effective to reduce the interface state density (D_{it}), which has been generally done with $(NH_4)_2S$ solution. However, the wet-based surface passivation process has several problems in respect of mass-production. So, we examined the interface S passivation by rapid thermal annealing under H_2S atmosphere to replace the wet-process with $(NH_4)_2S$ solution. The interface S passivation by H_2S pre-deposition annealing (pre-DA) resulted in the similar S concentration and distribution at the interface of HfO_2/Ge with those by $(NH_4)_2S$ solution treatment.

Typical C-V curves for TiN/HfO_2/Ge MOS capacitors with H_2S pre-DA in Fig. 1 shows the large decrease in frequency dispersion in the depletion region, which suggests the reduction of D_{it} near the valence band edge of Ge.[2] On the other hand, Ge 3*d* core level XPS spectra for HfO_2/Ge with various H_2S pre-DAs in Fig. 1(c) shows the interface S passivation by H_2S Pre-DA suppressed the defective interfacial layer (GeO_x) growth during ALD effectively.

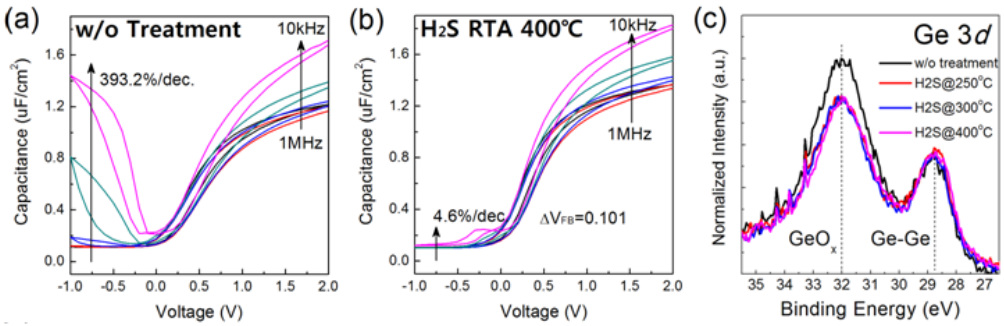

Fig. 1. Typical C-V curves for TiN/HfO_2/Ge (a) without and (b) with H_2S pre-deposition annealing, and (c) Ge 3*d* core level XPS spectra for HfO_2/Ge with various H_2S pre-deposition annealing.

[1] S. K. Wang, K. Kita, C. H. Lee, T. Tabata, T. Nishimura, K. Nagashio and A. Toriumi. J. Appl. Phys. 108, 054104 (2010)
[2] R. Engel-Herbert, Y. Hwang and S. Stemmer. J. Appl. Phys. 108, 124101 (2010)

Improved interface properties of atomic-layer-deposited HfO_2 film on InP using interface sulfur passivation with H_2S pre-deposition annealing

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We examined the interface sulfur passivation effect [1] in atomic-layer-deposited HfO_2 film on InP substrate using H_2S pre-deposition annealing (pre-DA) by rapid thermal process in order to replace the wet-based surface passivation process with $(NH_4)_2S$ solution which is inappropriate for conventional mass-production. SIMS depth profiles in Fig.1 shows the S concentration and distribution near the interface between HfO_2 and InP substrate were comparable for the both cases with H_2S pre-DA and $(NH_4)_2S$ solution treatment. In Fig.2, the typical C-V curves for the TiN/HfO_2/InP MOS capacitors with the surface sulfur passivation by $(NH_4)_2S$ solution and H_2S pre-DA were compared. With H_2S pre-DA at 350 ^oC, the frequency dispersion of capacitance in the depletion region decreased to ~ 7.9 %/dec., which is lower than that with $(NH_4)_2S$ solution treatment (~ 12.4 %/dec.). This suggests that interface state density near the valence band edge of InP was more effectively reduced by H_2S pre-DA than $(NH_4)_2S$ solution treatment. The thermal energy during H_2S pre-DA facilitated the surface reconstruction of InP to reduce the surface state density.[2]

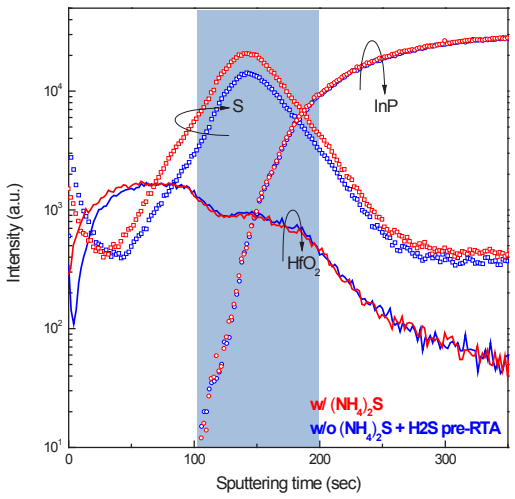

Fig.1 SIMS depth profiles for HfO_2 on InP with H_2S pre-DA and $(NH_4)_2S$ solution treatment.

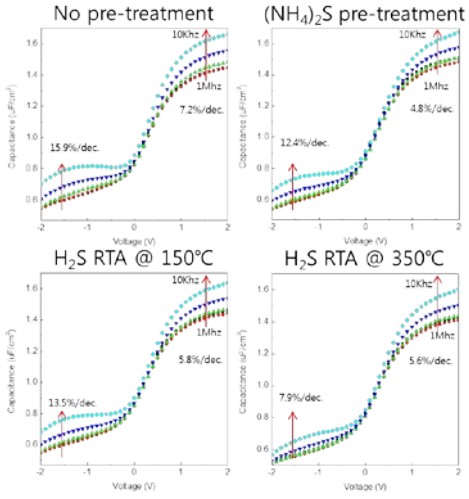

Fig.2 typical C-V curves for the TiN/HfO_2/InP MOS capacitors with surface S passivation by $(NH_4)_2S$ solution and H_2S pre-DA.

[1] C. H. An, Y. C. Byun, M. S Lee, and H. S Kim, J. Electrochem. Soc., 158, G242 (2011).
[2] M. Shimomura, K. Naka, N. Sanada, Y. Suzuki and Y. Fukuda, J. Appl. Phys., 79, 4193 (1996).

FinFET의 AC Stress Reliability 특성

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FinFET 의 channel 은 Si 의 (100)면과 (110)면으로 되어있으며, 그 중 측면(110)은 hole mobility 는 높지만, Trap density 가 높아서 계면신뢰성 열화가 쉽게 발생할 수 있다는 단점이 있다.[1] 특히 Fin 두께가 얇아질 수록, (110)면의 영향이 커지기 때문에, 이에 따른 신뢰성 특성의 변화에 대한 연구가 필요하며, 좀 더 구체적인 소자의 장기동작특성을 파악하기 위해, 실제 소자동작상황과 유사하게 stress pulse 가 간헐적으로 가해지는 상황에서의 신뢰성 특성에 대한 연구도 필요하다. 본 연구에서는 다양한 크기의 FinFET 소자를 활용, 지금까지 보고된 것보다 훨씬 짧은 pulse 를 이용하여, AC stress 를 인가하면서 소자 신뢰성 변화를 연구했다.

Fig.1 (a)는 detrapping 이 가능한 전압에서 relaxation time 이 주어지는 bipolar AC stress 의 경우, DC stress 에 비해 Vt shift 가 매우 작다는 것을 보여준다. 반면, relaxation 이 0V 에서 발생하는 Unipolar stress 는 DC stress 와 큰 차이가 없었다. 또한 Fig.1(b)에 보인 것과 같이 bipolar stress 조건에서도 relaxation time 이 줄어들 수록, Vth shift 가 증가되는 것이 관찰되었다. 이 결과는 detrapping time 이 positive bias temperature instability(PBTI)에 결정적인 영향을 미친다는 것을 보여주며. 따라서, PBTI 는 relaxation 이 충분히 주어지는 실제 소자동작상황에서는 큰 폭으로 감소할 것으로 생각된다.

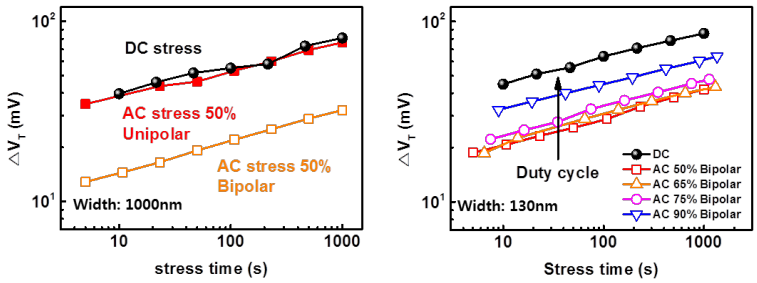

Fig 1. V_T shift of FinFET device by AC stress

Acknowledgement: This work was supported by the industrial strategic technology development program (10039174) of MOTIE, Korea and by the Future Semiconductor Device Technology Development Program (10044842) funded By MOTIE and KSRC(Korea Semiconductor Research Consortium
[1] S. Ramey et al., IRPS 4C5.1-4C5.5 (2013). [2] Dieter K. Schroder, Microelectronics Reliability 47, 841 (2007).

Effects of Electrostatic Discharges Stress On Bidirectional Flip Chip Transient Voltage Suppression Diodes

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By employing epitaxial growth and drive-in technology, a new Bidirectional Flip Chip Transient Voltage Suppression (BD-FCTVS) diode was specially developed to comply with strong requirements of electrostatic discharge (ESD) protection of Chip-on-Board (COB) high power LEDs. Characteristic current-voltage curves are investigated in conjunction with ESD stresses of the human body model (HBM), machine model (MM), IEC61000-4-2 and transmission line pulse (TLP) analysis. For instance, the TLP applications cover a wider range of use beyond estimating the ESD susceptibility of device level protection with peak pulse current I_{PP} up to 20A. Our result shows excellent dynamic resistance values as low as ~0.7Ω and very small clamping voltages as well. The BD-FCTVS can withstand up to ±4 kV of MM, ±8 kV HBM and ±29 kV IEC61000-4-2. In this research, the transient natures and electrical properties are described in detail on the basis of structural design and fabrication processes for BD-FCTVS. In conclusion, we will demonstrate the ESD performance substantially upgraded by not only employing epitaxial layer but also modifying process parameters like the doping profile at p-n junctions.

Keywords: ESD, HBM, MM, IEC, TLP, Bidirectional Flip chip TVS Diode.

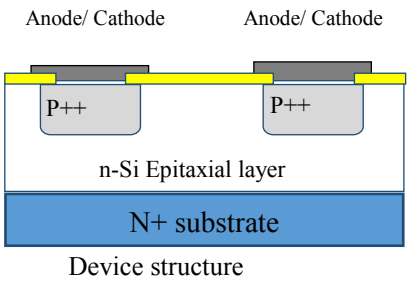

Fig 1. Schematic BD-FCTVS device structure

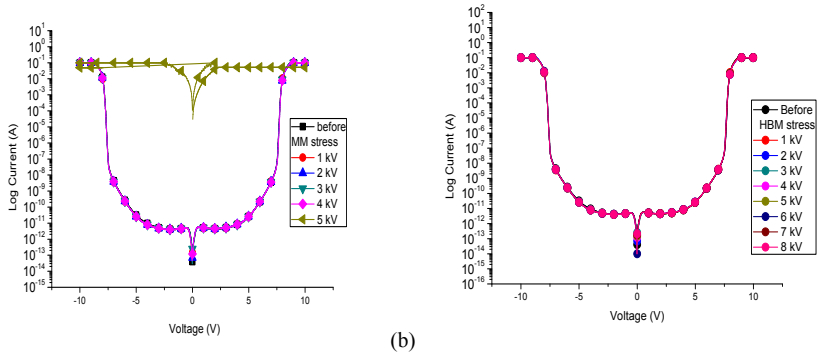

Fig 2. I-V characteristics of the BD-FCTVS(±8V) after ESD stress: (a) MM, (b) HBM

ESD Robustness of Bidirectional Flip Chip TVS Diodes

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As smart/mobile/wearable devices widely adopt high performance components, Filp Chip Transient Voltage Suppressor (FCTVS) diode becomes more popular for surface mount packages not requiring Au wire bonding. Bidirectional FCTVS diodes may provide merits of enhanced operation, efficient thermal dissipation and high integration density. However, because of the decrease in effective active/pad area, the planar structure of bidirectional FCTVS can be inforior to the vertical strutures in ESD performance. In this work, we propose a new bidirectional FCTVS with controlled pad distance and active area. Excellent ESD robustness was confirmed over ESD 30kV (IEC61000-4-2) for the new FCTVS diodes with VBs, 7~450 V. Analysis results of human body model(HBM), machin model(MM), surge, transmission line pulse(TLP)will be presented, and electrical properties will be evaluted in conjunction with device structures.

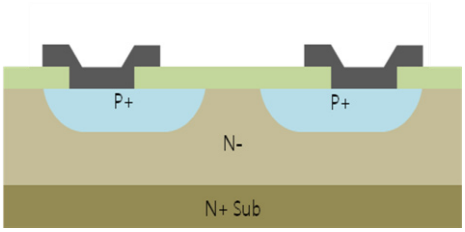

Fig 1. Bidirectional Flip Chip TVS Diode

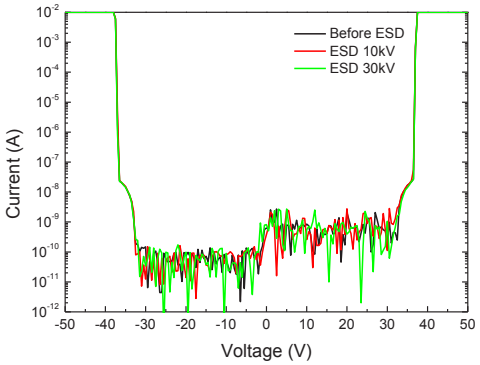

Fig 2. I-V characteristics before/after ESD stresses (IEC61000-4-2)

Nano Imprint로 형성된 Synaptic 소자 및 Spike Time Dependent Plasticity (STDP) 특성 평가

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Moore's Law에 따른 집적도 한계를 극복할 수 있는 차세대 소자로 나노 신경 모방 소자 (Neuromorphic Device)가 큰 주목을 받고 있다. 인간의 뇌 동작을 모방한 Neuromorphic Device는 기존 소자 대비 저전력으로 구동될 뿐만 아니라 자체적인 학습능력을 보유하고 있어 많은 연구가 진행 되고 있다. 2 Terminal 기반 소자 (ex. Memristor) 이외에, Neuromorphic 소자 형태의 3 Terminal Transistor 기반 소자는 현재까지 주로 Channel에 해당하는 물질의 증착 방식 및 다양한 재료 응용의 관한 연구가 활발히 진행되고 있으며 [1] 본 논문에서는 SiO_2와 ALD High-*k* Gate Dielectric을 적용시킨 Synapstor 소자 제작 및 이에 따른 측정결과를 보고한다. Transistor의 Channel은 기존의 Photo Lithography 방법이 아닌 비노광 방식인 Nano Imprint으로 형성되었다. Figure 1 은 Neuromorphic Device의 기본적인 학습능력의 전기적 특성인 Spike Time Dependent Plasticity (STDP)의 결과를 보여준다. 일정한 간격으로 반복되는 Pulse가 소자에 가해짐에 따라 V_g에 의해 I_{ds}가 점차 증가하는 Trend를 보이고 있음을 나타낸다. 이때 SiO_2 Gate Dielectric의 경우 Current Level의 Increase는 3V부터 10V까지 넓은 Range에서 관찰되었으나, HfO_2에서는 3V이상에서 Breakdown이 일어나 그 이상에서의 측정이 되지 않았다. 또한 HfO_2 에서의 결과로 볼때, SiO_2대비 구동 Range는 짧지만 동일한 전압의 V_g Power 에서 더 높은 I_{ds} Level (~2 orders)을 보이고 있음이 확인되었는데 이러한 이유들로는 Thermally Grown된 SiO_2와는 달리, ALD를 통해 증착된 HfO_2는 채널 형성 후 가해지는 고온의 열처리 공정에 의해 결정구조가 변화되어 전기적인 특성에 영향을 주었다고 예상할 수 있다. HfO_2에 대한 최적 조건의 실험 결과의 특성은 향후 보고 예정이다. 이 실험을 통해 열처리 시 수반되는 HfO_2의 결정구조 변화 제어 및 적절한 Oxygen Vacancy Control 유도를 위한 Dielectric Thermal Engineering만으로도 Synapstor의 Current Level 을 Tuning 할 수 있다는 가능성을 확인하였다. 따라서 본 실험인 SiO_2 및 HfO_2를 이용한 Synapstor의 Gradual Current 증가에 관한 재료 특성 의존성은 Synaptic 소자의 성능향상에 Guideline을 제시할 수 있을 것으로 판단된다.

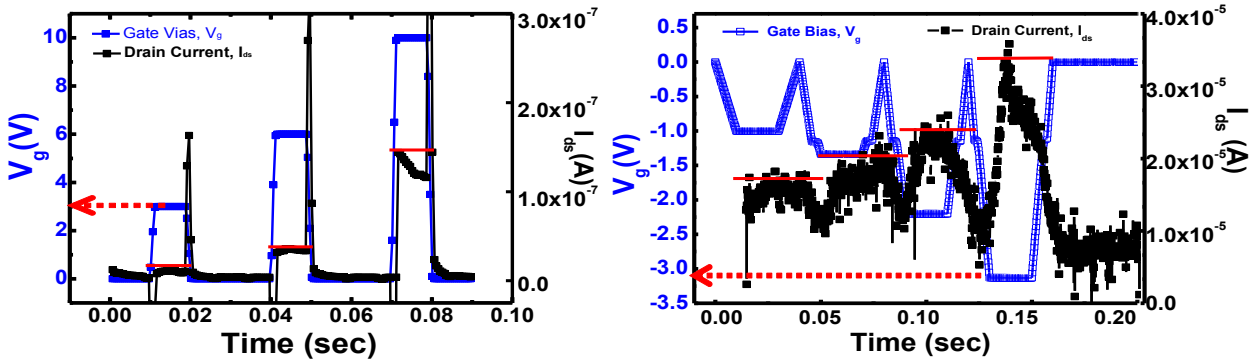

Fig 1. STDP characteristics for SiO_2 (left) and HfO_2 (right) gate dielectric synapstors, respectively

[1] Zhou, Jumei, et al. "Synaptic behaviors mimicked in flexible oxide-based transistors on plastic substrates." IEEE Electron Device Letters, Vol. 34, No. 11, pp. 1433-1435, 2013.

This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009460).

Investigation of Oxide Layer Appropriate for 3D NAND structure with Vertical Channel Fabricated Using Gate-first Channel-last Process

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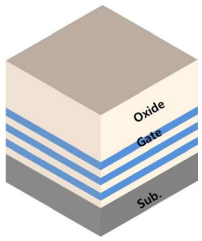
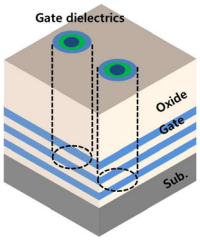
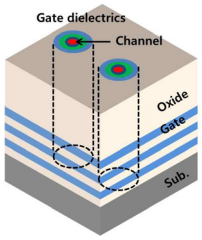
Nowadays, 3D NAND flah memories have attracted much attention due to bit cost scale issues [1,2]. In general, 3D NAND flash with vertical channel is fabricated using gate-first channel-last process flow. On contrast with plannar strcuture, gate dielectrics are already stacked prior to forming channel layer (fig. 1). Thus, it is difficult for us to use silicon dioxide film thermally grown as tunnel layer in gate dielectrics. LP-TEOS is commonly empoyed instead thermal oxide film. However, its insulative property falls short of our expectation (fig. 2). In this work, we attempt to investigate various way to improve electrical properties of silicon oxide thin film, appropriate for 3D NAND with vertical channel.



(a)



(b)



(c)

Fig 1. 3D NAND flash process flow. (a) gate staking, (b) hole open and gate dielectrics deposition (c) channel formation

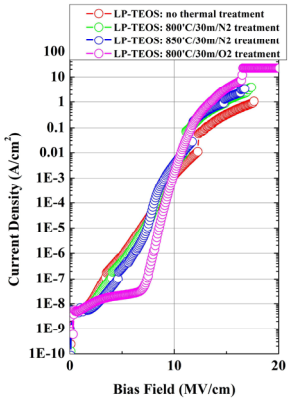


Fig 2. *J-V* properties of LP-TEOS thin films

[1] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata,Y. Matsuoka, Y. Iwata, H. Aochi and A. Nitayama, VLSI 2007, 14.
[2] J. Jang, H. Kim, W. Cho, H. Cho, J. Kim, S. Shim, Y. Jang, J. Jeong, B. Son, D. Kim, K. Kim, J. Shim, J. Lim, K. Kim, S. Yi, J. Lim, D. Chung, H. Moon, S. Hwang, J. Lee, Y. Son, U. Chung, and W. Lee, VLSI 2009, 192.

마이크로솔더링을 이용한 자외선 LED 광원모듈 제작

Fabrication of ultraviolet light source module by using micro-soldering

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Abstract : 자외선 (UV) LED (light Emitting Diode) 광원 응용에 대한 관심이 높아지고 있으나, 출력, 조사밀도 균일성 및 효율 특성이 개선되지 못하여 사용에 한계가 있다. 본 연구에서는 다수의 소형 칩을 저 전류에서 구동하는 광원 모듈을 제작하기 위해, 정전류다이오드 (CLD)를 이용하여 병렬회로를 구성하고 마이크로솔더링 기술을 이용하여 칩을 융착하였다. 광원 모듈은 80X90 cm^2의 회로기판 크기에 16,650개의 꼭지파장 385nm UV 플립 칩 (Flip-Chip) LED를 가로 방향 190 um, 세로방향 100 um 간격을 가지도록 배열하였다. 시뮬레이션 실험을 통하여 조사밀도는 3,000 mW/cm^2, 조사밀도 균일성은 95 % 이상으로 계산되었다. 제작 실험은 SAC (96.5Sn/3.0Ag/0.5Cu) 솔더를 이용하였으며, 플립칩은 750×750 μm^2 크기를 가지며, 전극은양극, 음극 모두 260 μm×150 μm의 동일 크기를 가진다. 이때 솔더 볼의 크기는 260×150×30 μm^3 이다. 제작한 UV 광원모듈의 신뢰성 특성과 구동전류 밀도에 따른 정전류 안정성 및 열 특성을 조사하였다.

Controlled Zr Doping for Inkjet-printed ZTO TFTs

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Controlled Zr doping for inkjet-printed zinc-tin oxide (ZTO) thin-film transistors (TFTs) was investigated to obtain better electrical properties for the first time. Contrary to the previous doping reports, the electrical properties of Zr-doped inkjet-printed ZTO (Zr-ZTO) TFTs was improved by a very small amount of Zr doping into ZTO semiconductor thin film. Comparing to a non-doped solution-processed ZTO TFT, a moblilty increases from 3.73 to 6.73 cm^2/Vs, an on-to-off ratio from 7.65X10^7 to 3.72X10^8, a threshold voltage from 3.70 to 3.35 V, and a subthreshold slope from 0.71 to 0.53 V/dec. This was attributed to the slight suppression of oxygen vacancies and suitable control of the carrier concentrations in semiconductor. The bias stability was also improved by a small amount Zr doping.

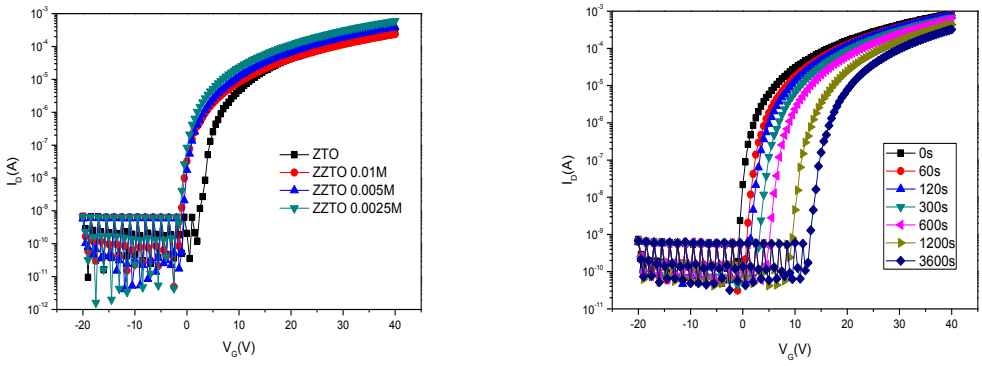

Fig 1. Zr-doped inkjet-printed ZTO TFT and its bias stability

[1] J. S. Lee, Y. J. Kwack, and W. S. Choi, ACS Appl. Mater. Interfaces. 5, 11578 (2013).

[2] Y. S. Rim, D. L. Kim, W. H. Jeong, and H. J. Kim, Appl. Phys. Lett. 97, 233502 (2010).

XPS analyses of ALD-Prepared Titanium-dioxide Thin Films With Oxygen Sources And Their Annealing Effect

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A titanium-oxide thin film was prepared by using atomic layer deposition with tetrakis(dimethylamino) titanium as titanium precursors. Different oxygen sources, oxygen plasma and water, were used to investigate TiO_2 thin film with thermal annealing. The average growth rate of TiO_2 with oxygen plasma source increased gradually with increasing substrate temperature. However, the growth rate of TiO_2 with water source decreased with the temperature with good surface roughness. A (101) crystallinity was observed at low temperature of 150°C after annealing. The XPS analyses were thoroughly carried out to verify the structural composition of ALD-grown TiO_2 thin films with different oxygen sources.

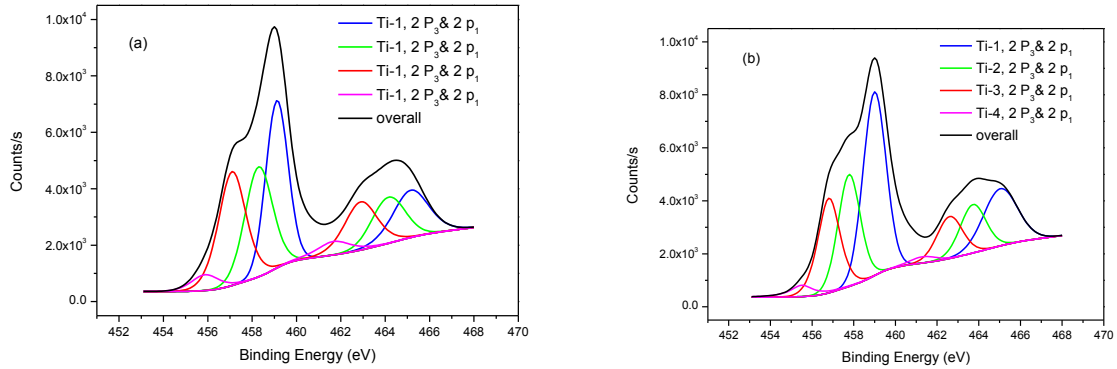

Fig 1. XPS spectra of titanium components, Ti $2p_{3/2}$ and Ti $1p_{1/2}$ core shells with (a) water source and (b) water source after thermal anneal

[1] T. Nam, J-K. Kim, M. Kim, H. Kim and W-H. Kim, J Korean Phys. Soc., 59, 452 (2011).
[2] W.-S. Choi, J Korean Phys. Soc., 57, 1472 (2010).

Floor Plane Subtraction using Parallel Operation for Indoor Applications

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Human motion-based algorithms have been widely studied in human-computer interfaces and digital image processing fields. To effectively perform motion recognition in depth images, robust foreground segmentation is of key importance. Therefore, unnecessary region such as wall, ceiling, floor plane, and so on must be correctly removed. In particular, floor plane exert harmful influence on segmentation between foreground and background region [1]. A random sample consensus (RANSAC) algorithm have been extensively used for plane detection and subtration. The RANSAC is randomly selected candidate data set so calculation iteration is unlimited [2]. In this paper, we propose a computationally efficient floor plane subtraction method using the RANSAC. The proposed system consists of four consecutive steps as shown Fig. 1. The depth smoothing is used to depth noise reduction in the input depth image. For expressing linear data of depth image, the 3D coordinate conversion is employed. For detecting floor plane, the converted 3D coordinate is then calculated for plane distance and inliers about predefined candidates in a parallel that is not calculation iteration by randomly candidate select. Also, a histogram analysis is conducted to avoid eorror detection of non floor plane such as wall, desk, ceiling, and so on. The floor plane subtraction is performed using the selected floor plane candidate as shown Fig. 1. marked in brown. When compared with conventional RANSAC, operation time efficient decreased. The proposed system is designed in a field-programmable gate array (FPGA) implementation with low hardware resources.

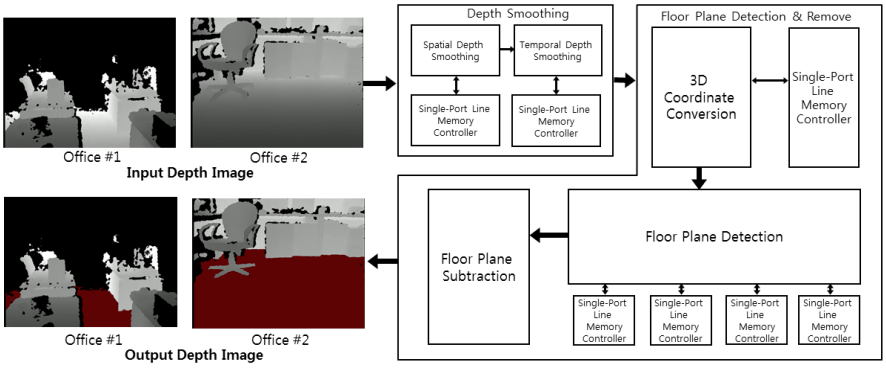

Fig 1. A block diagram of the proposed system

[1] D. Rempel, M.J. Camilleri, and D.L. Lee, Intl. J. of Human-Computer Studies, in press (2014).
[2] Z. Tomori, R. Gargalik, I. Hrmo, Proc. of the 20th Intl. Conf. on Computer Graphics, in press (2012).

Influence on Conduction Band Offset-controlled Dielectric Surface on the Performance of Low-temperature Photohemically-annealed IGZO TFTs

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Low-temperature solution-processed oxide semiconductor thin films attracted much attention because of their impact on the paradigm of future display and electronics. Unlike their competitors such as hydrogenated amorphous silicon (a-Si:H)- and polycrystalline silicon (poly-Si)-based thin films, oxide semiconductors possess the solution-processability, optical transparency and relative high performance as an amorphous form. It was hypothesized that high electron mobility of amorphous semiconductors arises from large spatial spread of spherical s-orbital of metal ions that form the conduction band. Among low-temperature process of sol-gel derived oxide semiconductors, photochemical activation has been known to be very effective in forming high-performance oxide semiconductor films at relatively low temperature (<150 ˚C). Despite recent successful demonstration of high-performance oxide semiconductor devices, further improvement in terms of the mobility is required to meet the performance criteria suitable for driver-circuit integration. So, higher mobility is still demanded for charging the capacitance within a specific time frame with lower voltage, which consequently results in low power consumption and increased device lifetime. Here, we present a promising way to improve the performance of low-temperature photochemically-annealed IGZO devices by the conduction band offset-controlled dielectric surface.

Structure and Electrical properties of Nitrogen doped ZnO thin film by Atomic Layer Deposition

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ZnO는 0에 가까운 Von과 전류 on/off 비율이 10^6 이상을 갖기 때문에 응용 가능성이 높은 산화 박막 트랜지스터로 많은 연구가 진행되고 있다. 최근, 10년간 ZnO는 3.3 eV 정도의 넓은 에너지 갭으로 인하여 투명 전자 소재로서도 큰 주목을 받고 있다. 그러나 ZnO는 박막 트랜지스터에 적합한 전기적 특성 관점에서 보면 높은 전하 이동도와 전기전도도로 갖고 있다는 한계점을 갖고 있으며 더 높은 μ_{FE}를 갖기 위한 노력이 필요하다. 전기적 특성을 향상시키기 위한 방안으로 dopant를 ZnO에 주입한 연구가 진행되고 있으며 Nitrogen을 ZnO의 dopant로 사용하였을 때 전하이동도가 감소하면서 mobility는 향상되어 박막 트랜지스터 특성이 향상된 결과가 보고되었다 [1]. 그러나 Nitrogen이 넓은 범위의 dopant로서 ZnO에 끼치는 전기적 특성 변화에 대한 연구는 진행되지 않았기 때문에 이에 대한 체계적인 연구가 필요하다.

본 연구에서는 균일하게 dopant density를 제어할 수 있는 Atomic Layer Deposition으로 Nitrogen doped ZnO을 증착하여 이의 구조적 및 전기적 특성 변화에 대한 연구를 진행하였다. XRD와 AFM 측정 결과 Nitrogen의 주입이 많아질수록 XRD의 intensity와 박막의 roughness가 줄어드는 것을 확인하였다. 이는 Nitrogen이 ZnO에 주입될때 ZnO의 Wurtzite 결정구조를 방해하기 때문으로 볼 수 있다. Nitrogen이 ZnO의 밴드갭에 미치는 영향을 알아보기 위해서 Ellipsometry 측정을 통하여 E_g을 계산하였고 Nitrogen이 도핑될수록 밴드갭이 줄어듦을 확인하였다. 이를 바탕으로 전기적 특성이 향상될 것을 예상하였고 홀 측정을 통하여 이와 상응한 결과를 얻었다. 앞으로, 향상된 전기적 특성을 갖는 Nitrogen doped ZnO로 박막 트랜지스터를 만들어 트랜지스터의 특성을 향상시키는 연구를 진행할 계획이다.

[1] S. J. Lim, Jae-Min Kim, Doyoung Kim, Soonju Kwon, Jin-Seong Park, and Hyungiun Kim, ECS, 157, H214-H218 (2010).

1-D Fiber-based Thin-Film-Transistors and Their Integration for large area 2 or 3-D Applications

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Fiber thin-film transistors (TFTs) have attracted lots of attention owing to board application in wearable electronics, flexible circuit, interfacing computers, skin-like pressure sensors and other application with human body. The most important consideration of Fiber-based TFTs is high carrier mobility and good electrical performance. We studied for metal oxide semiconductor (MOS) thin-film to apply to fiber-based TFTs because MOS TFTs have high electric performance, good uniformity, and various application. In this study, we demonstrated that MOS TFTs were fabricated by using facile dip-coating method on optical fiber. We shows transfer and output current characteristics of solution-processed indium oxide (InO_x) & IGZO TFTs, which are fabricated by using deep ultraviolet irradiation (DUV) with N_2 atmosphere on optical fiber [1]. The saturation mobility and on-off current ratio of fiber-based IGZO TFTs were 0.10~0.12 cm^2/V-s and $4x10^{6,}$ respectively. The demonstrated fiber-based devices by using facile dip-coating method can be used for flexible and wearable electronic application.

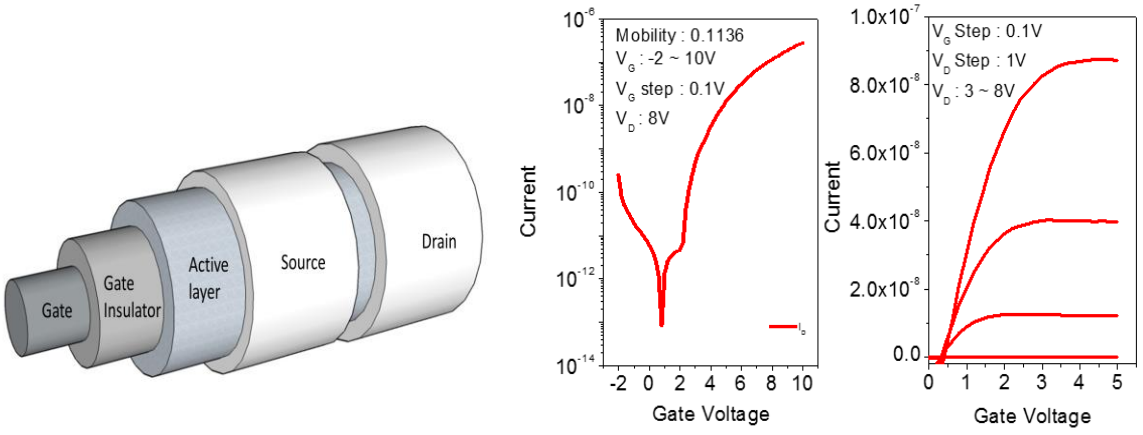

Fig 1. Structure of fiber Transistor and Transfer and output curve with gate voltage

[1] Y.H.Kim, J.S.Heo, T,H.Kim, S.J.Park, M.H.Yoon, J.W.Kim, M.S.Oh, G.R.Yi, Y.Y.Noh and S.K.Park, *nature. Lett.* **489** (2012) 128-132

Electrochromic mirror using viologen-anchored nanoparticle

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The Electrochromic (EC) devices can change reversibly their optical properties through darkening and bleaching state by changing external voltage. The EC devices have many advantages for commercialization such as low cost and environment friendly by the reasons of memory effects under open circuit status, high coloration efficiency and low power consumption. So the EC devices are possible to apply the display, smart window and electronic paper [1-2]. Among these, successed commercialization field is the electrochromic mirror(ECM) for the automobile. Now, the Gentex of America is market-dominating company because they have exclusive patents for liquid type ECM. In this paper, we made the ECM device as shown Figure 1 using the viologen-anchored nanoparticle and the simple method of screen printing. It has good optical properties of the high transmittance(%) and the fast response time(s). The driving voltage of the ECM device is +0.5V for the mirror state (bleaching state) and -2.5V for the darkening state respectively.

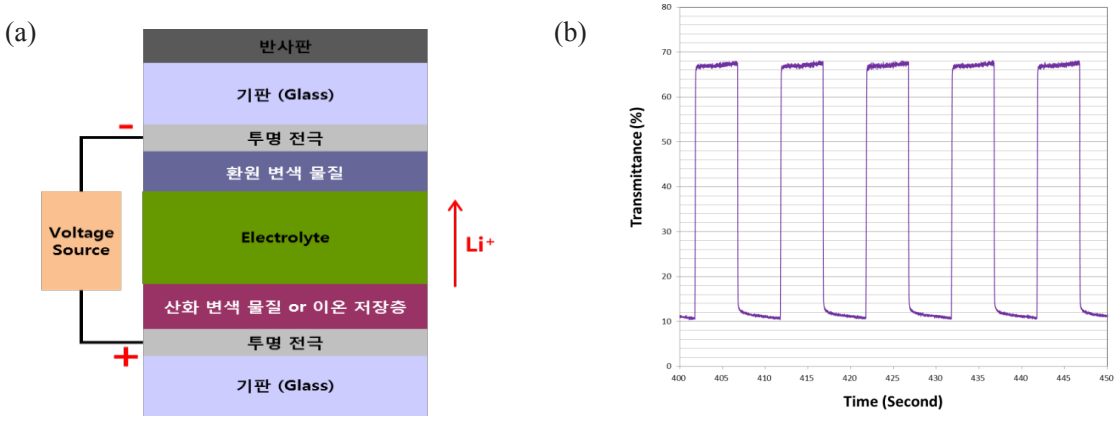

Fig 1. The schematic illustration of the electrochromic mirror device (a) and changes in the transmittance at 550nm during the repetition test of the device.

[1] X.W. Sun et al, Nano letters, 8, 1884-1889 (2008).

[2] T.Y Kim et al, Journal of Information Display, 15, 13-17 (2014).

Analysis of injection mechanism in organic light-emitting diodes with changing thickness of LiF interlayer

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LiF (Electron injection layer)의 두께를 가변 제작한 OLED 의 전기적 특성을 통해 전자 injection mechanism 에 대해 연구하였다. LiF 두께를 5Å/10Å/15Å 세 가지 조건으로 나누어 Luminance-Voltage (L-V) curve, Current density-Voltage (J-V) curve 와 Current efficiency-Voltage (CE-V) curve 를 이용해 분석하였다. 위 논문에서 구동전압 7V 이하를 저전압 구동영역 (Low voltage region: LVR), 7V 이상을 고전압 구동영역 (High voltage region: HVR)으로 나누었고 영역별 동작 mechanism 에 대해 연구하였다.

L-V curve 의 구동전압($100cd/m^2$)은 5Å(6.7V), 10Å(6.2V), 15Å(6.1V)이고 CE-V curve 는 15Å의 전류 효율(1.15cd/A)이 5Å(0.729cd/A), 10Å(0.76cd/A)보다 더 좋게 나타났다. 하지만, HVR 의 CE-V curve 에서 최대 전류 효율은 5Å(2.61cd/A), 10Å(2.95cd/A)의 효율이 15Å(1.31cd/A)보다 2 배 이상 좋게 나타났다 (Fig. 1(a)).

5Å의 경우, 상대적으로 증착된 fluoride 이온의 양이 적기 때문에 형성되는 surface dipole 의 양도 감소하여 전자를 끌어당기는 힘이 부족하다. 15Å의 경우, LVR 에서는 전기장의 영향보다 fluoride 이온의 전기음성도에 의해 전자를 쉽게 끌어 당겨 밝기와 효율이 좋게 나타난다 (Fig. 1(b)). 하지만 HVR 에서는 LiF 의 두께가 두꺼워질수록 절연체적 특성이 dominant 하여 터널링되는 전자 양이 감소하게 된다. 따라서 흐르는 전류 양에 비해 밝기가 나오지 않아 전류 효율이 떨어짐을 확인할 수 있다.

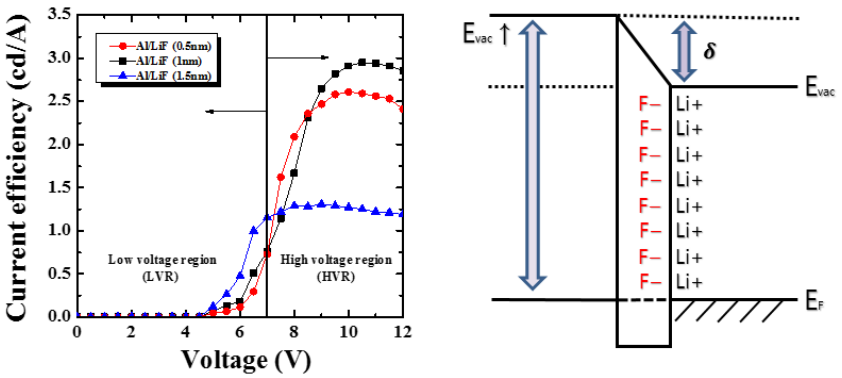

Fig. 1 (a) Current efficiency – Voltage (CE-V) characteristic graph
(b) Lowering electron injection barrier by surface dipole of LiF

A/D converter with Oxide Thin Film Transistor

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Oxide semiconductor thin film transistors (TFTs) have been widely studied and the high mobility characteristic and low-cost fabrication facilitate the system on a panel with various integrated circuits such as charge pump circuits, gate drivers, display backplane, and etc.

Therefor, there is increasing interest in the use of amorphous oxide semiconductors, such as amorphous-indium–gallium–zinc–oxide (a-IGZO), in designing integrated circuits. We developed AD converter (ADC) with a-IGZO TFTs. The transfer characteristics of a-IGZO TFT is shown in fig. 1 (a). The schematic for the ADC is shown in Fig.1 (b). Analog input voltages are compared with reference voltages. The reference voltages are not shown in Fig. 1 (b). The comparator was implemented with inverter circuit. The input voltages of 1.5V and 3.5V were converted to 3bit digital signal under full voltage of 8V. Fig. 1 (c) shows the digital output 001 for 1.5V and 001 for 3.5V.

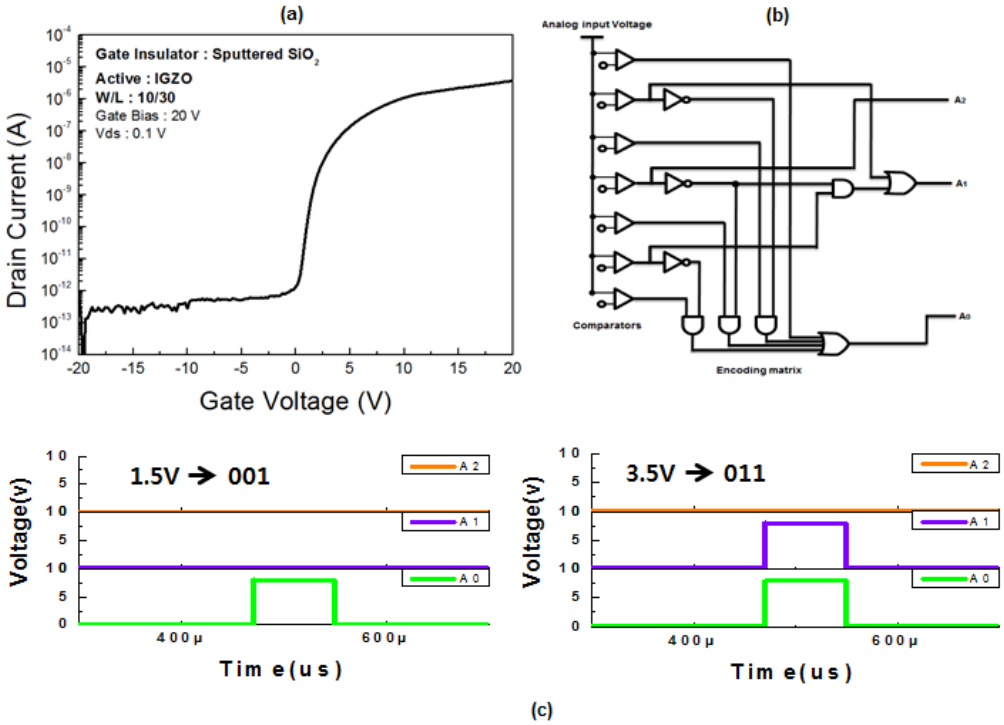

Fig. 1 (a) Transfer characteristics of the fabricated IGZO TFT (b) 3bit A/D converter

(c) 3 bit outputs for 1.5V and 3.5V for full voltage of 8V.

Functionalized Nanoporous Thin Films via Supramoleuclar Assembly of End-Functionalized Polymer Blends

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Supramolecular assembly of end-functionalized polymers, forming block copolymer-like supramolecules based on acid-base interaction, has utilized as a simple and facile method for generating functionalized nanoporous thin film. Different from the conventional block copolymer system having covalently bonded immiscible polymer blocks, those nanostructures have unique properties such as easy cleavability of the linkage between polymer blocks, which is advantageous to form porous structures. Moreover, functional groups left on the surface of porous structures after removing one domain can be potential active sites for additional functionality of the structures.

We report domain size-tunable nanoporous templates, based on utilizing supramolecular assembly of end-functionalized dendrimer with multi-arms and homopolymer. By controlling the number of end-functional groups of dendrimers as well as the molecular weight of homopolymers, domain size of thin nanoporous template films evolved in combination with the benzene/water co-solvent vapor annealing, could be successfully controlled. Our results suggest that end-functionalized polymer blend system having multiple ionic bonding sites can be a promising approach to achieve domain-size tunable multi-leveled nanoporous thin film.

Size-controllable functionalized nanoporous thin film by noncovalent bonding graft polymers

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Supramolecular self-assembly has been a big interest as a new method for bottom up lithography. It has great advantages not only for building nano-structures by easy method but also tuning the film surface properties by using end-functionalized polymer. The morphologies and structures for the thin film of supramolecular blend systems by end-functionalized polymers used which are mono-end-sulfonic acid terminated polystyrene (SPS) and poly(2-vinyl pyridine) (P2VP). The intermolecular complexes with P2VP as the backbone and SPS as the grafts were formed due to hydrogen bonding in their common solvent benzene. Graft polymer was formed micelle structure in benzene solution because of solvent affinity. We controlled micelle size from near 10nm to over 100nm by simply varing blend ratio or concentration in polymeric solution. We also demonstrated nanoporous film which has functionalized surface because chemical property of proper solution can affect its noncovalent bonding so it would remain functional groups on the surface of matrix, leading to nanoporous soft template with chemically useful functionalities rich on the surface of pores.

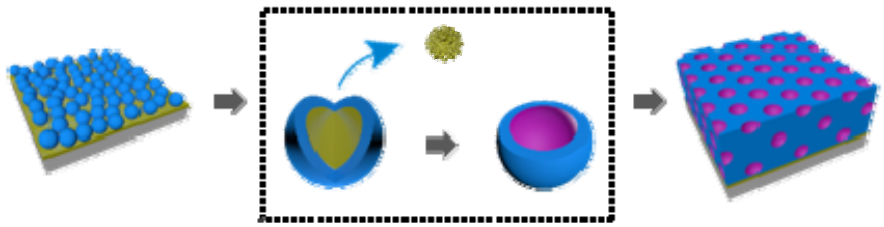

Fig 1. Schematic of micelle structure and porous thin film via supramolecular interaction

Mutual interaction observed in hydrothermal growth of one-dimensional ZnO nanorod arrays

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Precisely controlled growth of one-dimensional nanocrystals (i.e., wires, tubes and rods) has created opportunities to fabricate new types of devices with generic vertical configurations possessing advantageous electrical, optical, biological, and mechanical properties as well as high-density integration [1]. Solution-phase synthesis is a promising alternative to the conventional vapor-phase method owing to its advantages in commercial-scale production at low cost. This growth is usually achieved by a vapor-phase deposition method, in which key parameters determining the growth behaviors have been thoroughly investigated [2]. However, systematic investigation among neighboring crystals is still lacking in solution-phase synthesis. Here, we report on strong interactive growth behaviors observed during anisotropic growth of ZnO hexagonal nanorods arrays. In particular, we found multiple growth regimes demonstrating that the diameter of the rod is dependent on its height. Local interactions among the growing rods result in cases where height is (i) irrelevant to the diameter, (ii) increased with increasing diameter or (iii) inversely proportional to the diameter. These phenomena originate from material diffusion and the size-dependent Gibbs-Thomson effect that are universally applicable to a variety of material systems, thereby providing bottom-up strategies for diverse three-dimensional nanofabrication.

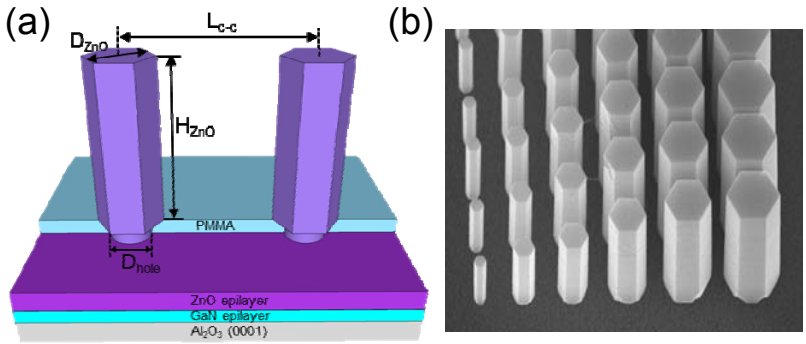

Fig 1. (a) Schematic illustrating geometry and definitions of the parameters (b) Height increment of ZnO nanorod along growing diameter

[1] A. M. Ionescu, and H. Riel, Nature 479, **329** (2011).
[2] M. T. Borgström, G. Immink, B. Ketelaars, R. Algra and E.P.A.M. Bakkers Nat. Nanotech. 2, **541** (2007).

Quantum transport simulation of spin-transfer torque (STT): nonequilibrium Green's function approach

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Spin-transfer torque magnetic random access memory (STT-MRAM) is one of promising candidates for the future memory device due to its higher scalability, lower power consumption, and faster operation [1]. Especially in the past two decades, there have been vigorous amount of attempts to study on its tunneling magnetoresistance (TMR) effect, spin-transfer nano-oscillator (STNO), and switching behavior [2-3]. In this work, we investigate the fundamental dependence of STT in 1D tri-layer magnetic tunnel junction (MTJ) on bias and polarized angles, respectively, solving the nonequilibrium Green's function. Furthermore, we make an attempt to identify the behavior of its parallel torque (in-plane torque, $\tau_{\parallel}$) and perpendicular torque (out-of-plane torque, $\tau_{\perp}$), which is exerted on the free-layer, for the numerical analysis of the magnetization vector's dynamics. In the presence of the spin current induced torque, we confirm that parallel torque shows monotonic dependence on bias, whereas perpendicular torque exhibits symmetric dependence.

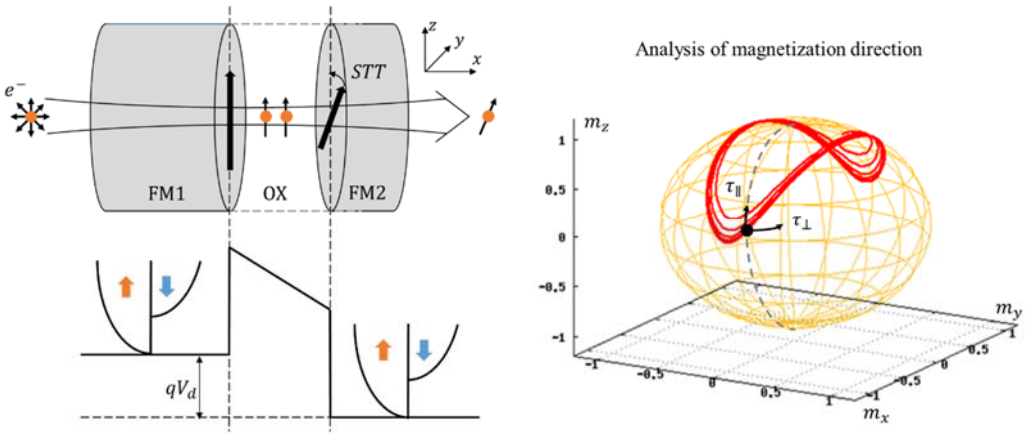

Fig 1. Band diagram of tri-layer MTJ structure and STT components

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Al2O3 scaling 을 통한 압전 폴리머/그래핀 터치 소자의 sensitivity 개선 연구

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그래핀은 특이한 밴드구조 때문에 전자와 공공의 이동 특성을 모두 가지는 양극성의 특징을 가지고 있으며, 전자 소자로의 응용에 있어서 전도도 조절은 매우 중요한 요소이다. 최근에 압전 폴리머인 PVDF-TrFE 를 이용하여 그래핀의 전도도를 조절하고, 이를 터치센서 소자에 응용하고자 하는 시도가 있었다.[1] 보고된 소자의 적층구조에서 그래핀의 안정적인 동작을 위해 Al2O3 절연막이 증착되는데, 핀홀 없는 균일한 막을 위해서는 일정 두께 이상이 필요하다. 하지만 터치센서 소자에 응용함에 있어서 두꺼운 절연막은 터치 소자의 sensitivity 를 감소시키는 문제가 있다. 본 연구에서는 Al 씨앗층을 이용한 Al2O3 scaling 을 통해서 그래핀과 압전 폴리머를 사용한 터치센서의 sensitivity 증가 가능성을 파악하였다.

Fig. 1 에서 소자의 공정 순서를 보여주고 있다. 그래핀을 ALD 공정을 이용해서 Al2O3 로 passivation 하기 전에 매우 얇은 Al 을 증착하고 후속 공정을 통해서 산화시킴으로써 후속 Al2O3 절연막이 잘 증착될 수 있는 기반을 제공함과 동시에 기존 보다 얇은 두께에서도 안정적인 소자 구동을 가능하게 한다. 이렇게 제작된 소자는 Fig. 2 에서 보듯이 3nm Al 로 기존 30nm Al2O3 보다 얇은 두께의 절연막에서도 Id-Vg 그래프에서 dirac 점이 보였으며, 여러 가지 하중에 의해서 dirac 점이 이동하는 정도가 기존 보고된 수치에 비해서 개선된 것을 알 수 있었다. 이러한 결과는 Al2O3 절연막의 scaling 을 통해서 터치 소자의 sensitivity 를 개선할 수 있다는 것을 보여주는 것이다.

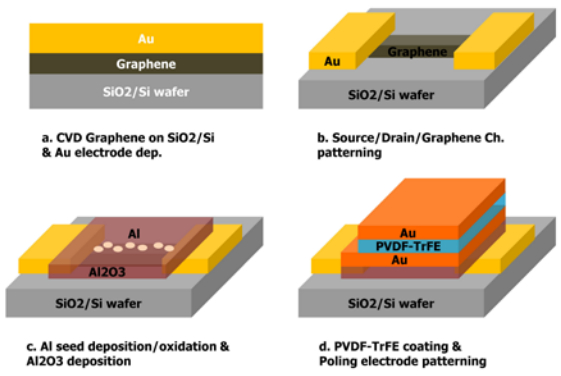

Fig. 1 압전 폴리머/그래핀 터치 소자의 공정 순서

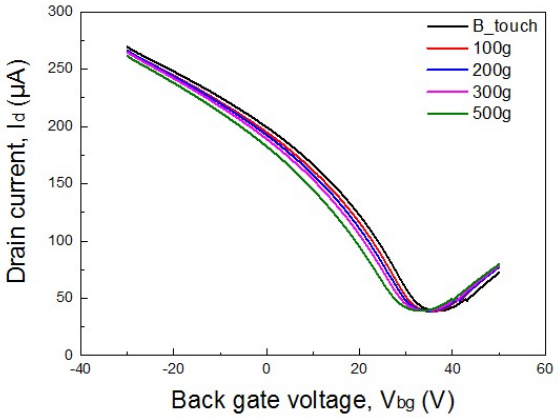

Fig. 2 Al2O3 scaling 터치 소자의 하중에 따른 동작 특성

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Acknowledgments: This work was supported by the Global Frontier R&D Program (2013M3A6B1078873) on Center for Hybrid Interface Materials (HIM) funded by the Ministry of Science, ICT & Future Planning

Asymmetric electrical characteristics of graphene-pentacene-metal heterostructure

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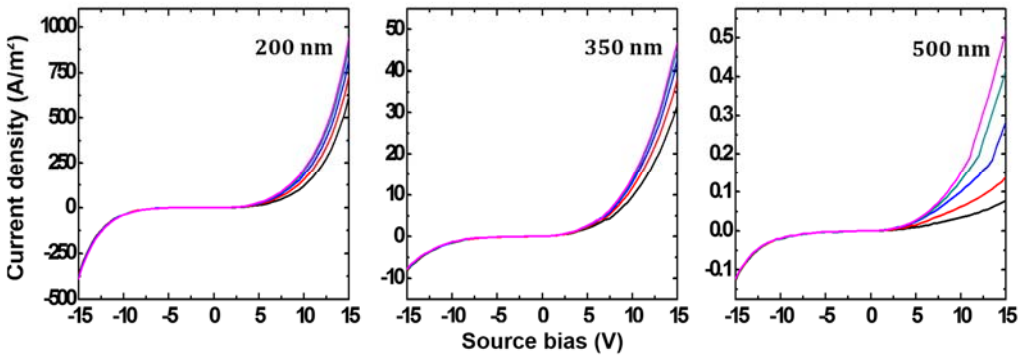
Graphene film has potentials to be used as electrodes in variaus electronic devices due to its outstanding electronic conductivity, transparency, and mechanical material properties. However, graphene has no band gap, so there is limitation for graphene to be used as an active material of convential field effect transistors. Recently, a few studies demonstrated an alternative architecture of graphene-based transistor, which is a vertical graphene heterostructure exploiting the absence of Fermi level pinning effect of graphene by its low density of states [1-2].

Here, we fabricated pentacene-graphene vertical heterostructure devices and characterized the electronic properties of these devices. The current flow in these devices was modulated by gate bias, indicating the gating effect in these devices. And we also demonstrated the barrier height modulation through the temperature-variable measurements. In particular, we observed that the current modulation induced by gate bias in positive source-drain bias(V_{sd}) was larger than that in negative V_{sd}. This phenomenon is attributed to the different contact properties of pentacene layer. This study may suggest a novel device platform of pentacene-graphene vertical heterostructure applicable to another organic materials or molecules.



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Inorganic-based Flexible Electronics for System on Plastic

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The demand for flexible electronic systems has recently increased due to their advantages over present rigid electronic systems. Although many researchers have studied various flexible electronic devices, their applications have been restricted to one or just a few components of the electronics and thus each electronic device must be integrated into a single device to perform its respective function within a flexible system. To realize such all-in-one flexible systems, the development of flexible memory is a key issue for data processing, information storage, and radio frequency (RF) communication.[1] Resistive random access memory (RRAM) is considered as a promising candidate for flexible memory in SoP due to its advantages of simple structure, high-density integration, low temperature process, high-speed switching property, and low power consumption.[2] In this presentation, to demonstrate fully functional flexible resistive memory, various structure of flexible resistive memory devices were demonstrated using several fabrication processes.

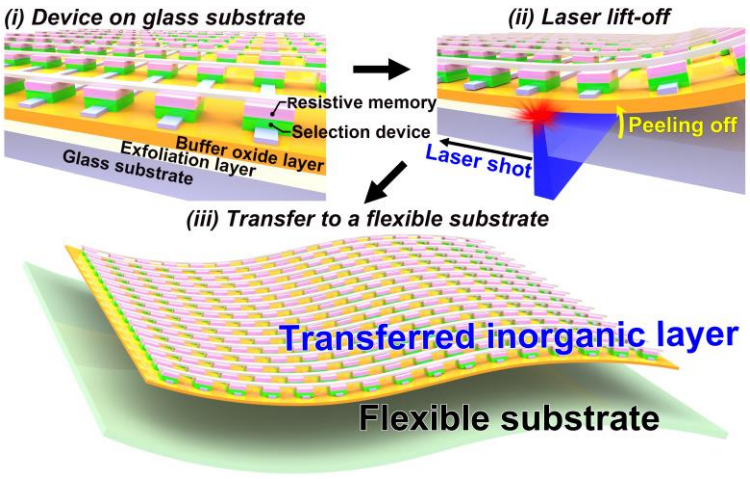

Fig 1. Schematic illustrations of the process for fabricating flexible crossbar-structured memory on a plastic substrate via the ILLO method

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Uncertainty of Contact Properties between Titanium and Naturally Occurring MoS_2

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Recently, there is a great interest in transition metal dichalcogenides (TMDs) such as MoS_2 because of their interesting electronic and optical properties.[1] However, high performance MoS_2 thin-film transistors (TFTs) require the formation of low-resistivity metal-MoS_2 junctions since non-ideal electric contacts formed on MoS_2 can fundamentally hamper any attempts to improve transistor performance.[2,3] The understanding of metal-MoS_2 junctions is further complicated as electronic properties of naturally-occurring MoS_2 can be variable.[4] In this paper, we fabricated bottom-gated TFTs based on mechanically exfoliated MoS_2 crystals and investigated the variability of electrical properties of Ti contacts. The current-voltage measurement indicated two distinct contact behaviors of TFTs, which were fabricated by the same processes and have the same device structures (Fig. 1). The current-voltage measurement at different temperatures further revealed two distinct transport behaviors: while a group of TFTs showed a phonon-scattering dominated transport, the other group of TFTs showed a thermally activated transport. Our results deliver experimental evidence of the variability of Ti contacts on MoS_2 highlighting the importance of understanding the variability of electronic properties of naturally occurring MoS_2 for further investigation.

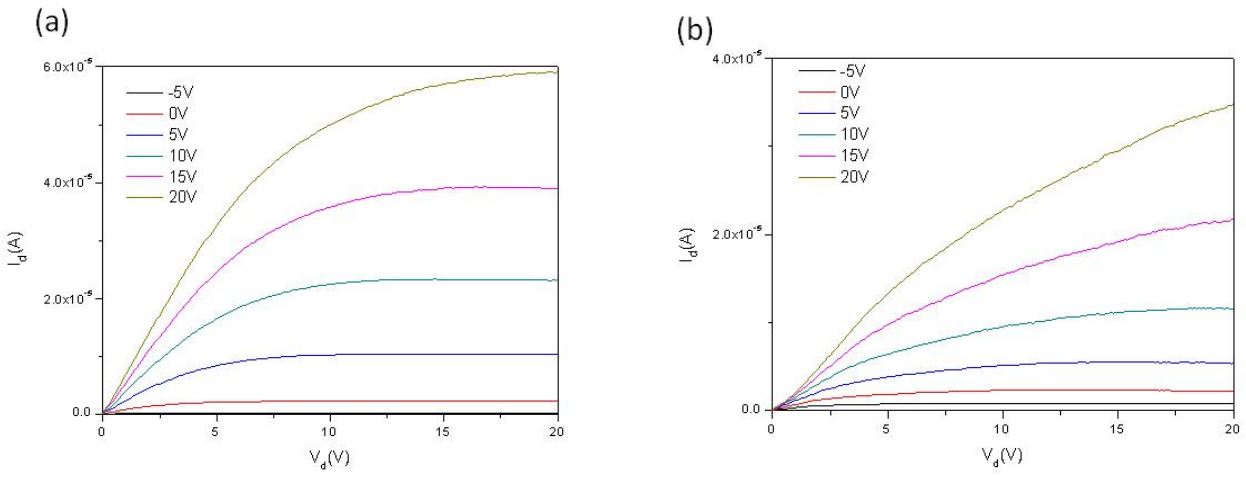

Fig. 1. Output characteristics of two MoS_2 TFTs exhibiting (a) an ohmic and (b) a Schottky contact behavior. Significant differences in conductance and saturation current can be observed.

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Simple solution-processed AC Driven Polymer Electroluminescence Device using silver nanoparticles in hole injection layer.

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Electroluminescent (EL) devices based on solution-processed printable materials that include fluorescent polymers and, more recently, colloidal semi-conducting quantum dots (QDs) are quite attractive for a variety of emerging mobile applications due to their low production costs and potential for fabrication into flexible, large area, lightweight devices.[1]

We report an extremely high brightness of solution-processed full color polymer AC EL device with brightness of approximately 2300 cd m^{-2} for blue. A novel strategy was employed to ensure high brightness. The self-assembled block copolymer micelles(PS-b-P4VP) were incorporated as dilute agents to restrict the inter-chain interaction of fluorescent polymers. Highly dispersed MWNTs with poly(styrene-*block*-4vinylpyridine) (PS-*b*-P4VP) micelles in toluene were homogeneously mixed with fluorescent polymers. This is consistent with our previous results regarding single-walled carbon nanotubes (SWNTs).[2]

The AC driven hole injection was used between fluorescent polymers with simple solution-processed silver nanoparticles in hole injection layer. We demonstrated an extremely high brightness of solution-processed polymer AC EL device with brightness of approximately 30000 cd m-2 for yellow.

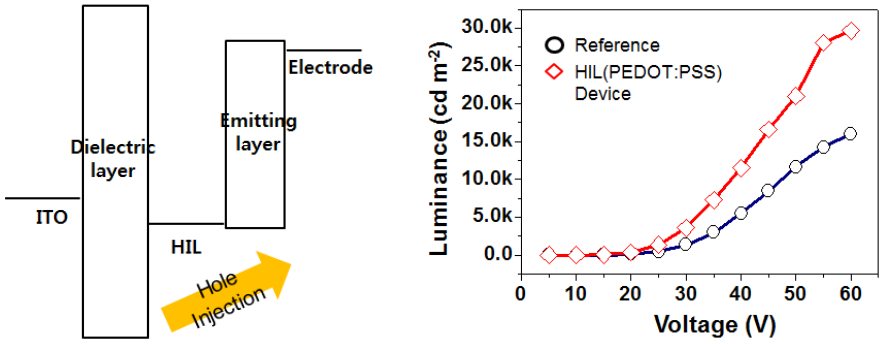

Fig 1. AC driven PLED device architecture and its luminance data

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Effect of Channel Length, Thickness and Annealing Temperature on Nanoscale GIZO Thin Film Transistor Performance

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Ga-In-Zn-O based thin film transistors (TFTs) have attracted considerable attention in the recent years due to their superior properties, which made this material a suitable candidate for switching applications in display, memory, and logic devices [1]. In memory devices, scalability is the basic requirement to achieve high operation speed, low power consumption and high storage capacity. Hence, it is important to scale down the channel dimensions (length and width) without degrading the TFT performance. Researchers studied different parameters (e.g., effect of channel length etc.,) to enhance device performance of scaled device [2]. However, in the previous studies, channel thickness and annealing temperature for nanoscale channel width has not been explored. These two parameters (thickness and annealing) adjust the channel resistance path and thereby enhance the switching behavior, applicable for the memory devices.

In our work, we studied the effect of channel thickness and annealing temperature on nanoscale channel width devices (W-500nm, L-100μm). Later, we studied the effect of channel length for various channel lengths (500nm, 1μm, 70μm, and 100μm), in which the channel width (500nm), thickness (90nm) and annealing temperature (200^{o}C) were kept constant. We found that the device with minimum channel length (L) of 500nm shows enhanced on/off current ratio of 10^6, with minimum threshold voltage (0.26V) as shown Fig. 1.

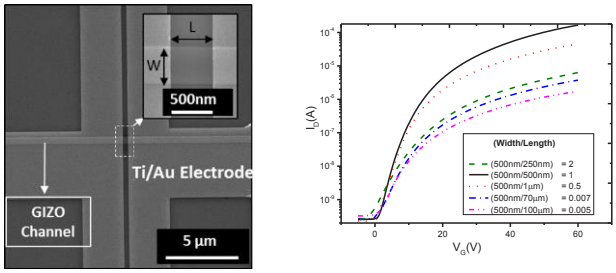

Fig.1 SEM image of nanoscale TFT (W/L- 0.5μm/0.5μm) and the transfer characteristics for different channel length

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Advanced method for preparing silicon nanopores array using AAO stencil and polymer interlayer

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Utilizing as an etching mask is one of the most popular applications of AAO template. In the etching process, a through-pore structred AAO template is placed on the substrate to be used as an etching mask. Ultra-thin AAO membrane can be attached onto the substrate by Van der Walls attractive force. However, the rough surface of AAO membrane cannot form a conformal contact with the substrate's surface. The resulting etched NP array also shows not-regular pore shapes and damages by unwanted etchings. [1]

In our research, we prepared an open-through structured AAO membrane, and utilized it as an etching mask. Silicon nanopore (SiNP) arrays are fabricated by reactive ion etching process. Additionally, we inserted polymer interlayer between AAO membrane and Si substrate to form a conformal contact. The SiNP array which is etched with polymer interlayer show more regular structure than the case without interlayer. Our result, which improves the uniformity and reproducibility of the etched SiNPs array, can be applied to the nano-fabrications and applications which require fine size-controls.

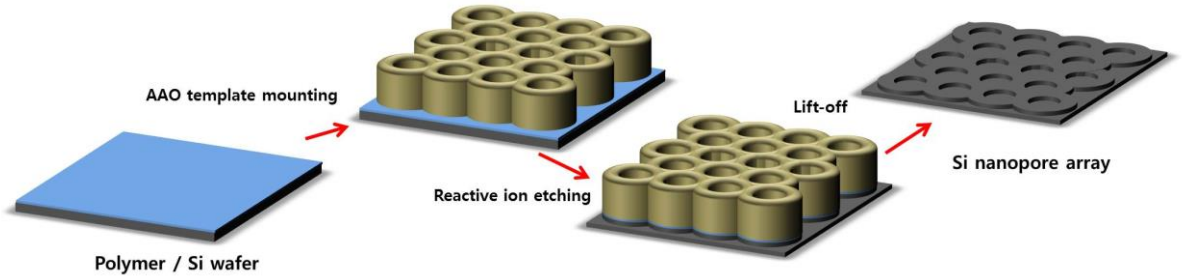

Fig 1. Process flow of fabrication of silicon nanopores (SiNPs) array

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Inkjet-printed source/drain contact for solution-processed single-walled carbon nanotube thin-film transistors

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Single-walled carbon nanotubes (SWCNTs) have been considered as active-channel materials of the next-generation flexible thin-film transistors (TFTs) owing to their excellent mechanical and electrical properties. After semiconducting-SWCNTs sorted by density gradient ultracentrifugation method were reported, the solution-processed SWCNT-TFTs have been widely used for various electronic applications such as logic circuits, radio-frequency devices, and readout circuits for sensor arrays because of their advantages such as facile scalability at low cost[1]. However, a conventional and expensive vacuum process used to fabricate source and drain (S/D) electrodes hinders development of the solution-processed SWCNT-TFTs in printable and flexible electronics for large-area applications. In order to fully utilize the advantages of the solution-process, the expensive vacuum process should be replaced by a cheap and scalable process such as inkjet-printing. Therefore, in this work, we demostrated a solution-processed SWCNT-TFTs with the inkjet-printed silver (Ag) source/drain electrodes and their electrical characteristics were compared with thoses of the TFTs with the thermally evaporated Ag and Au electrodes. We also characterized the work function of each layer and the corresponding contact resistance. The SWCNT-TFT with the inkjet-printed Ag S/D electrodes showed higher on-current level than that of the SWCNT-TFT with thermally evaporated Ag electrodes, and even exhibited comparable electrical properties with the SWCNT-TFT adopting the thermally evaporated Au electrodes. Such results can be explained by good contact properties between the inkjet-printed electrodes and the SWCNT active layer. The detail analysis will be discussed at conference.

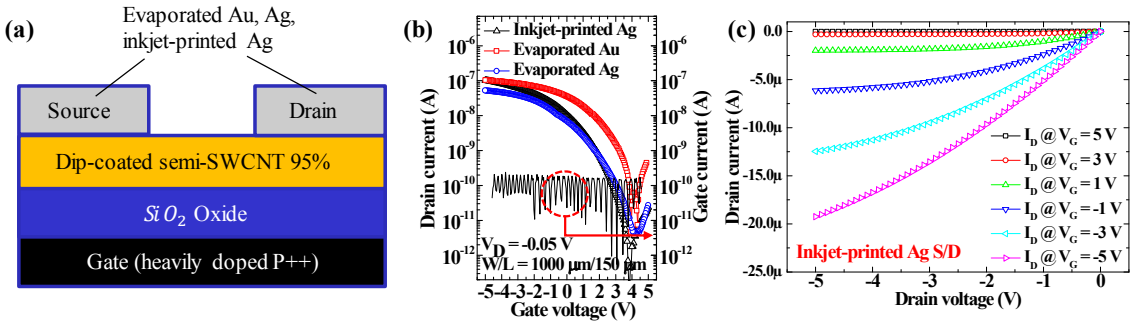

Fig. 1. (a) Schematic illustration of device structure for the SWCNT-TFTs. (b) Transfer characteristics of the SWCNT-TFTs with thermally evaporated Ag and Au, and inkjet-printed Ag electrodes. (c) Output characteristics of the SWCNT-TFTs with inkjet-printed Ag electrodes.

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Nanoscale Metal Pillar Arrays on Elastomeric Substrates for Surface-enhanced Raman Spectroscopy Platform

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The nanostructures found in nature have sometime an elaborate three-dimensional structure made up with the soft and flexible constituents, and they exhibit diverese mechanical and optical functions. Here, we introduce a low-cost and facile nanofabrication technique based on hot embossing process[1] that can enable the replication of sub-micro and nanoscale patterns on polystrene (PS) substrates. We have fruther developed this technique to achive nanoscale metal pillar arrays by conformal coating of metallic films on polymeric templates. The metal nanostructures consist of a large array of circular pillars with uniform diameter of 150 nm and height of 200 nm, and with the center-to-center spacing between the pillars of 500 nm. The Au nanopillars display a smooth surface and uniform dimater along the vertical direction, and thereby can be exploited as a flexible and large area surface-enhanced Raman spectroscopy (SERS) platform[2]. Raman spectroscopy studies revealed that our platforms exhibited 3×10^3 and 7.3 enhancements of Raman peak at 1624cm^{-1}, compared with bare planar silicon and gold coated planar PS substrates, respectively.

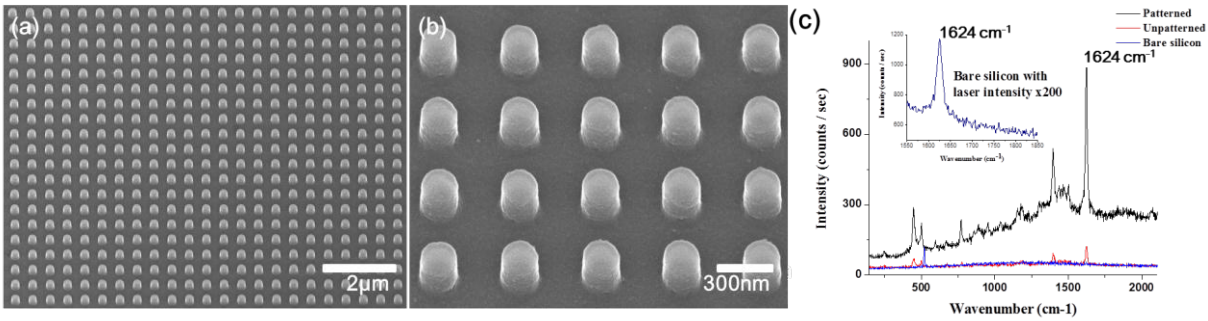

Fig 1. (a-b) Scanning electron microscopy (SEM) images of patterned PS substrate. (c) Raman spectra of Methylene blue (5×10^{-4}M) on the Au pillars on PS (black), Au film on planar PS (red) and bare planar silicon (blue) substrates.

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Design of thin film color filters with highly absorbing dielectrics

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Thin film comprised of one or more dielectric/metallic materials is used in wide range of applications. Typical dielectric thin film is based on interference effect of incident and reflected waves, which yields anti-reflection, high-reflection, and dichroism, as a result of multiple optical passes through transparent layers with thicknesses of the order of the wavelength. Highly absorbing dielectrics(e.g., germanium), however, are not used due to non-trivial phase shifts on the interface of layers. Furthermore, strong resonance occurs in thin films, which are much thinner than the standard quarter-wave dimensions, because of the large optical attenuation within the highly absorbing dielectrics interface and uncertain phase shifts[1]. Herein, we design these ultra-thin lossy films by calculation, fabricate the samples using e-beam evaporator by modifying the reflectivity of a gold(Au) surface with a Ge film of a few nanosclaes gradient in thickness, and measure with the UV/VIS/NIR spectrophotometer at visible wavelengths. As a result, these films emerged different colors(pink, blue, and violet) each. The wide optical absorption band influences the color by suppressing the reflectivity in a portion of the visible region. This study shows that various colors can be obtained the appropriate modification in reflectivity by controlling Ge thickness instead of using dyes. Accordingly, this concept will be applied to design color filters in order to express wide color types.

* This work was partly supported by the KBSI grant (D34500) and by Basic Science Research Program through the NRF funded by the Ministry of Science, ICT & Future Planning (2014R1A1A1005945).

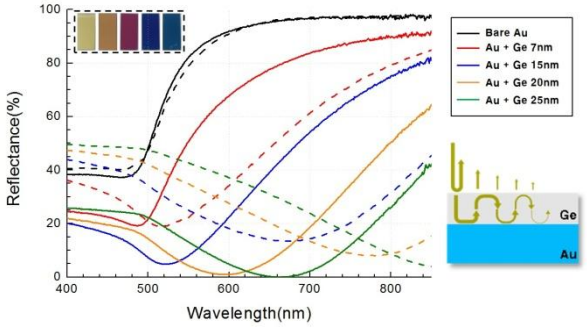

Fig1 | Reflectance of measurements(solid) and simulations(dash) following the scheme(right bottom), and the inset(left top) shows samples(0,7,15,20, and 25nm of Ge film).

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Design of hollow silica nanospheres in antireflection coating for high efficiency optical devices applications

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Reflection due to refractive index mismatch at the interface between two different media cause a significant loss of transmitted light, which can deteriorate the performance of many optical devices. Antireflection(AR) coatings are used to reduce this loss by destructive interference principle. AR properties are determined by both the low refractive index and optical thickness of a coating layer. However, conventional AR coatings have difficulties to find materials with adequate refractive indices. As a way to obtain two main factor of AR coating, the studies on various synthesis method of hollow silica nanospheres have been studied. Diameter and inner ratio of hollow silica nanospheres can be controlled to satisfy the AR conditions for various substrates [1]. While many experimental studies to generate hollow silica with different sizes and shapes were reported over the last few years, only few researches on the theoretical modeling of hollow silica were reported. In this study, we present design issues of hollow silica nanoparticles for AR coatings on various materials. A rigorous coupled wave analysis (RCWA) method were used for the calculation of E-field distribution and reflected power. This study would be fruitful for designing high performance AR structures for various optical device applications. *This work was partly supported by the KBSI (D34500) and by Basic Science Research Program through the NRF of Korea funded by the Ministry of Science, ICT & Future Planning (2014R1A1A1005945).

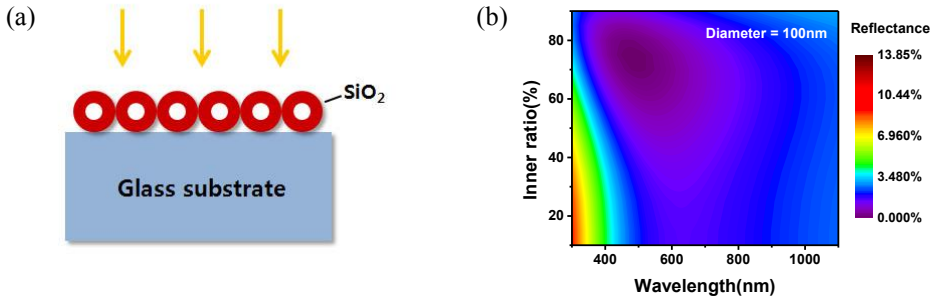

Fig 1. (a) Schematic of AR layer with hollow silica nanospheres, (b) Contour plot of the variation of reflectance of hollow silica nanospheres with a diameter of 100nm as a function of inner ratio and wavelength.

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Colloidal beads fabricated printing and rubbing processes for efficient light extraction from polymer light-emitting diodes

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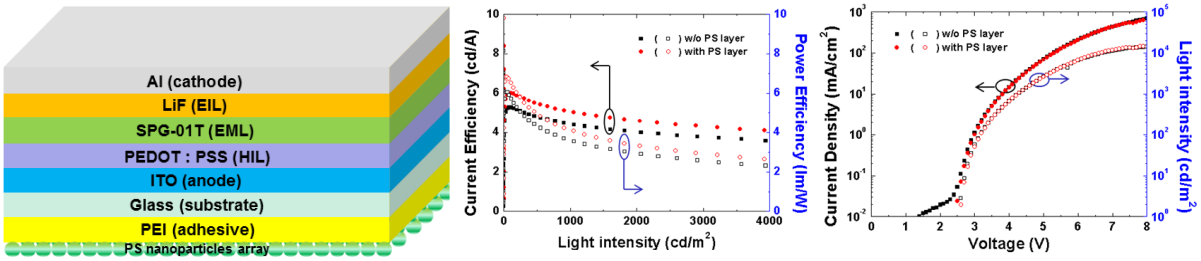
Organic light emitting diodes (OLEDs) have been key technology for flexible display and solid-state lighting applications. However, out-coupling efficiency of the conventional OLEDs is only up to approximately 20% due to the total internal reflection, absorption and surface plasmon modes [1]. Therefore, in order to extract more light from the OLEDs, especially from the glass/air interface, several methods have been proposed, which include texturing substrate surface and attachment of microlens array or colloidal particles [2]. It is noted that in most cases, rather complicated processes were used to produce such structures. In this study, we demonstrated a simple way to fabricate photonic crystal (PC) beads and thus extract more photons which were trapped in the substrate mode. We attached polystyrene (PS) colloidal photonic crystal (PC) beads on the glass substrate by using a simple rubbing [3] and transfer process after poly (ethyleneimine) (PEI) patterns were formed on the substrate via an inkjet printing process. Fig.1 shows structure of the polymer light-emitting diode (PLED) with the beads, and current and power efficiencies of the fabricated PLEDs. PC beads showed much improved light extraction in comparison with the conventional PLEDs. Details of the fabrication process and device performance will be discussed at the conference.



(a) (b) (c)

Fig 1. (a) Schematic diagram of a PLED device with PS particles array. (b) Current efficiency and Power efficiency versus light intensity of the PLED without/with PS particles array. (c) I-V-L characteristics of the PLED without/with PS particles array.

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Quantitative analysis of scanning electron microscope images by using Monte Carlo simulation technique

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Extraction of information about the three dimensional shapes and composition of the object from the two-dimensional scanning electron microscope (SEM) images is a very difficult problem. Monte Carlo (MC) simulation technique can provide vital information for quantitative analysis of SEM images [1]. A good approximation to a real object may be an imaginary object whose simulated image is best matched with real SEM image. In this presentation we report a case of quantitative analysis of the structure of a standard specimen by comparison of MC simulation images with real SEM images. The simulation images are synthesized by tracing the individual electrons within the specimen by using the MC technique. The backscattered and secondary electrons coming out of the specimen are collected and used to synthesize the simulated image which is to be compared with the real SEM image.

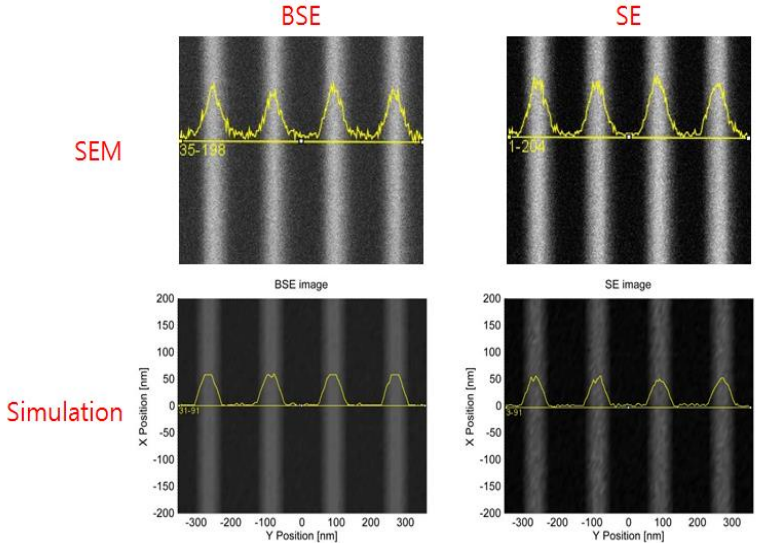

Figure 1. The image of SEM and computer simulation.

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Wafer defect inspection using component tree of SEM images

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Inspection is a very important issue for improvement of yield and productivity in semiconductor manufacturing industry. Many researches have been progressed to enhance accuracy and efficiency of defect detection and various inspection technologies have been developed[1]. Analyzing SEM images of silicon wafers is a general way of inspection of the wafer based on computer vision technology.

In this paper we propose a defect detection method using component tree of SEM images. A component is a set of pixels which remain after thresholding and connected with each other. When we change the threshold, components grow or shrink. There is an inclusion relation between the previous and current components, so the components can be organized in a tree structure. The component tree has essential features of the image, therefore it can be used to find defect and using component tree is more efficienct than analyzing whole image. Even though this method needs additional computation time for building component tree, we can build it in quasi-linear time by refering to [2].

We build a component tree and compute some attributes for each node such as area and volume. Area means a size of component and volume is related to difference between the component and its neighbors. Next, we delete the leaf nodes sequentially in order of small volume and find the components having enough volume as well as being not bigger than the predefined defect size. By marking the components we found and their children on the image we can identify the regions of suspicious defect.

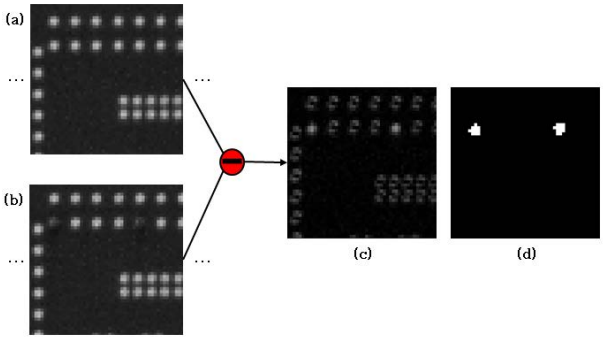

Figure 1 (a),(b) Input images. (c) Difference image (d) The two most significant lobes of (c).

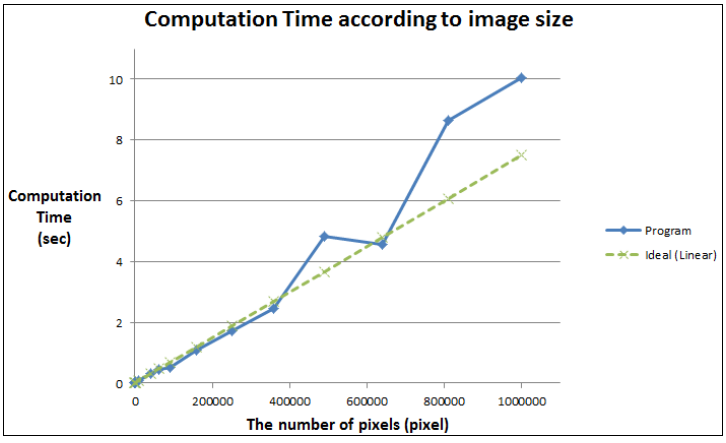

Figure 2 Computation time of whole process according to image size.

[1] Bong-Jin Yum, Jae Hoon Koo, and Seong-jun Kim, "Analysis of Defective Patterns on Wafers in Semiconductor Manufacturing: A Bibliographical Review", IEEE International Conference on Automation Science and Engineering, August 20-24, 2012.

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Dopant Depth Profiling on the Small Pattern by using Nano-SIMS

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Dopant depth profiling in large area have been investigated with quadrupole based SIMS and conventional magnetic sector based SIMS for several years [1]. Recently, depth profiling in small area have been of interest. To date, the accepted method of such a small area profiling has been based on the use of TOF SIMS instrument [2]. However, a disadvantage of such a conventional SIMS is their difficulty to achieve depth profiling in raster size below 30 micron. A beam of Cs^+ or O^- primary ions in Nano SIMS is focused and rastered on the surface of the sample, down to 50nm beam size [3]. Nano SIMS instruments can readily achieve small raster size less than 10 micron.

The instrument used in this study was Cameca Nano SIMS and IMS 6f. Depth profiles on Nano SIMS were acquired in small area below 10 micron. Small area depth profiling of Nano SIMS was compared with the results of a Cameca IMS 6f obtained in large area depth profiling. The profile shapes, sputter rates and detection limits obtained on Nano SIMS instrument will be discussed on the small pattern.

[1] R.G.Wilson, F.A.Stevie, C.W.Magee, "*Secondary Ion Mass Spectrometry*", John Wiley and Sons, New York, 1989
[2] E.Niehuis, T.Grehl, "*Dual Beam SIMS Depth Profiling*",Proceedings of SIMS XII, Elsevier, 2000, p. 49
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Color-Offset Analysis Methods to Enhance the Overlay Control

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The overlay control is mainly composed of scanner overlay performance, overlay key design and metrology. All the contributors are doing their best to extend their technology to future generation, delivering new scanners, new metrology tools, and new types of mark. However, in advanced applications, these extensions may not be able to meet the control requirement, consequently, additional breakthroughs are required. Overlay metrology accuracy has been considered that it is dependent on stack complexity and key deformation [1]. We have paid attention to key and process optimization, on the assumption that low residual number means more accurate measurement. However, cost and technology limit makes it impossible to meet well-optimized process every time. When well-optimized process is not used, both real misalignment and measurement inaccuracy would be considerable. In this study, we investigated methods to enhance the overlay control, approaches by extraction of real misalignment out of overlay measurement. So far, only the destructive inspections like vertical SEM have enabled us to measure real misalignment. However, we are not able to apply this destructive method to monitoring and overlay control for real products. Instead, a concept of non-destructive method is proposed in this paper.

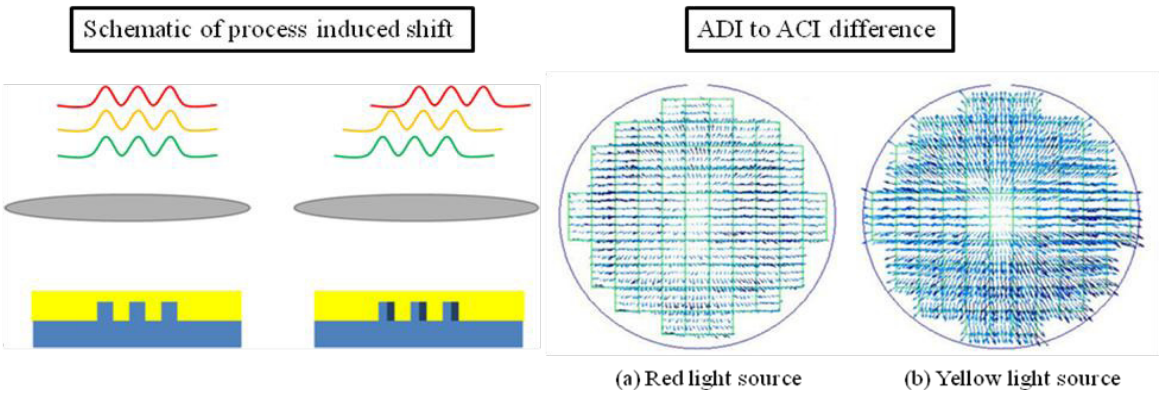

Fig 1. Color-offset induced by mark asymmetry

[1] J.-H. Yeo, J.-L. Nam, S.-H. Oh, J.-T. Moon and Y.-B. Koh, N. P. Smith, and A. M. Smout, Proc. SPIE 2725 (1996)

Fabrication Process of Modified Source Lens Structure for High Resolution Electron Optical Microcolumn

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Abstract

High-resolution electron beam is required for e-beam lithography, metrology and inspection of semiconductor or display devices. Microminiaturized electrostatic electron optical column is a prominent tool with millimeter in size and low voltage operation that can achieve few nm resolutions [1-2]. New electron optical microcolumn design, as shown in figure 1, has already been made with the modification in source lens system which is easy to align, enhances e-beam current and fabrication of the microcolumn becomes easier as well [3]. An additional electrode S_{2s} has been added to 3 source lens system (S_1, S_2 and S_3) with some modifications in which S_1, S_{2s} and S_2 have aperture diameter of 50 nm and S_3 has 10 nm. With the above configuration, the simulation result shows that the additional electrode controls the excessive degradation of the resolution which gives probe beam size to sub-50 nm with improved beam current of 10 nA at the target by applying beam energy of 1 keV [3]. We are trying to achieve the same result experimentally which was obtained by the above simulation work.

Electrode lens is fabricated with MEMS technology and anodic bonding is done with Pyrex. We present a new assembled microcolumn having above configurations and its experimental verification.

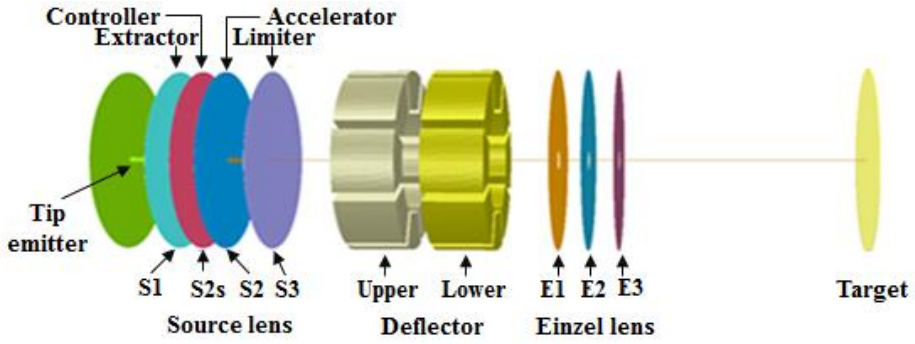

Figure 1. Column structure shows one additional electrode S_{2s} is inserted between S_1 and S_2.

References

[1] E. Kratschmer, H. S. Kim, M. G. R. Thomson, K. Y. Lee, S. A. Rishton, M. L. Yu, S. Zolgharnain, B. W. Hussey and T. H. P. Chang, J. Vac. Sci. Technol. B 14, 3792 (1996).
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A nano-focus X-ray source using carbon nanotube field emitters for semiconductor inspections

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A nano-focus X-ray computerized tomography (CT) has been a prominent tool for the nondestructive semiconductor inspections [1]. Also, as a strong candidate for field-induced electron emitters, carbon nanotube (CNT) has a favorable geometry of very high aspect ratio along with high electrical and thermal conductivity [2]. For most applications of CNT emitters in X-ray sources, it is important to keep the small focal spot of electron beam (E-beam) for the high-resolution X-ray images. In order to obtain a nano-focus X-ray source based on CNT emitters, we have designed special focusing lens systems with an electrostatic lens and electrostatic/magnetic lenses by using a commercial 3-D simulator. The field emission properties of the fabricated CNT emitters and the transmittance of E-beam through the gate are shown in Fig. 1. The designed X-ray source would be expected to show a small focal spot with a relatively high anode current, providing semiconductor inspections such as 3D micro-defect evaluation.

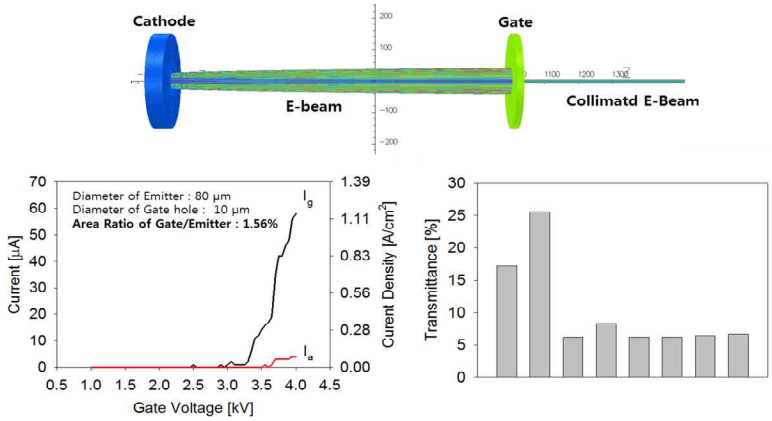

Fig 1. Field emission properties of the CNT emitters and transmittance of E-beam

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2D CNT tip을 이용한 초소형 전자칼럼의 전자빔 특성 연구

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전자빔 장치는 반도체 장치를 제조하기 위한 노광 공정 및 반도체 장치를 검사하기 위한 검사 공정에 주로 사용되어 왔다. 전자빔 장치를 이용한 공정은 공정 시간이 많이 걸린다는 단점이 있어 전자빔 장치를 이용한 공정의 throughput 을 향상시키기 위해 초소형 전자칼럼이 고안되었다[1-2]. 초소형 전자칼럼의 전자방출원으로는 주로 그림 1 (a)와 같이 텅스텐 FE (field emitter) tip 을 사용해 왔으나, FE tip 과 lens 의 aperture 를 정렬하는 데 어려움이 있었다. 또한 FE tip 은 1keV 이상의 에너지에서 불안정하게 작동되는 특성이 있다. 이와 같은 FE tip 정렬의 어려움과 1keV 이상에서 tip 의 특성을 향상 시키기 위해서 그림 1 (b)와 같이 2D CNT tip 을 전자칼럼의 전자방출원으로 이용하려는 연구를 진행하였다. CNT 를 금속의 단면 전체에 2 차원으로 형성하여, tip 과 aperture 정렬의 어려움을 해결하고, 전자현미경 이미지를 획득하였다(그림 1(c)). 본 논문에서는 2D CNT tip 을 이용한 초소형 전자칼럼의 특성에 대해 논의하고자 한다.

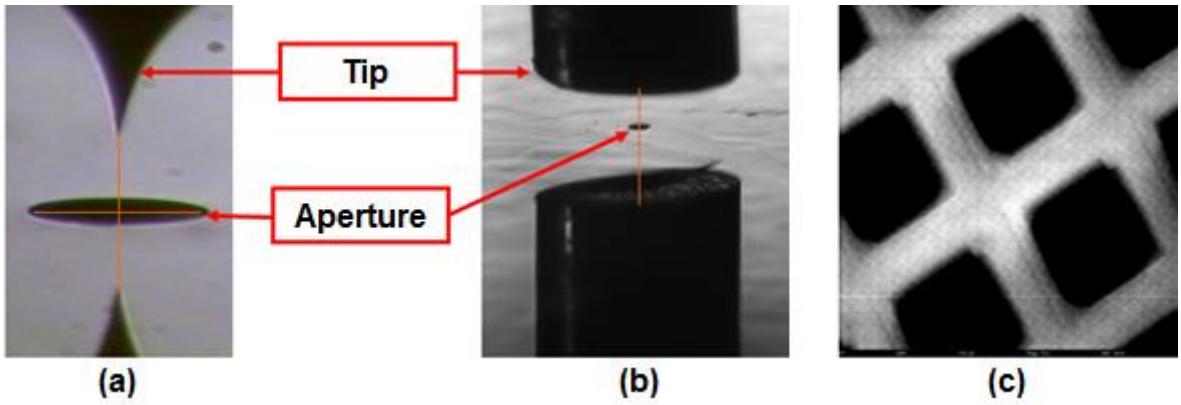

Fig 1. (a) FE tip 의 얼라인공정, (b) 2D CNT tip 의 얼라인공정, (c) 2D CNT tip 의 SEM 이미지

[1] E. Kratschmer, H.S. Kim, M.G.R. Thomson, K.Y. Lee, S.A. Rishton, M.L. Yu, S. Zolgharnain, B.W. Hussey, T.H.P. Chang, J. Vac. Sci. Technol. B 14 (6) (1996) 3792.
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전자 빔을 이용한 미세 오정렬 계측 시스템

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반도체 공정 미세화에 따라 회로패턴지역과 오정렬 패턴지역에서의 빛의 회절 특성이 달라져 상관도가 저하되어 광학적 방법으로 회로지역 패턴의 오정렬도 관리가 불가능해져 분해능이 높은 전자빔을 이용한 회로패턴지역의 오정렬을 실측하는 방법이 필요하다.

SEM 기술의 발전으로 인하여 웨이퍼 표면의 정보를 획득하는 기술뿐 아니라 하층부(표면에서 300-400nm 이하)의 정보를 획득하는 기술이 확보되어서 오정렬 값을 측정할 수 있는 기본 이미지 확보에 많은 진전이 가능하게 되었는데, 본 시스템에서는 포토 공정에서 PR를 입히고 develop후에 표면과 하층부의 이미지를 동시에 획득하여 오정렬을 측정하였다. 이미지 왜곡 현상을 최대한 영향을 적게 받으면서 오정렬 정밀도를 높이는 이미지 획득 방법을 다양한 테스트를 통하여 개발하였다.

한편, 전자 빔으로 획득한 영상은 윤곽선이 훼손되어 오차를 유발하는데[1], 이를 극복하기 위하여 영상처리 타원 또는 선형의 윤곽선을 검출하는 방법[2]으로 밝기 값에 따른 미분계수 또는 K-means를 이용한 영상분할과 sigmoid function fitting 기법에 따른 알고리즘을 개발하고, 정밀도 및 수행시간을 평가하였다. 제안 알고리즘의 오정렬 값은 같은 패턴을 갖는 10장을 실험하여 평균 0.24nm(3-sigma) 값을 나타내었고, i7-4770k 프로세서에서 OpenMP/SSE 명령어를 사용하여 평균 147ms의 고속 SW로 구현하였다.

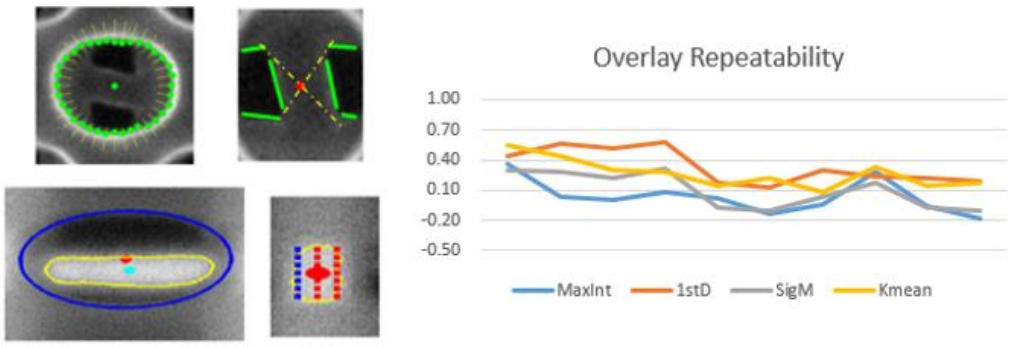

Figure 1. Overlay pattern and measurement result

[1] S. Lee, D. Lee, Y. Lee and S. Oh, Conference on Next Generation Lithography (2014).
[2] N. Chernov, Q. Huang and H. MA, British Journal of Mathematics & Computer Science, 4 (2014).

영상 내 물체 경계에서의 밝기 구배를 이용한 주사전자현미경의 분해능 측정

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영상의 분해능(resolutioin)은 반도체 계측검사에 쓰이는 모든 전자빔 장치의 핵심 사양이다. 분해능(resolution)을 측정하는 일반적인 방법은 영상의 선명도(shparness)를 추산하는 것이고, 이는 미분이나 푸리에 변환 등에 기반한 선명도 함수(sharpness function)를 통해 이뤄진다 [1].

기존 실험에서 우리는 영상 내 물체 경계에서 밝기 변화의 기울기를 이용해 영상의 선명도를 측정했다 [2]. 영상 내 물체 경계에서 밝기의 가파른 정도를 영상의 선명도로 정의하고, 맞춤 영역 크기 제한이 없는 평면 맞춤을 써서, 경계에서의 밝기 구배(gradient)를 구하여, 안정된 측정결과를 얻었다.

본 실험에서는 기존 실험 결과를 바탕으로 프로그램을 개선하였다. 우선 영상 내 물체 경계에서의 밝기 변화를 알기 위해 경계에 수직인 방향에 있는 화소들을 추적할 때 양방향 선형보간 알고리즘(bilinear interpolation algorithm)을 사용했다. 양방향 선형보간 알고리즘은 4-이웃의 값에 근거해 결과값을 계산한다. 또한 평균에서 많이 벗어나는 이상값(outlier)들을 버림으로써 프로그램의 신뢰도를 높였다.

이번 논문에서는 기준영상 및 표준시료 SEM 영상을 바탕으로 실제 FESEM의 분해능을 잰 결과를 발표하고, 아울러 개선된 프로그램의 성능 향상을 확인하고 논의하였다.

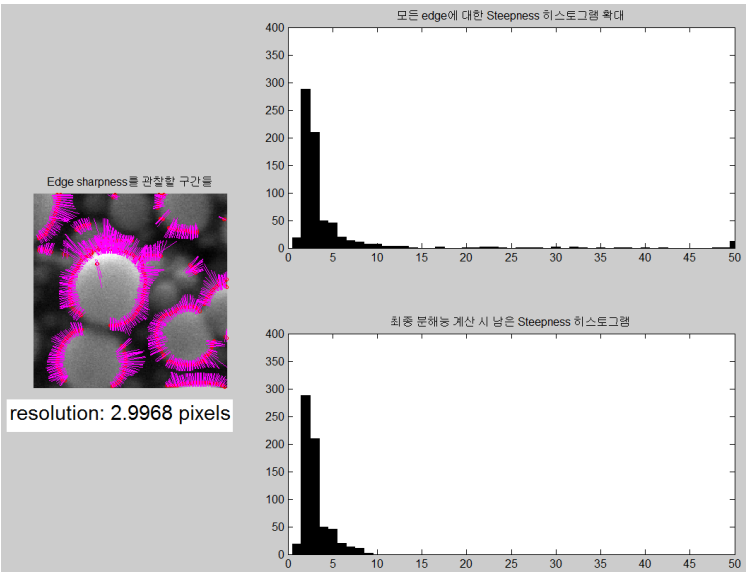

그림 1 (왼쪽) 물체 경계에서의 밝기 변화를 관찰하기 위해 구배 수직 방향으로 화소를 추적한 모습과 최종 계산 분해능 (오른쪽) 밝기 변화 기울기 히스토그램과(위) 그 중 이상값들을 버린 후의 히스토그램(아래)

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Impurity barrier 역할로써의 Barrier metal TiN 의 특성 평가

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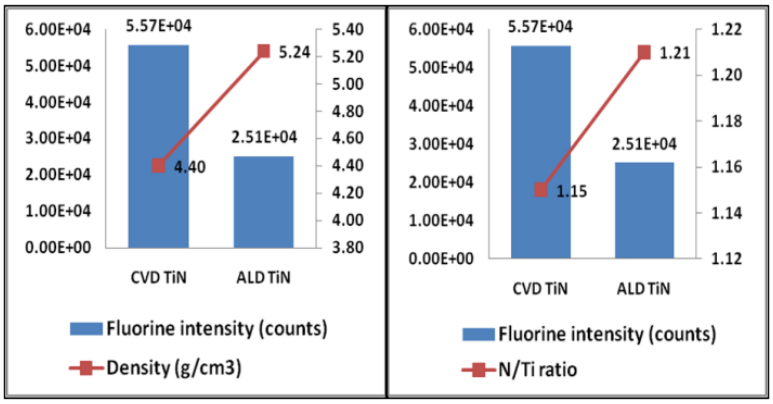
Memory device 의 Gate metal 은 Device shrinkage 에 따라 gas phase 로의 deposition 이 필수적이며 그에 따라 impurity 형성이 진행된다. 예를 들어 Gate metal 에 주로 사용되는 Tungsten 성분은 WF6 gas 로 deposition 되기 때문에[1] Fluorine 이 형성되는 구조이다. Gate module 인 Barrier metal, gate oxide 등의 두께는 지속적으로 얇아지는 추세로 이러한 impurity 의 diffusion 등은 device 에 악영향을 미치게 된다. 따라서 Impurity diffusion 억제를 위한 barrier metal 의 특성[2] 분석은 중요하다. 이 PAPER 에서는 W Gate metal 에 BM 으로써 TiN 을 적용한 특성 분석 결과에 대해 논하고자 한다.

TOF-SIMS, XPS, XRR 의 일련의 분석을 종합한 결과 Barrier metal TiN 은 N/Ti ratio 가 높을 경우, Density 가 높을 경우에 W 에 기인된 Fluorine diffusion 이 억제되는 것을 알 수 있었다. 이와 같은 분석 방법은 W/ TiN Stack 의 Fluorine diffusion 에 국한될 것이 아니라 여러 종류의 Thin film stack 의 Impurity diffusion 특성 확인에 적용될 수 있다.



	CVD TiN	ALD TiN
Fluorine intensity (counts)	5.57E+04	2.51E+04
Density (g/cm3)	4.40	5.24
N/Ti ratio	1.15	1.21

Fig1. Fluorine diffusion 정도와 Density, N/Ti ratio 와의 관계

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Comparison between CMOS and Nano-electromechanical (NEM) Switches

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Recently, a nano-electromechanical (NEM) switch has been investigated widely as a replacement of complementary metal oxide semiconductor (CMOS) switch [1]. One of the reasons NEM switches attract much attention of researchers is zero leakage current due to release operation of a beam. Also, NEM switches have low on-state resistance because they are made of metals whose resistivity values are low. In addition, their fabrication is compatible with standard CMOS fabrication process by using the back-end of line (BEOL) process. Thus, NEM switches are promising as future logic or memory devices [2]. However, most of previous NEM switch research has been focused only on unit cell analysis.

Thus, in this work, NEM switches are compared with CMOS switches in terms of circuit operation. Fig. 1 (a) shows the schematics of each circuit which was fabricated by using 0.18 um CMOS process. The fabricated NEM switch is the three-terminal structure that has the one movable beam and two electrodes. Also, the following two cases are considered for the CMOS switches : pass gates and tri-state buffers. Each switch connects two CMOS inverters and operates as one-to-two multiplexer (MUX). Fig. 1 (b) shows measured input and output signals of each circuit. When the same input signal is applied each circuit, the NEM switch circuit shows the fastest response.

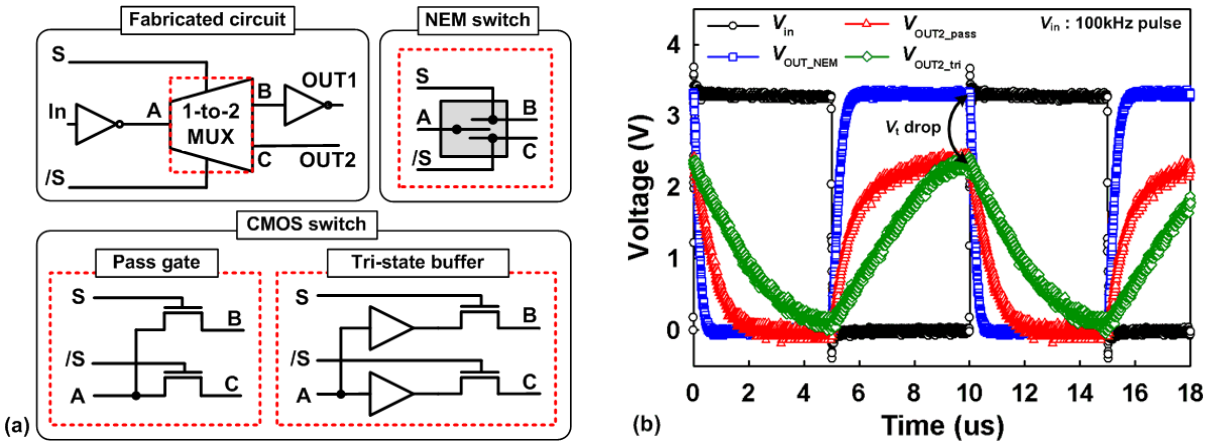

Fig. 1. (a) Schematics of each circuit. (b) Measured input and output signals of each circuit.

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[2] W. Y. Choi, H. Kam, D. Lee, J. Lai, and T.-J. K. Liu, in IEDM (2007).

On-Chip Jitter Tolerance Measurement Technique for CDR Circuits

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We propose an on-chip circuit technique to characterize the jitter tolerance of a binary clock and data recovery (CDR) circuit. The proposed jitter modulation scheme incorporates modulating-charge pump and pulse-generator circuits to apply a periodic triangular voltage directly to the control voltage. The range of the modulated jitter amplitude is 0.05 - 2 UIpp at 10 MHz, and the frequency range is 100 KHz - 20 MHz. The CDR circuit was fabricated in 65 nm CMOS, and the jitter tolerance was successfully measured at 5 Gb/s with a 2^7-1 PRBS pattern. The accuracy is within 23% of the theoretical limit. The whole CDR circuit consumes 29.9 mW at a supply voltage of 1.2 V.

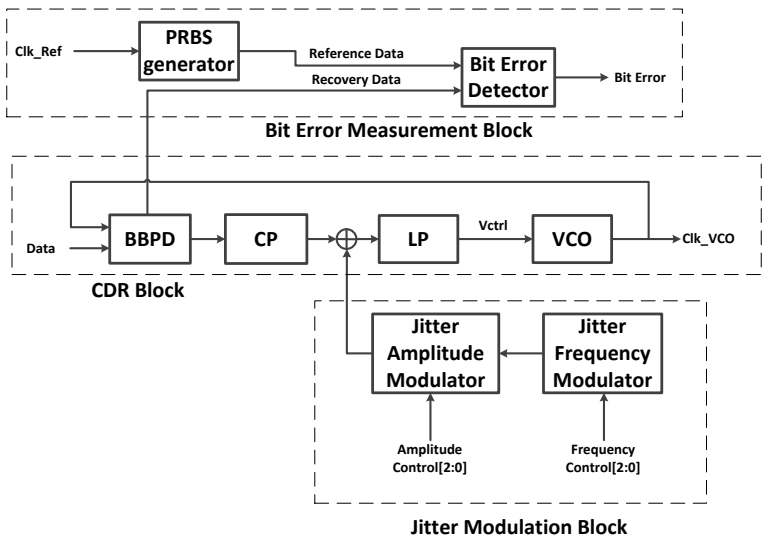

Fig 1. Proposed CDR circuit with on-chip jitter modulation and bit error measurement schemes.

[1] Y. C. Huang, P. Y. Wang, and S. I. Liu, "An All-Digital Jitter Tolerance Measurement Technique for CDR Circuits," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no 3, pp.148-152, March. 2012.

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This work was supported by the IDEC.

A Near-GND Receiver with a Data & Edge DFE

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The proposed receiver employs a 1-tap switched-capacitor decision-feedback equalizer (DFE) instead of a continuous-time linear equalizer to eliminate the need for a level shifting circuit and minimize the static power consumption.

Fig. 1 illustrates the overall architecture of the receiver. The receiver includes a decision feedback equalizer (DFE) that can compensate the both voltage and timing ISI. To equalize the voltage and timing ISI separately, the adder for tap-weight summation is implemented in each data and edge path. To minimize the power overhead of the data and edge DFE, the switched-capacitor adder [1] is used. Since the common-mode level of the receiver circuits can be independently chosen in the switched-capacitor adder, the receiver is fully compatible with near-ground input levels without an extra level conversion circuit. Clock recovery circuit (CDR) is also implemented to demonstrate the edge equalizer performance. Because the DFE adopts the two-way interleaved architecture using half-rate multi-phase clock, it requires four parallel sampling paths: data even, data odd, edge even and edge odd where data even and odd are samples at the eye center and edge even and odd are samples at signal transition points.

Fig. 2 shows a microphotograph and layout of the test-chip. Operating at 6.4 Gb/s, the DFE core circuits consume 1.1 mW from a 1.2 V supply. The BER bathtub in Fig. 2 shows that the timing margin is extended by roughly 2X from 0.24 UI to 0.56 UI where the input swing is 300 mV_{ppd} and the channel loss is -12 dB. Applying the edge DFE, the jitter of the CDR clock reduces from 30.9 ps_{pk2pk} to 24.2 ps_{pk2pk}.

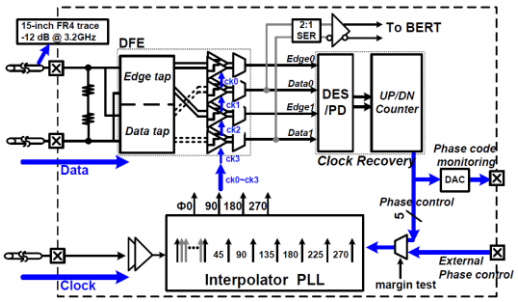

Fig. 1. Overall architecture of the receiver

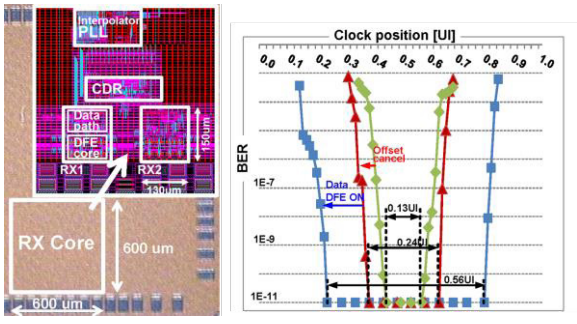

Fig. 2. Microphotograph and measured bathtub of the receiver

[1] A. Neyestanak, et al., "A 6.0-mW 10.0-Gb/s Receiver with Switched-Capacitor Summation DFE," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp. 889-896, Apr. 2007.

Chip fabrication and EDA tools were supported by the IC Design Education Center at KAIST.

A Fast Response Integrated Current-Sensing Circuit for Peak-Current-Mode Buck Regulator

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The PWM current-mode control method has been widely used in implementing fast buck regulators, but it requires high performance current sensors, to rapidly and accurately sense the external inductor current. Among the variety of current sensors, the on-chip current sensing method is suitable for an integrated buck regulator [1]. In this paper, we propose a new on-chip current sensor, which also adopts a sense FET [2].

Fig. 1 shows the circuit diagram of the PWM peak-current mode buck regulator. The PMOS power transistor M_P and the NMOS power transistor M_N are driven by the gate driver, which is controlled by the RS latch. The RS latch is set and reset by the clock signal from the oscillator and the output of the comparator. The current sensor circuit is composed of the Power Stage, the N-Current Sensor, the Duplicator, and the P-Current Sensor. Before the P-Current Sensor starts to sense the inductor current, the bias points at all the nodes in the P-Current Sensor are preset to the ideal bias points for sensing the valley point of the inductor current.

The die size of the entire buck regulator is 1.3×1.0mm^2. However, the proposed current sensor occupies only 300×80 μm^2. Using the deep-n-well of the BCDMOS process, the switching noise effect of the proposed buck regulator was minimized. The sensed voltage shows that the response time under 20ns, and the sensing accuracy of over 90%, with the load current of 200mA

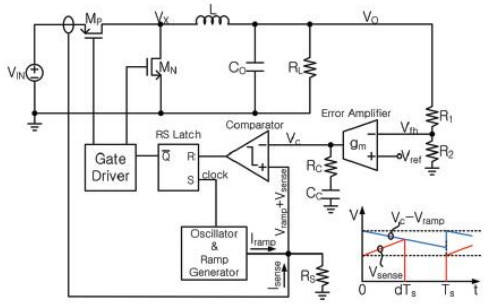

Fig. 1. Circuit diagram of the buck regulator

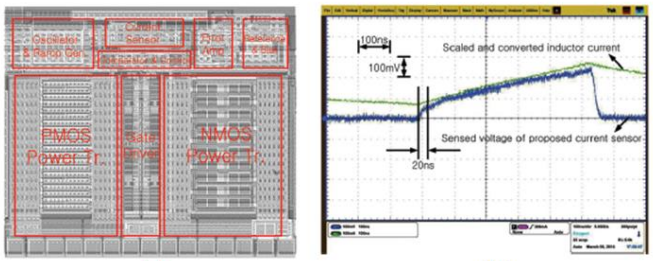

Fig. 2. (a) Micrograph and (b) Measured waveform

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[2] W. H. Ki, "Current sensing technique using MOS transistors scaling with matched bipolar current sources," *U.S. Patent 5,757,174*, May. 26, 1998

Chip fabrication and EDA tools were supported by the IC Design Education Center at KAIST.

A Wideband Differential Low-Noise-Amplifier With IM3 Harmonics and Noise Canceling

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For multi-mode and multi-band operation, the RF receiver should be able to handle wide bandwidth and a wideband LNA is one of the key circuit building blocks of the receiver. The LNA should meet rigorous requirements such as wide bandwidth, wide input matching, sufficient gain, low NF, and high linearity. Especially, the 2nd and 3rd harmonic distortion terms seriously degrade sensitivity in the wideband receiver front-end [1].

This paper presents a wideband 2-stage differential LNA which utilizes the canceling techniques of IM3 harmonic distiortion and noise. The 1st stage adopts a gm-boosted cross-coupled push-pull amplifier to achieve an input matching and reduce the NF. The 2nd stage simultaneously cancels the IM3 and thermal noise of the transistors in the 1st stage. The LNA has a gain of 16~18 dB in a wide bandwidth of 0.1~2.5 GHz, while consuming 13 mW from a 1.2V power supply. The NF is 1.7~2.7 dB and IIP3/IIP2 are -3~0 / 18~21.5 dBm, repectively. The LNA is fabricated in 65-nm digital CMOS technology and the chip area is 0.008 mm^2. This work was supported by the IDEC.

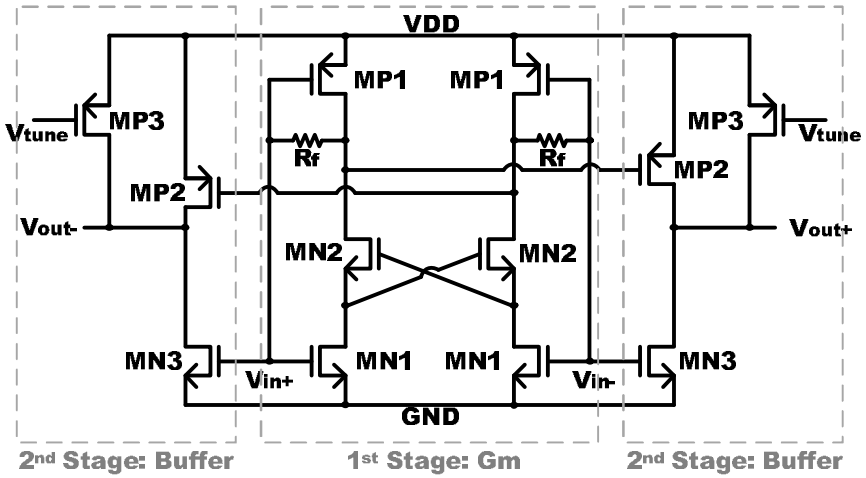

Fig 1. Schematic of the proposed LNA

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CMOS 기반 160 GHz 대역 전압제어발진기

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최근 다양한 정보통신 기술의 발전으로 인하여 초고속 통신에 대한 수요가 늘어나고 있고 이러한 기술 동향을 고려해 보면 미래에는 기존의 주파수 대역이 아닌 100 GHz 이상의 높은 주파수 대역이 새롭게 조명을 받을 것이라고 쉽게 예측할 수 있다 [1,2]. 이러한 주파수에서 동작하는 시스템을 구현하기 위하여 선행되어야 할 것 중 하나는 이 주파수 영역에서 발진하는 신호원을 구현하는 것이다 [3]. 본 연구에서는 삼성 65 nm CMOS 공정을 이용하여 160 GHz 대역 전압제어발진기를 개발하였다. LC 교차결합 구조를 이용하여 구현하였으며 코어에 버랙터를 연결하여 전압에 따른 발진 주파수의 변화가 가능하도록 하였다. 발진기의 원천주파수보다 두 배 높은 주파수 신호를 얻기 위하여 발진기의 차동 출력 신호에 의해 생성된 공통마디에서 출력이 나오도록 하는 푸쉬–푸쉬 (push-push) 방식을 사용하였다. 제작된 전압제어발진기의 동작 주파수의 범위는 152.7 GHz – 165.8 GHz 로 측정되었으며 이때의 출력 전력은 -17.3 dBm 에서 -8.7 dBm 까지의 값을 보였다. 이 회로의 위상잡음 (phase noise)은 10 MHz 오프셋에서 -90.9 dBc/Hz 로 측정되었고, 측정용 패드를 포함한 제작된 칩의 크기는 470 μm × 360 μm 이다.

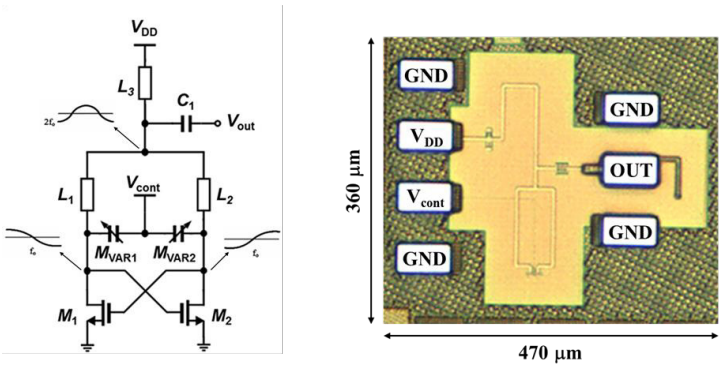

Fig 1. 160 GHz 전압제어발진기 회로도 및 칩 사진.

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A 130 GHz OOK Transmitter with 16 GHz Bandwidth in 65 nm CMOS Technology

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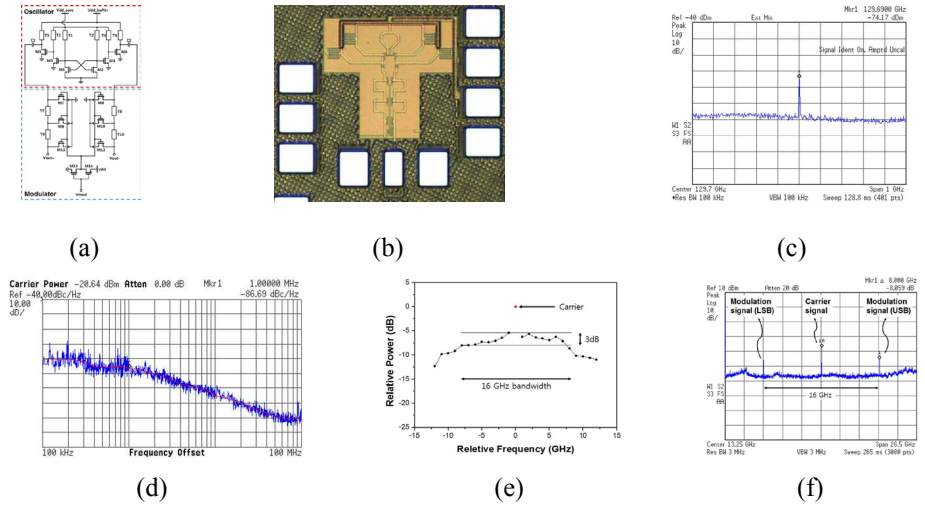
The paper proposes a 130 GHz OOK transmitter in a 65 nm CMOS technology. The system can be used for the D-band transceivers [1, 2]. The transmitter consists of a fundamental LC cross coupled oscillator and a OOK modulator. To reduce the chip area and DC power consumption with maximized output power, two stage tapered structure is used for output buffer rather than conventional power amplifiers (PA). The modulator is designed based on a differential SPST (single-pole-single-throw) switch pair, which exhibits a larger isolation compared to the series type switch [3]. The transmitter operates at 129.7 GHz and the calibrated output was -5.1 dBm. The measured phase noise of the transmitter was -86.7 dBc/Hz at 1 MHz offset. The transmitter shows around 16 GHz 3-dB bandwidth, and the insertion loss and the isolation are 6.4 dB and 28.1 dB, respectively. The chip occupies 560 μm × 450 μm includiong probing pads and consumes 55.2 mW.



(a) (b) (c)

(d) (e) (f)

Fig. 1 (a) Circuit schematic, (b) chip photo, (c) output spectrum, (d) phase noise, (e) output power of the modulated signal relative to the carrier, and (f) example of output spectrum with 8 GHz modulation frequency.

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Design of a PWM Current Mode DC-DC Boost Converter

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본 설계는 Current Mode에서 동작하는 PWM 스위칭 방식인 Boost Converter이다. 공정은 Magnachip 0.35㎛ 2poly/4metal CMOS 공정을 사용하였다. 동작 주파수는 1Mhz로 구동되며, 인덕터, 출력 커패시터, 스위치 MOS 트랜지스터, 피드백저항 등으로 구성되는 Power Stage와 Ramp-Oscillator, Error-amplifier, Comparator, Soft-Start 등으로 구성되는 제어 블록으로 구성되어 있다. 듀티비 0.55일 때 1.5 V 입력 전압 조건에서 출력 전압 3V가 나오도록 설계하였고, Chip Test 결과 원하는 동작을 하는 것을 확인하였다.

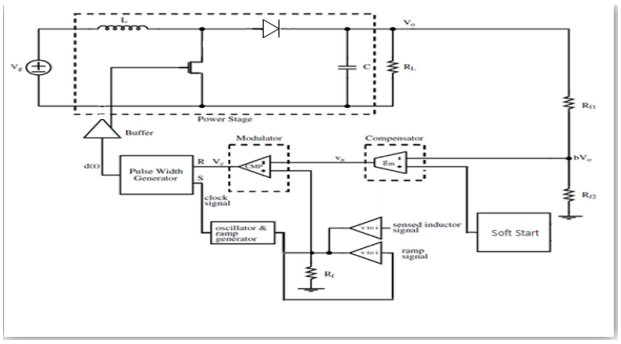

Fig 1. Circuit of PWM boost converter

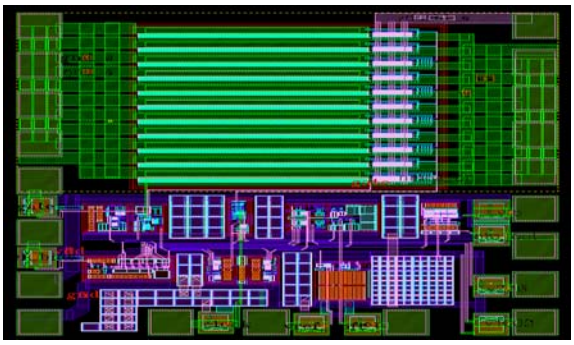

Fig 2. Top Layout

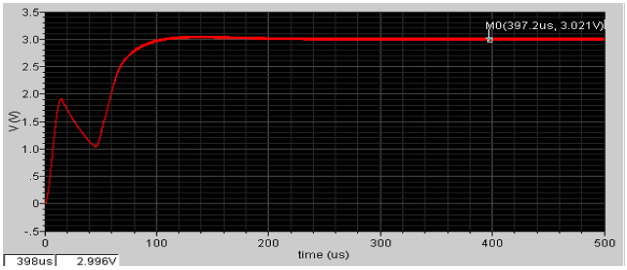

Fig 3. Simulation

Fig 4. Chip Test

[1] Chi Yat Leung et. al., "A 1-V Integrated Current-Mode Boost Converter in Standard 3.3/5V CMOS Technology", IEEE Journal of Solid-State Circuits, vol. 40, No. 11, November 2005.
[2] Robert W. Erickson: *Fundamentals of Power Electronics*, Kluwer Academic Publishers, 1997
[3] Y. Katayama, S. Sugahara, H. Nakazawa, M. Edo,"High-Power-Density MHz-Switching monolithicDC-DC Converter with Thin-Film Inductor", IEEE2000.
Current-Mode Control", IEEE Trans. On Circuits and Systems, Vol. 53, No. 1, Jan 2006.

Verification of CMOS Temperature Sensor using CMOS Cascode and Time-to-Digital Converter

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Recently, the degree of integration of IC increases the heat generated per unit chip area has increased. So, the IC chips must need a temperature sensor to monitor the temperature variation of devices. This paper presents low power, high resolution and high speed, wide sensing range on-chip temperature sensor only using two ring-oscillators which have the cascode CMOS inverter, counters and TDC(Time-to-Digital Converter). The proposed temperature sensor's delay element is composed of the simple CMOS inverter and the cascode CMOS inverter. And the delay variation of cascode CMOS inverter is larger than that of simple CMOS inverter. TDC measures the interval time between two temperature dependent signals. One signal has the temperature-insensitive delay element signal with the constant delay time in temperature ranges and the other signal has temperature-sensitive delay element signal with the sharp delay time variation [1]. The delay sensing scheme of the sensor is composed of the Coarse-Fine TDC, which detects time-delays and converts them into digital-code output [2]. Test board is measured from 30 ^{o}C to 60 ^{o}C. Power consumption is 50uW and sensing speed is 300ksamples/sec at 1.2V operation voltage in operation temperature. Effective resolution was 0.9722 ^{o}C from -20 ^{o}C to 120 ^{o}C and its chip area was only 0.050mm^2.

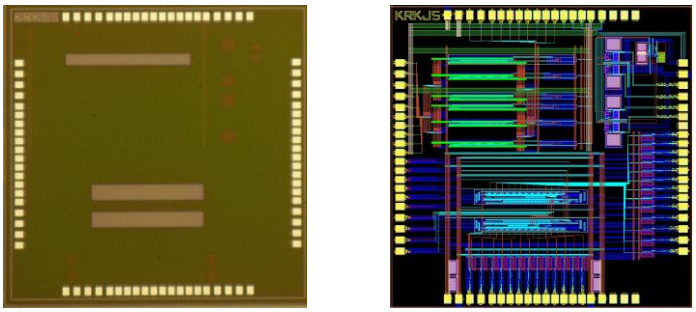

Fig 1. Chip and layout pictures

[1] Chen, Shi-Wen, et al., Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on. IEEE (2010).
[2] Jinse Kim, Seung Woo Hong, Reum Oh, Man Young Sung, proceedings of the KIEEME annual summer conference, Vol. 15, pp. 270 (2014).

This work was supported by the IDEC

mm-Wave 대역에서 전류소스 구조에 따른 VCO의 특성 비교 연구

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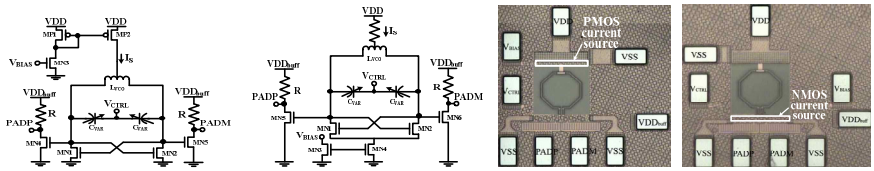
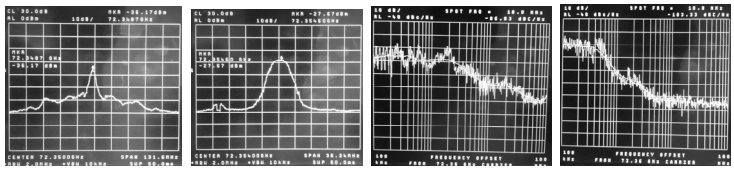
밀리미터 웨이브 대역의 클락 생성에 주로 전압 제어 발진기 (VCO)를 사용한다 [1]. 본 논문에서는 70GHz 대역에서 동작하는 2가지 구조의 VCO를 비교 연구 하였다. 설계한 VCO의 회로도는 그림 1과 같다. 제안하는 VCO의 코아 부분은 LC형 차동 NMOS 구조에 튜닝범위를 넓혀주기 위한 베렉터를 추가한 구조이다. 바이어스와 위상잡음 특성 개선을 위해 그림 1.(a)에서 PMOS 전류 미러를 추가했고, 그림 1.(b)에서 저항과 NMOS 전류소스를 전류원으로 사용했다. L_{VCO}와 C_{VAR}는 같은 크기를 사용하였으며 출력버퍼의 크기 또한 동일하다. 설계한 VCO는 65㎚ CMOS 공정을 사용하여 제작하였고, 그림 1.(c)와 그림 1.(d)는 제작한 VCO의 칩 사진이다.

칩 측정은 프로브 스테이션을 사용하여 웨이퍼에서 프로빙하였고, 측정결과는 그림 2와 같다. 측정환경에 대한 손실을 보상한 결과 PMOS 구조는 71.75~74.78㎓의 동작주파수에서 −17.87dBm의 출력이 측정됐다. NMOS 구조는 PMOS 구조에 비해 동작주파수가 약 1.3GHz 정도 낮은 70.42~73.36㎓에서 측정되었고 이때의 출력전력 −9.37dBm 이다. 10MHz 오프셋 주파수에서의 위상잡음과 소모전력은 PMOS구조는 −86.8dBc/Hz, 12mW이고 NMOS 구조는 −91.1dBc/Hz, 10.8mW이다. 측정결과 NMOS 구조가 PMOS 구조에 비해 저전력, 고출력 그리고 낮은 위상잡음 특성을 갖는다는 것을 확인했다. 설계한 2가지 구조의 VCO는 밀리미터 웨이브 대역에서의 위상잡음 특성향상과 저전력 회로연구를 위해 사용할 수 있다. 본 연구는 IDEC의 지원을 받았다.



(a) (b) (c) (d)

그림 1. (a)PMOS구조 회로도 (b)NMOS구조 회로도 (c)PMOS구조 칩사진 (d)NMOS구조칩사진



(a) (b) (c) (d)

그림 2. (a)PMOS구조 출력전력 (b)NMOS구조 출력전력 (c)PMOS구조 위상잡음 (d)NMOS구조 위상잡음

[1] F.Shirinfar et al., “A multichannel, multicore mm-Wave clustered VCO with phase noise, tuning range, and lifetime reliability enhancements,” IEEE, RFIC, pp. 235-238, Jun. 2013.
[2] HongMo Wang, “A 50GHz VCO in 0.25μm CMOS,” IEEE, ISSCC, pp. 372-373, Feb. 2001.

본 연구는 산업통상자원부 및 한국산업기술평가관리원의 산업원천기술개발사업(정보통신)의 일환으로 수행하였음. [10044092 , 7Gbps급 무선멀티미디어 통신서비스 제공을 위한 60GHz대역 무선LAN/PAN용 OFDM 기반 PHY 및 RF 트랜시버 핵심 IP 기술 개발]

Design of hysteretic buck converter with a low output ripple voltage and fixed switching frequency in CCM

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This paper presents hysteretic buck converter which is appropeiate for mobile application such as supply of power on AP. Designed converter generates 1.2V output voltage with 3.7V input voltage. PMIC for mobile must have low output ripple voltage and fast transient response because the load stages are designed in low voltage and low power condition. The proposed hysteretic buck converter is composed of ramp generator, delay time control circuit with PLL(Phase Locked Loop) structure and DCM(Discontinuous Conduction Mode)/CCM(Continuous Conduction Mode) selection circuit. The ramp generator makes a switching frequency of the converter be fast. Fast switching frequency allows the converter to operate in low output ripple voltage condition and to use a low inductor.[] The delay time control circuit improves EMI(Electro Magnetic Interference) shielding characteristic by fixing the switching frequency in CCM.[] The DCM/CCM selection circuit makes the converter operate in DCM with a switching frequency of lower than 2MHz to increase an efficiency of delivery power by decreasing a switching loss.

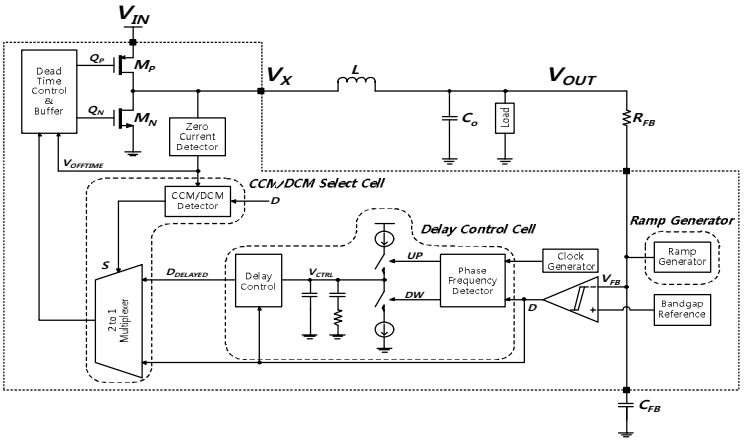

Fig 1. Proposed hysteretic buck converter block diagram

[1] R. Miftakhutdinov-TI Unitrode, "An Analytical Comparison of Alternative Control Techniques for Powering Next-Generation Microprocessors", Power Supply Design Seminar, (2001).
[2] C. Tso and J. Wu, "A Ripple Control Buck Regulator with Fixed Output Frequency", IEEE Power Electronics Letters, Vol.1 No.3 pp61, (2003).

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Design of SIMO Buck Converter with minimized Channel regulation and output voltage ripple for Mobile Devices

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Most important factor of PMIC(Power management IC) chip in Mobile devices is operating well in variety environment. And in mobile devices, minimize area of chip and external components is indispensable. Because of this reason, recently SIMO(Single Inductor Multiple Outputs) converter is well-known. SIMO converter use only one inductor to operatates many outputs, so it can reduce number and area of inductors. This factor improve efficiency of area density. But SIMO structure has some disadvatages to operate DC-DC converter. At first, each outputs influence each other. [1] And changing environment of output increase ripple of output voltage[2]. For solve these problems, this paper propose that SIMO Buck Converter which minimize ripple of output voltages and influence each outpus for Mobile devices. Proposed circuit can change reference voltage which controls maximum inductor current level to reduce ripple of output voltage using 4-bits comparators and reference voltage controller. And minimize influence of each outputs using 2_Phase_Selector circuit in Fig 1.

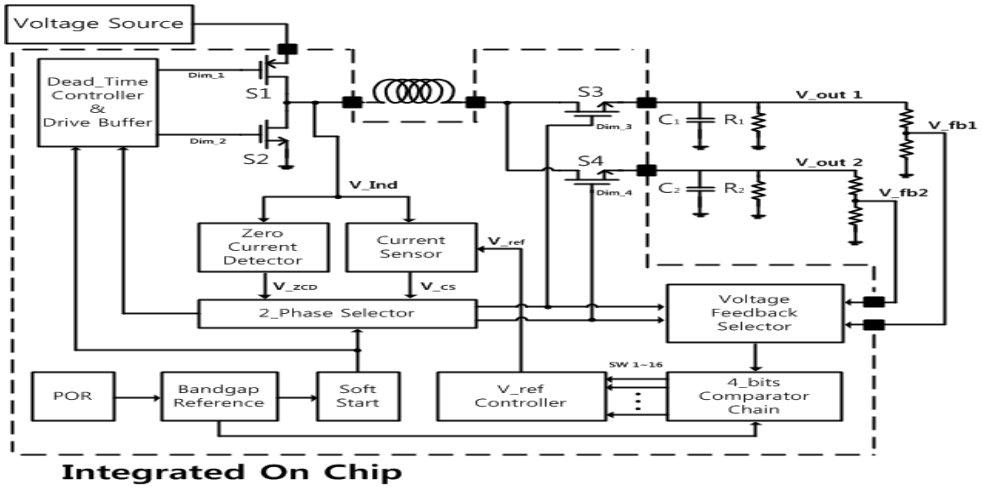

Fig 1. The layout of the proposed SIMO Buck Converter

This work was supported by the IDEC.

[1] Pradipta Patra “Control Scheme for Reduced Cross_Regulatiob in single inductor multiple output dc-dc Converters” IEEE transactions on inductrial electronics, Vol.60. No 11. Page 5095 ~ 5105, Novemver, 2013.
[2] Wei Xu “A single inductor dual-output switching converter with low ripples and improved cross regulation” Custom Integrated circuits Conference, IEEE, Page 303 ~ 306 , 2009

Design of a Low Power CMOS 10bit Flash-SAR ADC

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The block diagram of the proposed 10 bit Flash-SAR ADC is shown in Fig. 1. It is composed of Flash ADC for MSB 2 bits and SAR ADC for LSB 8 bits. SAR ADC consists of a capacitor DAC(C-DAC) with a split capacitor, a switch control logic circuit, and a 10 bit output register.

Fig. 1 shows the block diagram of two stage flash ADC. The proposed flash ADC consists of a low power sample and hold circuit, two bit flash reference voltage ladder, 1st and 2nd stage of comparator array, a 3 to 2 digital encoder, and a 10 bit output register. The output of the two bit flash ADC becomes the input of switch control logic circuit and initiates the data conversion. There are two comparators used in the flash ADC. Therefore, compared to the conventional two bit flash ADC, the two stage 2bit flash ADC can reduce 33% of power consumption because the proposed one only drives two comparators. The flash ADC is followed by an error correction circuit and 3 to 2 encoder. Error correction circuit corrects the digital error and the output of the error correction circuit is applied to the input of 3 to 2 encoder

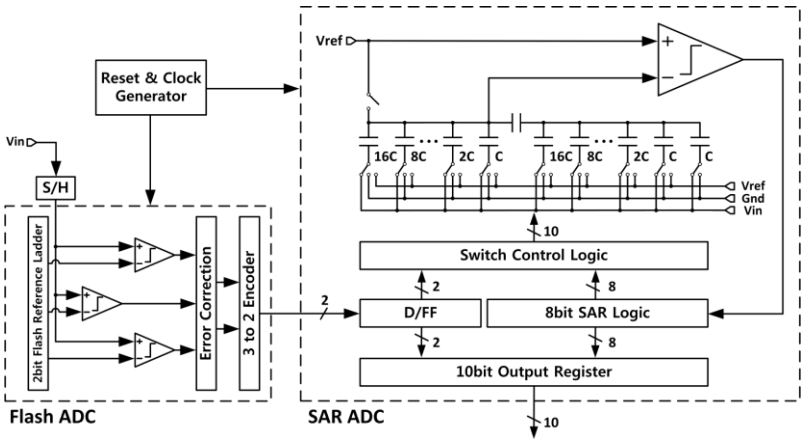

Fig 1. The layout of the proposed 10bit SAR ADC

[1]J. Um, Y.Kim, E.Song, J. Sim, "A Digital- Domain Calibration of Split-Capacitor DAC for a Differential SAR ADC Without Additional Analog Circuits" IEEE trans. on Circuit and System I Vol. 60, issue. 11, pp. 2845-2856, Nov 2013.

[2] D. Shi, S. Lee, and K. Yoon, “A 6-bit 500MS/s CMOS A/D Converter with a digital input range detection circuit”, The Journal of Korean Information and Communications Society, Vol. 38, no. 4, pp. 303-309, July 2013

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A low noise touch sensor with loop embedded resonator

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Capacitive sensor or an inductive sensor is widely used in various applications. A relatively high frequency periodic signal is used in the capacitive sensor and the inductive sensor by a sensor device to sense the change of a physical quantity. This is only the relatively high frequency of the signal applied, via a coupling of the developer in the sensing device, since it can obtain an output signal having a relatively large value. However, the noise component induced in the sensing device is shown in the output signal of the sensor circuit, greatly increasing the amplitude of the drive signal should be input to the sensor device in order to obtain a sufficient signal-to-noise ratio (SNR) [1].

The present invention is about a method for the sensor circuit to obtain a sufficient signal-to-noise ratio (SNR) in a capacitive sensor, or an inductive sensor circuit using the periodic for the relatively high frequency signal even though the sensor uses a relatively small amplitude input signals.

A low noise touch sensor with loop embedded resonator is designed in 65nm CMOS technology. Fig. 3 shows the low noise output of the second receiver. Blue line is non-touched panel lines output and yellow line shows the output of touched line.

This work was supported by the IDEC.

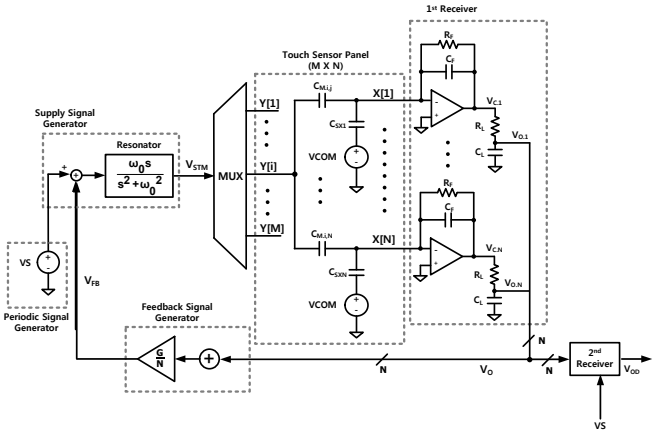

Fig. 1. Proposed touch sensor system.

[1] Jae-seung Lee, et al., “A 10-Touch Capacitive-Touch Sensor Circuit with the Time-Domain Input-Node Isolation,” in SID Symp. Dig. Tech. Papers, Jun. 2012.

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Baud-rate ADC-based Blind Sampling CDR

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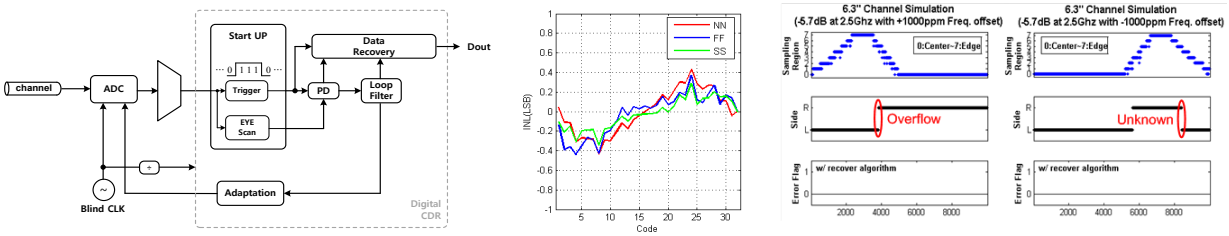
Since the reliable data restoration is the primary concern in the blind-sampling structure, the sampling rate is higher than the data rate. Typically oversampling ratio more than 3 times is used. If it is possible to reduce the oversampling ratio, data rate can be increased using the same sampling techniques. Reportedly, the sampling rate of the blind sampling can be reduced down to the baud-rate thanks to analog-to-digital converter (ADC) and digital loop filter [1].

Fig. 1 shows the architecture of the baud-rate blind CDR with high resolution ADC used in this study. It consists of five blocks - start up, phase detector (PD), loop filter, adaptation and data recovery. The ADC samples the amplitude information in discrete time interval. This 5-bit digital information is, then, sent to the PD where the sampling phase is analyzed by digital signal processing. The variation of data stream of ADC outputs is converted as the sampling offset (Δt) which is the difference between the sampling clock and the center of the data duration. Subsequently, the previous recovered data(Pre bit) and the following recovered data(Post bit) make it possible to determine which side of the eye the present data is sampled (Δs). Loop filter is the key element to extract the exact information (Δs, Δt) using the integral and differential components in it. Then, the transition of the sampling offset implies the frequency offset.

As shown in Fig. 1(b), 5bit flash ADC can convert input signal to digital code within 0.5LSB. Also, digital CDR can detect the overflow or underflow when the sampling side is changing from left to right or from right to left, respectively like Fig. 1(c). To accommodate this capability, the FIFO depth is adjusted in digital CDR block.



(a) (b) (c)

Fig 1. (a) Block diagram of proposed digital CDR, (b) INL simulation result of 5bit flash ADC, and (c) CppSim simulation results of data recovery under frequency offset

[1] C. Ting, J. Liang, A. Sheikholeslami, M. Kibune, H. Tamura, "A Blind Baud-Rate ADC-Based CDR," IEEE J. Solid-State Circuits, vol. 48, no. 12, pp. 3285- 3295, Dec. 2013.

Chip fabrication and EDA tools were supported by the IC Design Education Center at KAIST.

섬유전선을 위한 송수신기 설계

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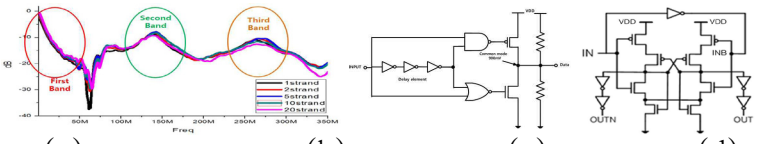
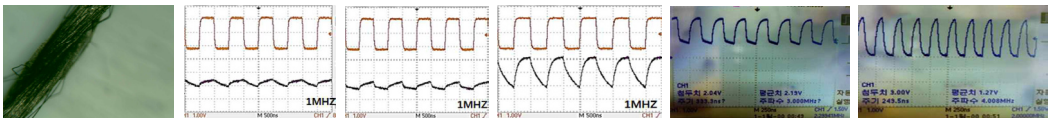
웨어러블 컴퓨팅은 물리, 의류, 전자, 기계 등의 여러 분야와 서로 긴밀하게 협동하여 연구해야만 가능하기 때문에 일반 구리선, 동축선, 광섬유가 아닌 섬유전선 기반에서의 데이터 송신을 위한 송수신기가 필요하다[1]. 섬유전선 통신에서 주파수에 따른 전력손실이 다르며, 주파수와 전선의 가닥수를 변경해가며 측정한 결과를 그림 1.(a)에 나타냈다. 측정결과 10MHz 이하인 첫 번째 대역에서의 손실이 가장작다. 본 논문에서는 3가지 대역에서 동작하는 것은 물론, 첫 번째 대역에서의 고효율 특성을 가지는 송수신기를 설계했다. 설계한 송신기는 입력 데이터의 상승엣지와 하강엣지를 검출하여 삼각파로 전송하며, 수신기는 한 개의 입력 신호로 내부에서 반전된 신호를 생성한 후 두 신호의 차이를 이용해 입력신호로 복원한다[2]. 그림 1.(b)와 (c)에 회로도를 나타냈다.

설계한 섬유전선용 송수신기는 0.18um CMOS 공정으로 제작 후 패키징하여 오실로스코프, 함수발생기, 전원공급기를 이용하여 측정했다. 2개의 섬유전선을 통해 2개의 송신기 출력과 2개의 수신기의 입력을 연결하는 차동신호 구조로 측정하였으며 그림 2.(a)~(d)에 사용한 섬유전선과 입력신호 주파수가 1MHz 일때의 결과를 나타냈다. 그림 2.(e)와 (f)는 입력 주파수를 3MHz와 4MHz로 변경하여 측정한 결과이다. 측정결과 제안하는 송수신기를 사용하면 전력손실이 거의 없이 데이터 통신이 가능하다는 것을 확인했다. 설계한 송수신기는 직물형 오디오 시스템 및 MP3 재킷과 같은 섬유전선을 이용한 웨어러블 컴퓨팅 분야에 사용할 수 있다. 본 연구는 본 논문(저서)은 산업통상자원부 기술료사업으로 지원된 연구임 (NO.10048747)



(a) (b) (c) (d)

그림 1. (a)주파수별 데이터 손실그래프 (b)엣지검출송신기 회로도 (c)수신기 회로도



(a) (b) (c) (d) (e) (f)

그림 2. (a)스테인레스 방적사 섬유전선 (b)송신기출력(1MHz) (c)수신기입력(1MHz) (d)수신기출력(1MHz) (e)수신기출력(3MHz) (f)수신기출력(6MHz)

[1] Hoi-Jun Yoo and Namjun Cho, "Body Channel Communication for Low Energy BSN/BAN," IEEE Asia Pacific Conference on Circuits and Systems, 2008.
[2] Thaddeus J. Gabara, "Basic Transmitter and receiver system," IEEE JOURNAL OF SOLID-STATE CIRCUITS, Jun. 1988.

A TDC-Less Fractional-N ADPLL Highly Synthesized with Digital Standard Cell Library

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Replacement of analog blocks with digital counterparts has been a major trend of circuit design to attain full advantages of scaled technology in area, speed, power, testability, and programmability without suffering from worsening process variations [1]. This paper presents a TDC-less approach in fractional-N ADPLL. For an effective improvement of resolution in frequency error representation, a fully synthesizable noise shaping 1st order 1b DSM to suppress large quantization noise is proposed. Without any fractional TDC-like block, both the in-band and out-of-band phase noise is suppressed (Fig. 1). All circuit blocks are implemented with automated synthesis using standard cell library excluding DCO part only. The proposed ADPLL is implemented in 65nm CMOS. With a 64MHz reference, PLL consumes 3.9mW from a 1.0V supply at DCO frequency of 2.248 GHz. Active area is 0.133 mm^2.

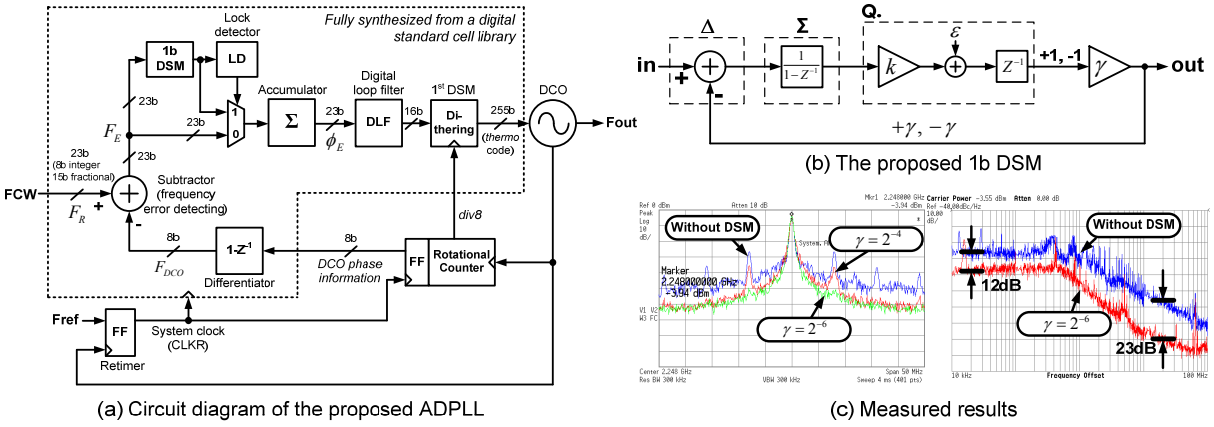

Fig 1. Circuit diagram and measured results

[1] Y. Park, et al., "An all-digital PLL synthesized from a digital standard cell library in 65nm CMOS," IEEE Custom Integrated Circuits Conf., pp. 1-4, 2011.
[2] N. August, et al., "A TDC-Less ADPLL with 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS," Int. Solid-State Circuits Conf., pp. 246-247, 2012.

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보조 B 급 코어와 자동조정 바이어스 회로를 이용한 2.6 GHz C 급 전압 제어 발진기 설계

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C 급 VCO 는 기존의 B 급 VCO 들에 비해 동일한 출력 전력 대비 낮은 위상 잡음 특성을 제공하기 때문에 널리 이용되고있다 [1]. 본 논문에서는 2.6-GHz 에서 자동조정 바이어스 회로 (adaptive bias circuit)와 보조 B 급 cross-coupled 코어를 이용하여 안정적인 스타트업을 구현한 C 급 VCO 회로 설계에 대해 다루고 있다. 그러나 C 급 VCO 는 낮은 게이트 DC 전압으로 인한 필연적인 스타트업 문제를 갖고 있어 회로의 안전성이 떨어진다고 알려져 있다. 그림 1(a)는 제안된 C 급 VCO 의 회로도이다. 보조 B 급 코어는 DC 전력을 더 사용하지만 C 급 VCO 의 부족한 음저항을 보충하여 안정적이고 빠른 발진을 도모한다. 그림 1(b)는 자동조정 바이어스 회로의 회로도이다. 그림 2 는 스타트업을 확인하기 위한 트랜지언트 시뮬레이션 결과이다. 그림 2 에서 (a)는 보조 B 급 코어와 자동조정 바이어스 회로가 같이 사용된 경우이고, (b)는 보조 B 급 코어만 사용된 경우, (c)는 자동조정 바이어스 회로만 사용된 경우, (d)는 스타트업 개선 기술이 사용되지 않은 C 급 VCO 의 경우이다. 제안된 VCO 의 경우인 (a)가 가장 빠른 발진 스타트업을 갖는 것을 확인할 수 있다. 제안된 회로의 시뮬레이션 결과는 다음과 같다. 주파수 조정 범위는 2.4~2.65 GHz (3coarse) 이고, 1MHz 오프셋 주파수에서 -135 dBc/Hz 의 위상 잡음 특성을 가지며, DC 전력 소모는 3.48 mW 이다.

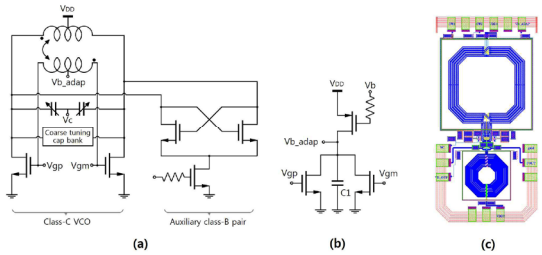

그림 1. (a) 제안된 C 급 VCO 회로. (b) 자동조정 바이어스 회로. (c) 레이아웃

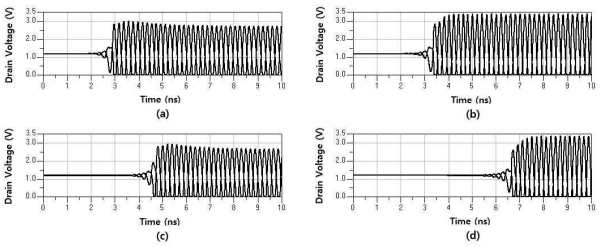

그림 2. 각 경우의 트랜지언트 시뮬레이션 스타트업 비교

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[1] A. Mazzanti and P. Andreani, , “Class-C harmonic CMOS VCOs, with a general result on phase noise,” IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

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3~10GHz UWB Frequency Synthesizer for MB-OFDM

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Recently, frequency of mobile or wireless communication is over than 10GHz and bandwidth of it is over than 1GHz. So using conventional VCO and PLL circuit is difficult to design frequency synthesizer. MB-OFDM or future RF circuits have frequency of over 10GHz and bandwidth of over 5GHz, it is difficult to design frequency synthesizer using conventional VCO and PLL circuits.[1] This article describes design of RF frequency synthesizer with 0.11 ㎛ silicon CMOS technology being used as an application of the MB-OFDM UWB system. To generate effective MB-OFDM clock signal a novel technique which different multiplying and dividing factors according to bands like 1~3 band is four times, 4-6 band is three times, 7~12 band is two times to reduce the tuning range of VCO It can reduce tuning range of VCO to 13,200~20,592MHz. It has been about 56.2% less oscillation bandwidth compared to the conventional VCO oscillation bandwidth of 6,864~20,592MHz. In order to achieve the new algorithm PMOS core structure of VCO used for excellent noise and bandwidth characteristics.[2] Especially to get good performance of speed, power consumption, and wide tuning range, PMOS core structure of VCO and widely tunable varactor has been used in design of the PLL.

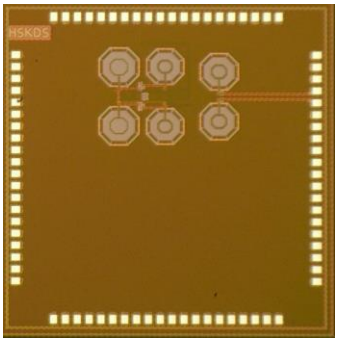

Fig 1. Fabricated Chip Photograph

※ This work was supported by the IDEC

[1] Donshik Kim, Sanghoon Chai, Journal of The Institute of Electronics Engineers of Korea, Vol. 50, No. 2, pp.134-139, February (2013)
[2] Taewon Ahn, Youn Moon, Journal of The Institute of Electronics Engineers of Korea, SD, Vol.42, NO. 6, pp.59-66, (2005)

A Low Power Spread Spectrum Driving Signal Mutaul-Capacitance Touch Sensor

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A mutual-capacitance touch sensor widely used on smart devices. However, the touch sensor suffers from display and human noise. A LCD panel has a VCOM plane or grid, which has capacitive-coupled noise from the gate driver pulse and the source driver image signals. These signals generates the display noise to the touch sensor. Also human fingers on a touch screen panel (TSP) works as an antenna. This brings random noise to a touch sensor. In this work, the frequency of VSTM is chosen to avoid the high display noise band [1] as well as a spread spectrum stimulating driving scheme is applied to suppress the effect of the human noise. In the proposed scheme, multiple frequency among the dip of the display noise are selected for the touch sensor driving signal (Fig. 1). The scheme avoid the display noise naturally. Also, even if random noise is asserted on a touch sensor by human finger on any driving signal frequency (fSTM1), other unharmed signals on different frequency (fSTM2, fSTM3,••• fSTM_N) can keep the sustainable touch sensor operation. The receiver is designed as a fully-differential structure which consists of a charge amp, a chopper, a low-pass filter, and an integrator.

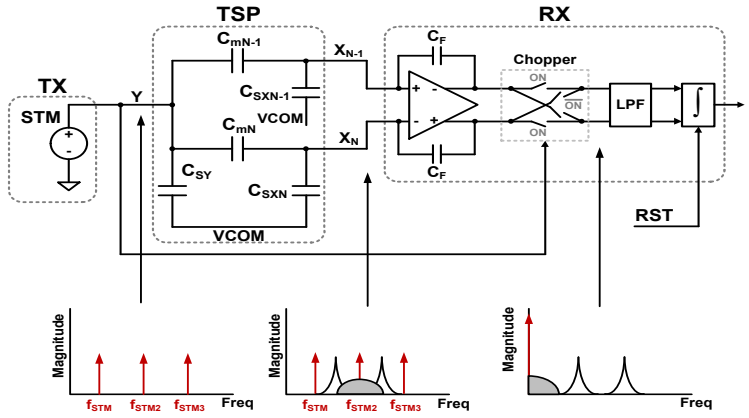

Fig 1. The receiver of the designed touch sensor

[1] J-S Lee, D-H Yeo, S-S Lee, H-J Kwon, J-Y Sim, B-S Kim, and H-J Park "A 0.4 Driving Multi-Touch Capacitive Sensor with the Driving Signal Frequency set to (n+0.5) Times the Inverse of the LCD VCOM Noise Period", IEEE International Symposium on Circuits and Systems, June, 2014

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SiGe 공정을 이용한 134 GHz 신호원

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100 GHz 이상의 주파수는 비단 무선 통신 분야뿐만이 아니라 이미징, 분광학, 생화학 등 다양한 응용 분야에서 연구 및 개발이 활발하게 진행되고 있다. 이 대역은 작은 부피로 집적이 용이하고 적은 비용으로도 시스템을 구현할 수 있다는 장점을 가지고 있다 [1]. 따라서 높은 주파수를 이용한 응용을 구현하기 위해서는 이 대역에서 높은 출력 전력을 갖는 신호원의 개발이 필수적이다 [2]. 본 논문은 TowerJazz 0.18 μm SiGe BiCMOS 공정을 이용하여 67 GHz 발진기, 67 GHz 증폭기, 그리고 134 GHz 주파수 체배기로 구성된 134 GHz 신호원을 개발하였다. 그림 1 에 본 연구에서 개발한 134 GHz 신호원의 회로도와 칩 사진을 각각 나타내었다. 발진기에서 발생한 신호가 증폭기를 거쳐 주파수 체배기에 의해 원천 주파수의 두 배가 출력으로 전달된다. 발진기는 우수한 위상잡음을 갖는 콜피츠 구조로 설계하였으며 [3], 증폭기는 이득을 높이기 위해 캐스코드 증폭기로 설계하였다. 증폭된 차동 신호는 주파수 체배기의 비선형성에 의해 두 번째 고조파 성분이 보강되어 단일 출력으로 신호를 내보낸다. 스펙트럼은 외부 혼합기를 사용하여 측정하였으며 그 결과 133.2 GHz 에서 동작하는 것을 확인하였다. 또한 이 때의 위상 잡음은 10 MHz 오프셋에서 −107 dBc/Hz 를 보였다.

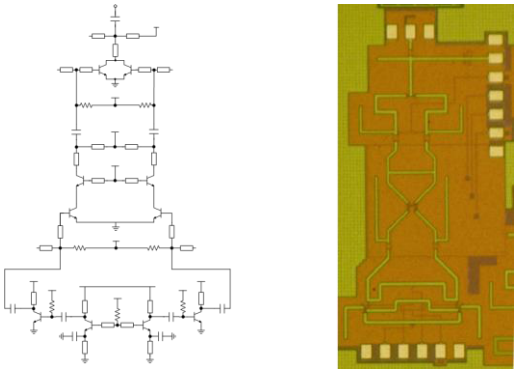

Fig 1. 134 GHz 신호원 회로도 및 칩 사진.

[1] Namhyung Kim *et al*, *IEICE Transactions on Electronics*, vol. E97-C, No. 5, pp. 444-447, 2014.
[2] D. Notel *et al*, in *Proc. Infrared Millimeter Waves Conf.*, 2007, pp. 269–270.
[3] P. Andreani *et al*, *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

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저전압 열에너지 하베스팅을 위한 DC-DC 부스트 변환기

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에너지 하베스팅은 빛, 진동, 열 등 주변의 버려진 에너지를 전기에너지로 변환하여 사용하는 기술이다[1]. 이 중 열에너지 하베스팅은 온도 1℃ 당 수십 mV (@10cm^2) [2]의 매우 작은 전압을 출력하기 때문에 회로를 구동하기 어렵다. 기존 연구[3]에서는 기계적인 스위치를 사용하여 움직임에 의해 스위치를 동작시켜 회로를 시동하는 방법을 사용하였다.

그림 1 은 본 논문에서 제안하는 DC-DC 부스트 변환기의 전체 블록 다이어그램이다. Start-up 블록은 200mV 의 입력 전압으로 승압된 펄스 전압인 V_{PG} 를 출력하여 반복적으로 M_{NS} 를 on/off 시켜 V_{DD} 를 1.2V 까지 승압시킨다. Voltage detector 는 승압된 V_{DD} 를 감지하여 start-up 을 끄고 REF&CLK generator, 비교기(CMP)를 구동시키기 위한 신호 'VD' 를 출력한다. CMP 는 V_{DD} 레벨을 감지하여, V_{DD} 가 2V 보다 작을 경우 CHG_V_{DD} 가 출력되어 V_{DD} 를 2V 까지 승압시키고, 2V 보다 클 경우 CHG_V_{OUT} 이 출력되어 V_{OUT} 을 2.8V 까지 승압시킨다. 또한 RCD 를 사용하여 인덕터에 역전류가 흐르는 것을 방지한다.

그림 2 의 (a)는 CHG_V_{DD} 와 V_{DD} 의 측정결과로써 V_{DD} 값은 CHG_V_{DD} 에 의해 약 2V 로 유지되는 것을 확인 할 수 있다. 그림 2 의 (b)는 CHG_V_{OUT} 과 V_{OUT} 의 측정결과이다. CHG_V_{OUT} 에 의해 V_{OUT} 은 약 3.2V 까지 상승되는 것을 확인 할 수 있다.

본 논문에서는 저전압 열에너지 하베스팅을 위한 DC-DC 부스트 변환기를 0.35um CMOS 공정을 이용하여 설계하였다. 설계된 회로는 외부소자를 사용하지 않고 집적화하여 설계하여 전압을 얻을 수 있으므로 다양한 응용회로에 활용 될 수 있다.

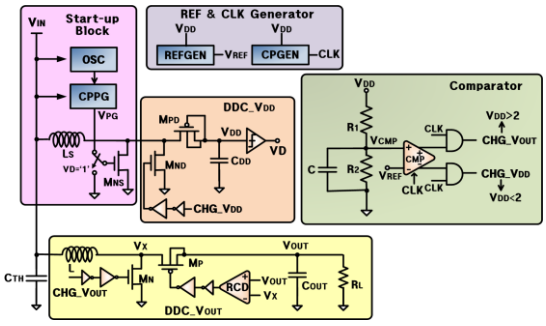

Fig. 1 DC-DC 부스트 변환기 블록 다이어그램

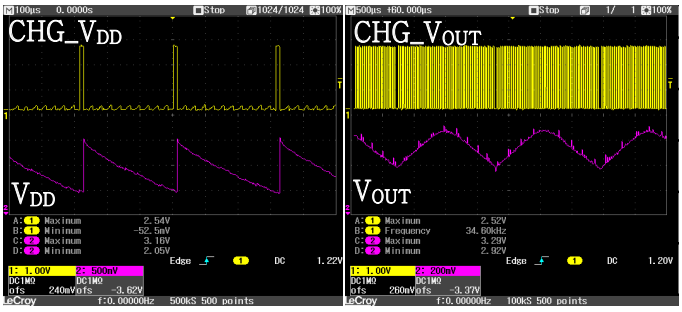

Fig. 2 (a) CHG_V_{DD} 와 V_{DD} (b) CHG_V_{OUT} 과 V_{OUT}

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[1] D. Dondi, et. al., "Modeling and Optimization of a Solar Energy Harvester System for Self-Powered Wireless Sensor Networks", IEEE Trans. on Industrial Electronics, vol. 55, no. 7, pp. 2759-2766, 2008.
[2 Tellurex Thermoelectric Energy Harvester-G1-1.0-127-1.27, Available: http://www.tellurex.com
[3] Y. K. Ramadass and A. P. Chandrakasan, "A Battery-Less Thermoelectric Energy Harvesting Interface Circuit With 35 mV Startup Voltage", IEEE JSSC, vol. 46, no. 1, pp.333-341, 2011.

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Design and Implementation of CMOS ADC for Radiation Detector Applications

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The excessive radiation can seriously damage not only the human body but also the electronic devices, leadind to the fatal and irreversible function of electronic systems. Therefore, the development of radiation detection system have been required to generate shut down signal before all the electronics system damaged [1]. In this paper, we present the design and implementation of CMOS analog-digital converter (ADC) circuit for radiation detection applications. Figure 1 shows the block diagram of the CMOS ADC circuit, which is consists of two parts: the two latches and the comparator block. The functions of two latches are to generate a system shut-down signal and a system re-operation signal. The time delay between the shut-down signal and the re-operation signal can be controlled by the 13-bit comparator. The CMOS ADC circuit was designed by Cadence design tool and fabricated by the Hynix Magnachip 0.35 μm CMOS technology. Figure 2 shows the signal response of the CMOS ADC circuit. When the nuclear event comparator output (NECO) was applied, the maximum output signals of the nuclear event output (NO) and the nuclear event flag (NF) was generated in 3 μs through SR latches. The NO turned to reset state after 75 μs owing to a fixed “1001” reference counter signal. On the other hand, the set state of the NF was maintained until the the nuclear event flag reset (NFR) signal generated, as shown in the figure. We confirmed proper operation of the system as we expected.

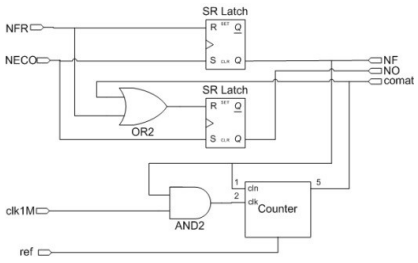

Figure 1 Block diagram of the system

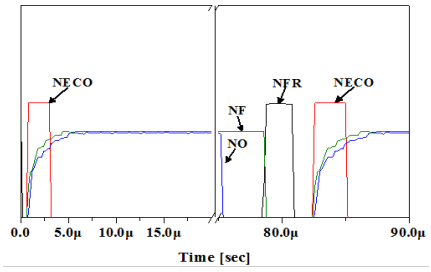

Figure 2 Signal response of CMOS ADC

[1] R.C. Baumann, IEEE Trans. Dev. Mat. Rel., 1, 17 (2001).

Acknowledgement
This work was supported by the IDEC, KAERI and the Kyungpook National University Research Fund 2012.

Identify applicable sponsor/s here. If no sponsors, delete this text box. (sponsors)

Taste sensor based on the gated lateral BJT with lipid/polymer membrane

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Recently, taste substances for classifying the five kinds of taste qualities as sourness, saltiness, sweetness, bitterness and umami. It is important to quantify the sense of taste by an artificial sensor for automation in the food industry. K. Toko developed the electronic taste sensor utilizes lipid/polymer membranes as a transducer of chemical substances to electric signals [1]. In this study, we proposed a taste sensor using a gated lateral bipolar junction transistor (GLBJT) for bitter (quinine) taste sensor [2]. The gated lateral BJT was fabricated using complementary metal-oxide semiconductor (CMOS) technology manufacturing process. The proposed device fabricated in a standard 0.35-μm CMOS logic process, which is provided by Magnachip/SK Hynix Co., Ltd. via the Integrated Circuit Design Education Center Multi-Project Wafer (IDEC-MPW) as shown in Fig. 1. (a). Quinine with bitter taste was used in this study as the sensing target. The sensing membrane which contains the trioctyl methyl ammonium chloride (TOMA) was fabricated on the floating gate of gated lateral BJT. The quinine was detected with the concentration varied from 1 fmol/L to 1μmol/L. The sensitivity of the gated lateral BJT taste sensor was approximately 1.894 μA/decade as shown in Fig. 1 (b).

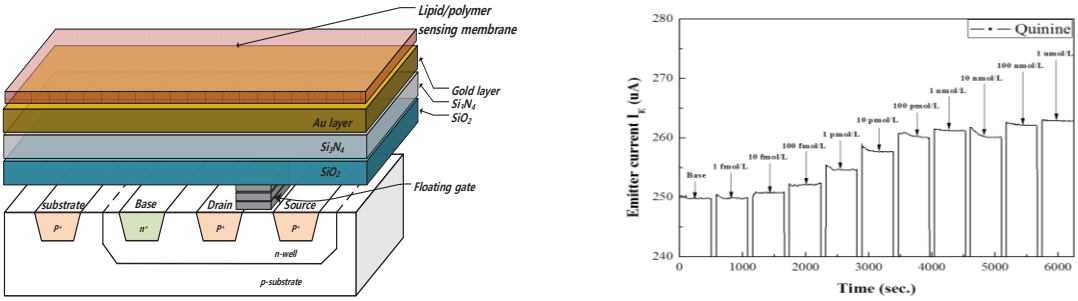

Fig. 1. (a) Schematic of gated LBJT; (b) response characteristics of the lipid (TOMA; trioctylmethyl ammonium chloride) membrane

[1] K. Toko, "Electronic sensing of the taste of beer and other foodstuffs", in *IEEE IEDM Tech., Papers IEDM '95., International*, December 10-13, 1995, pp. 143-148

[2] H.C. Kwon, D.H. Kwon, K. Sawada, S.W. Kang, "The Characteristics of H+ Ion-Sensitive Transistor Driving With MOS Hybrid Mode Operation", *IEEE Electron Device L.,* vol. 29, pp. 1138-1141, 2008.

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900 MHz 대역의 RFID 태그를 위한 LDO 레귤레이터

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현재 RFID 기술은 바코드를 대체할 기술로 많은 관심을 받고 있다 [1]. 수동 RFID 통신 시스템에서는 전압 체배기를 이용하여 별도의 전원 없이 자체적으로 RFID 태그에 전압을 공급한다. 그러나 전압 체배기로 얻어진 DC 전압은 비교적 큰 리플이 존재하기 때문에 회로의 전원 전압으로 사용하기에는 부적합하다. 따라서 이를 보완하기 위하여 레귤레이터를 사용한다. 본 논문의 LDO(Low Drop-Out) 레귤레이터의 회로도는 그림 1과 같다. LDO 레귤레이터는 전압 기준발생기와 연산증폭기, 부하로 이루어져 있고, 그 중 전압 기준발생기 회로는 LDO 레귤레이터의 동작에 필요한 기준 전압을 공급해준다. 연산증폭기는 출력의 전압을 감지하여 전압으로 넣어주는 피드백 구조를 사용하여 설계하였으며, 부하에 흐르는 전류에 따른 전압강하를 적게 하기 위하여 부하의 전력 트랜지스터가 한번에 100 μA 이상의 많은 전류를 흘릴 수 있도록 하였다. 본 회로는 동부 0.11 μm CMOS 공정을 사용하여 제작되었고, 제작된 회로의 칩 사진은 그림 2와 같다. 본 LDO 레귤레이터는 1.2 V ~ 3 V까지의 입력에 대해 1.06 V 의 평균값을 출력하였고, 대체로 일정한 값을 유지하였다. 이는 회로에 인가되는 전원 전압에 대해 영향을 받지 않는다는 것을 보여준다. 출력 전압에서 약 0.1 V의 칩 간 편차가 존재하는 것을 볼 수 있었는데, 이는 시뮬레이션 상에서 목표했던 10 % 이내의 오차를 만족하는 수치이다. 측정 결과는 그림 3과 같이 나타난다.

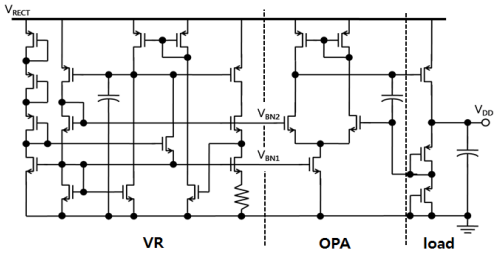

그림 1. 본 논문의 LDO 회로도.

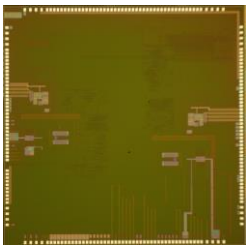

그림 2. 칩 사진.

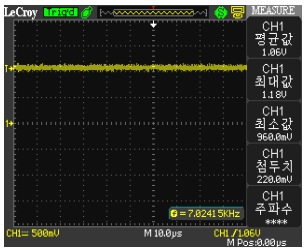

그림 3. LDO 의 출력결과.

[1] Medeiros *et al*, "Passive UHF RFID Tag for Airport Suitcase Tracking and Identification," *IEEE Antennas Wireless Propag. Lett.*, vol.10, pp.123-126, Mar. 2011.

This work was supported by the IDEC

D-band 대역 무선 송수신기를 위한 이득이 향상된 CMOS 혼합기

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CMOS 미세 공정기술의 지속적인 발전은 게이트 길이의 끊임없는 축소로 동작 속도를 향상시켜왔고, 현재에 이르러서는 100 GHz 이상의 높은 주파수에서도 동작하는 CMOS 소자가 등장하게 되었다. 그 결과 CMOS 직접회로기반의 D-band 에서 동작하는 초고속 데이터 통신시스템이 출현하게 되었다 [1]. 본 연구는 이러한 D-band 통신시스템을 구성하는 데에 중요한 역할을 하는 혼합기를 삼성 65-nm 디지털 CMOS 공정으로 이득을 향상시키는 방법을 적용하여 구현 하였다. 혼합기는 단일 길버트셀 구조에 기반을 하고 있으며 [2], 추가적인 PMOS 전류원을 그림 1 과 같이 하단 트랜지스터의 드레인에 마이크로스트립 선로로 연결함으로써 트랜스컨덕턴스를 증가시키면서 동시에 출력 임피던스 정합을 하였다 [3]. 이로 인해 단일 길버트셀 구조를 가진 혼합기 대비 변환 이득의 향상을 가져왔다. IF 출력 부는 일반적인 소스 팔로워 구조의 버퍼를 사용 하였다. 사용된 디지털 CMOS 공정은 RF 소자가 지원이 되지 않아 기존 RFCMOS 공정의 MOS 구조를 참고하여 설계자가 직접 액티브 영역 레이아웃을 수행하였다. 측정 결과 공정사에서 제공하는 RFCMOS 소자에 비해 다소 성능의 저하가 있었으나 디지털 공정으로 공정사에서 RFCMOS 소자를 제공하지 않아도 충분히 D-band 대역 혼합기가 구현이 가능함을 보였다.

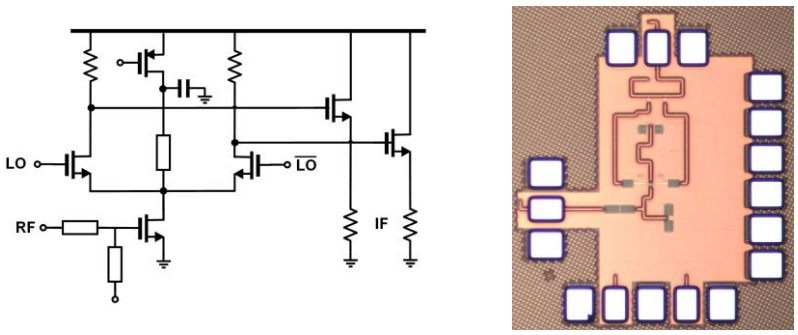

그림 1. 설계된 혼합기의 회로도와 칩사진.

[1] S. T. Nicolson *et al*., "A 1.2 V, 140 GHz receiver with on-die antenna in 65 nm CMOS," *in Proc. IEEE Radio Freq. Integr. Circuits Symp*., 2008, pp. 229–232.
[2] A. Maas, *Microwave Mixers,* 2nd ed. Norwood, MA: Antech house, 1993.
[3] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ: Pearson, 2012.

This work was supported by the IDEC.

트위스티드 연결 구조를 이용한 저전압 스윙 도미노 곱셈기

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본 논문은 트위스트 연결 구조를 이용한 새로운 도미노 곱셈기를 제안한다. 도미노 회로에서의 전체 소비전력 P_{total}은 다음과 같이 세가지 소비전력의 합으로 표현할 수 있다.

$$P_{total} = f_c \cdot C_L \cdot V_{DD} \cdot V_{sig} + I_{sc} \cdot V_{DD} + I_{leakage} \cdot V_{DD} \qquad (1)$$

식 (1)에서 전체 소비전력 중 가장 큰 영향을 미치는 것은 동적 소비전력이다[1-3]. 저전압 스윙 회로는 출력스윙을 줄여 동적 소비전력을 풀 스윙 회로의 (Vsig/VDD) ×100% 만큼만 소모, 소비전력을 감소시킨다. 본 논문에서 제안한 저전압 스윙 4x4 곱셈기는 풀 스윙 회로와 비교하여 31%의 소비전력 감소와 18%의 PDP (Power-Delay-Product) 감소를 보였다.

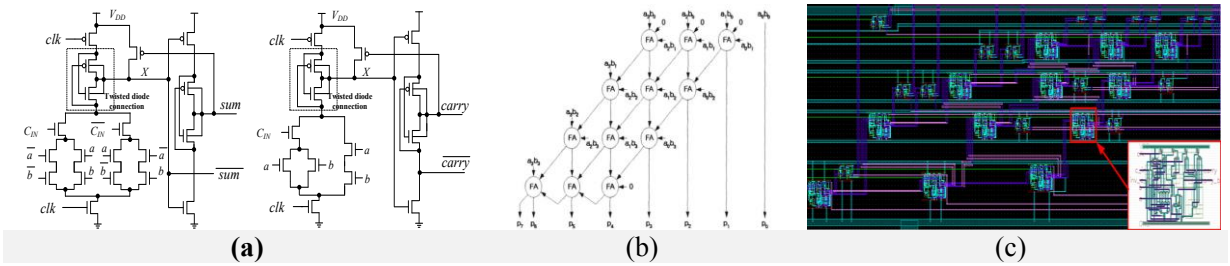

그림 1. (a)제안하는 저전압 스윙 전가산기, (b)제안하는 저전압 스윙 4x4 곱셈기 구조, (c)레이아웃

표 1. 풀 스윙 회로와 제안하는 회로의 시뮬레이션 비교

	Proposed	CMOS domino
Technology (nm)	180	
Number of bits	4	
Delay (ns)	2.072	1.751
Power (μW)	269.6	388.6
PDP (fJ)	558.6	680.4

[1] Z. Liu, V. Kursun, “Robust dynamic node low voltage swing domino logic with multiple threshold voltages” Int. Symp. ISQED., pp. 30–36, 2006.
[2] R. Mader, I. Kourtev, “Reduced dynamic swing domino logic”, Great Lakes Symp. VLSI, pp. 33–36, 2003.
[3] P. Chuang, D. Li, M. Sachdev, V. Gaudet, “Constant delay logic style”, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 3, pp. 554–565, 2013.

'This work was supported by the IDEC’

Q-enhanced LNA with VCO mode for Calibration

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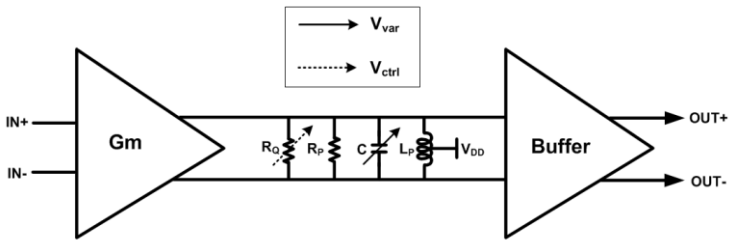
A low noise amplifier (LNA) with a blocker filtering should be applied due to stringent blocking requirement where exists large out-of-band blockers as close as in-band which can deteriorate the gain, noise, linearity of receiver front-end by desensitization [1]. Thus, blocker filtering LNA characteristic should be band pass filter (BPF) type with a high quality-factor (Q-factor). However, this Q-enhanced LNA should need to calibrate for offset center frequency because a narrow-resonance is prone to process-voltage-temperature (PVT) [2]. Therefore, Q-enhanced LNA is proposed for calibration by using VCO mode itself. As shown in Fig. 1, the proposed LNA with equivalent RLC load is proposed. The effective-transcondutance (Gm) structure consists of common-source amplifier and LC tank cross coupled load to be controlled output impedance by a specific bias (V_{ctrl}). Thus, Gm stage provides the variable Q-factor resistor (R_Q) which is resistance seen by output Gm and load inductor is represented as the paralleled parasitic resistor (R_P) and paralleled load inductor (L_P) in Fig. 1. Variable R_Q determined the Q-enhanced LNA mode or the VCO mode by cancelling the R_P. Therefore, this structure has potential for self-calibration of center-frequency LNA. Buffer stage output is 50 Ω with source-follower. Table 1 shows the measured summary of the LNA with VCO mode performances.



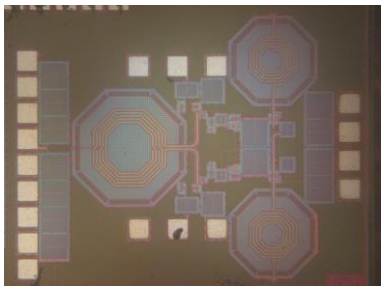


Fig 1. Block diagram of proposed LNA with equivalent RLC load (left), chip photo (right)

	Tech.	Gain / NF [dB]	Freq. [GHz]	IB-IIP3 [dBm]	Q_{LNA}	Area [mm^2]	Power Consumption [mW]	
This work	0.11 μm CMOS	27 / 2.4	2.32 ~2.51	-13	38	1.15	LNA mode (10.3)	VCO mode (5.2)

Table 1. Performance Summary

[1] H. Darabi, "A Blocker Filtering Technique for SAW-Less Wireless Receivers," *Solid-State Circuits, IEEE Journal of* , vol.42, no.12, pp.2766-2773, Dec. 2007
[2] H. Moon et al., "A 23 mV Fully Integrated GPS Receiver with Robust Interferer Rejection in 65nm CMOS", *ISSCC Dig. Tech. Papers*, pp.162-164, Feb. 2012.

This work was supported by the IDEC.

DPA-resistant cryptographic module

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All electric devices have different power consumption or eradiate different electromagnetic wave depending on their operation. Cryptographic modules used for security purpose also have similar characteristics, so such information can be used for attacking the modules. Especially, power analysis attacks [1] are known as a very effective attack, and there have been a lot of researches on them.

To protect cryptographic modules from power analysis attacks, there are two methods: hiding and masking. The hiding method makes the power consumption even, and the masking method makes the power consumption random without being affected by the operations of the cryptographic module. To make the power consumption even or random, the previous methods have additional circuits, which increase much more area and power consumption. Therefore, we propose a new hiding method.

The proposed method uses an extra capacitor and need little area increase. The ecnryption circuit uses charge not directly from the VDD but from the extra capacitor; therefore, the power analysis attack is ineffective.

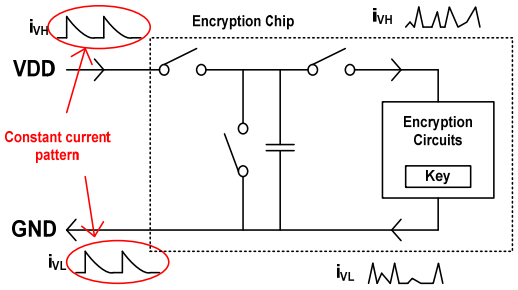

Fig 1. Architecture of the proposed method

[1] P. Kocher, J. Jaffe and B. Jun, In advances in Cryptology–CRYPTO'99, Springer Berlin Heidelber (1999).

This work was supported by the IDEC.

Offline User Authentication Method of Smart Card using PUF

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Due to security vulnerability, magnetic cards have been replaced by smartcards. A smartcard can operate by itself and store data in itself using its own CPU and memory, so the effect from the outside can be minimized.

Although smart cards provide much stronger security functions than previous magnetic cards, smart cards have security vulnerability as well. Some secret information such as keys and passwords are stored in servers or the volatile memory of smart cards. This information can be exposed by server hacking or some physical attacks on the memory. The server hacking is prevented if the secret data is not stored in servers, and the secret data or the key that is used to encrypt the secret data must not be stored in the memory of the smart cards. To solve these problems, we propose an offline user authentication that the smart cards perform user authentication by itself without being connected with the server, and possess its own key or personal identification number (PIN) using physical unclonable functions (PUFs) [1] without storing them in the volatile memory.

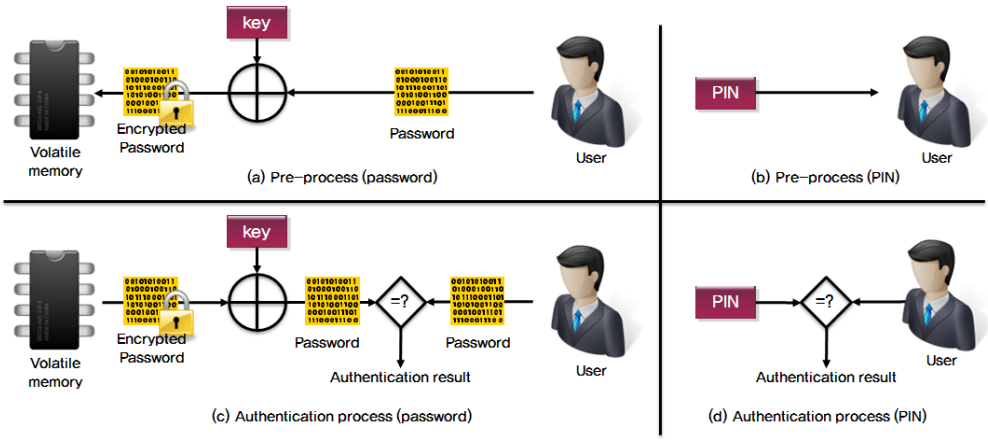

Fig 1. Preprocess and authentication process

[1] R. Pappu, B. Recht, J. Taylor, and N. Gershenfeld, Science 297 (2002).

This work was supported by the IDEC.

Design and Analysis of Differential Physical Unclonable Function

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A physical unclonable function (PUF) has been announced for identification and authentication [1-3]. A physical unclonable function (PUF) based on semiconductor process variation is implemented as hardware fingerprints. However, previous physical unclonable function revealed serious reliability problems when the process variation is not sufficiently large. we propose a differential-amplifier-based PUF which amplifies a small mismatch in the device characteristics from process variations and rejects the environmental noises.

Although an ideal differential amplifier should match input transistors and loads, there are actually mismatches in their characteristics such as threshold voltages, mobility, effective channel width and length, oxide thickness and so on. These mismatches cause both outputs to have different voltage levels. The comparator following the differential amplifier compares both outputs and decides either 1 or 0 depending on the polarity of the differential amplifier output. The differential amplifier improves the PUF reliability by amplifying small mismatch characteristics, which allows the voltage difference between the outputs to be more robust against the environmental disturbances. Thus high-reliability PUF can be realized even under noisy environments.

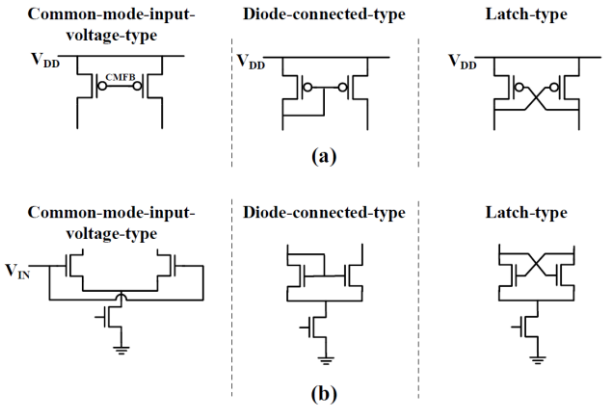

Fig 1. The Proposed PUF types

[1] C. Bösch, et al., CHES 2008, 2008, pp.181.
[2] M. Kalyanaraman, et al., HOST 2013, 2013, pp.13-18
[3] R. Helinski, et al., DAC 2009, 2009, pp. 676-681

This work was supported by the IDEC.

Self-bias controlled skimming current ROIC for bolometer

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마이크로 볼로미터는 저항형 센서로서 암흑전류가 매우 크고, 어레이로 제작 시 매우 불균일한 특성을 지니고 있어 각 픽셀 별 암흑전류 또한 매우 불균일하다. 따라서 온도안정화 장치가 없는 환경에서 마이크로 볼로미터의 불균일성을 보정하기 위해서는 픽셀(pixel)별로 암흑전류를 제거하는 current skimming control 이 반드시 필요하며, 본 논문에서는 그림 1 와 같이 암흑 볼로미터의 바이어스 전압을 자동으로 찾아주는 회로를 제안하고자 한다카메라의 셔터(shutter)가 닫히는 동안 스위치 Ø1 이 연결되고, 스위치 Ø2 가 닫히게 된다. 이때, 볼로미터로 흐르는 Ibias 로 인해 Vdark_bias 가 자동으로 찾아지게 되며, 셔터가(shtter)가 열리는 동안 스위치 Ø1 은 닫히고, Ø2 는 열리게 되어 이전 상태에서 저장된 Vdark_bias 로 인해 정확한 current skimming control 을 가능하게 한다.

아래의 결과를 보면, 일반 ROIC 와 제안한 ROIC 에 대해서 Active bolometer 의 저항 값을 변화시키며 출력 값을 비교해보면, 일반 ROIC 는 적외선 신호가 없을 때인 50kΩ 에서 dark current 가 제거되지 못하고 여전히 큰 신호를 나타내며, 신호가 커질수록 쉽게 포화되어 선형성을 잃게 된다. 하지만 제안한 회로의 경우, 적외선 신호가 없을 때인 50kΩ 에서 dark current 가 정확하게 제거 됨을 알 수 있다. 이로 인해 넓은 영역에 대해 선형성을 가질 수 있다.

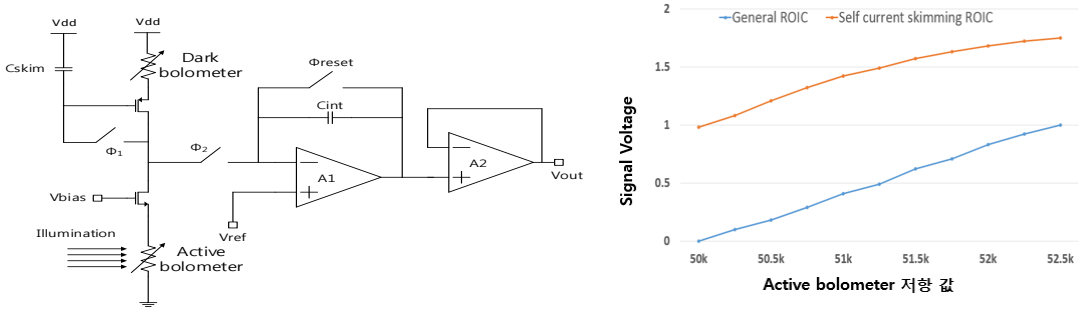

Fig 1. Self-bias controlled Circuit and result

Acknowledgement
This work was supported by IDEC

[1] William J. Parrish, James T. Woolaway, “Improvements in uncooled systems using bias equalization,” Proc. SPIE, (1999)
[2] P.K. Chan et al., “Designing CMOS folded-cascode operational amplifier with flicker noise minimization,” Microelectronics Journal 32, (2001)

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Light Sensing Circuit for Brightness Compensation in Retinal Prosthesis

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A human eye has the brightness-adaptation function that controls the sensitivity of the eye to incident light intensities according to the brightness of the environment [1-2]. Therefore, the brightness-compensating function should be implemented in a retinal prosthetic system to provide the neural stimulation similar to that in the normal eye. In this paper, a light sensing circuit for the brightness-compensating function is presented. The designed circuit is composed of a constant transconductance bias circuit and an operational amplifier. A photodiode is integrated for sensing the illuminating light intensities. A feedback resistor (R_F) is used to control the sensitivity of the circuit to the incident light intensities. An experiment using the fabricated chip is conducted on a test board. In the experiment, the illuminating light intensity is increased from 0 to 10,000 lux. The feedback resistance (R_F) is set as 510 kΩ or 2.2 MΩ. The output voltage increases as proportional to the incident light intensities. In addition, the rate of increase of the output voltage increases as the feedback resistance is increased. The experimental results show that the designed circuit can be utilized for the brightness-compensating function.

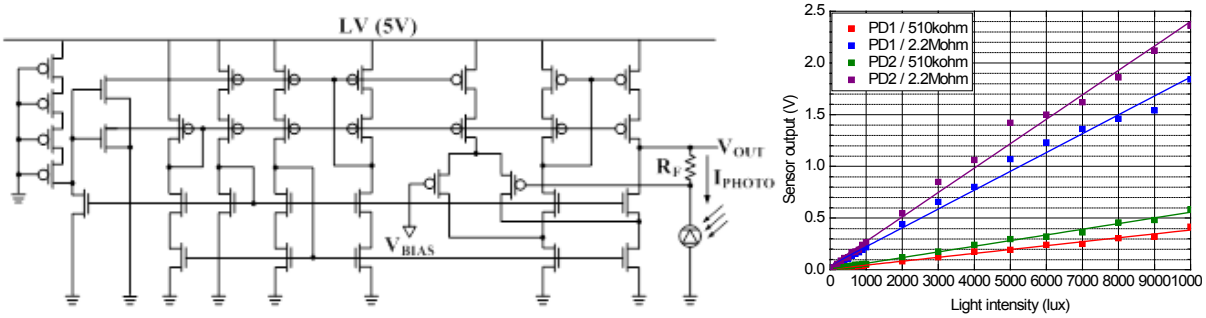

Fig 1. A schematic of the designed light sensing circuit and the experimental results

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[2] G. Jackson, M. Clark, I. Scott, L. Walter, D. Quillen, and M. Brigell, "Twelve-Month Natural History of Dark Adaptation in Patients with AMD," *Optometry. Vision Sci.*, vol. 91, pp. 925-931, Aug. 2014.

This research was supported by the public welfare & safety research program through the National Research Foundation of Korea (NRF) funded by Ministry of Science, ICT and Future Planning (2012-0008611). This research was also supported by IC Design Education Center (IDEC).

Authentication module based on PUFs

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Various things around us have networking ability and are connected with each other; for example, we can remotely start a car or warm up a house in advance before going home. This convenience, however, can have problems such as invasion of privacy at the same time unless the security is not guaranteed.

To build a safe network environment, each thing must have its own secret information with an authentication module to identify and authenticate itself. It is very important to safely generate and keep the confidential data, but it is not that easy with low cost and strong security. As a solution, Physical Unclonable Functions (PUFs) [1] can be used. PUFs are an unduplicable function and can generate random information even with the same design, so PUFs are usable as secret keys for authentication.

Using PUFs, we designed an authentication module for device authentication. The designed module includes cryptographic modules such as AES, SHA2, RSA, and RSA as well as PUF-based keys. The PUF-based keys are only kept in the authentication module, and its corresponding public key is generated from it and extracted to the outside. Using these keys the module performs device authentication.

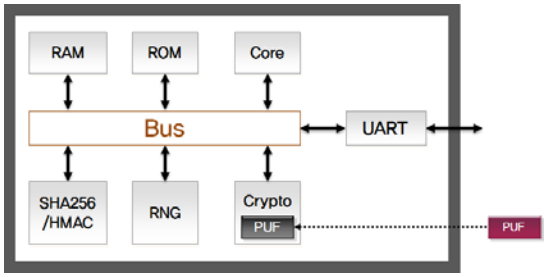

Fig 1. Structure of the authentication module

[1] R. Pappu, B. Recht, J. Taylor, and N. Gershenfeld, Science 297 (2002).

This work was supported by the IDEC.

CMOS Capacitor Integrated Ion Trap Chip Package

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An ion trap is a device which can trap charged particles using oscillating and static electric fields. The ions are confined at an RF null point where the RF pseudopotential is a local minimum. If the total electric field generated by static voltages is not zero at the RF null point, the position of trapped ions will be shifted, resulting in the micromotion of ions. One of the current methods to minimize the micromotion is to connect a low-pass filter to a DC electrode of the ion trap chip to eliminate the RF noise from digital-to-analog converter (DAC) [1]. In this paper, an RC low-pass filter circuit using a CMOS capacitor is presented. The capacitor chip includes a 17 × 1 CMOS capacitor array. One terminal of the capacitors in the array is connected to each other to provide the same ground. These capacitor arrays are integrated with the ion trap chip package, keeping the low-pass filters close to the trap electrodes to reduce the noise induced by the feed-throughs. The target cut-off frequency of the proposed RC low-pass filter is 160 kHz. The electrical characteristics of the fabricated capacitor array are measured by an LCR meter (4982A, Agilent Technologies). The capacitance of an individual capacitor device in the array is 0.055 nF which is 42-percent less than the designed value, however, the cut-off frequency of the low-pass filter can be adjusted by the external resistors.

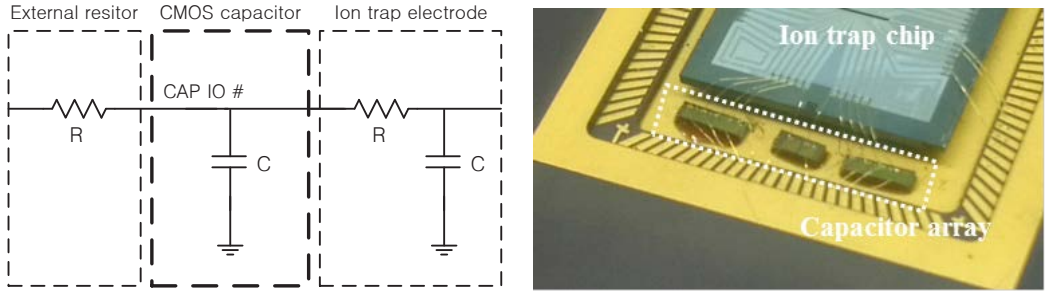

Fig 1. Implementation of RC low-pass filter and ion trap chip package with fabricated capacitors

[1] Allcock, D. T. C., et al., "Heating rate and electrode charging measurements in a scalable, microfabricated, surface-electrode ion trap," *Applied Physics B*, Vol. 107, No. 4, pp. 913-919, 2012.

This research was supported by ICT R&D program of MSIP/IITP. [10043464 , Development of quantum repeater technology for the application to communication systems]. This research was also partially supported by IC Design Education Center (IDEC).

Low noise circuit for Brain machine interface

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jungwoojang@snu.ac.kr

I. INTRODUCTION

Measuring neural signals makes it possible not only to analyze how brain works but also to predict intended limb movements[1]. For example, brain machine interface that consists of multichannel neural recording system can predict behavior of paralyzed patients in real time by measuring cortical activity, and it allows the machine to conduct actions that patients want. However, current integrated circuit system has unacceptable noise level and requires a lot of power consumption to be implanted. By now, the need for appropriate approaches to design BMI circuit system gradually increased[2]. In this paper, ultra-low noise amplifier and multiplexer are proposed which are proper to be inserted in brain.

II. DESCRIPTION

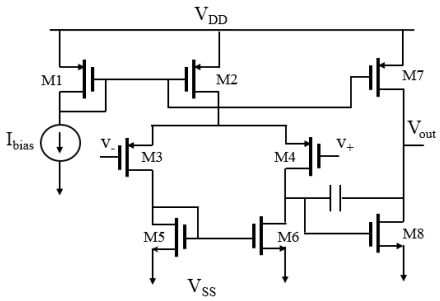


Fig. 1 Schematic of the proposed low noise amplifier

Fig. 1 shows schematic of the proposed unbuffered, two stage low noise amplifier. This topology is suitable for driving capacitive loads and for minimizing noise each transistor is designed to operate in weak, moderate, or striong inversion region[3]. In paricular, input transistors(M_3, M_4) which have the highest value of transconductance are critical for noise characteristics. A 16 channel analog multiplexer which used complementary shunt switch structure is proposed in Fig. 2. Outputs of amplifiers are connected to analog multiplexer and transmitted following circuit by switching signals. The input referred noise of analog multiplexer is not important since 40dB of gain of LNA attenuate the multiplexer's noise.

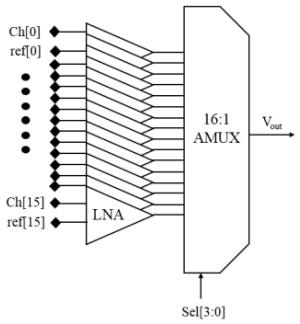
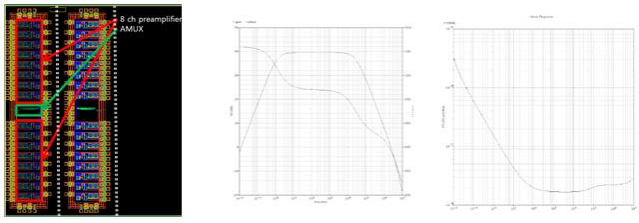


Fig. 2 Simplified block diagram of the chip

III. CHIP IMPLEMENTAION AND RESULTS



(a) (b) (c)

Fig. 3 (a) Chip photo, (b) Bode plot and phase,

(c) Input referred noise of LNA

The designed chip was implemented in Dongbu 0.35μm CMOS process, as shown in Fig. 3(a). Test was conducted by applying different sinusoidal wave to 16 channel amplifiers and the results were confirmed from the amplitude of output of analog multiplexer switching selection signals of multiplexer. Simulated data is shown in Fig. 3(b) that shows the mid band gain of 39.85 dB and Fig. 3(c) present the input referred noise of 3.66μV_{rms}.

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[2] RR Harrison, C Charles, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE* J. *Solid-State Circuits*, vol. 38, no. 6, pp. 958-965, June 2003

[3] Wattanapanitch W, Sarpeshkar R, *et al.*, "A Low-Power 32-Channel Digitally Programmable Neural Recording Integrated Circuit" *Biomedical Engineering, IEEE Transactions on*, vol. 5, no. 6, pp. 592-602, December 2011

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Design of Step-up DC-DC Converter for Mobile Applications

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I. INTRODUCTION

Nowadays, the demand of electronic devices market has been increased rapidly. Also, the functions of personal mobile electronic devices have become more useful and diverse, so they require various supply voltage levels to operate. This confirmed the indispensability of Power management Integrated Circuit (PMIC) designs. Mobile devices with limited battery power depend on the changes in load and the efficiency of battery power management that helps to extend the battery life. In the literature, there has been many studies conducted switch-mode methods with a high efficiency but hard to integrate on a single chip, because of the size. In this paper, we present a step-down DC-DC converter using the switch-mode method for the backlight LED of mobile devices. As an alternative solution to solve the aforementioned problem, the switch-mode method with control block is used and integrated on a single chip, excluding the capacitor, inductor and diodes.

II. DESCRIPTION

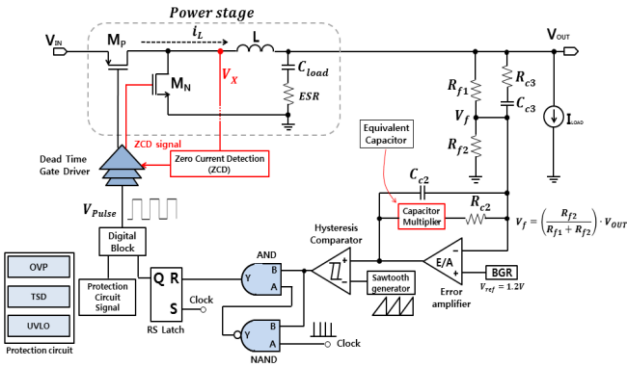

Fig 1. The block diagram of the proposed converter

The proposed circuit consists of a power block that composed of a power MOSFET, an inductor, a capacitor and a resistor, and a control block that regulates the PWM signal. The converter is also supported by other sub-circuits such as an UVLO (under voltage lock out), an OVP (over voltage protection) and a TSD (thermal shut down). These sub-circuits ensure the proper operation and protect the chip from break-down operation.

III. CHIP IMPLEMENTAION AND RESULTS

Table 1. Results of the proposed Converter

	Result of the proposed converter			
	Parameter	*Simulation*	*Chip*	*Unit*
CORE	Supply Voltage	3.3	3.3	V
	Output Voltage	4.3	4.3	V
	Ripple	50	70	mV
LDO	Supply Voltage	3.3	3.3	V
	Output Votlage	2.5	2.5	V
BGR	Supply Voltage	3.3	3.3	V
	Output Voltage	1.2	1.2	V
SW pulse	Frequency	1 M	892 k	Hz

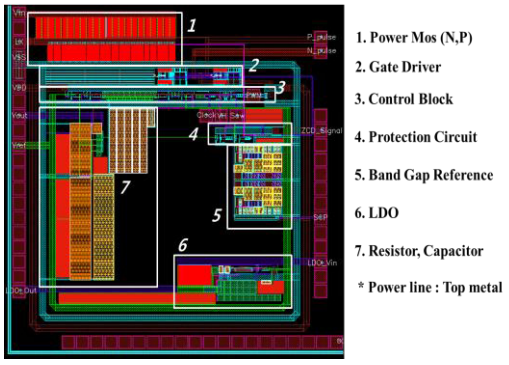

Fig 2. Image of the fabricated converter chip

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[1] P. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, "Analysis and Design of Analog Integrated Circuits," 4th ed. New York, Wiley, 2001.

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[3] Basso, Christophe. P. "Switch-Mode Power Supplies: SPICE Simulations and Practical Designs," McGraw Hill, 2008.

This work was supported by the IDEC'

Pulsed-V_{dd}의 실제 하드웨어 구현

김상민, 백돈규, 안용수, 이동수, 신영수
KAIST 전기및전자공학과

디지털 회로는 일반적으로 클럭을 이용하여 동기화한다. 클럭을 분배하기 위한 클럭 네트워크는 회로 전체로 클럭을 전달해야 하기에 설계하기 어렵고 또한 많은 면적과 wirelength 를 필요로 한다 [1]. 특히나 낮은 클럭 스큐를 위해 기존 트리 구조 대신 메시 형태의 클럭 네트워크를 사용하게 되면서 이러한 문제가 더욱 부각되고 있다 [2].

본 논문에서는 동기회로의 클럭 네트워크를 공급 전압 네트워크에 주기적인 펄스를 보내서 대체하고자 한다. 메모리 소자로는 펄스 래치를 사용하게 되며, 펄스 생성기에서 공급 전압 네트워크의 펄스와 동기 되는 펄스 신호를 만들어 래치를 구동하게 된다. 그림 1 (a)에 Pulsed-V_{dd} (PV_{dd})의 기본 개념이 설명되어 있다. PV_{dd} 신호는 전원 공급과 클럭 전달 역할을 동시에 한다. PV_{dd} 값이 0 으로 떨어지면 게이트 출력의 1 값들은 떨어지지만, 펄스의 크기가 작으므로 완전히 0 으로 떨어지기 전에 펄스가 종료되어 데이터 보존이 가능하다

PV_{dd} 회로는 IDEC 제 119 회 MPW, 상용 65nm 공정으로 설계되었다. PCI to Ethernet bridge 디자인을 구현하였으며, 게이트 수는 35 만개, 동작 주파수는 125Mhz, 총면적은 4x4mm^2 다. 기존 회로와의 클럭 스큐 차이를 확인하기 위해 동일한 디자인을 클럭 네트워크를 사용하여 구현하였다 (그림 2 의 FF core). 테스트 장비의 부족으로 본 회로의 PV_{dd} 펄스는 외부에서 입력으로 주는 대신 칩 내부에서 자체적으로 생성하여 PV_{dd} 디자인에 전달되었다. 본 논문의 칩은 설계 과정의 오류로 인해 실제 동작은 확인하지 못하였다.

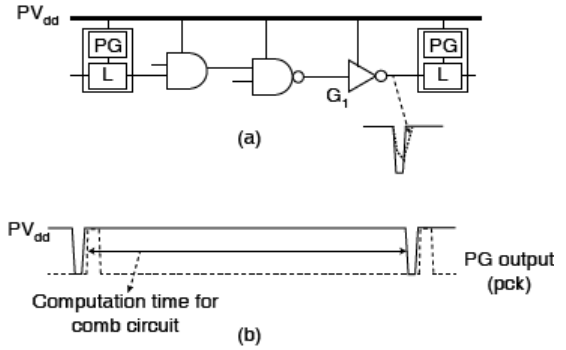

그림 1. (a) Pulsed-V_{dd}의 개념 (b) PV_{dd} 와 pck 파형.

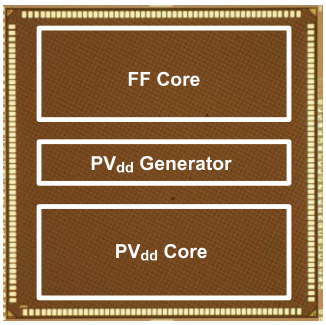

그림 2. 실제 칩 사진

ACKNOWLEDGEMENT
본 연구는 IDEC에서 칩 제작 지원을 받았음.

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Adaptive multisensor analog front-end with initial voltage setting and offset calibration schemes

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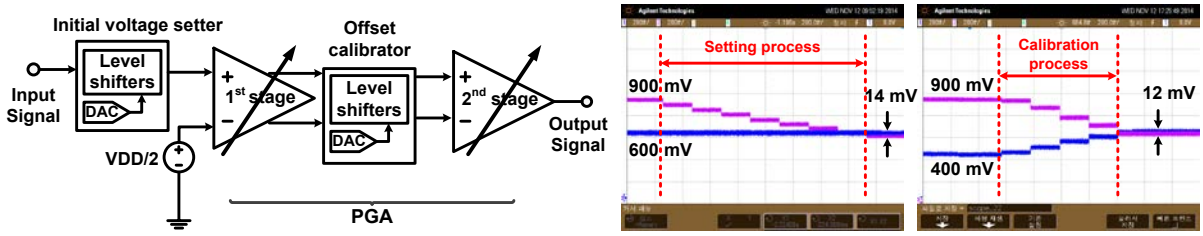
Sensor application systems, especially for smart devices, are increasingly adopting multisensors. Since their responses have different initial voltages and sensitivities [1], a programmable gain amplifier (PGA) which is able to adapt to these conditions is necessary. This work proposes two schems on this point. Firstly, the available gain can be limited according to their initial voltages, so the initial voltage setting block is inserted. Secondly, an offset problem may result in saturating an amplifier, so offset calibrater is implemented. As Fig. 1 (a) shows, the system consists of two main blocks, the initial voltage setter and the instrumentation-amplifier-based PGA [2] with offset calibrator. The initial voltage setter changes all initial voltages at the inputs to VDD/2, and this level assures the maximum signal swing range, allowing the gain of the PGA to be as high as possible. But the inevitable setting error causes an offset problem in the PGA, so the PGA first stage preamplifies the offset and the offset calibrator cancels it. The calibrated signal is again amplified by the second stage of the PGA. Figure 1. (b) shows the results of these processes. The intial voltage setting error is 14 mV and remaining offset after calibration is 12 mV. The power consumption is 4.8 mW and PGA gain goes from 18.5 dB to 49.5 dB.



(a) (b)

Fig. 1 (a) Overall architecture and (b) results of initial voltage setting and offset calibration

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Low ripple Digital LDO regulator 설계

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최근 leakage power 를 줄여 에너지 효율을 높이기 위한 sub/near-threshold logic 회로들의 연구가 활발하다. 이러한 로직은 공급 전원에 매우 민감하여 전압 레귤레이터는 ripple 이 적은 안정적인 전원을 공급해야 한다. 본 논문에서는 상황에 따라 ADC(Analog to Digital Converter) 해상도를 제한하는 controller 를 제안하여 load current 변화에 의한 DAC(Digital to Analog Converter)해상도 변화로 생기는 LCO(Limit Cycle Oscillation)를 해결한 Digital LDO 를 설계하였다. 주요 루프는 그림 1 과 같이 구성되어 있다. VTC(Voltage to Time Converter) 와 PUD(Phase Up/Down Detector), Cyclic TDC(Time to Digital Converter)로 구성된 ADC 와 controller 그리고 switch array 와 load 로 구성된 DAC 로 이루어져 있다. 그림 2 는 load current 변화에 따른 출력 ripple 측정결과 이다. 전원 전압 700mV, 목표전압은 550mV, load capacitor 는 달지 않았다. Load current 25mA 를 기점으로 DAC 의 해상도가 ADC 의 해상도 보다 더 낮아지게 되어 ripple 이 커지는 현상을 확인할 수 있다. Idea block 적용할 경우 load current 가 5mA 일 때 56mV 에서 7.2mV 로 8 배가량 개선되는 것을 확인 하였다. 그림 3 은 controller block diagram 이고, 그림 4 는 die photo 이다.

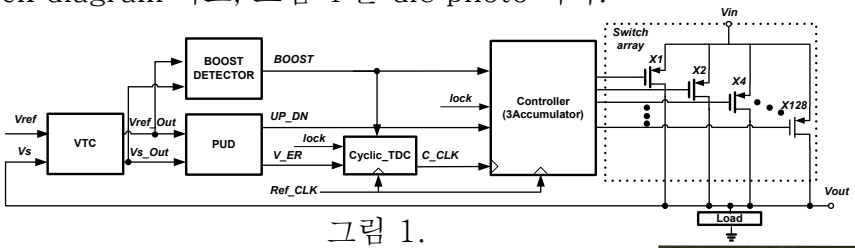
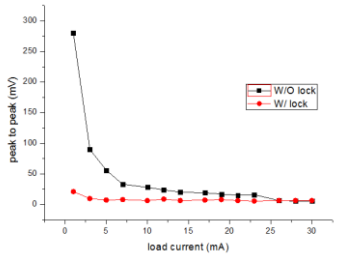


그림 1.



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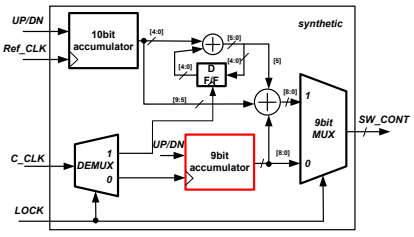

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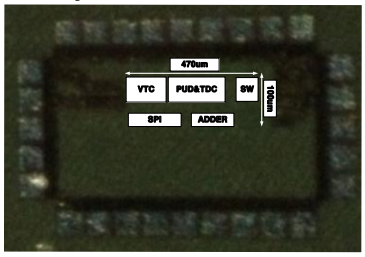

그림 4.

[1] Oh, T.-J., Hwang, I.-C. "A 110-nm CMOS 0.7-V Input Transient-Enhanced Digital Low-Dropout Regulator With 99.98% Current Efficiency at 80-mA Load." Very Large Scale Integration(VLSI) Systems, IEEE Transactions on 2014

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Vector-Sum Phase Shifter Using dB-Linear VGA

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I. Introduction

The phase shifter adjusts the phase of incoming signal in order to obtain the required beam pattern, which is a very important factor in electronic phase array systems [1]. Among many topologies, vector-sum phase shifter capitalizes the phase shifting technique by summing the controlled I/Q signal. This kind of phase shifter needs VGA (Variable Gain Amplifier) and quadrature phase generator for the controlled I/Q signal. We propose the vector-sum phase shifter to ensure phase shift continuously using dB-linear VGA.

II. Design of The Proposed Phase Shifter

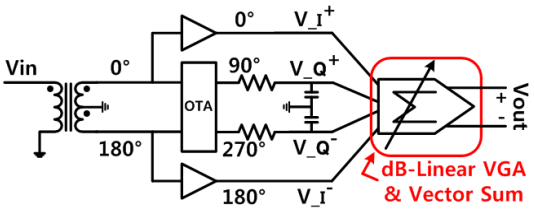

Fig. 1. Block diagram of the proposed phase shifter

Fig. 1 is the block diagram of the proposed vector-sum phase shifters. I/Q signals (I: 0°, 180°, Q: 90°, 270°) are made through a transformer and an RC filter, and then phase is shifted by vector-sum using the dB-linear VGA. Fig. 2 is the circuit of proposed dB-linear VGA and vector-sum. dB-linear gain controller excites the control input voltages (VC1, VC2), and generates the bias voltages (VB1, VB2) for having characteristic which regulates the tail current of VGA. Also, incoming I/Q signals are changed to the form of current (I_I, I_Q) through input transistor, then the magnitude of I/Q current signals are changed by dB-linear gain controller. Controlled I/Q current signals perform vector-sum at P of Fig. 2. Based on this method, added signals are constantly maintained, because the gain is controlled dB-linearly. The phase of shifted signal is continuously adjusted, because input control voltage is continuously adjusted.

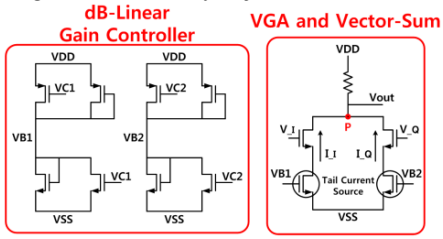

Fig. 2. Circuit of the dB-linear VGA & vector-sum

III. Simulation and Result

Fig. 3 is the post-layout simulation result of the proposed phase shifter. According to input control voltages, phase of signals are shifted continuously, and the gain is designed around -4dB. A center frequency is chosen to be 915 MHz, and maximum power consumption is 40mW including output buffers.

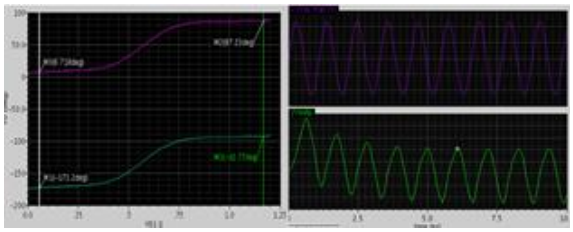

Fig. 3. Simulation result of the proposed phase shifter

Table 1 shows a comparison table of vector-sum phase shifters and Fig. 4 shows the microphotograph of the proposed phase shifter.

Table 1. Comparison of Vector-Sum Phase Shifter

	Tech	V_{DD} (V)	Freq (GHz)	Phase Resol.	Gain (dB)	P_{DC} (mW)
[2]	0.18μm CMOS	1.8	3 ~ 4	22.5	-11 ~ -13	15.6
[3]	0.18μm CMOS	1.8	0.75 ~ 2.67	11.25	-17.4 ~ 3.5	13.9
This work	0.11μm CMOS	1.2	DC ~ 1.2	Cont.	-4	40

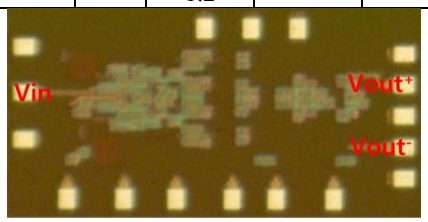

Fig. 4. Microphotograph of the proposed phase shifter

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860 MHz Non-Foster Circuits with Noise Canceling Method

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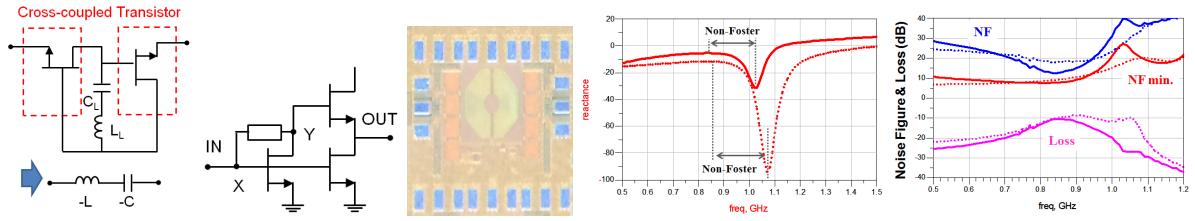
Noise Figure (NF) is the most important factor of LNA. To overcome the trade-off between antenna size and Q, the negative reactance slope of the non-Foster circuit versus frequency is used in MHz frequency, mainly [1][2]. However, there are still three major challenges using non-Foster circuit, which are noise, stability and power consumption. In this paper, non-Foster circuits with noise canceling method is designed and fabricated using standard 65nm CMOS process.

To design the circuit of negative capacitance and inductance, the Linvill's negative impedance converter (NIC) method is used. As shown in the Fig. 1 (a), The NIC is composed of cross-coupled two FETs with several capacitors and inductors. The main operation of the NIC is performed by inverting the polarity of the C_L and L_L. However, NIC generate huge noise for this operation. Because the transistors are noise source and have positive feedback structure.

To reduce the noise of NIC, it is necessary that canceling the noise from transistor itself. Proposed NIC is using the noise canceling method in the Fig. 1 (b) to the cross-coupled transistor cell of Linvill's NIC. As shown in the Fig 1 (d), the reactance slope versus frequency is negative at 860 MHz. The series connection of NIC and electrical small antenna is simulated and the results is in the Fig. 1 (e). In this case, the effectiveness of the non-Foster circuit can be confirmed by improvement results of the NF and minimum NF which are 5.2 and 1.48 dB respectively.



(a) (b) (c) (d) (e)

Fig 1. (a) circuit topology, (b) noise canceling method, (c) chip photograph, (d) Negative reactance slop and (e) Simulation results with (solid) and without (dot) noise canceling method

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A Phase Controlling System for Focused Ultrasound

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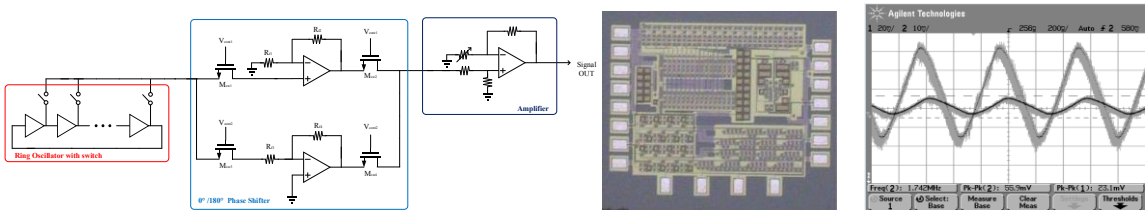
Recently, the research on a non-invasive medical application with focused ultrasound has been conducted. To achieve focused ultrasound, acoustic waves from a transducer array should arrive at a target point at the same times. To compensate the path difference from the each element of transducer to focal point, the time of phase delays of signals are needed. In this paper, a phase controlling system for focused ultrasound is proposed in 0.18um CMOS technology.

Fig. 1 shows the proposed phase controlling system. Fist of all, the ring oscillator which has multi-stage inverter pair chains determines frequency of signal, a resolution of controlling phase. The signal can be delayed by going through each the inverter stage due to the gate delay so that 16 stage inverter pair chains provides phase delay of π in steps of 11.25°. A 0°/180° phase shifter is included to cover the full range of phase up to 2π. The OP amp increase the amplitude of the signal for excitation of the phase array transducer with inverting and non-inverting input. The gain of amplifier would be variable by controlling the ratio of feedback resistance and input resistance.

The measurement result is represented in Fig. 1 (c). The phase delay of a 2MHz signal that has 3.3Vpp swing is demonstrated by simulation. However, the amplitude of measured signal is 56mVpp, which means performance of ring oscillator has problem because of a variation of load condition of a ring oscillator. Because the parasitic capacitance of output pad to verify an each building block limits the performance of designed chip.



(a) (b) (c)

Fig.1 (a) propased systm design (b) micrograph ot the fabricated chip (c) Measurement result

[1] Dr. George. K. et al., “Ultrasound-Asisted Convection-Enhanced Drug Delivery to the brain”, AIUM 2011, New York City.

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Ku-band 정지-위성 통신 시스템을 위한 VCO와 VGA의 설계

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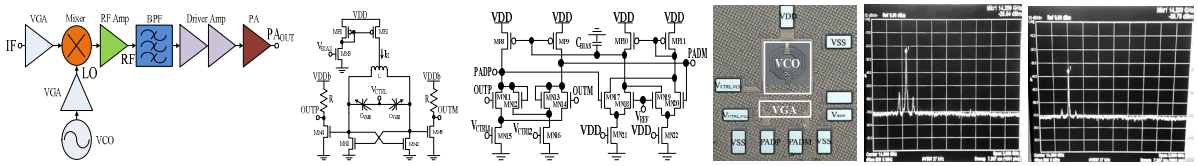
Ku(12/14GHz) 대역은 정지 위성 서비스 (FSS : Fixed Satellite Service) 에 사용되며 송신부 블록도를 그림 1.(a)에 나타냈다 [1]. 12.4~ 15.4GHz의 클락 생성을 위해서는 전압 제어 발진기 (VCO) 가 필요하고, 위성 통신에서 눈, 비 등의 기상 요인들에 의한 신호 감쇠를 보상하기 위한 증폭기도 필요하다. 본 논문에서는 Ku-band 정지-위성 통신에 적용할 수 있는 VCO와 가변 이득 증폭기 (VGA) 를 설계했다. 설계한 VCO와 VGA의 회로도는 그림1.(b), (c)와 같다. 그림 1.(b)에서 제안하는 VCO는 NMOS 교차쌍 LC형 구조이며 바이어스를 위한 전류 미러와 VGA 입력단과 VCO 출력과의 분리를 위한 버퍼를 추가했다. 그림 1.(b)와 그림1.(c)에서 제안하는 VGA 구조는 [2]와 같은 구조를 65nm 공정으로 최적화하여 설계했다. 기존 회로와의 차이점은 15GHz의 높은 주파수에서 동작하기 위해 W/L을 최적화하여 기생성분을 최소화하는 레이아웃을 진행하였고 30mV 이하의 낮은 진폭이 오동작을 유발할 수 있기 때문에 바이어스 회로를 추가하여 트랜지스터의 게이트 바이어스 전압을 V_t근처로 설계했다.

칩은 65㎚ CMOS RF 공정을 사용했고, 측정은 프로브스테이션에서 진행했다. 그림 1.(d)는 칩사진이고, 그림 1.(e),(f)는 측정결과이다. VCO는 12.2~15.7GHz의 동작범위를 갖고 VGA는 이 동작주파수를 입력으로 받았을 때 동일한 출력전력을 갖는다. VGA는 VC전압에 따라 출력 크기를 제어하며 입력이 -19dBm일때 -16~-28dBm의 출력을 갖는다. VCO의 소모전력은 7.2mW이고 VGA의 소모전력은 3.6mW이다. 설계한 VCO와 VGA는 Ku-band 정지-위성 통신 시스템에 사용될 수 있다. 본 연구는 IDEC의 지원을 받았다.



(a) (b) (c) (d) (e) (f)

그림 1. (a)Ku대역 송수신 클락 생성 블록도 (b)VCO 회로도 (c)VGA회로도 (d)칩사진 (e)VGA출력전력(VC=0V) (f)VGA출력전력(VC=1.2V)

표 1. 기존 연구와의 성능 비교

	Process	Output Freq.[㎓]	Gain range[dB]	P_{DC} [㎽]
[2]	0.18um CMOS	40MHz~1GHz	-48~36	6.48
This work	65㎚ CMOS	12.2~15.7GHz	-19~3	3.6

[1] C.-H. Lee, A. Sutono, S. Han and J. Laskar, "A Compact LTCC Ku-Band Transmitter Module with Integrated Filter for Satellite Communication Applications," IEEE, Microwave Symposium Digest, MTT-S International, Vol.2, pp.945-948, May. 2001.

[2] Quoc-Hoang Duong et al., "An All CMOS 84dB-Linear Low-Power Variable Gain Amplifier," Symposium on VLSI Circuits Sigest of Technical Papers, pp.114-117, Jun. 2005.

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Hough Transform Accelerator for Lane Detection

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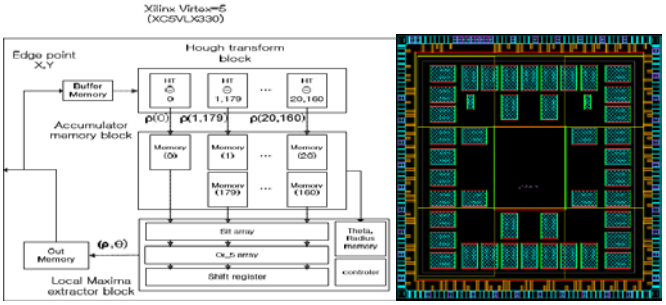
I. INTRODUCTION

Recently, modern cars are being equipped with a highly sophisticated computerized assistance system such as LDWS (Lane Departure Warning System) for safe driving. LDWS is a mechanism designed to warn a driver when the vehicle begins to move out of its lane on roads without a turn signal. LDWS consists of many image processing algorithms, and lane detection is the most important part of the LDWS. There are several approaches for the lane detection algorithm, such as B-snake[1], Histogram based segmentation[2], Edge linking[3], and Hough transform[4]. Among these, Hough transform is the mostly preferred method due to its robustness against noise. However, its computational complexity is very high hence is not easy to be implemented in real time. In this paper, we propose a hardware architecture for Hough transform optimized for LDWS to be used as an accelerator engine with small hardware cost.

II. DESCRIPTION

The aim of the Hough transform is to represent geometric forms of the edge information using a parametric space defined by ρ and Θ, where ρ is the distance from the origin to the straight-line and Θ is the angle between the normal and the X-axis. For efficient operation, we can reduce computation and logic area by limiting the angles of the lines to (-20, 20) degrees which are enough for lane detection applications and its arithmetic computations were performed in parallel to speed up the processing time.

Our hardware platform is described in Figure 1-(a). An ARM-based embedded processor board and Xilinx FPGA are used to verify the function of our Hough hardware and the entire LDWS system. The proposed hardware is on Virtex-5 XC5VLX330 device.



(a) (b)

Fig. 1 Hardware block diagram and its chip layout

In Figure 1-(a), the host extracts the edge points from the received image and stores them in Buffer memory. For each Θ, the value of ρ is calculated in the Hough transform block on each edge point of the Buffer memory.

III. CHIP IMPLEMENTATION AND RESULT

Our chip has been synthesized with 206,420 gates and 25.6Kbyte SRAM in Samsung 65nm CMOS process. The chip is described in Figure 1-(b) whose size is 4mm × 4mm. While the Hough transform takes 45ms with a general embedded environment, the designed hardware generates 10,000 fps at 100MHz, which is enough for real time processing. Table I is the result comparison of the execution time when implementing the Hough transform in software and hardware. For the software we used a single ARM Cortex-A9 processor operating at 1.4 GHz Compared to the software implementation, the hardware accelerator was about 450 times faster when processing VGA images (640×480 pixels) with roughly 5,000 edge pixels. We assured that our design operates correctly.

	ARM Cortex-A9 1.4GHz(ms)	Proposed system(ms)
Hough Transform on VGA(5000 points)	45~50	0.1~0.2

Table 1 Comparison of processing time (hardware and software)

ACKNOWLEDGEMENT

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[4] M. Aly, "Real time detection of lane markers in urban streets," IEEE Intelligent Vehivles Symposium, pp. 7-12, June 2008.

Low Power Signal Processing Unit for Pulse Oximetry

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There is growing interest for health monitoring application, which can monitor blood-oxygen saturation, heart rate, or etc. Blood-oxygen saturation (SpO2) and heart rate can be easily measured using non-invasive method with photoplethysmogram (PPG) signal. For blood-oxygen saturation measurement, red and infrared light-emitting diode (LED) light which passes through subject's finger and photo-detector are normally utilized [1]. De/oxygenated hemoglobin absorb red and infrared light differently by its concentration. Hence, the current from photo-detector is used to calculate the ratio of de/oxygenated hemoglobin. It should be noted that these kind of signals are changed along with heartbeat which has 30~240Hz frequency [2]. In pulse oximetry design, the hardware like DSP and microcontroller operates much faster than heartbeat frequency, therefore it wastes clock cycle until next input signal comes in. For optimizing pulse oximetry system, we design signal processing unit and folded architecture is implemented on computational units to reduce area and leakage power. Each computational unit operates in a different time slot to minimize peak power.

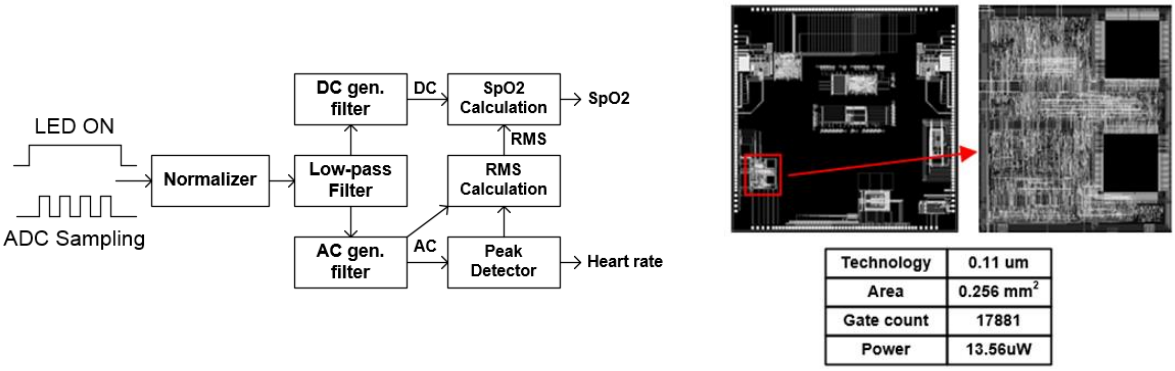

Fig 1. Block diagram of signal processing unit for pulse oximetry and implementation result

[1] Tavakoli, M. et al., "An Ultra-Low-Power Pulse Oximeter Implemented With an Energy -Efficient Transimpedance Amplifier," Biomedical Circuits and Systems, IEEE Trans., vol. 4, no. 1, pp. 27-38, Feb. 2010.
[2] Li, K. et al., "Onboard Tagging for Real-Time Quality Assessment of Photoplethysmograms Acquired by a Wireless Reflectance Pulse Oximeter," Biomedical Circuits and Systems, IEEE Trans., vol. 6, no. 1, pp. 54-63, Feb. 2012.

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Fault-tolerant ECU platform including an in-vehicle Ethernet controller

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An electronic control unit (ECU) is a key component in implementing automotive functionalities such as braking systems, power steering systems, as well as engine control systems. A single-chip ECU platform exhibiting much stronger fault-tolerance than conventional structures is implemented. A block diagram and a die photo of the single-chip ECU platform is shown in Fig. 1. The Core-A embedded processor [1] with additional fault-tolerant techniques is employed as a main controller. Compared to the conventional controllers, the proposed fault-tolerant Core-A processor provides much stronger fault-tolerance because a double-error correcting (DEC) BCH code is employed. A low-complexity search-less DEC BCH decoder [2] is implemented to correct bit errors of the memory system while the register file inside the processor is protected by the single-error correcting Hamming code. In addition, a 100BASE-TX Ethernet controller is included to provide a new solution of in-vehicle control network reducing the wiring harness in vehicles. Lastly, there are various kinds of peripheral interfaces such as inter-integrated circuits (I2C) and 4-channel serial peripheral interface (SPI). The ECU platform is fabricated in a 65nm CMOS process. The platform occupying area of 0.80mm^2 operates at a maximum operating frequency of 208MHz.

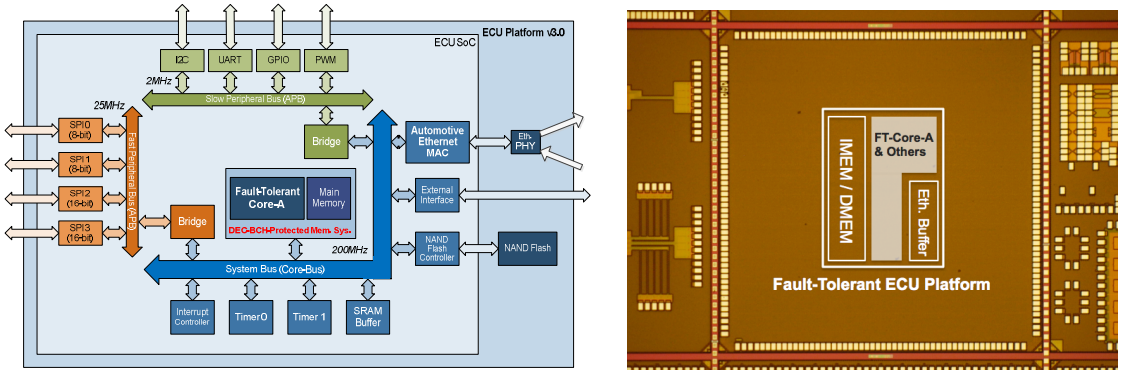

Fig 1. A block diagram and a chip die photo of the single-chip ECU platform

[1] J.-H. Kim *et al.*, "Design of high-performance 32-bit embedded processor," in *Proc. IEEE Int. SoC Design Conf.*, Nov. 2008, pp. III-54 - III-55.
[2] I. Yoo and I.-C. Park, "A search-less DEC BCH decoder for low-complexity fault-tolerant systems," in *Proc. IEEE Workshop Signal Process. Syst.*, Oct. 2014, pp. 44-49.

This work was supported in part by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (No. 2010-0028680) and the IC Design Education Center (IDEC).

디지털 제어 가유전체 전송선로를 적용한 Q-대역 In-Situ 임피던스 튜너

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I. INTRODUCTION

30GHz 이상의 밀리미터파 대역에서는 트랜지스터의 정확한 동작을 파악하고 설계하기가 매우 어려운 과제이다. On-wafer 에서 source pull 을 하여 입력 반사계수에 따른 특성을 측정한다면 정확한 트랜지스터 입력단의 특성 파악이 가능하다. 본 연구에서는 트랜지스터의 정확한 evaluation 을 위해 임피던스 튜너를 설계하였다. 병렬 R, C 로 기본 임피던스 튜너 셀을 설계하고 이것을 디지털 제어 가유전체(DiCAD) 전송선로를 사용하여 Q-대역에서 In-situ 임피던스 튜너 (IST)의 튜닝 범위를 확대하는 것을 목적으로 한다.

II. DESCRIPTION

A. *DiCAD 설계*

DiCAD 전송선로는 CPW 전송선로 밑에 신호 진행 방향과 수직 방향의 strip 을 지나가게 한 뒤, 각각의 strip 을 switch 를 사용하여 접지시킨 것이다. 이를 통해서 switch 의 on/off 에 따라 전송선로의 위상 차이를 바꿈으로써 반사계수를 바꿀 수 있다. EM 시뮬레이션을 통해 CPW 밑의 strip 이 접지 되어 있을 경우와 floating 되어 있을 경우, 위상차이와 삽입 손실 차이를 Table 1 에 비교 및 정리하였다. Width 가 27um 이고 Spacing 이 27um 일 때 큰 위상 차이를 갖는 동시에 손실이 작아 가장 적합하였다.

Strip 의 접지를 위한 스위치는 사용하는 주파수 대역인 Q-대역에서 적합한 게이트 너비를 갖도록 설계하여야 한다. 스위치를 off 하였을 때는 고립 특성이 좋아야 하고 on 하였을 때 Ron 이 작아야 물리적으로 접지와 단락시켰던 시뮬레이션 결과와 비슷한 결과를 얻을 수 있다. 제공되는 모델을 통한 소신호 시뮬레이션 결과, 40GHz 에서 가장 적절한 트랜지스터는 3um X 20 였다.

B. *IST 설계*

IST 설계는 R, C 병렬 토폴로지를 이용하였다. 가변 저항은 cold-MOS 를 사용하여 구현하였으며, 가변 캐패시터는 varactor 를 이용해 구현하였다. 각각의 바이어스는 게이트 바이어스만 필요하므로, 간단히 저항을 이용하여 구현하였다. 목표가 되는 Q 대역에서의 튜닝 범위는 IST 뒷 부분에 달릴 DiCAD 전송선로를 고려하여 낮은 저항값에 위치하도록 하였고, DiCAD 전송선로와 함께 IST 전체의 반사계수가 inductive 한 영역에 위치하도록 트랜지스터의 사이즈를 최적화하였다. 전체 IST 의 schematic 은 Fig. 1 과 같다.

III. CHIP IMPLEMENTAION AND RESULTS

DiCAD 를 각각 0μm, 180 μm, 360 μm 로 하였을 때의 시뮬레이션 결과가 Fig 2. (a)와 같다. 시뮬레이션 결과 40GHz 에서 inductive 한 영역의 많은 부분을 포함하는 튜닝 범위를 확인할 수 있었다. Fig. 2 (b)는 본 회로의 사진으로, CMOS 공정을 이용해 작은 die size 에 집적하였다.

IV. ACKNOLEGEMENT

이 논문은 2014 년도 BK21 사업에 의하여 지원되었음.

Width(um)/ Spacing(um)	*위상차이(도)*	*삽입손실 차(dB)*
W:27 / S:27	18.8	0.170
W:19.8 / S:27	19.5	0.571
W:16.2 / S:27	19.1	0.875

Table 1.Width 와 Spacing 에 따른 위상차이와 삽입손실

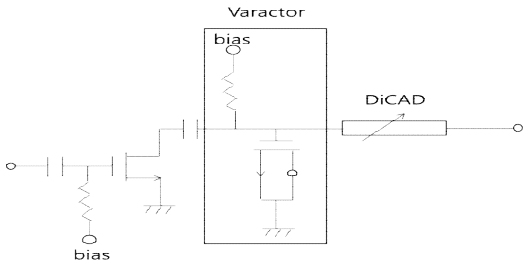
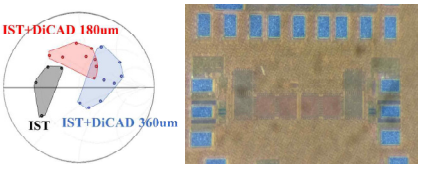


Fig 1. Schematic of proposed IST



(a) (b)

Fig 2. (a) Tuning range of proposed IST at 40 GHz,
(b) Chip photograph of fabricated circuit

REFERENCE

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