N. VLSI CAD 분과

## [WJ3-N] Memory & Architecture

| | |
|---|---|
| **Date** | Feb. 26, 2014 (Wed.) |
| **Place** | Room J / 제1공학관 501호 (# 501, Engineering Building I) |

Session Chair: 이종은 교수(UNIST), 김윤진 교수(숙명여자대학교)

**WJ3-N-1** **15:50-16:05** **A Dual-Retention Time Architecture towards Secure and High Performance STT-RAM Main Memory Subsystem**
저자: Taemin Lee, Sungjoo Yoo, and Sunggu Lee
소속: Department of Electrical Engineering, Pohang University of Science and Technology

**WJ3-N-2** **16:05-16:20** **LPDDR2-NVM 기반의 상변화 메모리 시스템 설계**
저자: Jaehyun Park and Naehyuck Chang
소속: Department of Electrical Engineering and Computer Science, Seoul National University

**WJ3-N-3** **16:20-16:35** **New Processing Element for Imperfect Nested Loops on Coarse Grained Reconfigurable Architecture**
저자: Seongseok Seo, Hyeonuk Sim, and Jongeun Lee
소속: School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology

**WJ3-N-4** **16:35-16:50** **Intra/Inter-CGRA Co-Reconfiguration for Efficient CGRA-Based Multi-Core Architecture**[1]
저자: Heesun Kim, Seungyun Sohn, and Yoonjin Kim
소속: Department of Computer Science, Sookmyung Women's University

**WJ3-N-5** **16:50-17:05** **FPGA Prototyping of Programmable Regular Iterator Generator**
저자: Hyeonuk Sim, Seongseok Seo, and Jongeun Lee
소속: School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology