The 21st Korean Conference on Semiconductors
제21회 한국반도체학술대회
February 24–26, 2014 / Hanyang University, Seoul, Korea

G. Device & Process Modeling, Simulation and Reliability 분과

[WJ1-G] Thin-Film Transistors/Reliability

Date	Feb. 26, 2014 (Wed.)
Place	Room J / 제1공학관 501호 (# 501, Engineering Building I)

Session Chair: 신민철 교수(KAIST), 최재훈 박사(SK hynix)

WJ1-G-1 10:50-11:05
A Novel Characterization Technique for Location of Laterally Distributed Grain Boundary in Polycrystalline Silicon Thin-Film Transistors
저자: Jaeyeop Ahn, Hagyoul Bae, Hyunjun Choi, Jun Seok Hwang, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim
소속: School of Electrical Engineering, Kookmin University

WJ1-G-2 11:05-11:20
The Effect of Passivation on the Positive Bias Stress-Induced Instability of Polymer Thin-Film Transistors
저자: Jaewook Lee, Jaeman Jang, Hyeongjung Kim, Chunhyung Jo, Sungwoo Jun, Kyung Min Lee, Dong Jae Shin, Juntae Jang, Sungju Choi, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim
소속: School of Electrical Engineering, Kookmin University

WJ1-G-3 11:20-11:35
Capacitance-Voltage Technique for Extraction of Intrinsic Subgap DOS in AOS TFTs with Bias-Dependent Channel Conduction Factor Model
저자: Hyunjun Choi, Hagyoul Bae, Jaeyeop Ahn, Jun Seok Hwang, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim, and Dong Myong Kim
소속: School of Electrical Engineering, Kookmin University

WJ1-G-4 11:35-11:50
Prediction Technique and Mechanism for PCB Pattern Crack in NAND Package of SSD
저자: JungHoon Kim, JinYoung Choi, JaeWoo Jung, Jin-Hyuk Lee, JongYun Yun, and JoonHee Lee
소속: Solution Development Team, Samsung Electronics Co., Ltd.

WJ1-G-5 11:50-12:05
Analysis of Power Integrity of Multi-Layer 3D IC with PEEC-Based PDN
저자: Seungwon Kim, Ki Jin Han, and Youngmin Kim
소속: School of Electrical and Computer Engineering, Ulsan National Institute of Science and Techology