The 21st Korean Conference on Semiconductors
제21회 한국반도체학술대회
February 24-26, 2014 / Hanyang University, Seoul, Korea

K. Memory (Design & Process Technology) 분과

[TK2-K] 3D Memory Techniques

Date	Feb. 25, 2014 (Tue.)
Place	Room K / 제1공학관 502호 (# 502, Engineering Building I)

Session Chair: 곽동화 박사(삼성전자),

TK2-K-1 **11:10-11:40** **Scaling Issues and Trends of NAND Flash Memory**
저자: Jaeduk Lee, Youngwoo Park, and Gyoyoung Jin
소속: Semiconductor R&D Center, Samsung Electronics

TK2-K-2 **11:40-11:55** **Towards High Performance Selector Device for 3D Stacked Cross-Point Arrays**
저자: Jiyong Woo, Daeseok Lee, Euijun Cha, Sangheon Lee, Sangsu Park, and Hyunsang Hwang
소속: Department of Materials Science and Technology, Pohang University of Science and Technology

TK2-K-3 **11:55-12:10** **A New Programming Method to Alleviate the Program Speed Variation for Three-Dimensional Channel Stacked Array Architecture**
저자: Joo Yun Seo, Yoon Kim, Sang Ho Lee, and Byung-Gook Park
소속: Inter-university Semiconductor Research Cener and Department of Electrial Engineering, Seoul National Univerisity

TK2-K-4 **12:10-12:25** **3차원 플래쉬 메모리를 위한 매우 얇은 다결정 실리콘 채널 층을 갖는 정션리스 플래쉬 메모리의 특성에 관한 연구**
저자: 박종경[1], 김승윤[1], 이기홍[2], 피승호[2], 이석희[1,2], 조병진[1]
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