

The 21st Korean Conference on Semiconductors
제21회 한국반도체학술대회
February 24–26, 2014 / Hanyang University, Seoul, Korea

G. Device & Process Modeling, Simulation and Reliability 분과

[TJ1-G] Device Physics & Simulation

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| Date | Feb. 25, 2014 (Tue.) |
| Place | Room J / 제1공학관 501호 (# 501, Engineering Building I) |

Session Chair: 김대환 교수(국민대학교), 이상기 박사(동부하이텍)

- TJ1-G-1 09:30-10:00 Recent Advances in Deterministic Solvers for the Boltzmann Transport Equation and Future Research Directions**
저자: Sung-Min Hong
소속: School of Information and Communications, Gwangju Institute of Science and Technology
- TJ1-G-2 10:00-10:15 Simulation of III-V UTB SB-MOSFETs using Tight-Binding Band-Structure Calculations**
저자: Howon Choi, Jaehyun Lee, Yolum Lee, and Mincheol Shin
소속: Department of Electrical Engineering, KAIST
- TJ1-G-3 10:15-10:30 3D Simulation of Threshold Voltage Variations Due to Random Grain Boundary and Discrete Dopants in Sub-20 nm Gate-All-Around Poly-Si Transistors**
저자: Jungsik Kim¹, Hyeongwan Oh³, Junyoung Lee³, Jiwon Kim³, Chang-Ki Baek², and Jeong-Soo Lee^{1,3}
소속: ¹Department of IT Convergence Engineering, Pohang University of Science and Technology, ²Creative IT Engineering and Future IT Innovation Lab, Pohang University of Science and Technology, ³Electrical Engineering, Pohang University of Science and Technology
- TJ1-G-4 10:30-10:45 Simulation of Dual Material Gate InAs Schottky Barrier Field Effect Transistor**
저자: Wonchul Choi, Jaehyun Lee, and Mincheol Shin
소속: Department of Electrical Engineering, KAIST