O. System LSI Design 분과

[TG1-O] VLSI System Design and Applications I

Date	Feb. 25, 2014 (Tue.)
Place	Room G / 제1공학관 405호 (# 405, Engineering Building I)

Session Chair: 이한호 교수(인하대학교),

TG1-O-1 **09:30-10:00** **Two-Level Cache Organization for a Merge Mode Prediction in a Hardware-Based HEVC Encoder**
저자: Tae Sung Kim[1], Hyuk-Jae Lee[1], and Chae Eun Rhee[2]
소속: [1]Department of Electrical Engineering and Computer Science, Seoul National University, [2]Department of Information and Communication Engineering, Inha University

TG1-O-2 **10:00-10:15** **Hardware Optimization for Low Complexity Edge Detection**
저자: Juseong Lee and Jongsun Park
소속: School of Electrical Engineering, Korea University

TG1-O-3 **10:15-10:30** **NAND Flash Memory Controller using Multi-Rate BCH Codes**
저자: Kijun Lee, Sejin Lim, and Jun Jin Kong
소속: Memory Division, Samsung Electronics Co., Ltd.

TG1-O-4 **10:30-10:45** **WBAN을 위한 저면적 저전력 BCH 복호기**
저자: 정보석, 김철호, 이한호
소속: 인하대학교 정보통신공학부

TG1-O-5 **10:45-11:00** **System Level Exploring of Memory Configuration for Low Power**
저자: Sung Yang, Hoi-Jin Lee, Young-Min Shin, and Jae-Cheol Son
소속: SoC Processor Development Team, System LSI Business, Samsung Electronics Co., Ltd.