N. VLSI CAD 분과

[TF2-N] CAD & Low Power

Date	Feb. 25, 2014 (Tue.)
Place	Room F / 제1공학관 404호 (# 404, Engineering Building I)

Session Chair: 이종은 교수(UNIST), 김윤진 교수(숙명여자대학교)

TF2-N-1 **11:10-11:40** **Wear-Leveling Algorithm for Phase Change Memory using Danger-Line First Address Randomization**
저자: Dong-gun Kim
소속: Design Technology System Architecture Team, SK hynix

TF2-N-2 **11:40-11:55** **Identifying Redundant Inter-Cell Margins and Its Application to Technology Mapping**
저자: 이유종, 심성보, 신영수
소속: KAIST 전기및전자공학과

TF2-N-3 **11:55-12:10** **PEEC-Based Dynamic IR Drop Analysis with On Chip Decoupling Capacitor of the Double-Gate FinFETs**
저자: Jaemin Lee and Youngmin Kim
소속: School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology

TF2-N-4 **12:10-12:25** **Design and Optimization of Mesh Clock Network with Multi-Level Clock Gating**
저자: Jinwook Jung, Dongsoo Lee, and Youngsoo Shin
소속: Department of Electrical Engineering, KAIST

TF2-N-5 **12:25-12:40** **Synthesis of Multi-Stage Gate-Level Clock Gating**
저자: Inhak Han and Youngsoo Shin
소속: Department of Electrical Engineering, KAIST