L. Analog Design 분과

## [TF1-L] 아날로그 및 혼성 신호 회로 설계 1

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| **Date** | Feb. 25, 2014 (Tue.) |
| **Place** | Room F / 제1공학관 404호 (# 404, Engineering Building I) |

Session Chair: 박성민 교수(이화여자대학교), 문용 교수(숭실대학교)

**TF1-L-1** **09:30-09:45** **Area-Efficient 20-Gbps Optical Receiver Circuit in 65-nm CMOS Technology**
저자: Hyun-Yong Jung, Jin-Sung Youn, and Woo-Young Choi
소속: Department of Electrical and Electronic Engineering, Yonsei University

**TF1-L-2** **09:45-10:00** **입력 지터 감소 기법을 적용한 2.5 Gb/s BMCDR 회로 설계**
저자: 정재훈[1], 최정환[1], 백광현[2]
소속: [1]삼성전자 메모리사업부, [2]중앙대학교 전자전기공학부

**TF1-L-3** **10:00-10:15** **A Single-Stage 40dB-Linear Digitally-Controlled Variable Gain Amplifier for Ultrasound Analog Front End**
저자: Seong-Eun Cho[1], Ji-Yong Um[2], Byungsub Kim[2], Jae-Yoon Sim[2], and Hong-June Park[1,2]
소속: [1]Division of IT Convergence Engineering, Pohang University of Science and Technology, [2]Department of Electronic and Electrical Engineering, Pohang University of Science and Technology

**TF1-L-4** **10:15-10:30** **Constant Off-Time Control with Time Calibration Method for Buck Converter**
저자: Haneul Kim, Kyoungjin Lee, Jehyung Yoon, Hyoung-Seok Oh, and Byeong-Ha Park
소속: Power Device Development Team, System LSI Division, Samsung Electronics Co., Ltd.

**TF1-L-5** **10:30-10:45** **A 25-Gb/s Quarter-Rate CDR in 65-nm CMOS Technology**
저자: Dae-Hyun Kwon and Woo-Young Choi
소속: Department of Electrical and Electronic Engineering, Yonsei University

**TF1-L-6** **10:45-11:00** **A Multi-Channel 1-Gb/s/ch Inverter Transimpedance Amplifier Array with Replica in 0.18μm CMOS**
저자: Hanbyul Choi, Xiao Ying, Seung-Hoon Kim, and Sung Min Park
소속: Department of Electronics Engineering, Ewha Womans University