Area-Selective Chemical Vapor Deposition of Co for Reduction of Cu Electromigration

Jaehong Yoon[1], Soohyeon Kim[1], Han-Bo-Ram Lee[2], Byeongchul Cho[3], and Hyungjun Kim[1]*

[1] School of Electrical and Electronic Engineering, Yonsei University, Seoul, 120-749, Korea

[2] *Department of Materials Science and Engineering, Incheon National University, Incheon, 406-772, Korea*

[3]*Wonik IPS, 332-1 Cheongho-ri, Jinwi-myeon, Pyeongtaek-si, Gyeonggi-do, korea*

E-mail : hyungjun@yonsei.ac.kr

Electromigration (EM) of Cu interconnect is a main problem in reliability of nanosized Si devices. The current density increases with decreasing the feature size of Cu interconnect, leading to a rapid drop of EM lifetime. One of the causes of EM failures is diffusion of Cu atoms along the interface between Cu and dielectric capping. It was reported that the Cu diffusion at the interface can be effectively suppressed by capping with a proper metal layer.[1] The metal capping layer for EM needs to have two properties, low resistivity and deposition selectivity. There is a trade-off between EM improvement and increase in Cu resistivity when a metal capping layer is applied, so that a metal with low resisitivity on Cu line is necessary. Metal capping layer is need to be selectively formed on surfaces of Cu lines only but not on ILD surfaces. Low deposition-selectivity of metal capping may casue line-to-line leakage.

In this study, Co films were deposited on patterned Cu by chemical vapor deposition (CVD) with high deposition selectivity between Cu and SiO_2. Cyclopentadienyl dicarbonyl Co ($CoCp(CO)_2$) and H_2 gas were employed as a precursor and reactant, respectively. Since as-dep CVD Co was contaminated with C, post-depsoition treatment using NH_3 plasma was adopted to reduce C contamination. Although the Cu/SiO_2 surfaces were exposure to NH_3 plasma, deposition selectivity of CVD Co was remained. Eelectrical properties of Cu lines capped with CVD Co, such as resistivity and EM were examined.

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Silicidation of Ni prepared by Atomic Layer Deposition with NH_3 Gas Reactant

Soohyeon Kim, Jaehong Yoon, Han-Bo-Ram Lee, and Hyungjun Kim
Department of Electrical and Electronics Engineering, Yonsei University, Seoul, Korea
Department of Materials Science and Engineering, Incheon National University, Incheon, Korea
E-mail : hyungjun@yonsei.ac.kr

NiSi 는 기존의 실리사이드 물질인 $TiSi_2$ 와 $CoSi_2$ 에 비해 낮은 Si 소비량과 낮은 저항, 우수한 열적 안정성을 갖기 때문에 반도체 소자 공정에서 가장 적합한 컨택 물질로 각광받고 있다. 그러나 소자의 크기가 점점 작아짐에 따라, 높은 종횡비 (aspect ratio)를 갖는 컨택 홀에서 기존 금속박막 증착방법인 PVD (Physical Vapor Deposition)를 사용해서는 균일한 박막을 얻을 수 가 없기 때문에 고단차 증착이 가능한 새로운 증착법이 필요하다.[1] ALD (Atomic Layer Deposition)는 원자층 단위에서 두께 조절이 가능하고, 우수한 단차 피복성을 갖기 때문에 나노 스케일의 입체적 구조를 코팅하기에 매우 적합하다. 이에 따라 본 연구진은 NH_3 플라즈마를 반응물로 사용한 Plasma Enhanced ALD (PE-ALD) Ni 공정을 보고한 바 있다.[2] PE-ALD Ni 의 경우 초기 NH_3 플라즈마 노출에 의해 박막과 Si 기판 사이에 SiN_x 중간층이 형성되는 것을 관찰하였다. 본 연구에서는 플라즈마 반응물 대신에 $Ni(dmamb)_2$ 전구체와 암모니아 가스를 반응물로 이용하여 300 °C 의 온도에서 Ni 박막 증착 공정을 개발하였다. PE-ALD Ni 공정을 이용한 Ni 박막과 Thermal ALD Ni 공정을 이용한 Ni 박막을 각각 열처리 하여 실리사이드 실험을 진행하였다. XRD 분석 결과, PE-ALD Ni 박막은 400-500 °C 열처리 후 NiSi 결정이 약하게 관찰되며 700 °C 열처리 후 $NiSi_2$ 결정이 두드러지게 나타났다. 그러나 Thermal ALD Ni 박막은, 500 °C 열처리 후 대부분이 NiSi 로 형성되고, 600 °C 열처리 후 $NiSi_2$ phase 가 관찰되었다. 이러한 silicidation 의 변화를 금속 박막의 확산에 대한 박막의 quality 와 interlayer 의 영향으로 설명하였다. 이와 더불어, 높은 conformality 를 보이는 thermal ALD Ni 을 나노 스케일의 contact hole (100 nm 이하)에 증착하여 입체적 구조 내에서의 silicidation 도 연구하였다.

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Highly conformal Cu_2O Thin Films by Atomic Layer Deposition using a new non-fluorinated Cu precursor

Hangil Kim[1], Seung-Joon Lee[1], Taehoon Cheon[2], Sang-Kyung Choi[3] and Soo-Hyun Kim[1*]
[1]*School of Materials Science and Engineering, Yeungnam University, 214-1, Dae-dong, Gyeongsan-City, 712-749, Korea*
[2]*Senter for Core Research Facilities, Daegu Gyeongbuk Institute of Science & Technology, Sang-ri, Hyeongpung-myeon, Dalseong-gun, Daegu, Korea*
[3]*Center for Research Facilities, Chungnam National University, Yuseong-gu, Daejeon, Korea*

E-mail : *soohyun@ynu.ac.kr

Copper oxide thin films have been investigated for many applications including gas sensors, resistive RAM, photodiodes, anode in batteries, p-type thin film transistors (TFT), other all-oxide transparent electronics. Cu_2O is also a p-type semiconductor having a band gap of 2.0-2.6 eV [1] and mobility of 5 cm^2/Vs at room temperature (293K) [2]. So, Cu_2O is the most studied because of its high optical absorption coefficient in the visible range and its reasonably good electrical properties. Atomic layer deposition (ALD) is an attractive and versatile technique allowing the growth of highly conformal oxide films at low temperatures. Although much work has been devoted to the growth of metallic Cu interconnects by ALD, very little attention has been put on the growth and characterization of copper oxides [2, 3]. F-containing precursor of trimethylvinylsilyl -hexafluoroacetylacetonato copper(I), which has a vapor pressure of 1 torr at 60 °C [2], and nonfluorinated copper precursor of bis(tri-*n*-butyphosphane)acetylacetonato copper(I) [3], which has a vapor pressure of 0.015 torr at 98 °C was used to make ALD-Cu_2O thin film. In this study, ALD-Cu_2O films were deposited on thermally grown SiO_2 and sapphire substrates at a deposition temperature ranging between 120 and 240 °C using bis(1-dimethylamino-2-methyl-2-butoxy) copper(II) (figure 1) and water vapor. This precursor is thermally more stable and has good properties, which are free of fluorine in the precursor and highly volatile. The vapor pressure is quite higher (1.2Torr at 80 °C) than other Cu precursors. Figure 2 shows the grazing incidence angle (θ= 3°) XRD patterns of the typical ALD-Cu_2O film deposited on SiO_2 substrate. Four peaks from cubic-structured Cu_2O crystal were clearly shown in figure 2. And Cu_2O thin film has excellent step coverage around 100% with ALD characteristic (Figure 3). XRD analysis (Fig. 4) showed that these ALD-Cu_2O films were reduced to metallic Cu film after annealing at 500 ℃ in H_2/Ar ambient, which has been evaluated as a seed layer for Cu electroplating.

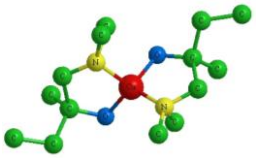

Figure 1.
Bis(1-dimethyl-amino-2 -methyl-2-butoxy)copper

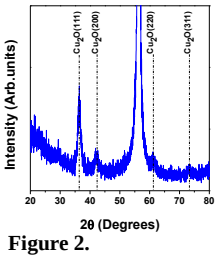

Figure 2.
XRD gragh on SiO_2 substrate

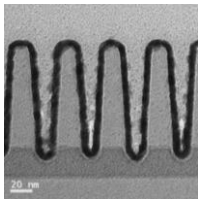

Figure 3.
Step coverage of ALD-Cu_2O film

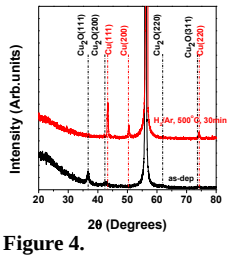

Figure 4.
XRD gragh of Cu after reduce process of Cu_2O on SiO2 substrat

Acknowledgements
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Growth of Ru thin film by thermal atomic layer deposition using a new beta-diketonate Ru precursor and O_2 or NH_3 molecules as a seed layer for Cu electroplating

Seung-Joon Lee[1], Minyoung Lee[1], Taehoon Cheon[1,2], Soo-Hyun Kim[1*], Masayuki Saito[3], Kazuharu Suzuki[3], and Shunichi Nabeya[3]

[1] *School of Materials Science and Engineering, Yeungnam University, 214-1, Dae-dong, Hyeongsan-si, 712-749,Koera.*
Phone/FAX: +81-53-810-3816/+81-53-810-4628 E-mail: [*]Soohyun@ynu.ac.kr
[2]*Center for Core Research Facilities, Deagu Gyeonbuk institute of Science & Technology, Sang-ri, Hyeonpung-myeon, Daseng-gun, Daegu, 711-873, Korea*
[3]*TANAKA Kikinzoku Kogyo K.K., 22, Wadai, Tsukuba, Ibaraki 300-4247, Japan*
E-mail: *soohyun@ynu.ac.kr

Ruthenium (Ru) thin films have been widely investigated in semiconductor device technologies, such as an electrode for the DRAM capacitor, a seed layer for Cu metallization, and a gate electrode on account of their low resistivity (Ru: ~7 μΩcm) and high chemical stability and high work function (Ru: 4.7 eV). Ru nanostructures are expected to be used in various systems including nonvolatile memory devices with Ru nano-crystals, the fabrication of nano-devices, and the formation of nano-catalysts. For these applications, the Ru film should be deposited with excellent step coverage and thickness uniformity. In these respects, atomic layer deposition (ALD) process can be a potential solution to prepare Ru thin film. In this study, Ru films were deposited by thermal ALD using a sequential supply of a new beta-diketonate Ru precursor with a high vapor pressure of 0.6 Torr at 100°C and O_2 or NH_3 molecules at the deposition temperature ranging from. In the case of ALD-Ru process using O_2 molecules, the deposition was performed between 225 and 310°C. The growth rate was little changed as ~ 0.08 nm/cycle between 250 and 275°C, indicating of the ALD temperature window. A very short incubation cycles of 14 was shown, indicating of the fast nucelation of the present ALD-Ru process. We also investigated Ru ALD process using NH_3 molecules as a potential non-oxidizing reactant. In this case, the deposition temperature should be increased above 300°C for depositing the film. The step coverages of both ALD-Ru films (Fig. 1) were excellent, approximately ~100% (using O_2 molecules) and 90% (using NH_3 molecules) over the trench structure (top opening width : 25nm) with the aspect ratio of ~4.5. The deposited Ru films have been evaluated as a bottom electrode of high-*k* MIM capacirot and a seed layer for Cu electroplating.

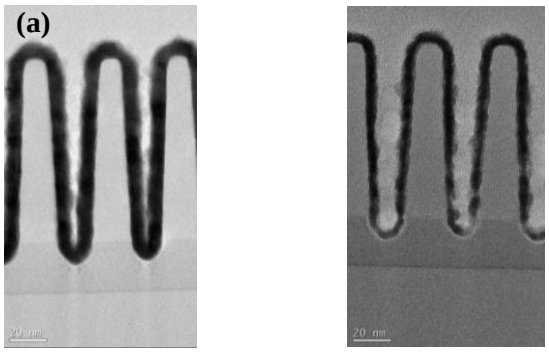

Fig 1. Step coverage of Ru film at (a) using O_2 molecules, (b) using NH_3 molecules

Acknowledgement

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Development of Yb silicide with low schottky barrier by forming epitaxial layer

Sekwon Na, Jun-gu Kang, Juyun Choi, Hyoungsub Kim and Hoo-jeong Lee
School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 440-746, Korea
E-mail : hlee@skku.edu

As the scale-down of complementary metal-oxide-semiconductor field-effect-transistors (CMOSFETs) continues, the contribution of the source/drain resistance becomes significant, which makes it a critical issue to find a novel contact formation scheme with low source/drain series/contact resistances [1]. Rare-earth metal (Er, Yb, etc) silicides have been noticed as a promising candidate for n-type channel transistors owing their low Schottky barrier heights on n-type Si (0.27-0.4eV) [2]. We explored the possibility of using ytterbium silicide as a contact material. The ytterbium was deposited using RF magnetron sputtering system and annealed using RTA to form ytterbium silicide. The formation of Yb silicides has been studied by transmission electron microscopy (TEM), X-ray diffractometer (XRD). In addition, the electrical characteristics of the diodes were measured using an HP semiconductor parameter analyzer (HP4145B). Upon annealing at a higher temperature, the crystalline $YbSi_{2-X}$ layer formed as a flat layer of a uniform thickness with epitaxial relation with the underlying Si lattice. This epitaxial silicide layer leads low schottky barrier height between Yb and Si. The high resolution electron micrograph image shows that the epitaxial $YbSi_{2-X}$ was formed fully at 500℃, which has the minimum SBH with 0.39eV.

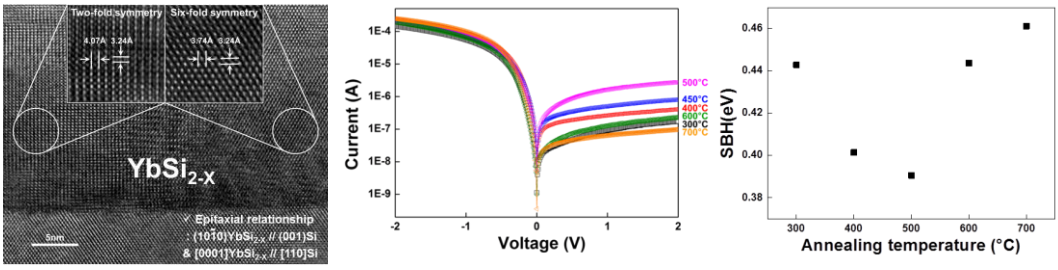

Fig 1. HRTEM image of epitaxial $YbSi_{2-X}$ and its electrical data

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Design of Power MOSFET merged poly-silicon Zener Diode for ESD protection

Sin Su Kyoung, Jong Min Geum, Eun Sik Jung, Ey Goo Kang, Tae young Kang and Man Young Sung*
Department of Electrical Engineering, Korea University, Seoul 136-701, Korea
Department of Electrical Engineering, FarEast university, Eumsunggun 369-700, Korea
Department of Electrical Engineering, PowerCubeSemi Co., Bucheoncity 421-742, Korea
E-mail : semicad@korea.ac.kr, keg@kdu.ac.kr, tykang@powercubesemi.com

ESD(Elctro Static Discharge) threats the Power MOSFET as same as IC chip. Conventional ESD protection is achieved from bypass external diode between gate and source on Power MOSFET. Because there is no area for protection diode on Power MOSFET.

As the smaller size of power module is needed, external ESD protection diode is needed into Power MOSFET. The merged ESD diode is made of using some poly silicon gate. ESD limiter voltage can be obtained by using zener diode design[1,2]

In this paper, we designed the merged ESD protection zener diode and get design characteristics by experiment. The zener breakdown voltage(BV) and gate resistance depends on boron dose and p type low doped area of zener diode. As the low doped area is larger, zener BV and gate resistance are larger. And the doping level of low doped area is lower, zener BV and gate resistance are lower.

The offered design parameter of merged ESD protection zener diode are meaningful, which the parameters can be applied to the power devices having merged ESD protection.

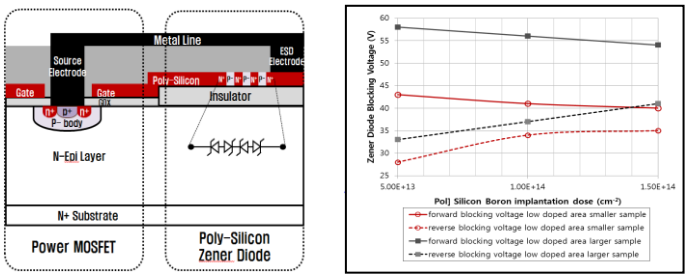

Fig 1 Merged poly-silicon diode structure and blocking voltage experimental results depending on boron implantation dose and low doped area size

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Metamaterial enhanced power transfer system for wireless charging applications

A. L. A. K. Ranaweera, Phu Ho Van Quang, Thuc Phi Duong, Byoung-Suk Lee, and Jong-Wook Lee
Department of Electronics and Radio Engineering, Kyung Hee University, Suwon 446-701, Korea
E-mail : jwlee@khu.ac.kr

In recent years, the potential of wireless power transfer (WPT) has attracted considerable interest for various applications in the areas of both home and industry [1]. To extend the power transfer to a mid-range distance, a new method that uses resonance coupling has recently been demonstrated [2]. We investigate a planar metamaterial slab for enhanced magnetic coupling in a resonator coupled wireless power transfer (WPT) system operating at around 6.5 MHz (Fig. 1). The metamaterial slab is realized using an array of three-turn spiral resonators (3T-SR). Fig. 2 shows the experimental setup used for WPT with the thin metamaterial slab placed between the Tx and Rx coils. Using the proposed approach, the measured peak efficiencies at 0.6 and 1.0 m are 74.0 and 50.1%, respectively (Fig.3). To realize a complete wireless charging system, we fabricate a multi-mode Li-Ion charger using 0.18 μm CMOS process (Fig.4).

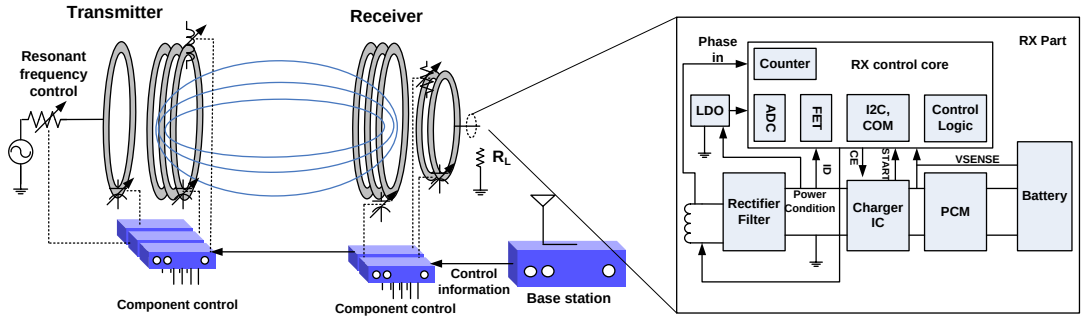

Fig 1. Wireless power charging system using resonance coupled power transfer

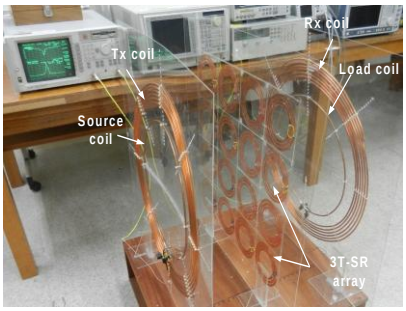

Fig 2. Fabricated transmitter

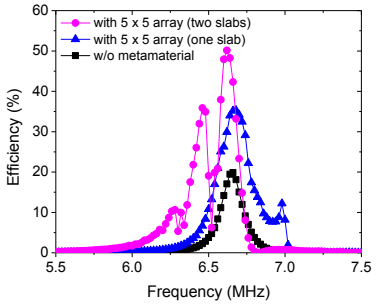

Fig 3. Measured result

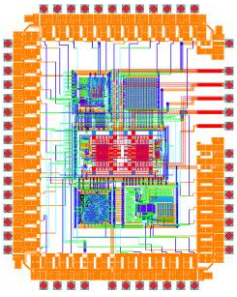

Fig 4. Charger IC

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Structural Effect of Triarylamine-based Multiple Functioned Coadsorbents for Highly Efficient Dye-Sensitized Solar Cells

Ban-seok You[a], In-Taek Choi[b], Won-Seok Choi[b], Hwan-Kyu Kim[b*] and Ji-Woon Yang[a*]

a. Department of Electronics and Information Engineering, Korea University, 2511 Sejong-ro, Sejong 339-700, Korea

b. Global GET-Future Laboratory, Department of Advanced Materials Chemistry, Korea University, 2511 Sejong-ro, Sejong 339-700, Korea.

E-mail : jyang@korea.ac.kr

Abstract

Triarylamine-based multiple-functioned coadsorbents containing a carboxylic acid acceptor linked by extended π-conjugation aryl linkers were newly designed and synthesized. Their structural effect on photophysical, electrochemical properties and Dye-Sensitized Solar Cells (DSSCs) performances were systematically investigated. As a result, The DSSCs based on HC-A4 (8.6%) shows better power conversion efficiency (PCE) than HC-A3 (7.7%), while HC-A5 (6.4%) not.

Introduction

DSSCs have received considerable attention as a new generation of sustainable photovoltaic devices because of their high incident solar light-to-electricity conversion efficiency, colorful and decorative nature, and low cost of production.[1] Our group developed the new coadsorbents (**HC-A3**) showing better PCE employed by hole conducting.[2] In this study, extended **π**-conjugation aryl linkers (**HC-A4** and **HC-A5**) are newly synthesized and applied to enhance the harvesting light at short wavelength with the increased UV-visible absorbance.

Experimental

HC-A4 and **HC-A5** are synthesized with triarylamine-based multiple-functioned coadsorbenst containing a carboxylic acid acceptor linked.[2] The molecular structures of **HC-A3**, **HC-A4** and **HC-A5** have low molecular weight Y-shaped structures with an anchorable carboxylic acid acceptor linked by various conjugated aryl moieties, such as phenylene, naphthalene and anthracene units (**Fig 2**). **Fig 3** shows the UV-vis absorption and emission of the three coadsorbents.

Fig 1 shows principle of DSSCs. FTO plates were cleaned in detergent solution, water and ethanol in an ultrasonic bath. The FTO substrates were immersed in 40 mM aqueous $TiCl_4$ solution at 70 ℃ for 30 min and washed with water and ethanol. A TiO_2 colloidal paste was screen-printed onto FTO/glass and sintered at 500 ℃ for 30 min in air. The TiO_2 electrodes were sintered at 500℃ for 30 min. Counter electrodes were prepared by coating with a drop of H_2PtCl_6 solution on an FTO plate and heating at 400℃ for 15 min. The dye-adsorbed TiO_2 photoanodes were assembled with Pt-coated FTO using a thermal adhesive film as a spacer to produce a sandwich-type cell. The hole was sealed with cover glass using Surlyn.

Results and Discussion

The photovoltaic properties of the DSSCs with **HC-A3**, **HC-A4**, or **HC-A5** only are summarized in **Table 1**. Among them, **HC-A4** showed the best cell performance because of its highest light harvesting effect at shorter wavelengths. The IPCE and *J-V* spectra for the DSSCs with **HC-A3**, **HC-A4**, and **HC-A5** alone are presented in the insets in **Fig 4.** The maximum IPCE of the **HC-A4**-based solar cell was slightly higher than that of **HC-A3** in the range from 300nm and 550nm. These results indicate that it has the better light harvesting effect at shorter wavelength regions for co-sensitization. However, **HC-A5** exhibited the lowest cell performance compared with the **HC-A3** and **HC-A4,** while its UV-visible spectra was broadened as shown in **Fig 3**. Lower electron injection efficiency into the TiO_2 CB from its higher dihedral angle was a possible reason as shown in **Fig 5.**[3] The DSSCs fabricated with the **NKX2677** dye and the new coadsorbents and photovoltaic performance were measured for comparison as shown **Fig 4**. In particular, **NKX2677/HC-A4** in the DSSCs, the J_{sc} and V_{oc} was significantly increased compared to the others. The larger J_{sc} was owing to the better light harvesting efficiency (**Fig 3 and Fig 4. (a)**), and the higher V_{oc} was due to increased recombination resistance (**Fig 6. (a)**). Electrochemical impedance spectroscopy (EIS) was performed in the dark under a forward bias of -0.62 V. **Fig 6. (b)** shows longer electron lifetime ($\tau_n = C \cdot R_{rec}$) in the DSSC with **NKX2677/HC-A4** (160.1 ms) than those with **NKX2677/HC-A3** (148.3 ms) and **NKX2677/HC-A5** (40.6 ms). [4]

Conclusions

We have designed and synthesized multi-functional coadsorbents with naphthalene and anthracene as an extended **π**-conjugated aryl unit. The DSSC with new coadsorbents (**HC-A4**) exhibited higher V_{oc} and J_{sc} values than **HC-A3**-based DSSCs.

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[3]. J. Yang, et.al., J. *Mater. Chem.* **2012**, 22, p.24356
[4]. J. Bisquert, et.al., *Phys. Chem. C*. **2009**, 113, p.17278

Table 1. Photovoltaic parameters of the DSSCs with different coadsorbents under AM 1.5 G (100 mW cm^{-2})

Device	J_{sc} /(mA cm^{-2})	V_{oc} /(mV)	FF (%)	η (%)
HC-A3	4.15	692	77.5	2.2
HC-A4	5.24	711	76.7	2.8
HC-A5	0.29	486	74.1	0.1
NKX2677	13.7	608	74.8	6.2
NKX2677 / HC-A3[2]	16.3	634	74.5	7.7
NKX2677 / HC-A4	17.4	664	74.2	8.6
NKX2677 / HC-A5	15.3	599	70.1	6.4

Performance of DSSCs was measured with a black metal mask (0.16 cm^2). Electrolyte: 0.6 M DMPII, 0.5 M TBP, 0.05 M I_2 and 0.1 M LiI in CH_3CN. NKX2677 dye concentration was 0.3 mM. **HC-A3**, **HC-A4** and **HC-A5** concentration was 7 mM. TiO_2 nanocrystalline particle size: 20 nm.

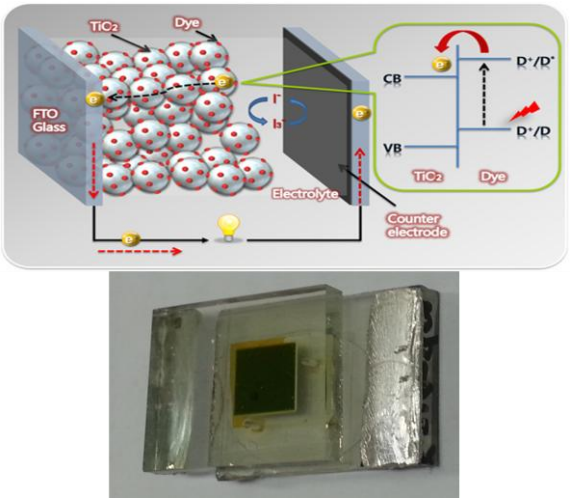


Figure 1. Operation principle of Dye-Sensitized Solar Cells

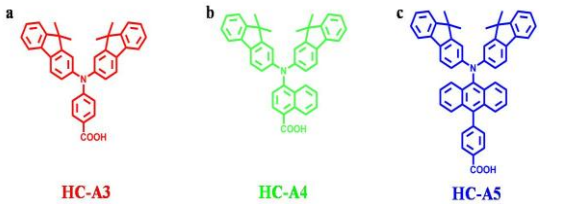


Figure 2. Molecular structures of (a) **HC-A3**, (b) **HC-A4**, (c) **HC-A5**.

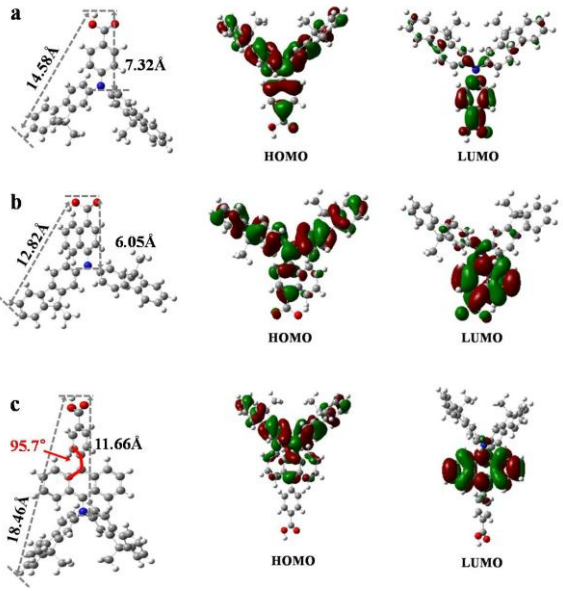


Figure 5. The optimized structures and the dihedral angles between the conjugated linker (a) **HC-A3**, (b) **HC-A4**, (c) **HC-A5**.

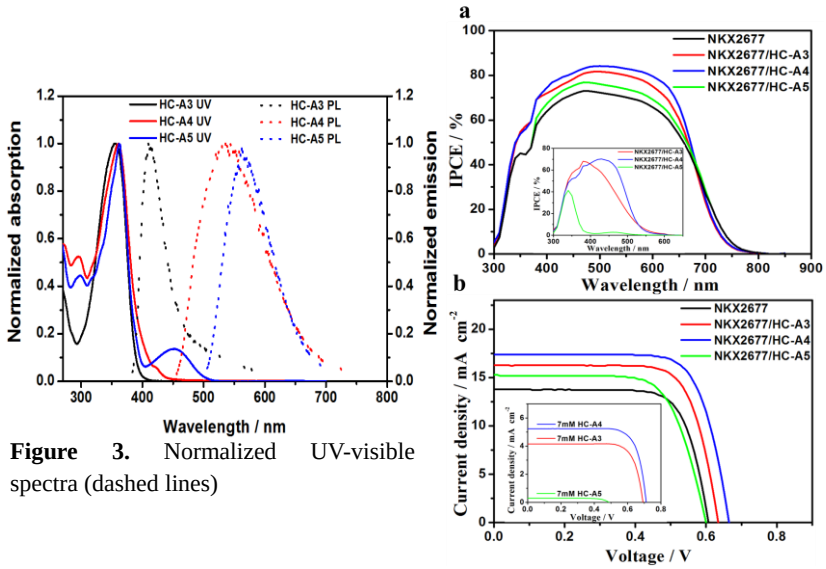


Figure 3. Normalized UV-visible absorption (solid lines) and emission spectra (dashed lines)

Figure 4. (a) IPCE action spectra and (b) *J–V* characteristics of the DSSCs

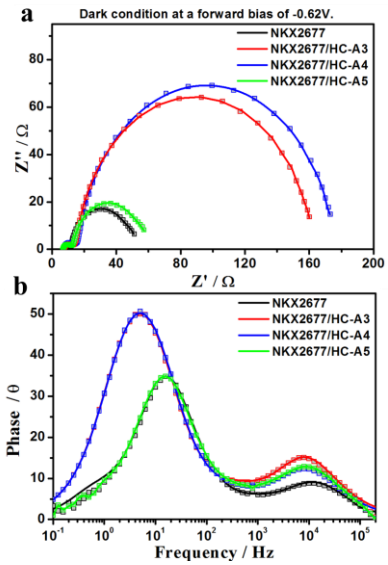


Figure 6. (a) Nyquist and (b) Bode phase plots from the EIS spectra for the DSSCs.

Performance Enhanced of Inverted Organic Solar Cells with a Ga-doped ZnO Electron Transport Layer Prepared using a Sol-Gel Method

Hye-Jeong Park, Kyung-Sik Shin, Gyu Cheol Yoon, and Sang-Woo Kim
School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 440-746, Korea
E-mail : kimsw1@skku.edu

Photovoltaic (PV) cells based on organic materials have limited PV performance because of short excitons diffusion length and low carrier mobility of organic materials. Hence, in order to improve the PV performance, inverted organic solar cells (IOSCs) with high electron mobility and transparent inorganic materials such as ZnO have been extensively investigated. The typical dopants that have been used to enhance the conductivity of ZnO are B, Al, In, Ga. Among them, Ga-doped ZnO (GZO) is more stable with respect to oxidation and moisture due to the greater electronegativity of Ga in comparison with Al. An introduction of Ga can increase free electron density by replacing the Zn atoms [1].

In the present work, we investigated the influence of the Ga-doping in the ZnO interlayer as an electron transport layer (ZnO ETL) on the nanoscale phase separation in the bulk heterojunction layer coated on the ETL. The short circuit current densities of IOSCs fabricated using a G-ETL got improved significantly in comparison to those of IOSCs fabricated with a P-ETL. The IOSCs fabricated with a 2at.% G-ETL demonstrated power conversion efficiencies of 3.51% (P3HT:PC_{60}BM) and 5.43% (PCDTBT:PC_{70}BM), which were higher than the power conversion efficiencies of 2.88% (P3HT:PC_{60}BM) and 4.90% (PCDTBT:PC_{70}BM) of the IOSCs fabricated with a P-ETL under simulated air mass 1.5 global full-sun illumination.

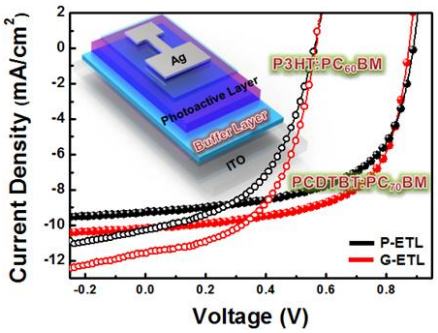


Fig 1. *J-V* characteristics of IOSCs fabricated with ZnO ETLs doped with different Ga contents

[1] A. K. K. Kyaw, X. W. Sun, C. Y. Jiang, G. Q. Lo, D. W. Zhao, and D. L. Kwong, Appl. Phys. Lett. 93, 221107 (2008).

Effect of MoO_X and TiO_X Nano-particle Layer on Lifetime Enhancement for PCDTBT:$PC_{71}BM$ Polymer Solar Cell

Jin-Seong Park[1,2], Seung-Wook Baek[1,2], Ji-Heon Kim[1,2], Jae-Hyoung Shim[1,2], Yun-Hyuk Ko[1,2], Gon-Sub Lee[2] and Jea-Gun Park[1,2]*

[1] *Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea*

[2] *Advanced Semiconductor Materials and Devices Development Center, Hanyang University, Seoul 133-791, Korea*

E-mail : parkjgL@hanyang.ac.kr

Many researches in polymer-solar-cells (PSC) have put a great effort to enhance thier lifetime. Replacement of materials with less influence from oxygen and humidity could be a solution to enhance lifetime of PSC. Poly(3,4-ethylenedioxythiophene):Poly(styrenesulfonate) (PEDOT:P-SS), Bathocuproine (BCP), widely used buffer layer material, could be vulnerable by oxygen and humidity. According to other researches, metal oxides such as Molybdenum Oxide (MoO_X) and Titanium Oxide (TiO_X) are appropriate candidates as a buffer layer material for high Power-Conversion-Efficiency (PCE).

Therefore, to confirm the effects of lifetime enhancement, we applied MoO_X as an anode buffer layer material and TiO_X as a cathode buffer layer material. We fabricated PSCs with the structure of Glass/Indium Tin Oxide (ITO)/Anode Buffer Layer/Poly[N-9'-heptadecanyl-2,7-carbazole-alt-5,5-(4',7'-di-2-thienyl-2',1',3'-benzothiadiazole)]:Phenyl-C71-butyric acid methyl ester (PCDTBT:$PC_{71}BM$)/Cathode Buffer Layer/Al. We observed that the PCE of PSC with MoO_X and TiO_X nano-particle layer was degraded by 7.01 % after ~165 hours. In contrast, PSC with the structure of Glass/ITO/PEDOT:PSS/PCDTBT:$PC_{71}BM$/Al lost photovoltaic performance in ~70 hours. The photovoltaic performance of PSC with MoO_X and TiO_X nano-particle layer is Open-Circuit Voltage (V_{OC}) of 0.803 V, Short-Circuit Current Density (J_{SC}) of 6.624 mA/cm^2 , Fill Factor (FF) of 61.93 % and PCE of 3.291 %. After 165 hours, V_{OC} and J_{SC} were degraded by 0.31 % and 7.06 %, respectively. We will report Effect of MoO_X and TiO_X Nano-particle Layer on Lifetime Enhancement for PCDTBT:$PC_{71}BM$ Polymer Solar Cell and its mechanism.

* This work was financially supported by the Brain Korea 21 Plus Program in 2013, Republic of Korea.

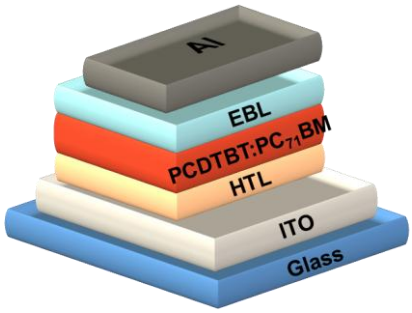


Fig 1. Structure of fabricated Polymer Solar Cells

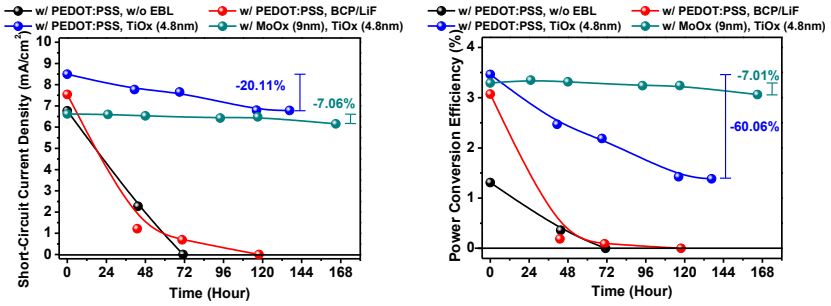


Fig 2. Short-Circuit Current Density and Power Conversion Efficiency of Polymer Solar Cells

5V input level shifter circuit for IGZO TFTs

KeeChan Park[a], HongKyun Lym[a], HwanSool Oh[a], JaeEun Pi[b], Chi-Sun Hwang[b], and Sang-Hee Ko Park[b]

[a]: *Department of Electronics Engineering, Konkuk University, Seoul 143-701, Korea*

[b]: *Oxide Electronics Research Team, ETRI, DaeJeon 305-700, Korea*

E-mail : keechan@konkuk.ac.kr

In-Ga-Zn-O(IGZO) thin-film transistors (TFT) exhibit high performance and low process cost compared with silicon-based TFTs. However it is difficult to implement the display-driving circuitry using the IGZO TFTs because only n-channel TFT is available and the threshold voltage (V_T) tends to vary and even becomes negative.

We report a IGZO TFT-based level shifter circuit that operates with 5V input signals as shown in Fig. 1. Spice simulation results in Fig. 2 show that the proposed level shifter works successfully for the V_T range from -2V to +1V and the rise time is only 2μsec when the V_T is -1V or 0V. The measured result of the fabricated sample exhibits the rise time of 1μsec in Fig. 2 (b).

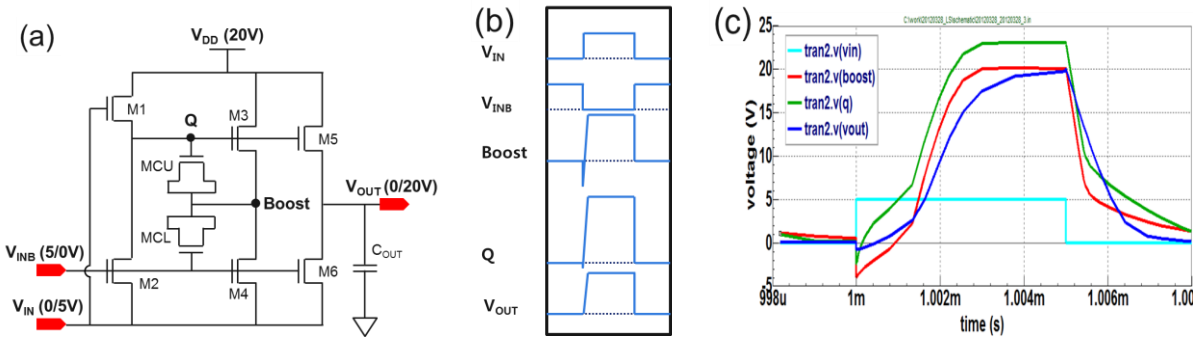


Fig 1. (a) Level shifter circuit. (b) Node voltage waveform. (c) Spice simulation result for V_T = 0V.

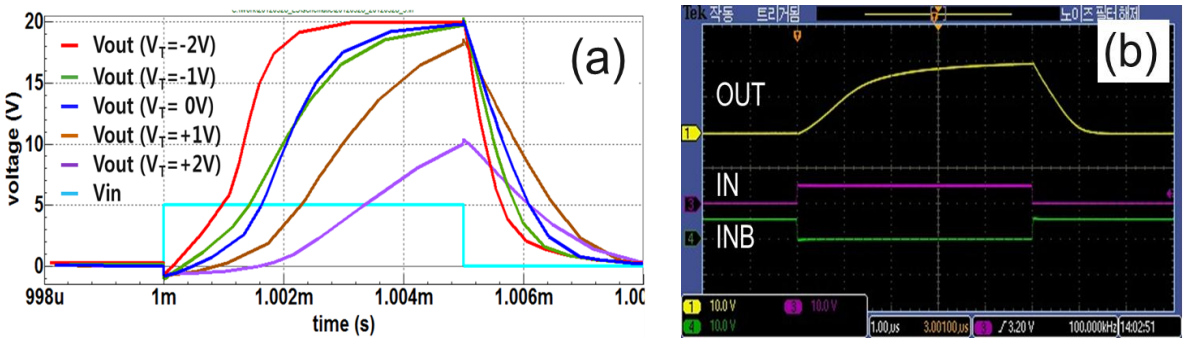


Fig 2. (a) Simulation results for various V_Ts. (b) Fabrication result.

Scan Driver Considering Stress Characteristics of a-IGZO TFT for FPDs

Jin-Yeon Kim, Seong-Jin Ahn, Jun-Seok Na, Seong-Kwan Hong, and Oh-Kyong Kwon
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : okwon@hanyang.ac.kr

An amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) has gained attention as a next-generation backplane TFT in flat-panel displays (FPDs) because of its high mobility and good uniformity [1]. However, a-IGZO TFT has electrical instability on gate bias stress and high current stress, which cause the threshold voltage shift(ΔV_{th}) of a-IGZO TFT [2]. When the integrated scan driver is designed on display panel using a-IGZO TFTs, it is important to consider the characteristics on the aforementioned stresses. Especially, pull-down TFTs in the output stage are exposed to positive ΔV_{th} because high driving current flows through the pull-down TFTs to discharge the output nodes and the positive DC bias is applied to the gate terminals. In this study, we propose a scan driver considering on gate bias stress and high current stress. Fig 1 (a) shows the schematic diagram of the proposed scan driver. The proposed scan driver reduces the stress time and degree of the pull-down TFTs (T4, T5) in the output stage because the gate terminals of them are biased to AC instead of positive DC and the high voltage level of AC bias is less than VDD. The target specifications of the proposed scan driver include the panel resolution of extended graphics array (WQXGA, 2560 × 1600), the frame frequency of 60 Hz, the capacitive load of 120 pF, and the resistive load of 6.6 kΩ. As shown in fig 1(b), the proposed scan driver successfully generates the output signals even though ΔV_{th} is varied from -4.0 V to +4.0 V.

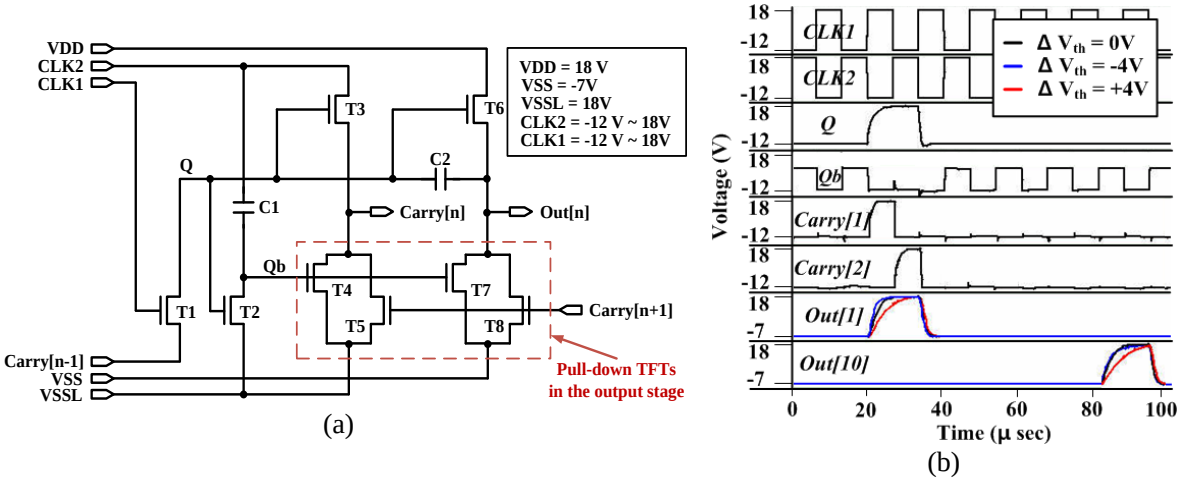


Fig 1. (a) Schematic diagram and (b) simulated waveforms of the proposed scan driver

[1] M. J. Gadre, and T. L. Alford, Appl. Phys. Lett, 99, 051901-1(2011).
[2] M. Mativenga, S. Hong, and J. Jang, Appl. Phys. Lett., 102, 023503-1(2013).

Compensation of missing pixel for RGBz CMOS image sensor

Joonho Lee, Daekwan Kim, and Taechan Kim
AIT, Image Development Team, S.LSI, Samsung Elec., Korea
E-mail : joonhov.lee@samsung.com

이미지 센서의 기술이 발달하면서 ToF 방식을 이용한 거리를 측정하는 센서가 발표되었다[1,2]. 그러나 기존에 발표되었던 거리를 측정하는 센서는 그 구조로 인해서 Color Image 를 표현하지 못한다. 그러나 Color 와 거리를 동시에 표현하는 문제를 해결하기 위해 1.5M color pixel & LineZ 방식을 이용하여 Color 와 거리를 동시에 표현할 수 있는 센서가 발표됐다[3]. 그러나 Color 와 거리를 동시에 표현하기 위한 Color and Line Z pixel Array 방식(Fig 1)에서의 LineZ 때문에 Color Image 를 복원하는 과정에서 Data 의 손실이 발생하게 된다. 본 논문에서는 광학 기구를 이용하여 Image 를 De-focus 하고 De-focus 된 Missed pixel 의 Image data 를 주변 부 pixel 로 전달하여(Fig 2) 잃어 버린 Image Data 를 복원하였다.

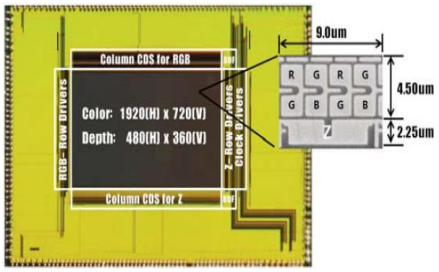


Fig 1. Chip layout of the 1.5Mpixel RGBz sensor

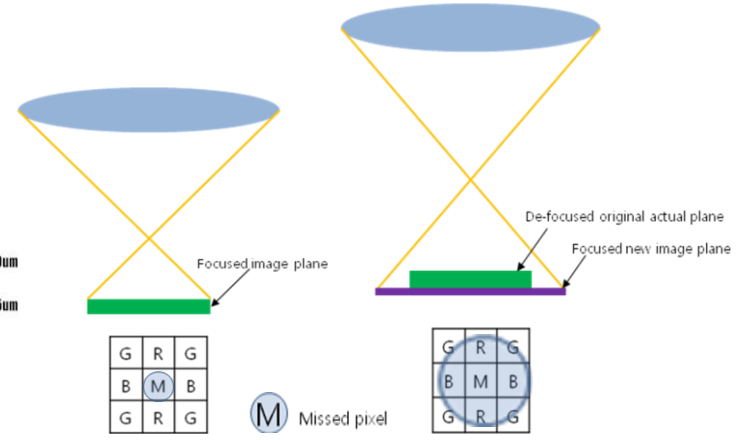


Fig 2. Using De-focus image on missed pixel

[1] R. Miyagawa and T. Kanade, “CCD-based range finding sensor”, IEEE Trans.Electron Devices, vol.44, no. 10, pp. 1648-1652, 1997.
[2] R. Lange, et al. “Demodulation Pixels in CCD and CMOS Technologies for Time-of-Flight Ranging”, Proc, of SPIE, vol. 3965A, pp. 177, 2000.
[3] Wonjoo Kim, Yibing, Ilia Ovsiannikov, SeungHoon Lee, Yoondong Park, Chihee Chung, Eric Fosum, ISSCC 2012, Session 22, Image Sensors, 22.7.

Effectively Novel Color Emphasis for Image Enhancement using Image-dependent Method

Hosang Cho, Sungmok Lee, Chang-Wan Kim, and Bongsoon Kang
Department of Electronic Engineering, Dong-A University, Busan 604-714, Korea
E-mail : bongsoon@dau.ac.kr

In order to enhance an HD video containing low luminance regions, every single video frame needs to be processed with regard to brightness, contrast, and color correction. several system implementation costs are required, including frame memory buffers, increasing complexity, computational time delay, and the size of system-on-chip design. In the paper, we propose a cost-effective image enhancement algorithm under low luminance conditions that achieves both luminance improvement and color emphasis in a low-complexity fashion. In order to avoid a tradeoff between global and local characteristics of luminance from a complexity perspective, the addition model is employed to achieve the intensity range limited luminance enhancement that prevents decreasing contrast and controls adaptive gain [1]. The color emphasis extends the distribution of the chrominance information (Cb/Cr) toward the saturation adjustment. Using the intensity range limited luminance enhancement, the proposed method takes advantage of low complexity. The proposed algorithm was developed in the Windows Program using the OpenCV, and the verified the performance by real-time. The proposed visibility enhancement system is implemented by Verilog-HDL.

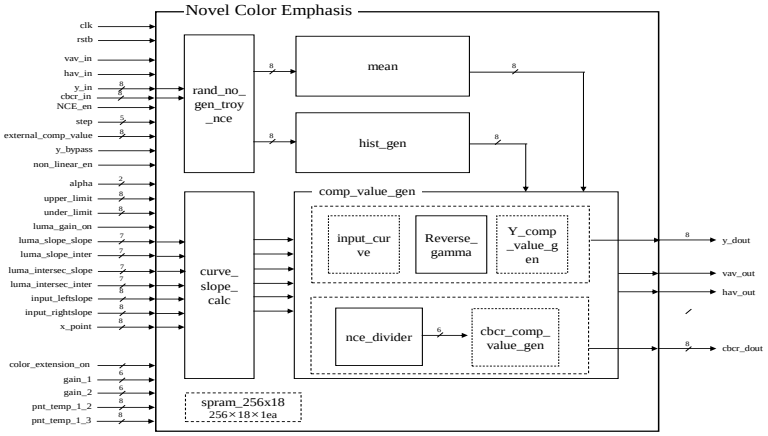


Fig 1. Block diagram of the proposed algorithm

[1] S. Lee, J. Yang, W. Choi, H. Yang and B. Kang, The Korea Institute of Signal Processing and Systems, in press (2009).

Oxide TFT-based shift register circuit tolerant of clock duty variation

JaeWon Lee, SangYeon Kim, SeungO Kim, HwanSool Oh, and KeeChan Park
Department of Electronics Engineering, Konkuk University, Seoul 143-701, Korea
E-mail : keechan@konkuk.ac.kr

Oxide thin-film transistors (TFT) attract a lot of attention for display applications due to their high performance and low process cost. However it is difficult to integrate the driving circuit using the oxide TFTs because the threshold voltage (V_T) tends to vary and even becomes negative. We propose a new oxide TFT-based shift register circuit that works over wide V_T range and is tolerant of clock duty variation. The proposed circuit employs four clock signals and the low level voltage of two clocks is lower than that of the other two clocks in order to turn off the TFTs completely even though they have negative V_Ts. As the sizes of the display panels increase, clock waveform of the shift register is distorted due to large RC delay. Our new circuit work successfully even though the clock duty ratio changes by such distortion. Fig 2 shows the operation results for 50% and 40% duty clock signals.

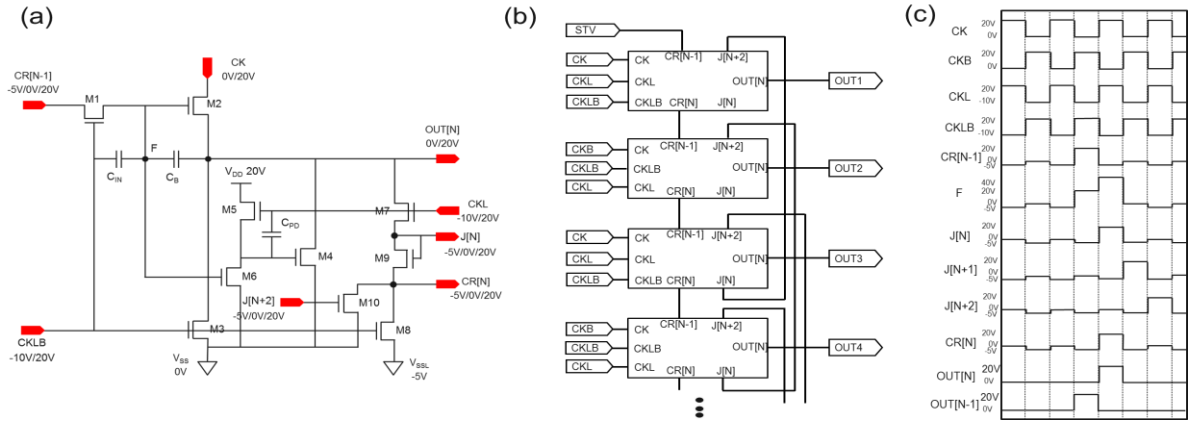


Fig 1. (a) Shift register unit circuit. (b) Block diagram of shift register. (c) Timing diagram.

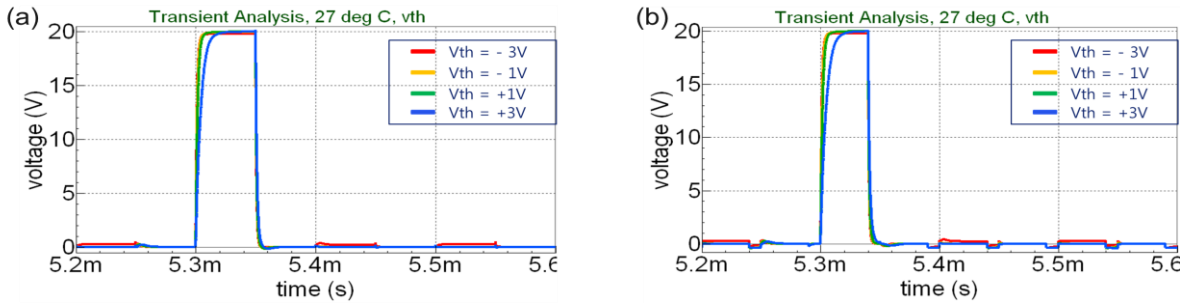


Fig 2. (a) Output voltages for 50% duty ratio. (b) Output voltages for 40% duty ratio.

Area-Efficient 20-Gbps Optical Receiver Circuit in 65-nm CMOS Technology

Hyun-Yong Jung, Jin-Sung Youn, and Woo-Young Choi*
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea
*E-mail : wchoi@yonsei.ac.kr

Recently, the demands for high-speed optical receivers with small chip-area are increasing for optical interconnect applications. The popular technique of circuit bandwidth enhancement with passive inductors require a large chip area and may not be suitable for certain applications with tight cost requirements [1-2]. We investigate the maximum receiver circuit bandwidth possible within standard 65-nm CMOS without using passive inductors. The receiver circuit is composed of transimpedance amplifier (TIA) with DC-balancing buffer, post amplifier (PA), and output buffer. The TIA is designed in the shunt-feedback configuration with active feedback. The PA is a 6-stage differential amplifier with interleaved active feedback. The measured transimpedance gain and 3-dB bandwidth of the fabricated optical receiver circuit are 74.5 dBΩ and 12 GHz, respectively. With the fabricated receiver circuit, 20-Gb/s $2^{31}-1$ electrical pseudo-random bit sequence data are successfully received with the bit-error rate less than 10^{-12}. The receiver circuit has a small chip area of 0.13 mm × 0.3 mm. The power consumption excluding the output buffer is 120 mW with 1.2-V supply voltage.

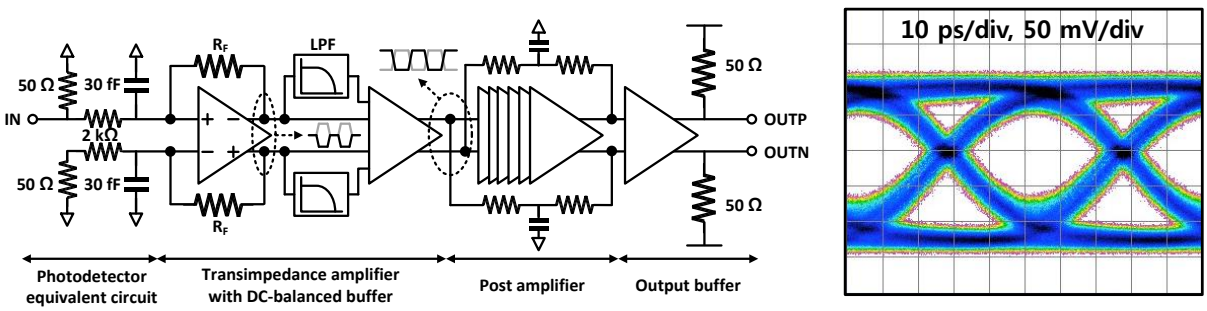


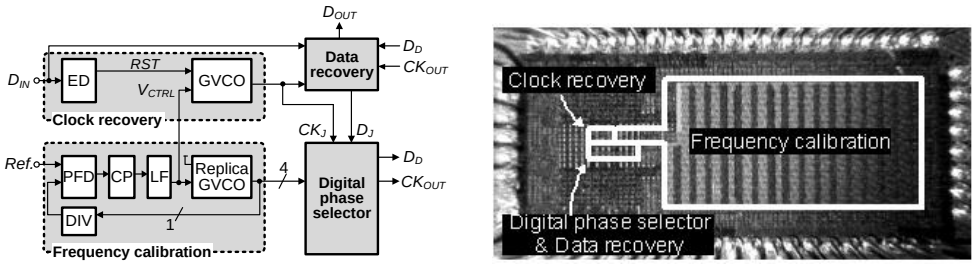
Fig 1. Block diagram and 20-Gbps eye diagram of the optical receiver circuit.

[1] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, and H. Jäckel, "A low-power 20-GHz 52-dBΩ transimpedance amplifier in 80-nm CMOS," J. Solid-State Circuits, vol. 39, no. 6, pp. 885-894 (2004).
[2] T. Takemoto, F. Yuki, H. Yamashita, Y. Lee, T. Saito, S. Tsuji, and S. Nishimura, "A compact 4 x 25-Gb/s 2.0 mW/Gb/s CMOS-based optical receiver for board-to-board interconnects," J. Lightwave Tech., vol. 28, pp. 3343-3350 (2010).

입력 지터 감소 기법을 적용한 2.5 Gb/s BMCDR 회로 설계

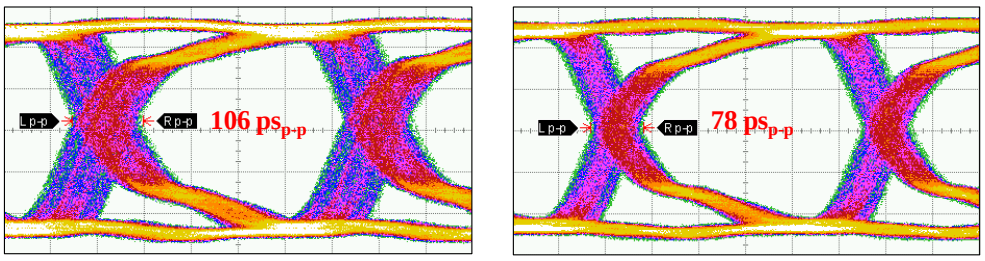
정재훈 [1], 최정환 [1], 백광현 [2]
삼성전자 메모리사업부 DRAM 설계팀 [1]
중앙대학교 전자전기공학부 [2]
E-mail : jh2013.jung@samsung.com

본 논문에서는 XGPON(10 Gigabit-capable Passive Optical Network) 시스템에 적용되는 2.5 Gb/s 의 입력 데이터율을 가지는 BMCDR(Burst-Mode Clock and Data Recovery)을 제안한다. 기존 GVCO(Gated Voltage Controlled Oscillator) 기반 BMCDR 의 무궤한(Non feedback) 위상 추적(Phase tracking) 방식에 기인한 복원 클럭과 데이터의 지터(Jiiter)를 감소시키기 위하여 주파수 보정회로(Freqeuncy calibration circuit)의 다중 위상 출력을 사용하는 설계 기법이 적용되었다. 제안된 BMCDR 은 55 nm CMOS 공정을 사용하여 설계되었으며 루프필터(Loop filter) 및 PAD 를 포함한 전체 설계 면적은 2 mm^2 이고 I/O 회로를 제외한 전력 소모량은 24 mW 이다. 2.5 Gb/s 의 2^{31} PRBS(Pseudo Random Binary Sequince) 데이터 입력 시 BER(Bit Error Ratio)은 2^{-10} 이하로 측정되었으며, 0.2 UI(80 ps) 입력 지터 인가 시 최종 복원 데이터의 rms 와 peak-to-peak 지터는 각각 17 ps 와 78 ps 로 측정되어 제안된 지터 감소 기법이 적용되지 않은 출력과 비교 시 약 26 %의 지터 성능 향상을 달성하였다.



(a) (b)

그림 1. 제안된 BMCDR (a) 구조도 (b) Die photo



(a) (b)

그림 2. 복원 데이터 Eye-diagram (a) 기존 구조 (b) 지터 감소 기법 적용 구조

A single-stage 40dB-Linear Digitally-Controlled Variable Gain Amplifier for Ultrasound Analog Front End

Seong-Eun Cho[1], Ji-Yong Um[2], Byungsub Kim[2], Jae-Yoon Sim[2], and Hong-June Park[1,2]
[1]*WCU (Division of IT Convergence Engineering),*
[2]*Department of Electronic and Electrical Engineering,*
Pohang University of Science and Technology (POSTECH)
E-mail : saisti@postech.ac.kr

This paper presents a variable gain amplifier(VGA) for an analog front-end(AFE) of ultrasound imaging machine. The VGA receives an echo signal from LNA, and amplifies the received echo signal for time-gain compensation. The conventional VGAs [1-2] with an open-loop topology cannot cover more than 20dB range with a single stage. Also, they consume high power and have a small output swing at the highest gain. The proposed VGA controls 40dB voltage gain in a single stage, and has a large output swing. The VGA has a closed-loop topology, and consists of an op-amp, a non-binary-weighted capacitor array, and a gain-control block. The gain of VGA is controlled by the capacitance ratio of input and feedback capacitors connected to an op-amp. The non-binary-weighted capacitor array is used to control the capacitance values of input and feedback capacitors. This non-binary-weighted capacitor array reduces the required number of capacitors and the complexity of the gain-control block. Also, the power consumption of VGA is almost constant for the entire range of gain, in contrast with those of the conventional open-loop VGAs [1-2]. The proposed VGA has been designed by using a 0.35um CMOS process. The VGA consumes 1.9mW with a 3.3V supply. In the post-layout simulation, HD3 of -100.9 dB is achieved for the output voltage swing of 1 Vpp. The linear-in-dB gain range is [-14, 25] dB with 16 steps. The maximum gain error and the bandwidth of VGA are 1.5 dB and [1.5, 4.5] MHz, respectively.

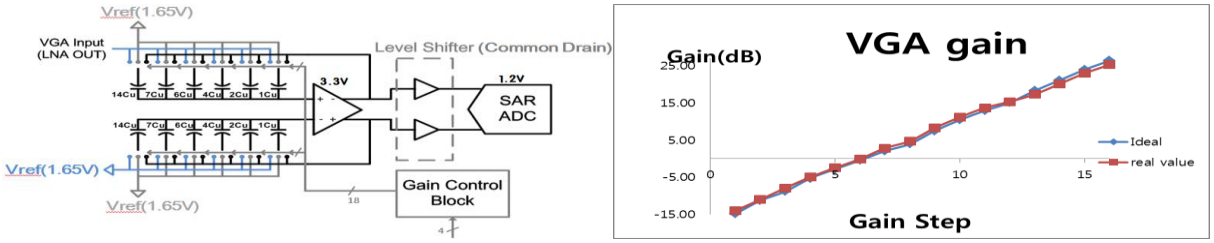


Fig 1. Circuit diagram and its gain data

[1] H. H. Nguyen, et al., "A High-Linearity Low-Noise Reconfiguration Based Programmable Gain Amplifier," European Solid State Circuits Conference, pp. 166-169, September 2010
[2] H. H. Nguyen, et al., "84 dB 5.2mA digitally-controlled variable gain amplifier", Electron. Lett., 2008, 44, (5), pp. 344-345

Constant Off-Time Control with Time Calibration Method for Buck Converter

Haneul Kim, Kyoungjin Lee, Jehyung Yoon, Hyoung-Seok Oh, and Byeong-Ha Park
Power Device Development Team, System LSI Division, Samsung Electronics Co., Ltd.
E-mail : haneule.kim@samsung.com

The dc-dc converters are popular in battery powered devices like lab top, cellular phones, etc., because of high efficiency, which is critical for extended battery life. And it is well-known that constant off-time control scheme has advantages such as fast response time and easy of compensation compared to the fixed frequency modulator [1]. However, it is difficult to generate a constant time regardless of process variations as well as supply fluctuation. Previously the phase frequency detector (PFD) was utilized to produce a constant off-time but there were still varying parameters to be calibrated such as current mirror mismatch, resistor and capacitor variation, and offset of amplifier [2]. This paper proposes a novel off-time controller (Toff) with auto-calibration scheme that cancels out the above variations related. The effectiveness of proposed controller was confirmed in PFM mode operation of buck-converter fabricated on 0.13 m CMOS process. The error rate has been measured as lower 4%.

BandgapEN_CALFREQ_ON_DUTYIBGRVREFCOMPOUT(a) Block diagram of the TOFF Cal_CodeProcess variationTfrequencyVREFVRAMPCOMPOUTCal_CodeCal_okToffCal_Completion(b) Time diagram of the TOFF

Fig 1. Block diagram & time diagram of the proposed Toff

400ns (0.25%)1.05VToff Target = 401nsVOUTLXInductor current(a) Inductor current byTOFF at Vout 1.05V 690ns (1.98%)0.8VToff Target = 704ns(b) Inductor current by TOFF at Vout 0.8V VOUTLXInductor current(c) Inductor current by TOFF at Vout 1.575V 275ns (3.27%)1.575VToff Target = 266nsVOUTLXInductor current

Fig 2. Measured off-time (Toff) at various operation cases where Toff is auto-calibrated to a predefined target value in accordance with output voltage change

[1] Ridley R B, “A New Continuous-Time Model for Current-Mode control with Constant Frequency, Constant On-Time, and Constant Off-Time, in CCM and DCM”, *IEEE PESC*, pp.382-389, 1990.

[2] L. Cheng, Z. Hong, “A Constant Off-time Controlled Boost Converter with Adaptive Current Sensing Technique”, *IEEE ESSCIRC*, pp. 443-446, 2011.

A 25-Gb/s Quarter-Rate CDR in 65-nm CMOS technology

Dae-Hyun Kwon and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : kwonkkun@yonsei.ac.kr

Clock and data recovery circuits (CDR) are widely used in high-speed interface systems for restoring data and clock signals from noisy and asynchronous signals. As the required data rate for many applications is getting higher, CDR circuits with the full-rate clock face speed limitations and multiphase CDR circuits can be a better solution [1,2] as it allows easier implementation and provide deserialized out data. This paper reports a 25-Gb/s qurater-rate CDR circuit with quarter-rate clocks implemented in 65-nm CMOS. It is composed of phase detectors (PDs), charge-pumps (CPs), off-chip loop filter, and voltage controlled oscillator (VCO). All circuit blocks are designed in CMOS logic except CPs in order to minimize power consumption. CPs are designed in fully-diffrential topology for enhancing the operation speed, which prevents dithering of control voltage. Fig. 1 below shows the block diagram of our CDR and the eye-diagram of one of four 6.25-Gb/s recovered data when 25-Gb/s PRBS 2^{31}-1 data are introduced into our CDR bonded on FR4 PCB. The bit-error rate is less than 10^{-12} and the measured peak-to-peak jitter is 28.3 ps. It consumes 40-mW excluding output buffers.

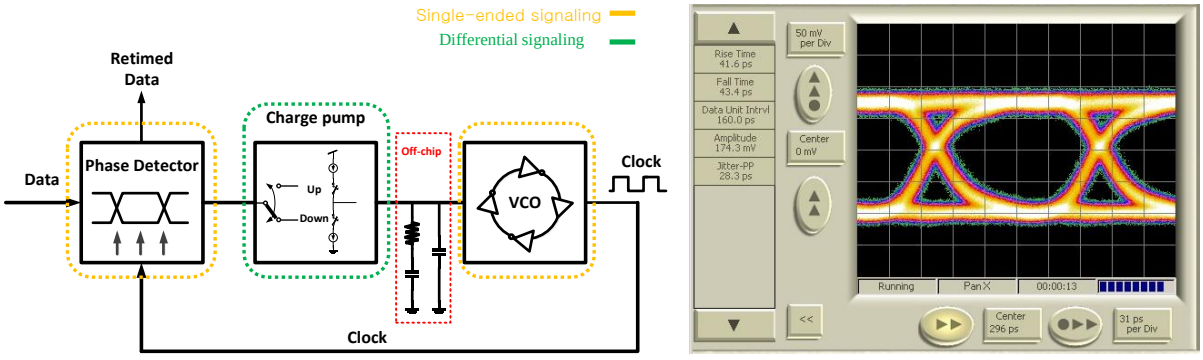


Fig 1. Block diagram of CDR and the measured eye-diagram of retimed data

[1] Jri Lee, and Behzad Razavi, IEEE J.Solid-State Circuits (2003), VOL. 38, NO. 12
[2] Jeong-Kyoum Kim, Jaeha Kim, Gyudong Kim, and Deog-Kyoon Jeong, IEEE J.Solid-State Circuits (2009), VOL. 55, NO. 5

A multi-channel 1-Gb/s/ch inverter transimpedance amplifier array with replica in 0.18μm CMOS

Hanbyul Choi, Xiao Ying, Seung-Hoon Kim, and Sung Min Park
Department of Electronics Engineering, Ewha Womans University, Seoul 120-750, Korea
E-mail : choihan0725@naver.com, smpark@ewha.ac.kr

Recently, the parallel optical interconnects have reemerged as an attractive solution for the applications of short-range digital links such as HDMI, DVI, board-to-board interconnections, etc [1]. Also, the demands utilizing the parallel optical interconnection have been rapidly grown for distance measurments as an immiment world-wide market, i.e. LADAR systems in unmanned vehicles for three-dimensional image processing.

This paper presents a gigabit multi-channel linear transimpedance amplifier(TIA) array which exploits the inverter input configuration for panoramic scan LADAR systems. It employs a replica to avoid large passive low-pass filter and hence smaller chip area [2]. The post-layout simulations of the inverter TIA with replica in 0.18μm CMOS demonstrate the transimpedance gain of 73.4dBΩ, the bandwidth of 926MHz with 0.62dB peaking around the -3dB frequency, the noise spectral density of 8.96pA/sqrt(Hz) corresponding to -25dBm sensitivity for 10^{-12} BER and 0.6A/W responsivity, the signal-to-crosstalk ratio of 38.06dB, and the power dissipation of 26.1mW from a single 1.8-V supply.

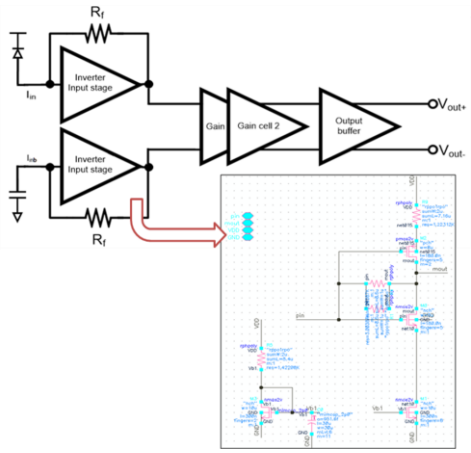


Figure1. Schematic of INVTIA

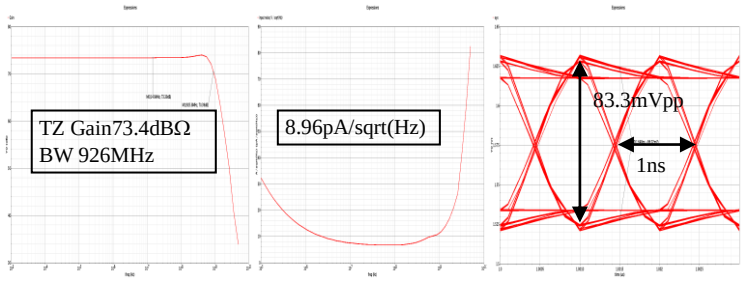


Figure2. Post-layout simulation results

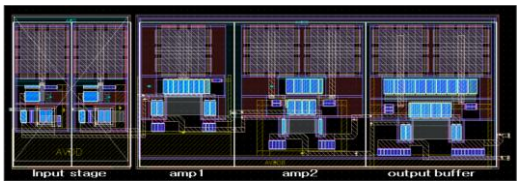


Figure3. Layout of INVTIA

[1] J. Lee et al., "A 2.5-Gb/s CMOS Optical Receiver for Active Optical HDMI Cable Applications", *SoC conference*, (2012).
[2] S. G. Kim et al., "A 1.8Gb/s/ch 10mW/ch -23dB Crosstalk Eight-Channel Transimpedance Amplifier Array for LADAR Systems", *IEEE ISOCC*, in press (2013).

Two-level cache organization for a merge mode prediction in a hardware-based HEVC encoder

Tae Sung Kim, Hyuk-Jae Lee and *Chae Eun Rhee
Department of Electrical Engineering and Computer Science, Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-747, Korea
**Department of Information and Communication Engineering, Inha University, Incheon 402-751, Korea*
E-mail : chae.rhee@inha.ac.kr

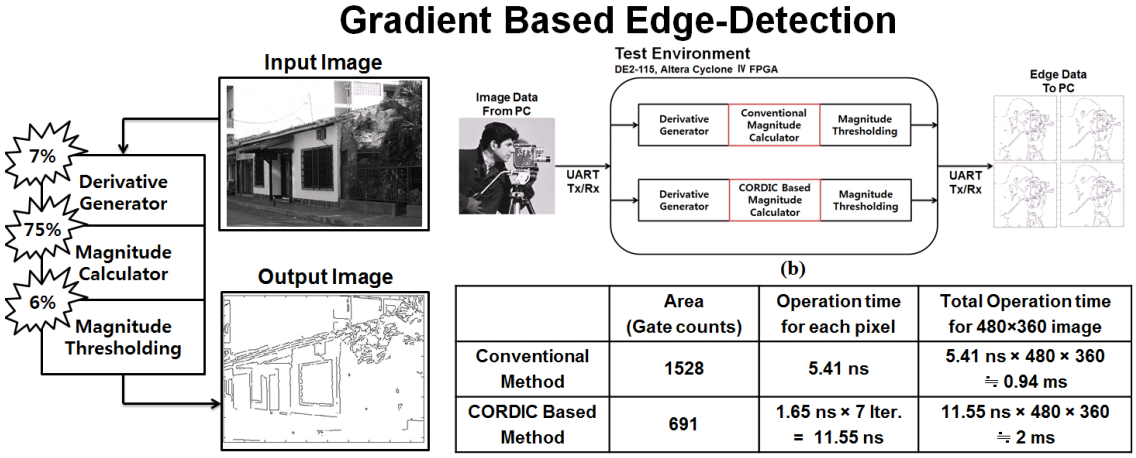
The merge mode is one of new features of High Efficiency Video Coding (HEVC). The main purpose of a merge mode is to find out neighboring blocks which can share the motion vector (MV) with the current block [1]. If the current block is determined as a merge mode, MV information does not have to be transferred to decoder side. Thus, a bitrate is significantly reduced and the coding efficiency is improved. The most intensive computation of a merge mode prediction comes from motion compensation (MC). For each block, the MC should be performed for maximum five candidates. One difficulty is that the amount of required reference data are very large due to the various block sizes and candidates. The other is that the MV of each candidate is inconsistent and unpredictable. Thus, it is hard to pre-fetch and there are not many chances to reuse data. Due to the characteristics of reference data for a merge mode prediction, the bottleneck for the parallel processing, especially to support high-resolution videos, is not computational complexity but data loading. This paper proposes a two-level cache organization. For the level 1 cache, big size memory is used and shared with the motion estimation (ME) module. Level 2 cache is just for the merge mode module and loads the required data from level 1 cache. The merge mode module can access to level 1 and 2 caches, separately or together. Even if level 2 cache has all required data, a merge mode module is allowed to access to both caches depending on circumstances. This inter-level cache access makes the available data bandwidth flexible. When the amount of reference data which should be loaded at one time is very large, the data width is extended by combining the data width of each cache. When the required data are placed in different memory addresses, two caches act like a multi-port memory. Simulation results show that the merge mode processing time is reduced significantly with a small hardware overhead.

[1] P. Helle, S. Oudin, B. Bross, D. Marpe, M. Bici, K. Ugur, J. Jung, G. Clare, T. Wiegand, IEEE Trans. Circuits Syst. Video Technol. 22, 1720 (2012).

Hardware Optimization for Low Complexity Edge Detection

Juseong Lee and Jongsun Park
School of Electrical Engineering, Korea University, Seoul 136-713, Korea
E-mail : juseong_lee@korea.ac.kr

최근 스마트 기기의 보급화로 인해 사진 및 동영상에서 윤곽선과 같은 특징 정보를 이용한 물체 인식, 차선 인식 등 인식 기술의 응용 분야가 활성화 되고 있다. 윤곽선 정보는 다양한 영상처리 알고리즘의 전처리 과정에 필수적으로 사용되어 여러 알고리즘이 개발되고 있다[1]. Fig 1. (a)와 같이 기본적인 Gradient 기반 윤곽선 검출 하드웨어가 구성되는데 전체 하드웨어 면적에서 Magnitude 연산모듈이 전체 면적의 75%를 차지하는 것을 확인하였다. 이 모듈은 윤곽선 검출을 위한 다양한 알고리즘에 필수적으로 쓰이기 때문에 하드웨어 복잡도를 줄이는 것이 필요하다. 따라서, 본 논문에서는 CORDIC(COordinate Rotational Digital Computer) 알고리즘을 이용하여 Magnitude 연산모듈의 최적화를 통한 저 면적 윤곽선 검출기를 제안한다. CORDIC 은 삼각함수를 비롯한 여러 초월함수 계산을 효율적으로 할 수 있는 연산 기술로 Shifter 와 Adder 만을 이용하여 벡터회전 및 Magnitude 같은 복잡한 연산을 간단한 하드웨어로 할 수 있어 벡터연산을 기반으로 하는 다양한 분야에 활용되고 있다[2]. Fig 1. (b)에서 설계검증을 위해 FPGA 와 PC 간 직렬 통신으로 테스트 환경을 구축하여 성능검증을 진행하였다. 그 결과 실시간으로 영상 데이터를 입력했을 때 두 모듈 모두 정상 동작 하며 실시간 동작이 가능한 것을 확인하였다. 회로 합성 결과 Fig 1. (c)의 결과와 같이 CORDID 기반 Magnitude 연산 모듈은 55% 면적 감소의 효과와 약 2 배의 연산시간 증가가 있었다. 하지만, 설계된 CORDIC 기반 방법의 경우 480×360 해상도의 영상 데이터당 총 2ms 의 연산시간이 필요하므로 30 FPS(Frame Per Second)를 만족한다. 이는 실시간 동작이 가능한 인식 기술에 실제로 적용 가능함을 나타내는 점이다. 본 논문의 결과를 토대로 이후 다양한 알고리즘의 저 면적 설계를 위해 CORDIC 기반 Magnitude 연산이 적용 될 수 있다.



	Area (Gate counts)	Operation time for each pixel	Total Operation time for 480×360 image
Conventional Method	1528	5.41 ns	5.41 ns × 480 × 360 ≒ 0.94 ms
CORDIC Based Method	691	1.65 ns × 7 Iter. = 11.55 ns	11.55 ns × 480 × 360 ≒ 2 ms

(c)

Fig 1. Gradient Based Edge-Detection Hardware (a) Block Diagram and Complexity Analysis, (b) Test Environment, (c) Area & Performance Comparison Table

[1] Jongho Choi, Kwangjin Ko and Dongil Han, “Hardware Design and Implementation of Advanced Edge-Dection engine based on Canny Edge Filter for Robustness to Quantization Noise,” KHCI Conference, pp.582-584, 2011.1
[2] J. E. Volder, “The CORDIC trigonometric Computing technique,” IRE Trans. Electron. Computers, Vol. 8, pp.330-334, Sept. 1959.

NAND Flash Memory Controller using Multi-Rate BCH Codes

Kijun Lee, Sejin Lim, and Jun Jin Kong
Memory Division, SAMSUNG ELECTRONICS, Hwasung City, Korea
E-mail : {kijuni.lee, sejin08.lim, jjkong}@samsung.com

Bose-Chaudhuri-Hocquenghem(BCH) code 는 NAND Flash memory 용 controller 에 널리 이용되는 error correcting code(ECC)이다. NAND Flash memory 용 controller 가 제품별/세대별 서로 다른 NAND Flash momory 의 신뢰성을 보장하거나, 신뢰성 별 데이터 저장 용량 조절 및 NAND Flash memory 수명 연장 또는 처리 속도(throughput)를 조절하기 위해 다양한 ECC CODEC 을 지원되어야 한다. 이러한 특성을 갖는 BCH CODEC 을 설계하기 위해서는 서로 다른 길이의 부호 및 다양한 정정 능력이 지원되어야 하고, 최대 지원 가능한 부호 길이, 메시지 길이 그리고 지원하고자 하는 최대 정정능력을 고려하여 적합한 Galois field 를 선택해야 한다. 메시지 길이와 정정능력에 따라서 encoder 는 생성 다항식을 선택하거나 그를 구성하는 최소 다항식(minimal polynomial)을 선택하고, decoder 는 syndrome unit 의 선택, Berlekamp-Massey(BM) unit 의 loop 수 그리고 Chien search unit 의 multiplier 들을 선택하도록 한다. Syndrome unit, BM unit 과 Chien search unit 은 최소 부호길이와 최대 정정능력의 경우에도 3-stage pipeline 되도록 설계하여 모든 부호에 대해서 on-the-fly 지원하도록 설계되었다. 그리고 BM unit 의 소모 전력을 줄이기 위해 BM unit 의 loop 별 동작 cycle 수를 늘리도록 설계하였다.

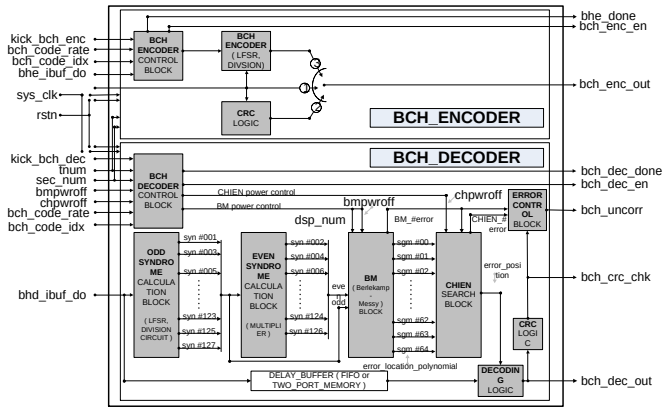


Fig 1. (a) BCH Block Diagram

NAND Status	Initial → End-of-Life
Reliability of Raw NAND Flash memory	Good → Bad
BCH Correction ability	Small → Big
Capacity of NAND	High → Low
Throughput	High → Low
Latency	Small → Large
Power	Low → High

Table 1. Summary of Characteristics

[1] Todd K. Moon, Error Correction Coding: mathematical methods and algorithms, Wiley-Interscience. (2005).
[2] R. Micheloni, A. Marelli, R. Ravasio, Error Correction Codes for Non-Volatile Memories, Springer. (2008).

WBAN을 위한 저면적 저전력 BCH 복호기

정보석, 김철호, 이한호
인하대학교 정보통신공학부
E-mail : hhlee@inha.ac.kr

최근 Wireless Body Area Network (WBAN) 기술은 단거리 무선통신으로서 인체 내,외부에 여러 가지 용도에 따라 다양한 서비스를 제공 할 수 있으므로 인간과 가장 가까운 환경에서 구현되는 네트워크 기술로 크게 주목을 받고 있다. WBAN 에 적용할 Forword Error Correction (FEC)을 선정함에 있어서 가장 중요한 이슈는 에너지 효율을 위한 낮은 하드웨어 복잡도와 에너지 소비를 줄이는 것이다. IEEE 802.15.6 WBAN 표준에 명시되어 있는 (63, 51) BCH 부호를 이용하여 낮은 하드웨어 복잡도와 낮은 전력 소모를 가지는 modified Step-by-Step (m-SBS) 알고리즘을 이용한 (63, 51) BCH 복호기 구조를 제안한다.

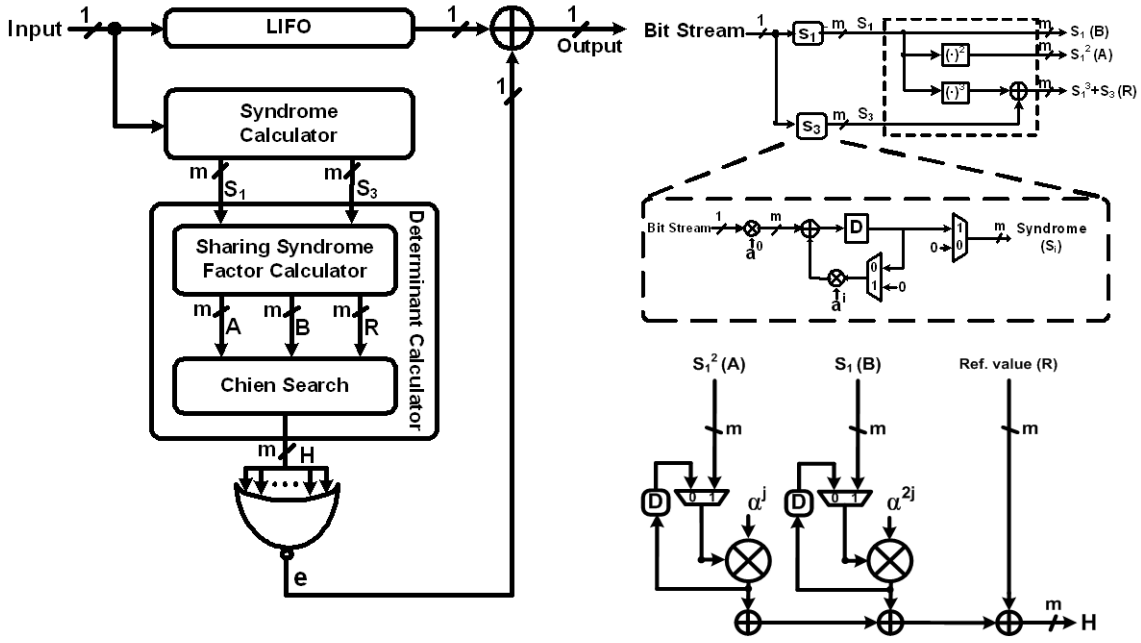


그림 1. m-SBS 알고리즘을 이용한 (63, 51) BCH 복호기.

[1] J. Yeon, S. J. Yang, C. Kim, H. Lee, "Low-Complexity Triple-Error-Correcting Parallel BCH Decoder," Journal of Semiconductor and Science Technology, vol.13, no. 5, pp. 465-472, Oct. (2013).

[2] J. Y. Khan and M. R. Yuce, "Wireless body area network (WBAN) for medical applications," New Developments in Biomedical Engineering, Ch. 13, InTech. (2010)

감사의 글: 본 논문은 산업통상자원부 및 한국산업기술평가관리원의 산업원천기술개발사업(정보통신)의 일환으로 수행하였음.

System level exploring of memory configuration for low power

Sung Yang, Hoi-jin Lee, Young-min Shin, and Jae-cheol Son
SoC Processor Development Team, System LSI Business, SAMSUNG ELECTRONICS
E-mail : yang.sung@samsung.com

본 논문에서 우리는 시스템 레벨에서 시스템 구성을 위한 메모리 구성 정보를 받아서 가능한 모든 메모리 구성 조합을 만들고 그 조합들의 PPA(Power/Performance/Area) 곡선을 통해 최적의 메모리 구성 조합을 찾아주는 방법을 제시한다. [그림.1]

시스템을 구성하는 메모리 서브 블락은 각기 다른 종류의 메모리들로 이루어져 있는데, 서브 블락을 구성하는 메모리의 종류를 선택할 때 단순하게 엔지니어의 직감이나 경험에 의해 이루어 진다면 최적의 PPA 조합을 이룰 수 없을 뿐만 아니라 개발 시간을 허비할 수 도 있다.

본 논문은 최근 메모리 컴파일러의 발전으로 대부분의 IP 공급업체에서 메모리 컴파일러를 제공하고 있으므로, 이 메모리 컴파일러에서 유효한 데이터를 생성하여 시스템 레벨에서 최적의 PPA 를 갖는 메모리 구성 조합을 찾아낸다. 그 결과 고성능을 유지하면서 파워 및 면적을 효과적으로 줄일 수 있음을 보여준다.

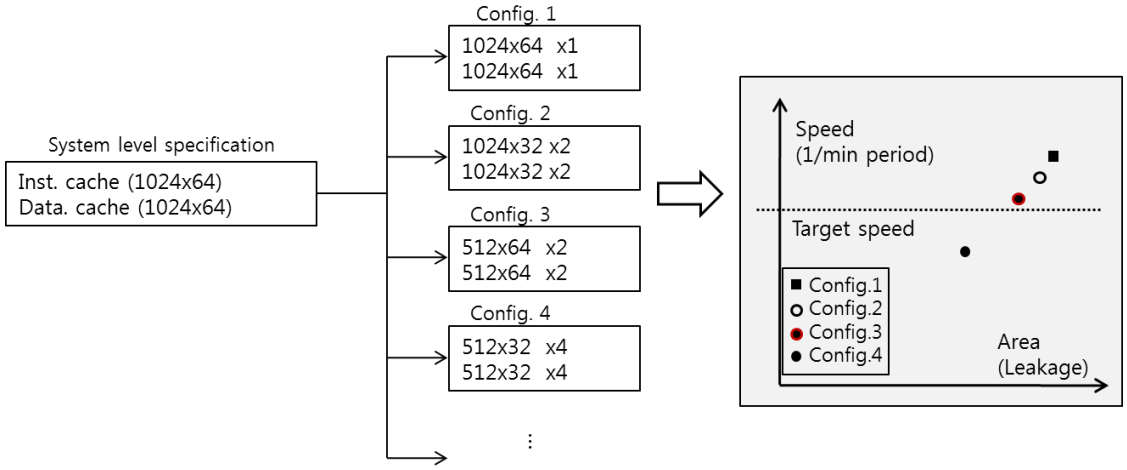


그림 1. 시스템 레벨 최적의 메모리 구성 조합 탐색 알고리즘

Recent advances in deterministic solvers for the Boltzmann transport equation and future research directions

Sung-Min Hong
School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju 500-712, Korea
E-mail : smhong@gist.ac.kr

As much as the semiclassical transport in semiconductors is concerned, the Boltzmann transport equation (BTE) for electron/hole gases gives the most accurate information. Even when the quantum effects (for example, the quantum confinement effect) cannot be neglected, for some practically important cases, the BTE may provide valuable information to describe the spatiotemporal behavior of electron/hole gases. Therefore, the development of the BTE solver has been an important topic in the semiconductor modeling society for a long time. Numerical solvers for the BTE can be divided into two groups (stochastic/deterministic).

In this invited talk, recent advances in deterministic solvers for the BTE [1] are reviewed. Among many existing techniques for calculating the solution in a deterministic manner, only two of them, which can be practically applicable to the semiconductor device modeling, are mainly discussed. The first one, the spherical harmonics expansion (SHE) solver, describes quantities defined on the three-dimensional momentum space using the spherical harmonics. The other one, the multi-subband BTE solver, is applicable to the MOS transistors because it considers the quantum confinement effect by solving the Schrödinger equation in each cross section perpendicular to the carrier transport direction.

In the latter part of this talk, we discuss about future research directions related with the deterministic BTE solvers. Especially, the combined simulation of the carrier transport with other important physical effects is considered. The coupled electron-phonon BTE solver is discussed as a realistic example. Since there are not so many efforts based on the deterministic BTE solver in this aspect, the attempts using other microscopic transport solvers – the Monte Carlo technique and the Non-Equilibrium Green's Function technique – are also considered. Another example – coupling with the Maxwell's equations – is presented.

Acknowledgment: This work was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009594). Also it was partially supported by GIST College's 2013 GUP Research Fund.

[1] S.-M. Hong, A.-T. Pham, C. Jungemann, Deterministic Solvers for the Boltzmann Transport Equation, ISBN 978-3-7091-0777-5, Springer Verlag Wien/New York, 2011.

Simulation of III-V UTB SB-MOSFETs using tight-binding band-structure calculations

Howon Choi, Jaehyun Lee, Yolum Lee, and Mincheol Shin
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : mshin@kaist.ac.kr

III-V materials are fascinating alternatives as a channel material due to both small effective mass and high mobility. In this work, we investigated the performance of ultra-thin-body (UTB) Schottky-barrier (SB) MOSFETs with III-V channel materials to increase on-state currents (I_{on}); the Γ-, Λ-, and Δ-valleys of various III-V materials such as InAs, InSb, GaSb, and GaAs were described by the effective mass Hamiltonian with the full inverse-mass tensor. The effective masses were extracted from $sp^3d^5s^*$ tight-binding calculations. To consider the ambipolar behavior, we also calculated hole currents with the six-band $k \cdot p$ Hamiltonian. The currents are obtained by self-consistently solving the Poisson equation and non-equilibrium Green's function equation. I_{on}/I_{off} does not impove because of small band-gap for InSb and InAs and density of state (DOS) bottleneck [1] for GaAs, respectively. Only GaSb devices show better performance than Si devices. Their band-gap (0.66eV) is suitable to satisfy off-current criteria, 0.1 μA/μm, and currents from Λ-valley solve the DOS bottleneck problem. The current contributions of Λ-valley are around 80% , while GaAs devices strongly depends on Γ-valley. The reason of this phenomena is that the energy difference between Λ- and Γ-valley is intrinsically small. This study may provide a useful guideline for designing III-V channel SB devices.

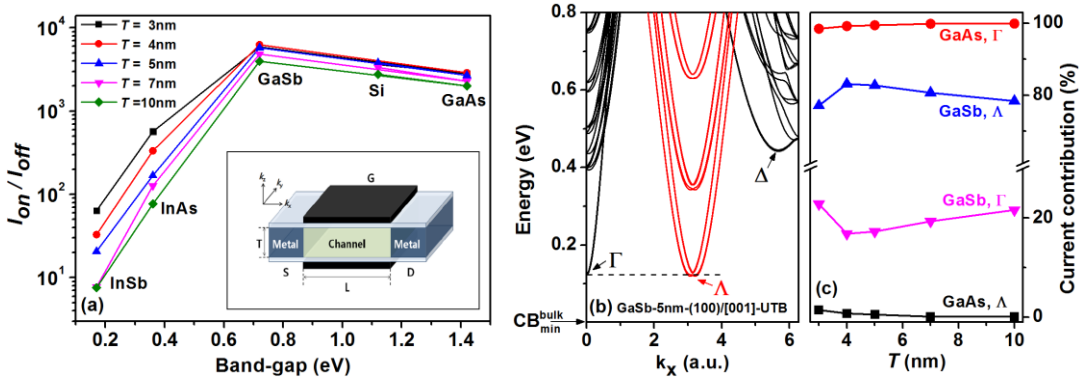


Fig 1. (a) I_{on}/I_{off} versus the band-gap with $L = 4T$, SBH = 0 eV, and EOT = 1 nm. (Inset) Schematic diagram of UTB DG SB-MOSETs. (b) CB profiles of GaSb with 5nm-thick UTB in (100)/[001] from tight-binding method. (c) Current contribution of Γ- and Λ-valley for GaAs and GaSb devices.

[1] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur and M. Rodwell, IEDM Tech. Dig., 109 (2007) .

3D Simulation of Threshold Voltage Variations Due to Random Grain Boundary and Discrete Dopants in Sub-20 nm Gate-All-Around Poly-Si Transistors

Jungsik Kim[(a)], Hyeongwan Oh[(c)], Junyoung Lee[(c)], Jiwon Kim[(c)], Chang-Ki Baek[(b)], Jeong-Soo Lee[(a , (c)]

Department of IT Convergence Engineering[(a)], Creative IT Engineering and Future IT Innovation Lab [(b)], Electrical Engineering[(c)], Pohang University of Science and Engineering (POSTECH), Pohang 790-784, Korea

E-mail : irijeori@postech.ac.kr

In nanoscale polysilicon (Poly-Si) channel, grain boundaries and discrete dopants are critical issues determining the device performances. Random grain boundary (RGB) can trap the free carriers and form a potential barrier to disturbe the carrier flow. According to previous study, single RGB with different positions in Poly-Si channel can cause V_{th} variations [1]. In addition to a RGB issue, random discrete dopants (RDDs) has been issued as the device is aggressively scaled down. Depending on density and position of RDDs, Poly-Si channel device would show the fluctuation of the electrical performances such as V_{th}, subthreshold swing, and drain induced barrier lowering [2]. In this work, we use a 3D simulation to investigate the effect of RGB and RDDs on the V_{th} variation for sub-20 nm GAA Poly-Si channel. The GAA Poly-Si devices show less V_{th} variation due to its superior channel controllability, compared with the planar devices. In addition, the V_{th} variations and related conduction energy band profiles due to random nature of RGB and RDD are discussed.

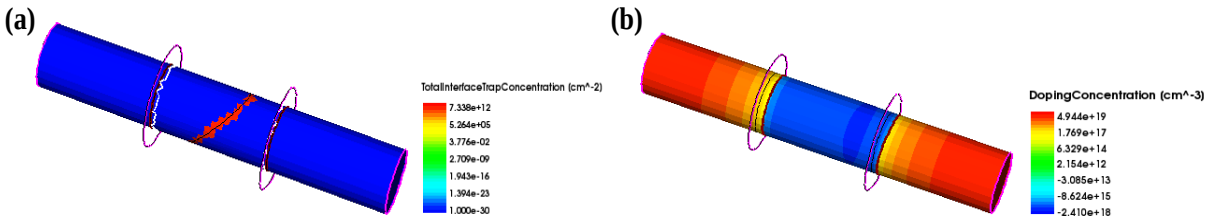


Fig 1. A schematic of GAA transistors with random (a) grain boundary and (b) discrete dopant.

[1] Y. Li, J Y Huang, B.-S. Lee, Semiconductor Science and Technology, (2008).
[2] C.-Y. Chen, J.-T. Lin, M.-H. Chiang, IEEE Nanoelectronics Conference (INEC), (2013).

Simulation of dual material gate InAs Schottky barrier field effect transistor

Wonchul Choi, Jaehyun Lee, and Mincheol Shin
Department of Electrical Engineering, KAIST, Daejeon 305-732, Korea
E-mail : mshin@kaist.ac.kr

Recently, Schottky barrier MOSFETs (SB-MOSFETs) have been proposed for promising nano-scale devices [1]. Despite many advantages, low on-current is a major drawback of the devices since on-current is tunneling currents through Schottky barrier. In order to increase on-current, InAs, which is known for its small effective mass, is considered for the channel material in this work. We have however found that small on-off ratio due to large ambipolar currents is a serious problem in the InAs SB devices. The ambipolar current can be suppressed by so-called dual-material gate (DMG) [2]. In the DMG structure two different materials with different work functions are used for the gate and controlled by a common gate voltage. However, the advantages of DMG structure in SB-MOSFETs has not been investigated before. In this work, we have computationally investigated the effect of DMG structure in InAs SB-MOSFETs and our primary objective of this work is to reduce the ambipolar current. Our simulation results shows that ambipolar current can be suppressed down to about I_d=0.1 μA/μm and on-off ratio is more than 10^3.

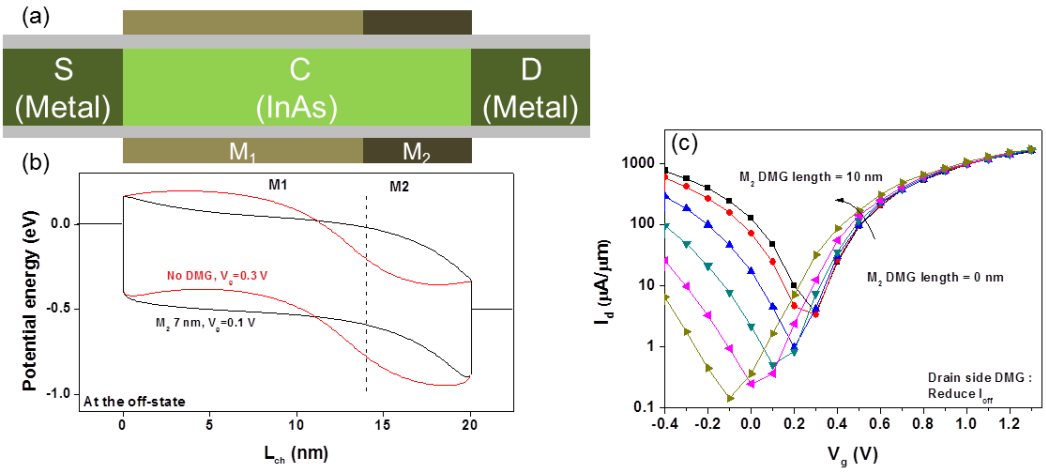


Fig 1. (a) Schematic image of InAs SB-MOSFETs with DMG (b) Potential profile at the off-state (c) I-V characteristics of InAs SB-MOSFETs with various DMG length of metal gate

[1] J. M. Larson and J. Snyder, IEEE Trans. Electron Devices, 53, 5 (2006).
[2] W. Long, H. Ou, J.-M. Kuo, and K. K. Chin, IEEE Trans. Electron Devices, 46, 5 (1999).

멤리스터 브리지 시냅스를 사용한 생체형 병렬 영상처리 시스템

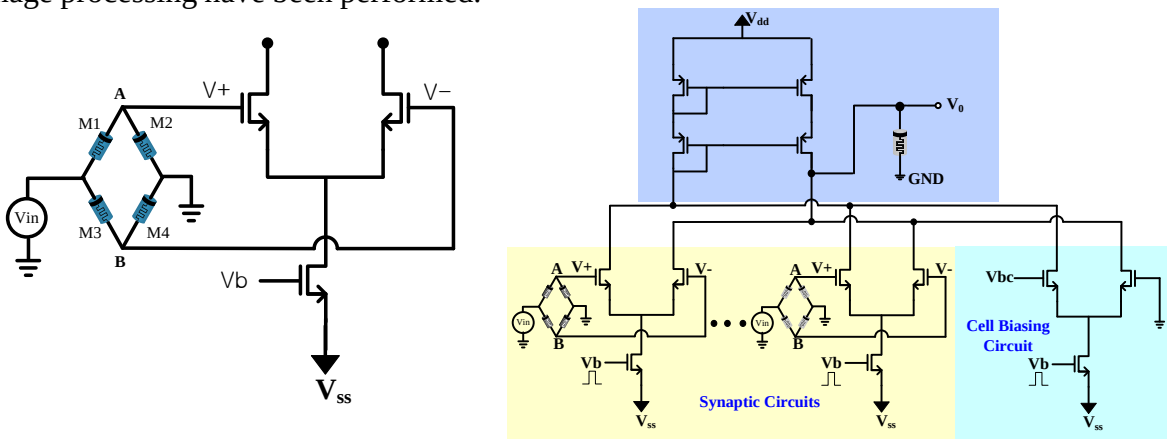
Bio-modeled Parallel Image Processing System using Memristor Bridge Synapses

Hyongsuk Kim, Maheshwar Sah, Changju Yang

Div. of Electronics Engineering, Chonbuk National University, Jeonju 561-756, Korea

E-mail : hskim@jbnu. ac.kr

Image processing inherently requires a big amount of processing operations. Parallel processing system is needed to meet the technological demand of real time image processing. Cellular Neural Network (CNN) [1], which is a high speed analog parallel image processing system with a biological vision-like architecture, belongs to this technical category. A bottleneck of the CNN technology is the implementation difficulty of massive neural synapses in a chip since every synapse requires an analog multiplier. Recently, a new circuit element called memristor [2] with which artificial synapse can be easily implemented is invented and shed bright light on bio-inspired parallel image processing system. In this paper, a simple and compact memristor-based bridge circuit which is able to perform signed synaptic processing in neuron cells is presented. The proposed memristor-based synapse is composed of 4 memristors which makes a bridge type configuration. By programming each memristor of the memristor bridge circuit, neural weighting values can be installed with the memristor bridge synapses. The memristor bridge synapse-based Cellular Neural Networks is designed and simulations of image processing have been performed.



(a) (b)

Fig 1. Memristor bridge synapse (a) and a memristor bridge synapse-based neural cell (b)

[1] L. O. Chua and L. Yang, B, “Cellular neural networks: Theory,” IEEE Trans. Circuits Syst., vol. CAS-35, no. 10, pp. 1257–1272, Oct., 1988.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” Nature, vol. 453, no. 7191, pp. 80–83, 2008.

Emulation of spike-timing dependent plasticity in phase-change memory cells for neuromorphic applications

Dae-Hwan Kang, Hyun-Goo Jun, Kyung-Chang Ryoo, Jae Hee Oh, and Hongsik Jeong
Flash PA, Memory Div. Semi.Biz. SEC, San 16, Banwol-dong, Hwasung-si, Gyeonggi-do, 445-701 Korea
E-mail: daehwan.kang@samsung.com

We emulate the spike-timing dependent plasticity (STDP) behavior of biological synapse in two phase change memory (2-PCM) cells with 3x nm technology as shown in Fig. 1, which has been considered as a formulated Hebbian learning rule of our cognition, learning and memory abilities [1]. Various STDP behaviors are successfully realized in 2-PCM synapse by varying the interval of set pulses on two cells and their pulse shape as well, which helps to design diverse synaptic connection abilities. It is also demonstrated that the signal transfer rate may be increased to speed up learning or memory ability by reducing the time interval between pre-synaptic and post-synaptic spiking potential. Finally, we suggest a proto-type of phase change memory neuron (PCMN) architecture including both neuron spiking and STDP, which makes very promising candidate for electronic neuron in the large-scale neuromorphic system applications accompanied with its much small form factor and low energy per synaptic event comparable to ones of biological neuron [2].

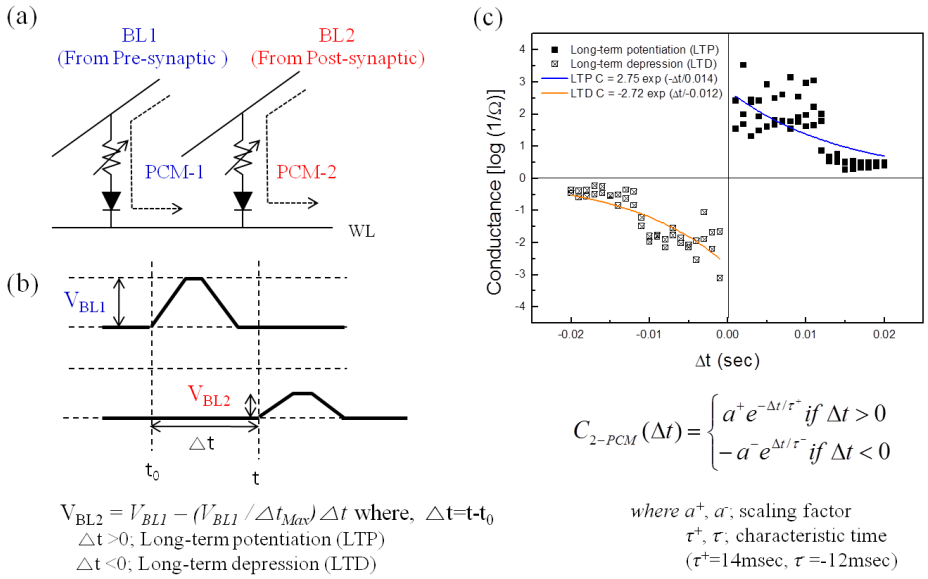


Fig 1. (a) A schematic of 2-PCM synapse in phase change memory cell array (b) Pulse shape with time interval of △t and (c) Conductance with respect to △t which is quite analogous to STDP in biological neuron [1].

[1] C. Zamarreno-Ramos, L. A. Camunas-Mesa, J. A. Perez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, and B. Linares-Barranco, *Frontiers in Neuroscience*, Vol. 5, Article 26, 1 (2011).
[2] Chi-Sang Poon and Kuan Zhou, *Frontiers in Neuroscience*, Vol. 5, Article 108, 1 (2011).

Improved synaptic characteristics of filamentary ReRAM by adopting interfacial oxide for neuromorphic device application

Behnoush Attarimashalkoubeh, Sangheon Lee, Daeseok Lee, Amit Prakash, Jeonghwan Song, Kibong Moon and Hyunsang Hwang

Department of Material Science and Engineering, POSTECH, Pohang, Gyeongbuk, Korea

E-mail: hwanghs@postech.ac.kr

A synaptic system is similar to a two terminal device [1] which works based on formation/annihilation of nano-scale conductive filaments [2] or interfacial redox reaction [3]. One highlighted candidate type is oxide based ReRAM which exhibits excellent scalability down to 50nm, high speed operation, and retention characteristics [4].However conventional filamentary devices are difficult to obtain appropriate synaptic behavior due to the abrupt switching behavior in SET and RESET conditions. In this work, we developed triple-layer: W (TE) /Ti/HfO_x/TaO_x/Pt (BE) structure to obtain gradual conductance change by controlling filament properties.

Furthermore, to mimic biological synaptic behavior for neuromorphic application, the device conductance expected to continuously increases under the consecutive external inputs pulse[5]; in an ideal synaptic device, conductance changes with applying stair-case positive and negative pulses must be gradual[6]. In this work, appropriate synaptic behavior obtained by adopting a new pulse scheme and STDP characteristic significantly improved, also good retention at 85℃ is reported.

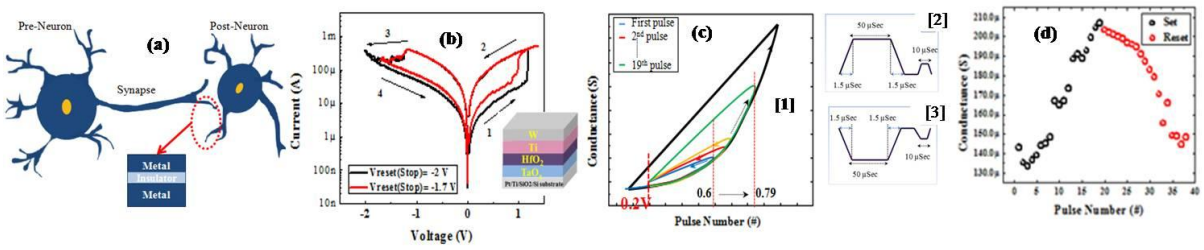


Fig 1. a) Analogy between biological and classic two terminal memory devices, b) Measured I-V characteristic of THE TRIPLE device,c) Schematic process flow of applying consecutive increasingly amplitude pulses (from 0.6 to 0.79V), and read in 0.2V for SET. For RESET same work done and d) Symmetric Conductance change after applying continuous staircase pulses.

Acknowledgment: This work was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (2012-0009460).

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[1] Smith, L. S. Handbook of Nature inspired and innovative computing: integrated classical models with emerging technologies; Springer: New York,2006, pp 433-475.[2] M. J. Lee, et al, Nano. Lett. , Vol. 9, (2009),pp. 1476-1481. [3] S. Park et al, Electron Device Meeting (IEDM) 2012. [4] J. Park et al, Electron Device Letter, Volume 32,(2011), pp. 63-65. [5] W. Lei, et al,IEEE, International Symposium on Circuits and Systems, (2010), pp. 13-16.[6] D.Kuzum, Nano let, Vol.12, (2012),pp. 2179-2186.

Improvement in the ON/OFF Ratio (~10^7) and Switching Uniformity of an Atom Switch Using TiO_x Layer for Reconfigurable Logic Application

Behnoush Attarimashalkoubeh, Amit Prakash, Sangheon Lee, Jaesung Park, Jeonghwan Song, Daeseok Lee, Jiyoung Woo, Kibong Moon, Yunmo Koo and Hyunsang Hwang.
Department of Materials Science and Engineering,
Pohang University of Science and Technology, Gyeonbuk, Korea
E-mail: hwanghs@postech.ac.kr

Atom switch which rely on the electrochemical redox reaction and field induced Cu or Ag ions migration in a solid electrolyte, has sought to be one of the most promising candidate for field-programmable gate array (FPGA) application owing to very high ON/OFF ratio (10^5-10^7), low ON state resistance (<1000 Ω), excellent scalability and BEOL process compatibility [1-3]. However, generally a trade-off between high ON/OFF ratio and uniformity in switching cycles exists. In this study, an atom switch with improved high ON/OFF ratio (~10^7) and switching cycle uniformity is reported by inserting an ultrathin TiO_x layer in W/Cu/TiO_x/AlO_x/Pt structured device with size of 250 × 250 nm^2 as shown in Fig. 1(a). The TiO_x layer helps to control the Cu diffusion into the atomic layer deposited AlO_x layer (2.5 nm) which in turn improves the switching cycle uniformity and ON/OFF ratio [Fig. 1(b)] as compared to that in the without TiO_x layer device [Fig. 1(c)]. In addition, TiO_x layer could also protect Cu to be oxidized [1] and improve the interface between Cu and AlO_x. Cycle-to-cycle cumulative probability plot of LRS and HRS shows tight distribution with small dispersion ratio of [Fig. 1(d)]. The switching mechanism can be attributed as the formation/dissolution of Cu nanobridge in the AlO_x layer.

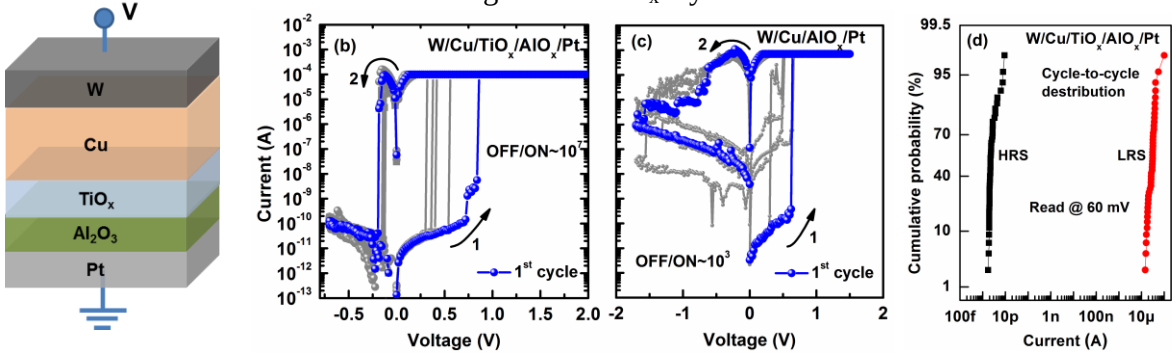

Fig 1. (a) Schematic structure of atom switch in W/Cu/TiO_x/AlO_x/Pt structure with via-size of 250 nm. Switching characteristics of (b) with TiO_x layer and (c) without TiO_x layer devices. Large ON/OFF ratio of >10^7 is obtained after TiO_x layer insertion. (d) Small dispersion in LRS and HRS during 50 dc sweep cycles can be seen in cumulative probability plot.

Acknowledgement: Development of low power reconfigurable IC with 100nsec program/erase speed and sub-100 nm (10045085).

References: [1] M. Tada et al, IEDM 2009, p. 38.5.1. [2] M. Tada et al, IEDM 2010, p. 16.5.2. [3] S. Kim et al, Appl. Phys. Lett, vol. 99, p. 192110, 2011.

Transparent Flexible Nanogenerators Based on 1D/2D Piezoelectric and Triboelectric Nanomaterials

Sang-Woo Kim

School of Advanced Materials Science and Engineering, SKKU Advanced Institute of Nanotechnology (SAINT), CINAP, Institute of Basic Science (IBS), Sungkyunkwan University (SKKU), Suwon 440-746, Korea

E-mail : kimsw1@skku.edu

Energy harvesting systems based on piezoelectric and triboelectric nanomaterials are in great demand, as they can provide routes for the development of self-powered devices which are highly flexible, stretchable, mechanically durable, and can be used in a wide range of applications. Our recent research interest mainly focuses on the fabrication of nanogenerators (NGs) based on 1D/2D nanomaterials such as zinc oxide nanowire/nanosheets and graphene. In this talk, I will address the first demonstration of DC power generation using piezoelectric 2D ZnO nanostructure and an anionic layer. The device made from such 2D piezoelectric nanosheets/anionic layer heterojunction has potential for use as a mechanically durable and smallest size power package, which can be used to charge wireless nano/micro-scale systems with no need for a rectifier circuit. The combined effect of buckling the ZnO nanosheets, anionic layer, and coupled semiconducting and piezoelectric properties of ZnO nanosheets are the main causes of the efficient DC power generation [1]. Further I will present the growth of lead-free single-crystalline ferroelectric V-doped 2D ZnO nanosheets and the realization of a high-performance flexible DC power output NG based on V-doped 2D ZnO nanosheet networks for the first time [2]. Furthermore, the efforts toward developing triboelectric NGs using those materials are in progress.

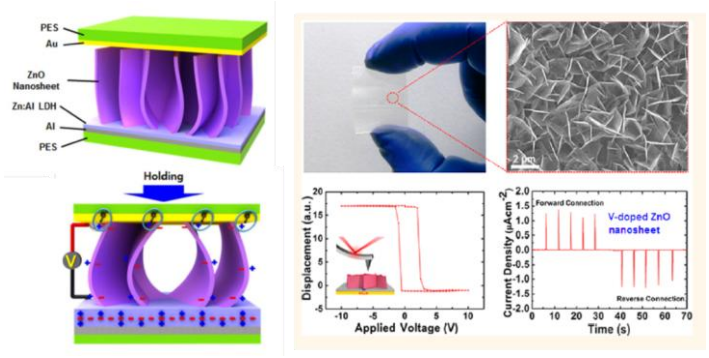

Fig 1. 2D piezoelectric material-based nanogenerators

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[2] M. K. Gupta, J.-H. Lee, K. Y. Lee, and S.-W. Kim, *ACS Nano*, 2013, *7*, 8932-8939.

Investigation of gate bias stress effect on MoS_2 field effect transistors

Kyungjune Cho, Woanseo Park, Tae-Young Kim, and Takhee Lee
Department of Physics and Astronomy, Seoul National University, Seoul 151-747, Korea
E-mail : tlee@snu.ac.kr

Recently, molybdenum disulfide (MoS_2) has attracted a lot of attention due to its intriguing electrical properties compared to the substantioal limitaions of graphene in electronic transistors [1]. We investigated the gate bias stress effects of multi-layered MoS_2 field effect transistors (FETs) with a back-gated configuration. When a positive (negative) gate bias stress was applied to the device, the current decreased (increased) and the threshold shifted in the positive (negative) gate bias direction. The electrical instability of the MoS_2 FETs can be significantly influenced by the electrical stress type, relative sweep rate, and stress time in an ambient environment. These phenomena can be explained by the charge trapping due to the adsorption or desorption of oxygen and/or water on the MoS_2 surface with a positive or negative gate bias, respectively, under an ambient environment. This study will be helpful in understanding the electrical-stress-induced instability of the MoS_2-based electronic devices and will also give insight into the design of desirable MoS_2 devices for electronics applications [2].

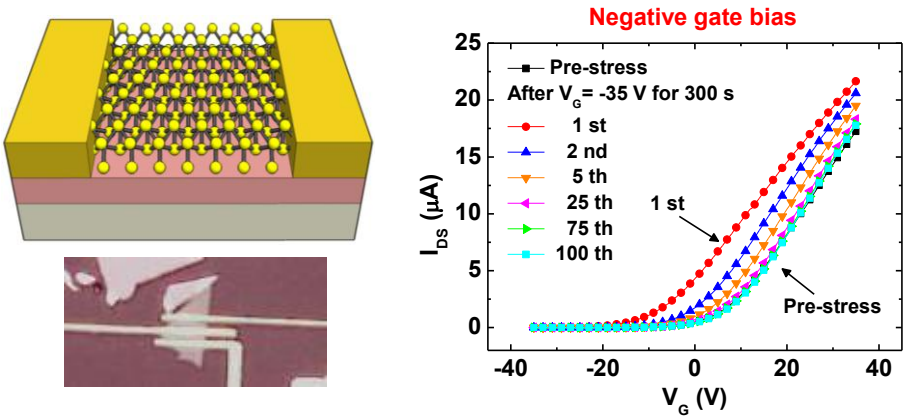


Fig 1. MoS_2 FET device and the electrical data of gate bias stress effect.

[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, Nature Nanotechnol. 6, 147 (2011).
[2] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee, ACS Nano, 7, 7751 (2013).

Ambient dependent photonic response of graphene photodetectors for optical interconnect

유태진 [1], 강창구 [2], 이상경 [2], 최선희 [2], 이병훈 [2*]

[1]*GIST College,* [2]*School of Materials Science and Engineering*

Gwangju Institute of Science and Technology, 1 Oryong-dong, Buk-gu, Gwangju 500-712, Korea

E-mail : bhl@gist.ac.kr

그래핀은 2 차원 구조이며, 투명하고, 얇은 두께에도 높은 광 흡수도 (~2.3%)를 가지고 있다 [1]. 또한 빛에 의한 carrier multiplication 특성을 보이므로, 빛에 의하여 전자와 정공을 다량으로 생성해 낼 수 있고 [2], 이렇게 생성된 전하들은 높은 이동도 (200,000 $cm^2/V \cdot s$) 를 가지고 있으므로, photodetector 로 제작 하였을 때, 반응 속도가 빠른 것으로 알려져 있다. 이 때문에 그래핀을 광배선 도파로, 수광소자로 활용하기 위한 연구가 진행되고 있다. 이러한 장점에도 불구하고, 그래핀의 표면이 공기 중에 노출 되었을 경우 산소나 물 분자들의 영향으로 생기는 photodesorption 때문에, 광 민감도 저하와 저항의 변화가 발생한다는 것이 실제 응용에서는 심각한 문제로 지적되어 왔다 [3,4].

본 연구에서는 환경에 따른 그래핀 photodetector 의 photocurrent 및 photodesorption 특성을 확인 하기 위해, 대기 중과 고 진공상태 (~10^{-7}Torr)에서 광 특성을 측정하였다. 공기 중에서 산소나 물 분자로 인한 photodesorption 현상이 발생하여 전류의 base line 이 계속 변화하는 것을 관찰하였으나, 산소나 물 분자의 영향이 거의 없는 진공에서는 전류의 base line 의 변화 없이 빛에 따라 안정된 photodetector 의 특성을 보였다. 이 실험을 통해 그래핀 photodetector 에 미치는 외부 환경의 영향을 알 수 있었고, 향후에는 그래핀을 suspend 구조로 제작하여 그래핀의 윗면과 아랫면을 모두 환경에 노출시킨 상태에서 대기와 진공 중에서 광 특성을 측정하여 환경의 영향을 직접적으로 관찰해 볼 계획이다. 이 실험 결과를 통하여 그래핀 photodetector 에 미치는 환경의 영향을 이해하고, 나아가 안정된 동작 특성을 보이는 그래핀 photodetector 를 구현할 수 있을 것으로 기대된다.

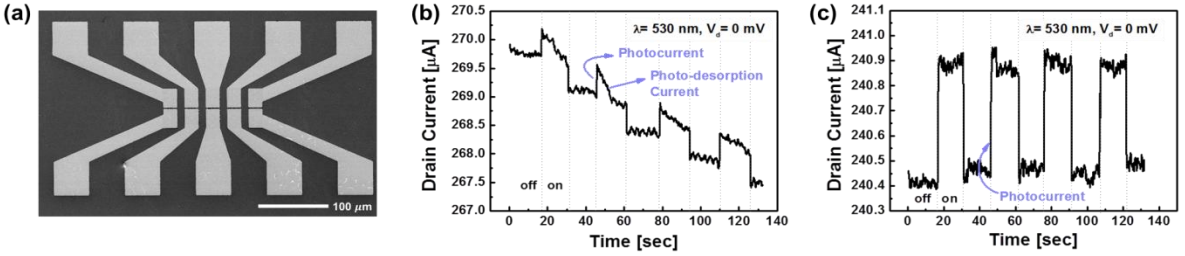


Figure 2 (a) 소자 구조 SEM image, 광 반응성 측정 (b) 대기중, (c) 진공(~10^{-7}Torr), on/off 주기 15 초, 빛의 세기 2 mW/cm^2, 파장 530 nm, V_d = 100 mV, V_g = 0V).

[1] R. R. Nair et al., Science **320,** 5881 (2008). [2] T. Winzer et al., Nano Lett. **10,** 12 (2010). [3] Y. Shi et al., Small **5,** 17 (2009). [4] C.G. Kang et al., Opt. express 21, 20 (2013).

Monitoring the electrical property of graphene transistor by the oxygen vacancy generation of top oxide layer.

Taekwang Kim[1*], Hyewon Du[1], Somyeong Shin[1], Jong-Hyuk Yoon[2], Eun-Kyu Lee[2], Seungmin Cho[2], Sunae Seo[1*]

[1] Department of Physics, Sejong University, Seoul, 143-747, Korea

[2]Micro device & machinery solution division, Samsung Techwin R&D center, Seongnam-si, Gyeonggi-do 463-400, Korea

Fermi level tuning in graphene is crucial for the applications such as conducting electrode or semiconducting electronic device. It is generally achieved by both non-covalent and covalent molecular doping. Former is related with weak Vander Waals interaction which keeps electronic band structure of graphene intact. However, the molecular doping is sensitive to the air exposure so that the degradation of electrical property induce reliability issue without passivation.

Here, we suggest self-passivated and well-controlled graphene doping by changing the resistivity of interfacial oxide. The oxygen in transition metal oxide is released at the high temperature under vacuum due to the concentration gradient at the interface leaving electrons which is probable to be conduction electrons by thermal activation. This indicates oxygen vacancy generates impurity level close to conduction band minimum and forms insulating oxide into N-type semiconductor. We monitored the annealing time dependent electron doping concentration of graphene under vacuum. Along with the change of charge neutrality point, to understand the conduction mechanism of graphene at room temperature with Fermi level increase, we investigated the mobility variation of electron and hole carrier versus doping concentration. The top metal oxide layer could contribute to Fermi level tuning in graphene and allow this change reliable by self-passivation compared with molecular doping. By the optimization of metal oxide thickness and doping concentration, we suggest this method could provide reliable doping to reduce sheet resistance without mobility degradation.

Cu electrodeposition on Ru seed layer prepared by atomic layer deposition

Seunghoe Choe[a], Myung Jun Kim[a], Hyun Seok Ko[b], Young Kwang Kim[c], Oh Joong Kwon[c], and Jae Jeong Kim[a],

[a]*School of Chemical and Biological Engineering, Seoul National University, Seoul 151-742. Korea*
[b]*Department of Material Science and Engineering, Incheon National University, Incheon 406-772, Korea*
[c]*Department of Energy and Chemical Engineering, Incheon National University, Incheon 406-772, Korea*
E-mail : jjkimm@snu.ac.kr

Eletrodepostion of Cu was adopted as a metallizaiton process with the introduction of a Damascene structure. Cu metallization through electrodepostion necessarily requires a seed layer and a barrier layer which make the sturucture complex. The seed layer is usually formed through Physical Vapour Deposition (PVD), however, the continuous reduction of chip dimension needs thinner film with good step coverage which is hard to be accomplished with PVD process. Thus, ALD-Cu and ALD-Ru deposition were introduced as an alterantive processes, because ALD process is superior than other processes in making thin and continuous film[1]. In this study, the Cu electrodepostion on the ALD-Ru was investigated.

Ru blanket and patterned wafers with the structure of ALD-Ru/PVD-Ta were used as a working electrode. Cu wire and Ag/AgCl (sat. KCl) electrod were employed as a counter and a reference electrode. As a pretrment step, electrochemical oxide reduction (EOR) was studied as shown in fingure 1. After optimizing the EOR step, Cu electrodepostion was performed, and the properties of Cu film and the process characteristics were analyzed. In addition, gap-filling of Cu was also conducted and a successful gap-filling was obtained. Through this study, various chatacteristics of Cu electrodepostion on ALD-Ru were obatained.

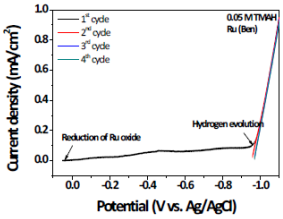


Figure 1. Changes of voltammetic curve depending on EOR cycles.

[1] S. Yeo, S.-H. Choi, J.-Y. Park, S.-H. Kim, T. Cheon, B.-Y. Lim, S. Kim, Thin Solid Films, 546, 2 (2013)

Cu-Ag superfilling for damascene metallization

Myung Jun Kim[a], Taeho Lim[a], Kyung Ju Park[a], Oh Joong Kwon[b], and Jae Jeong Kim[a]
[a]*School of Chemical and Biological Engineering, Seoul National University, Seoul 151-744, Korea*
[b]*Department of Energy and Chemical Engineering, Incheon National University, Incheon 406-772, Korea*
E-mail : jjkimm@snu.ac.kr

Cu interconnection, one of essential component in semiconductor devices, has been fabricated via damascene process including metal electrodeposition. The size of Cu interconnection has been decreased to enhance the integrity of devices. The rapid down-scaling raises the issues such as a reduction of the electrical conductivity and an increase in the potential for electromigration failure. In the aspect of reliability, the codeposition of secondary metal with Cu is expected to improve the electromigration resistance [1]. Among various metals, Ag can be a candidate to be codeposited, because Cu-Ag shows the comparable conductivity to Cu [2]. However, the superfilling of Cu-Ag has not been intensively investigated. In this presentation, we introduce the superfilling of Cu-Ag using electrodeposition and the properties of Cu-Ag film with comparing those of pure Cu and Ag films. The mechanism of superfilling will be explained based on the electrochemical analyses and the atomic distributions of Cu and Ag within the filling features [3,4].

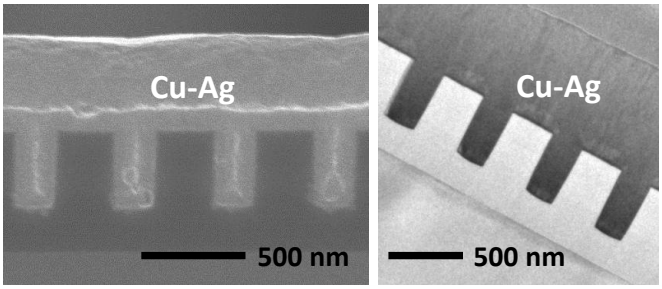


Fig 1. Cross-sectional images of superfilled Cu-Ag by electrodeposition

[1] K. Barmak, C. Cabral Jr., K.P. Rodbell and J.M.E. Harper, J. Vac. Sci. Technol. B 24, 2485 (2006).
[2] M.J. Kim, H.J. Lee, S.H. Yong, O.J. Kwon, S.-K. Kim and J.J. Kim, J. Electrochem. Soc. 159 D253 (2012).
[3] M.J. Kim, S.H. Yong, H.S. Ko, T. Lim, K.J. Park, O.J. Kwon and J.J. Kim, J. Electrochem. Soc. 159 D656 (2012).
[4] M.J. Kim, K.J. Park, T. Lim, O.J. Kwon and J.J. Kim, J. Electrochem. Soc. 160 D3126 (2013).

Real-Time Observation of Cu Electroless Deposition: Synergetic Suppression Effect of 2,2'-Dipyridyl and 3-N,N-Dimethylaminodithiocarbamoyl-1-propanesulfonic Acid

Taeho Lim, Myung Jun Kim, Kyung Ju Park, Kwang Hwan Kim, and Jae Jeong Kim
School of chemical and biological engineering, Seoul National University, Seoul 151-744, Korea
E-mail : jjkimm@snu.ac.kr

Electroless Cu filling using organic additives has been extensively studied for a number of years [1]. However, most studies observed the effect of additives by *ex-situ* methods. We introduced an open-circuit potential measurement assisted by a quartz crystal microbalance as a new *in-situ* method. The effect of 2,2'-dipyridyl and 3-N,N-dimethylaminodithiocarbamoyl-1-propanesulfonic acid (DPS) during Cu electroless deposition was observed in real time in this study. During Cu electroless deposition, the addition of 2,2'-dipyridyl reduced the deposition rate. DPS switched its role sensitively according to its concentration: deposition was accelerated at low concentrations and strongly suppressed at high concentrations. However, synergetic suppression effect was observed even at low DPS concentrations when 2,2'-dipyridyl was added together. In this system, the rate of suppression depended on DPS concentration: the addition of the higher DPS concentration led to the faster decrease in the deposition rate to its minimum value. The minimum deposition rate was independent of the DPS concentration. Using the synergetic suppression effect, electroless Cu filling of 55-nm trenches was also successfully achieved.

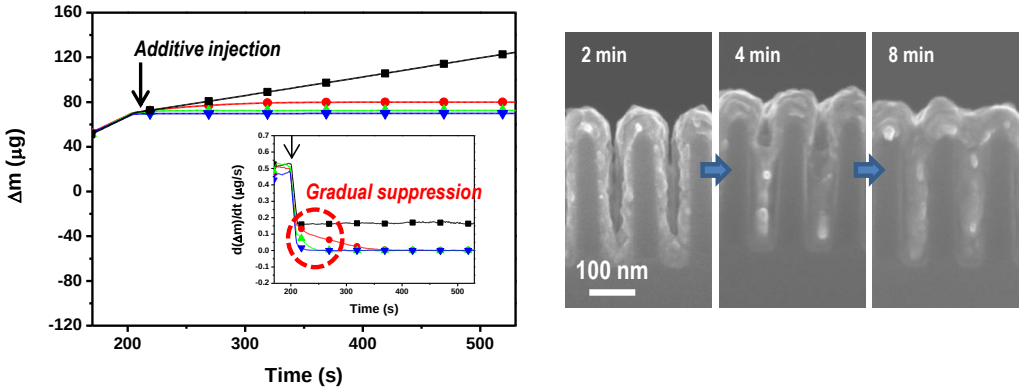


Fig 1. (a) Mass change of Cu electrode and (b) filling profiles in the presence of both 2,2'-dipyridyl and DPS

[1] C. H. Lee, S. C. Lee, and J. J. Kim, Electrochim. Acta, 50, 3563 (2005).

Effect of pulsed electric field on dielectric breakdown in damascene Cu interconnects

Han-Wool Yeon[1], Jun-Young Song[1], Jang-Yong Bae[2], Yu-Chul Hwang[2] and Young-Chang Joo[1,*]
[1]*Department of Materials Science & Engineering, Seoul National University, Seoul, 151-744*
[2]*Product Quality Assurance Team, Memory Division, Samsung Electronics, Gyeonggi-Do 445-701*
E-mail : didigi21@snu.ac.kr

Time dependent dielectric breakdown (TDDB) in damascene Cu interconnects become a significant reliability issue due to harsh applied electric field on the dielectrics which is induced by aggresive scaling of nano-electronics. TDDB mechanisms have been evaluated by direct current (DC) stress on dielectrics [1]. However, most of devices are operated under pulsed electric field. Therefore, an in-depth study about TDDB under pulsed electric field condition in addition to under DC condition is required. In this paper, we inivestigated the effect of pulsed electric field on dielectric breakdown in damascene Cu interconnects. Under 225 ^{o}C-6.5 MV/cm with pulse frequency is 1 kHz, time to failure (TTF) under bipolar pulse condition is the longest and TTF under unipolar pulse condition and TTF under DC condition is similar (Fig. 1 (b)). These results are consistent with dynamic TDDB results when Cu migration is dominant breakdown mechanism. However, as pulse frequency increases to 100 kHz, TTF under unipolar condition increases (Fig. 1 (c)). It is suggested that intrinsic bond-breakage of dielectrics significantly affect the dielectric breakdown in addition to Cu migration [2]. The details of pulse shape and frequency dependence of TDDB will be also disscused.

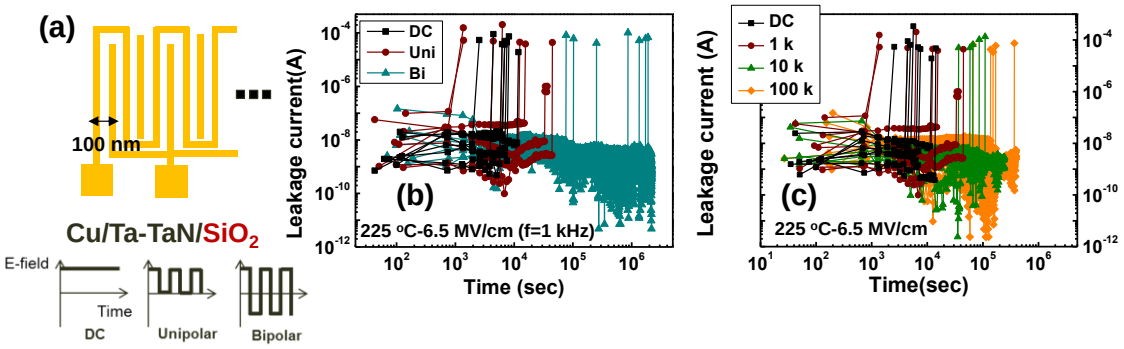


Figure 3 (a) Schematics of damascene Cu serpentine pattern, (b) Pulse shape dependence of TTF (c) Pulse frequency dependence of TTF under DC and Unipolar pulse condition.

[1] J. W. McPherson, Microelectronics Reliability, 52, 1753 (2012)
[2] J. W. McPherson, H. C. Mogul, J. Appl. Phys., 84, 1513 (1998)

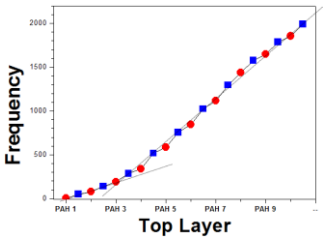
Flexible Cu barrier of PAH/PSS laminar structures using Layer-by-Layer (LbL) method

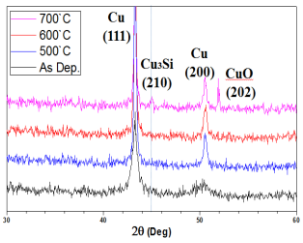
Daekyun Jeong, Chiyoung Lee and Jaegab Lee
Department of Advanced Materials Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : lgab@kookmin.ac.kr

For three dimensional integrated circuits (3DIC), through-silicon via (TSV) has been rapidly investigated in these days. Especially, copper TSV is the most preferred materials for its high electrical conductivity, easy deposition process. But as Cu circuit is integrated in TSV, problems are occurred by the small via hole size, Cu thermal expansion, and post annealing process to reduce residual stresses inside TSV also affect to Cu protrusion.[1]

In order to prevent the TSV damages by the Cu protrusion, flexible barrier layers have been inserted between Cu and Si by using Layer-by-Layer (LbL) materials. Flexible LbL materials are laminated with polyallylamine hydrochloride (PAH) and polystyrene sulfonate (PSS) by solution dipping methods. Using quartz crystal microbalance (QCM), we have measured the LbL formation mass which has be transited to amount of thickness increasing.[2] As LbL dipping cycles are increased, formation ratio of LbL thickness is saturated at more than 3 times. In these results, more than 3 bilayers are continuously formed on Si surface. LbL layers have improved the adhesion between upper Cu and bottom Si, so they have good adhesion by tape test.

To test the barrier properties, we have annealed the Cu/LbL/Si structure at 500, 600 or 700℃ in vacuum condition for 30min. X-ray diffraction (XRD) and Rutherford backscattering spectroscopy (RBS) results of annealed samples have showed the barrier property of LbL materials. LbL 30nm layer has good barrier property at 600℃ annealed condition, but annealed sample at higher temperature 700℃ has occurred Cu diffusion to Si and Cu_3Si peak has been detected by XRD and RBS results. So flexible LbL material can prevent Cu thermal expansion and diffusion with increasing temperature.





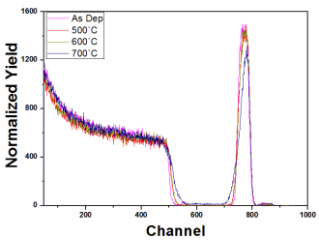


Fig 1. QCM (Quartz crystal microbalance) measured result of PAH/PSS laminar structure

Fig 2. XRD and Fig 3. RBS spectrum of thermal treated samples

[1] F. X. Che, W. N. Putra, A. Heryanto, A. Trigg, X. Zhang, C. L. Gan, IEEE Trans. Comp. Packag. Manuf. Technol. 3, 732 (2013)

[2] J. Cho, Polymer Science and Technology 19, 48 (2008)

Nanostructured Si for Efficient Solar Energy Conversion

Jihun Oh

Graduate School of EEWS (Energy, Environment, Water and Sustainability), KAIST, Daejon 305-701, Korea

E-mail : jihun.oh@kaist.ac.kr

Nanostructured Si is a promising material for low-cost and high efficiency Si solar cells and solar fuel production. Nanostructures have excellent photon management properties such as broad-band antireflection (AR) and light trapping properties that eliminates the conventional Si_3N_4 AR coatings and can allow use of a thin crystalline Si film. Despite this promises, however, nanostructured Si solar cells showed poor optoelectrical performance due to enhanced recombination associated with the nanostructures. In this talk, I will show that nanostructured Si made by a metal-assisted etching technique could suppress optical reflection of silicon to below 3% across the usable solar spectrum with λ <1.2 μm by forming a density-graded layer. With this reduced reflection, we demonstrate an independently confirmed 18.2%-efficient nanostructured Si solar cell under simulated AM 1.5 G illumination by controlling recombination mechanisms in the nanostructures [1]. In addition, I'll present the advantages of using nanostructured Si for photoelectrical water splitting for solar H_2 fuel production [2].

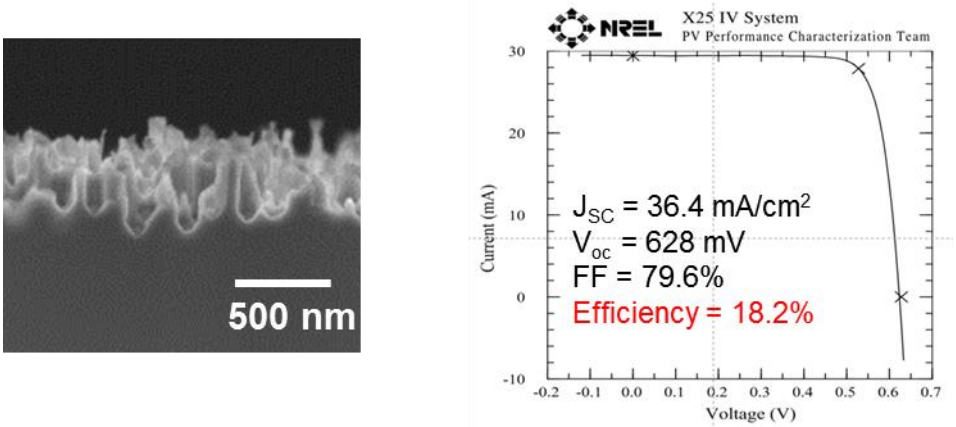


Fig 1. Nanostructured Si solar cells

[1] J. Oh, H.-C. Yuan, and H.M. Branz, Nature Nanotechnology 7, 743(2012).
[2] J. Oh, T.G. Deutsch, H.-C. Yuan, and H.M. Branz, Energy and Environmental Science 4, 1690 (2011).

Effect of Size and Depth of Silicon-nano-holes on Surface Reflectance Reduction for {111} Pyramid-textured Silicon Solar-cells

Jae-Hyoung Shim, Seung-Wook Baek, Ji-Heon Kim, Yun-Hyuk Ko, Jin-Seong Park, Gon-Sub Lee and Jea-Gun Park

Department of Electronics and Computer Engineering, Hanyang University, Seoul 133–791, Republic of Korea

E-mail : parkjgl@hanyang.ac.kr

In recent years, silicon solar cells have been researched to improve power-conversion-efficiency (PCE) through plasma doping, selective emitter, back contact cell, and metallization, surface texturing and anti-reflection coating. In particular, silicon surface texture with various morphologies is one of the effective techniques to achieve high PCE resulting from reducing light reflection at the surface of silicon solar-cells.

In this study, we investigated how the silicon nano-holes affected on the photovoltaic performance of conventional p-type silicon solar cells by utilizing metal-assisted chemical-etching method, as shown in Fig. 1. The size and depth of nano-holes could be controlled by the Ag film thickness deposited by evaporator and etching-time of metal-assisted chemical-etching. However, these nano-structures act as an obstacle for surface passivation using low-frequency plasma-enhanced chemical vapor deposition (PECVD). Therefore, we optimized size and depth of nano-holes by adjusting Ag film thickness and etching-time to take advantages both low surface reflectance and proper surface passivation. As a result, we confirmed the specific correlation between PCE and nano-hole structures which made by metal-assisted chemical-etching (etching time 1 min & Ag film thickness 70 nm), as shown in Fig. 2 . We will report the effect of size and depth of silicon-nano-holes on surface reflectance reduction for {111} pyramid-textured silicon solar-cells and its mechanism.

* This work was financially supported by the Brain Korea 21 Plus Program in 2013, Republic of Korea.

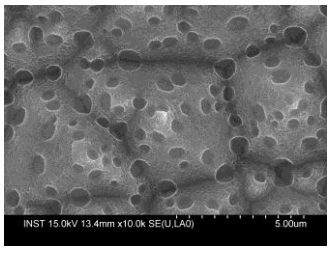


Fig 1. The surface morphology for p-type silicon solar-cells implemented with nano-holes

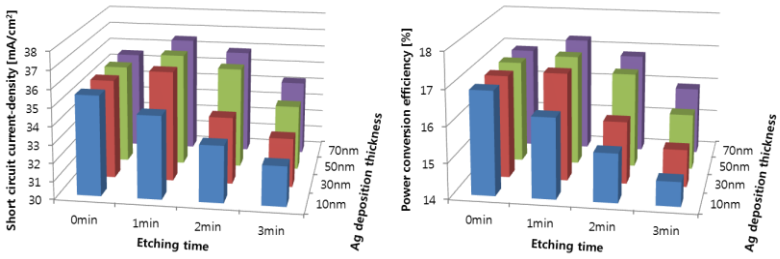


Fig 2. Short circuit current-density and power conversion efficiency for p-type silicon solar-cells implemented with nano-holes

Effect of Se&S composition ratio on Quantum-yield, Power-conversion-efficiency, Energy-down-shifting for CdSe/ZnS Core/Shell Quantum-dot Implemented Silicon Solar-cells

Seung-Wook Baek, Ji-Heon Kim, Jae-Hyoung Shim, Yun-Hyuk Ko, Jin-Seong Park, Gon-Sub Lee and Jea-Gun Park

Department of Electronics and Computer Engineering, Hanyang University, Seoul 133–791, Republic of Korea

E-mail : parkjgl@hanyang.ac.kr

Silicon solar cells mainly absorb visible light, although the Sun also emits ultraviolet (UV), visible and infrared lights. Since the surface reflectance of a {111} textured SiN_X anti-reflective layer in the UV wavelength region (250~450 nm) is higher than ~27%, silicon solar-cells cannot convert UV light into photovoltaic power effectively. We implemented the concept of energy-down-shift using CdSe/ZnS core/shell quantum-dots (QDs) on p-type silicon solar-cells with a {111} textured SiN_X film anti-reflective layer to absorb more UV light, CdSe/ZnS core/shell QDs demonstrated clear evidence of energy-down-shift, which absorbed UV lights and emitted green-light photoluminescence-signals with 542 nm wavelengths. The implementation of 0.2 wt% green-light emitting CdSe/ZnS core/shell QDs reduced the surface reflectance of the {111} textured SiN_X anti-reflective layer from 27 to 15% and enhanced the external-quantum-efficiency of solar-cells around 30% in the UV wavelength region, thereby enhancing power-conversion- efficiency for p-type silicon solar-cells by 5.5%.

* This work was financially supported by the Brain Korea 21 Plus Program in 2013, Republic of Korea.

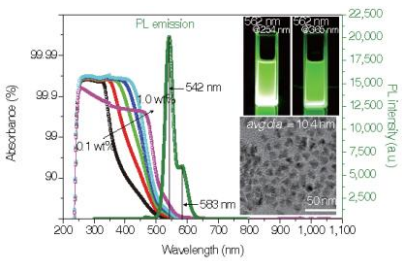


Fig 1. The UV-visible absorbance and photo- luminescence intensity

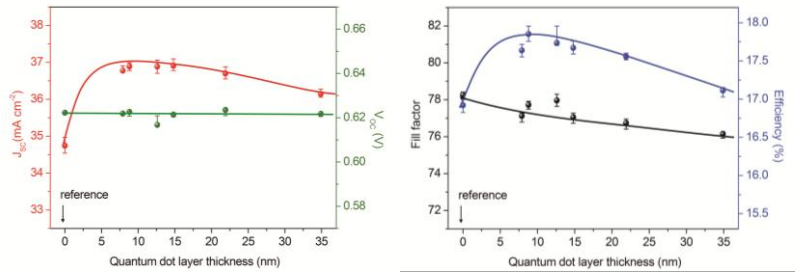


Fig 2. Photo-voltaic performance for p-type silicon solar-cells implemented with QDs

Silicon Solar-cells Implemented with Energy-down-shifting using CdZnS/ZnS Core/Shell Quantum-dot

Yun-Hyuk Koh, Seng-Wook Baek, Gon-Sub Lee, and Jae-Gun Park
Department of Electronics and Computer Engineering, Hanyang University, Seoul 133–791, Republic of Korea
E-mail : parkjgl@hanyang.ac.kr

In recent study, silicon solar cell performance has been great progressed due to mature understanding about silicon material properties and fabrication process optimization, etc. However, the power-conversion-efficiency (PCE) of silicon solar cells has increased slowly for last 10 years. In order to overcome the current limitation of the PCE of silicon solar-cells, the following technologies has been studied such as nano-structures on surface for light confinement, selective emitter or local back contact structures for better absorption of the sun light, etc. Thus, a novel technology to improve the PCE of silicon solar-cells should be introduced. In our study, we investigated how CdZnS/ZnS core/shell quantum dots implemented on <111> textured p-type silicon solar-cells enhance the PCE of silicon solar-cells. In particular, the CdZnS/ZnS core/shell quantum dots show low amount of absorption in visible wavelength, as shown in Fig. 1. The implementation of CdZnS/ZnS core/shell QDs reduced the surface reflectance of the {111} textured SiN_X anti-reflective layer from 25 to 17% and enhanced the external-quantum-efficiency of solar-cells around 33% in the UV wavelength region, thereby enhancing power-conversion-efficiency for p-type silicon solar-cells by 1.08%, as shown in Fig. 2.

* This work was financially supported by the Brain Korea 21 Plus Program in 2013, Republic of Korea.

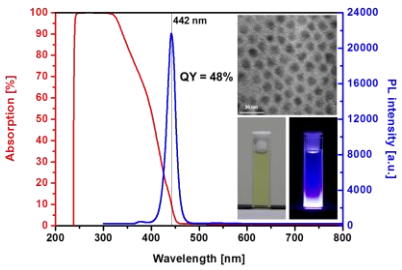


Fig 1. The UV-visible absorbance and photo- luminescence intensity

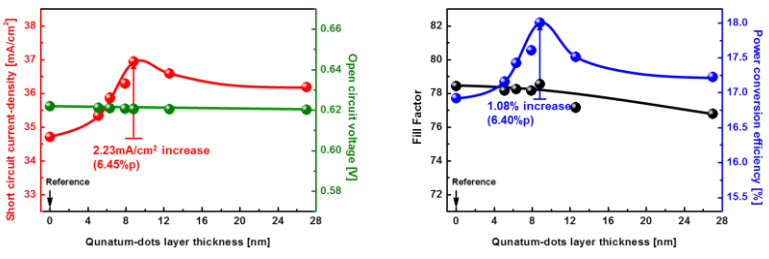


Fig 2. Photo-voltaic performance for p-type silicon solar-cells implemented with QDs

Effect of ultra-thin active layer thickness on the subthreshold slope and bipolar bias stress-induced degradation in amorphous InGaZnO thin-film transistors

Dongjae Shin, Sungwoo Jun, Kyung Min Lee, Hyeongjung Kim, Chunhyung Jo, Jaeman Jang, Jaewook Lee, Sung-jin Choi, Dong Myong Kim, and Dae Hwan Kim [a)]

School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

E-mail : [a)] drlife@kookmin.ac.kr

Subthreshold slope (SS) as well as threshold voltage (V_T) can be controlled by changing only the active layer thickness of amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) with keeping the other process conditions the same [1]. However, the effects of ultra-thin active layer have been rarely investigated.

In this work, we report the effect of ultra-thin (thinner than 40 nm) active layer thickness (T_{active}) on SS and bipolar bias stress-induced degradation in a-IGZO TFTs by using the device simulation result which was well calibrated with experimental *I-V* characteristics taken from a-IGZO TFTs with T_{active}≥50 nm [Fig. 1(a) and (b)]. Subgap density-of-states (DOS) [Fig. 1(c)] extracted from the photonic response of *C-V* curve [2] and the DOS-incorporated DeAOTS-based device simulation [3,4] were used as main methods. It was found that the SS optimum existed around T_{active}~XX nm and its related mechanism will be discussed. The surface electric field and electron/hole concentration in IGZO TFTs under positive/negative bias stress were also investigated as the function of T_{active}. We also found that the positive/negative bias stress made the IGZO TFTs more/less degraded as T_{active} becomes thinner. Our result implies that T_{active} plays critical role of optimizing either SS or the degradation under real circuit operation, e.g., duty of each frame, especially cases of using dynamic bipolar gate bias.

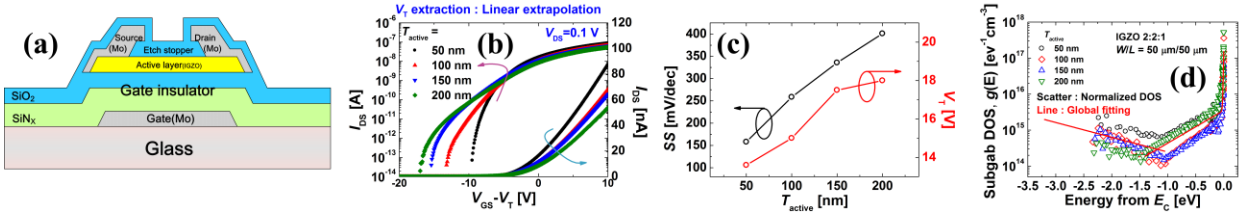


Fig 1. Schematic of a-IGZO TFT and measured T_{active}-dependent electrical performance

[1] D. Kong et al., IEEE Trans. Electron Devices 32, 1388 (2011).
[2] H. Bae et al., SID Symposium Digest of Technical Papers. 44, 1033 (2013).
[3] Y. W. Jeon et al., IEEE Trans. Electron Devices 57, 2988 (2010).
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Oxide-based thin-film transistors with artificial superlattice channel structure

Cheol Hyoun Ahn and Hyung Koun Cho
School of Advanced Materials Science and Engineering, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do, Republic of Korea
E-mail : c2hyoun2@skku.edu

Recently, oxide-based thin-film transistors (TFTs) have been emerged as promising alternatice materials a-Si for the realiztion of next-genertion display, becuase of their excellent mobility, transparency, and utility of low-temperature process [1, 2]. However, instability on oxide-based TFTs under various condition such as bias, temperature, and illumination stress have been issued for commercialization becuase of the was always exposed to light, gate voltage stressed suring operation. To obtain highly stable oxide-based TFTs, many studies have been devoted to the development of robust channel layers by adjusting the oxygen content and adding defect stabilizer elements for suppressed defect in channel layer. Unfortunately, the these TFTs normally suffer from relatively low mobility [3].

In this work, we have introduced a novel channel structure for the realization of high-performance and high-stability in the oxide TFTs, which was based on the atomically controlled ZnO/Al_2O_3 superlattice structure [4]. The performance and device stability of superlattice TFTs were investigated and compared with ZnO TFTs. The superlattice TFT exhibited high field effect mobility of > 27 cm^2/Vs. Also, superlattice TFT were showed high-stability under gate bias and temperature stress. The microstructures of ZnO and superlattice thin film were anlyzed using atomic for microscopy, X-ray diffraction, and transmission electron microscopy. The electrical performance of the TFT devices was measured using an HP4145B semiconductor parameter analyzer.

[1] K. Nomura et al. Nature 432, 488-492 (2004)
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[4] C. H. Ahn et al. Sci. Rep. 3, 2737 (2013)

Oxygen vacancy-dependent density-of-states and its effect on the negative bias illumination stress-induced degradation in amorphous oxide semiconductor thin-film transistors

Kyung Min Lee, Sungwoo Jun, Hyeongjung Kim, Chunhyung Jo, Jaeman Jang, Jaewook Lee, Dong Jae Shin, Jun Tae Jang, Sungju Choi, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim [a].

Department of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

[a] E-mail : drlife@kookmin.ac.kr

Negative bias illumination stress (NBIS)-induced instability have emerged as a challenging issue for mass production of the display backplanes using amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) [1]. On the other hand, oxygen vacancy (V_O) has been well known as critical material/process-controlled parameter for AOS technology [2]. However, details for the effect of the amount of V_Os on the density of subgap states (DOS) experimentally extracted from TFT characteristics have been rarely addressed. Here we report the V_O-dependent DOS and its effect on NBIS degradation in amorphous InGaZnO (a-IGZO) TFTs [Fig.1 (a)]. The amount of V_Os was controlled by changing the oxygen flow rate (OFR) of the dc sputtering with a gas mixture of Ar/O_2 (35/OFR sccm) from 21, 42 to 63. DOS was extracted by the monochromatic photonic capacitance-voltage technique [3]. It was found that the OFR-controlled amount of V_Os changed the DOS near valence band edge as well as that the DOS near conduction band edge [Fig. 1(c)], which explained well the OFR-dependent I-V/mobility curve [Fig. 1(b)] and NBIS degradation [Fig. 1(d)]. Noticeably, the OFR-sensitive DOS peak was found to be located around in 1 eV above valence band edge, which was consistent with [4]. Physical mechanism and details on methods will be presented. Our results are expected as great promise in not only the physical insight on the V_O-effect on the trade-off between the performance and instability but also the method for optimizing the amount of V_Os in AOS TFT technology.

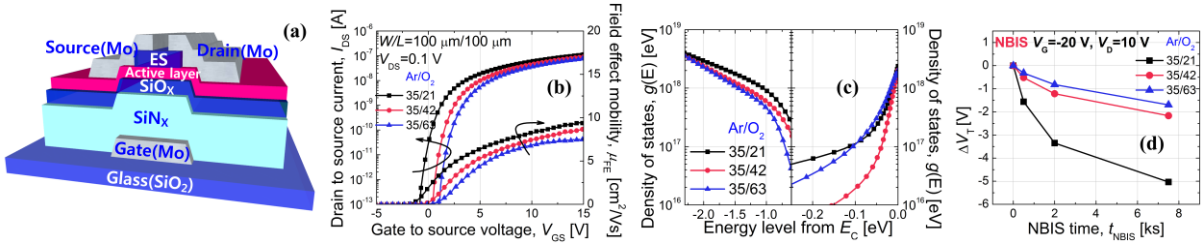

Fig. 4. (a) a-IGZO TFTs device structure, (b) the I_{DS}-V_{GS} transfer curve and field-effect mobility, (c) extracted the subgap DOS, (d) and the NBIS-induced ΔV_T as a function of stress time.

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High Bright Full Color Electroluminescence Device driven by Alternating Current (AC)

Sung Hwan Cho, Ihn Hwang, Cheolmin Park*
Department of Materials Science and Engineering, Yonsei University, Seoul, 120-749, Korea
E-mail : cmpark@yonsei.ac.kr

We report an extremely high brightness of a solution-processed polymer AC EL device with its brightness of approximately 6000 Cd m^{-2} operating at an applied voltage and AC frequency of 75 V and 400 kHz, respectively. Two novel strategies were employed for such a high brighness of the device: the utilization of AC driven fluorescence resonance energy transfer (FRET) between fluorescent polymers with different colors[1] and incorporation of dilute agents, self assembled block copolymer micelles that restricted the interchain interaction of a fluorescent polymer[2]. The Efficient long range FRET of a solution-blended BGR fluorescent polymers synergistically occurred with the interchain nonradiative fluorescent quenching further suppressed by insulating nanometer scale micelles, giving rise to such a high brightness of light emission approximately 10 times greater than that of the individual color emission.

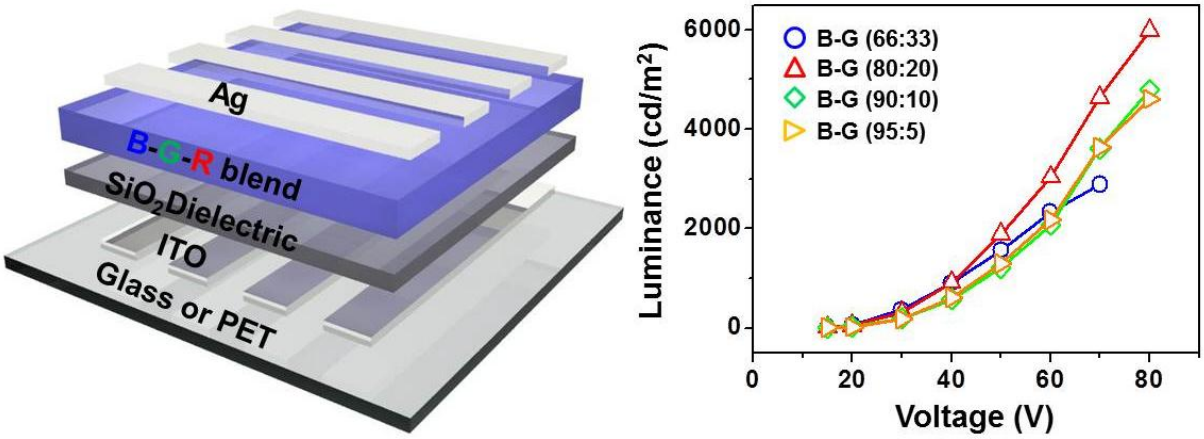

Fig 1. The schematic of novel AC EL device architecture and its Luminance-Voltage characteristics

[1] S. Kan, X. Liu, F. Shen, J. Zhang, Y. Ma, G. Zhang, Y. Wang, J. Shen, Adv. Funct. Mater. 13, 603 (2003).
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Effect of the RF power in sputter system on performance and photoelectric degradation of amorphous indium-gallium-zinc-oxide thin-film transistors

Jun Tae Jang, Kyung Min Lee, Hyeongjung Kim, Jaeman Jang, Dong Jae Shin, Sungju Choi, Jaewook Lee, Chunhyung Jo, Sungwoo Jun, Sung-Jin Choi, Dong Myong Kim and Dae Hwan Kim[a)]

Department of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

E-mail : a) drlife@kookmin.ac.kr

Although the radio frequency (RF) power is a critical process-controlled parameter which determines not only the performance but also the photoelectric degradation, its effect on electrical performance and reliability of the RF-sputtered amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistors (TFTs) has been seldom systematically investigated [1– 2].

Here we analyzed the effects of RF power on the dc performance and the negative bias illumination stress (NBIS)-induced degradation which has been pointed out to be a main hurdle to real commercialization of a-IGZO TFT-driven active-matrix liquid crystal displays (AMLCDs). It was found that the RF power controlled very sensitively the trade-off between the dc performances such as ON current, mobility and subthreshold swing [Fig. 1(a), (b)], and the long-term NBIS instability [Fig. 1(c)]. The RF power-dependent density of subgap states in a-IGZO TFTs also suggested that higher power made the states near the conduction band edge [$g_A(E)$] less and those near the valence band edge [$g_D(E)$] more, and vice versa, explaining very well the RF power dependencies of the performance and instability. Finally, related physical mechanisms, details on parameter-extraction and analysis, and the recovery after NBIS will be discussed.

Our results are expected to give useful physical insight on optimizing the sputtering power for high-performance highly reliable oxide TFT technology.

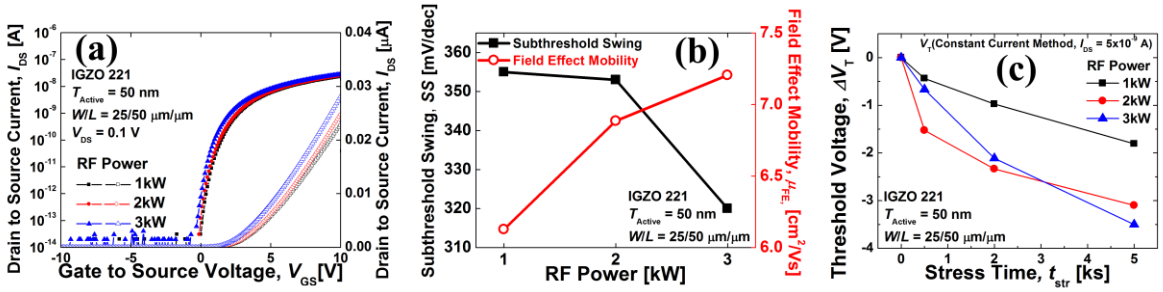

Figure 1 (a) Initial transfer characteristics, (b) SS and field effect mobility, (c) Stress time-evolution ΔV_T of RF power split in a-IGZO TFTs.

[1] H. Q. Chiang, *et al*, *J. Non-Cryst. Solids*, vol. 354, pp. 2826 – 2830 (2008)

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Precharging of Counter Electrode in Viologen-anchored TiO_2 Nanostructure Electrode Based Ultrafast Electrochromic Devices

Seong M. Cho, Chil Seong Ah, Tae-Youb Kim, Juhee Song, Hojun Ryu

Reflective Display Research Section, Next Generation Display Research Department, Convergence Components and Materials Research Laboratory, Electronics and Telecommunications Research Institute, 218 Gajeongno, Yuseong-gu, Daejeon, 305-700, KOREA

E-mail : smcho@etri.re.kr

Electrochromic materials have been attracting much interests for several decades because of their unique property to control the transmittance of visible light[1]. The electrochromic materials can be applied to smart window, electrochromic mirror for atomobile and elecrochromic display. For the application as display, the electrochromic device should have very fast swithing speed. Recently utrafast electrochromic devices utilizing viologen-anchored TiO_2 nanostructured electrode were suggested[2] and have attracted great attention because of their ultrafast switching speeds. In prestent study, the elecrochromic cells with a viologen-anchored TiO_2 nanostruectured electrode and a Sb-doped SnO_2 nanostructured electrode were constructed, and the effects of precharging of the counter electrode (Sb-doped SnO_2) with Li^+ ions before the cell construction were investigated. The precharged device showed much stronger modulaton of transmittance compared with those of the unprecharged devices. It means that by precharging the counter electrode the operating voltage of the electrochromic device could be substantially lowered. The precharging conditions were optimized with respect to the operation voltage and the amplitude of transmittance modulation.

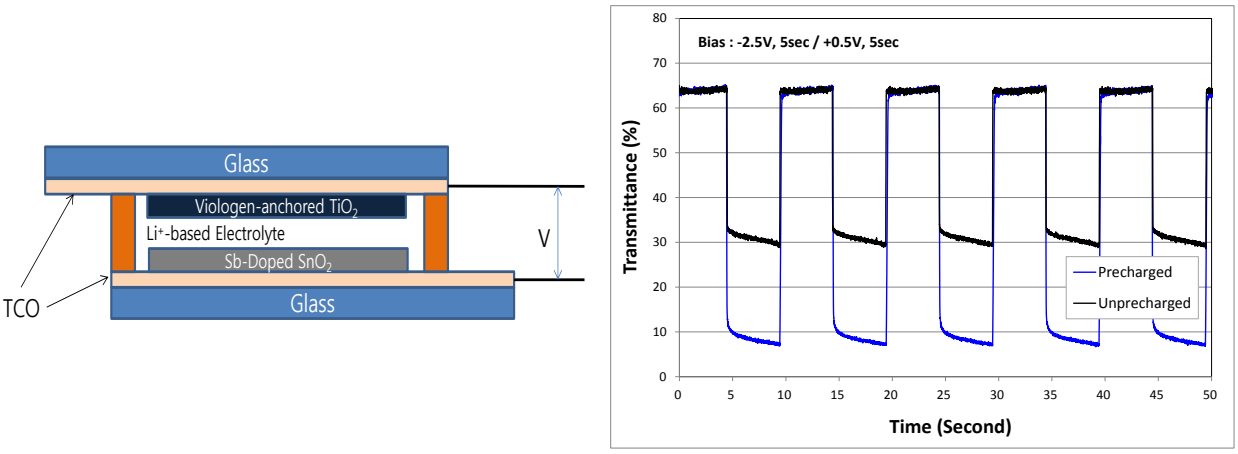


Fig 1. The structure of the ultrafast electrochromic device and transmittance modulation of the electrochromic device

[1]. C.G. Granqvist, *Handbook of Inorganic Electrochromic Materials*, Elsevier, Amsterdam (1995).

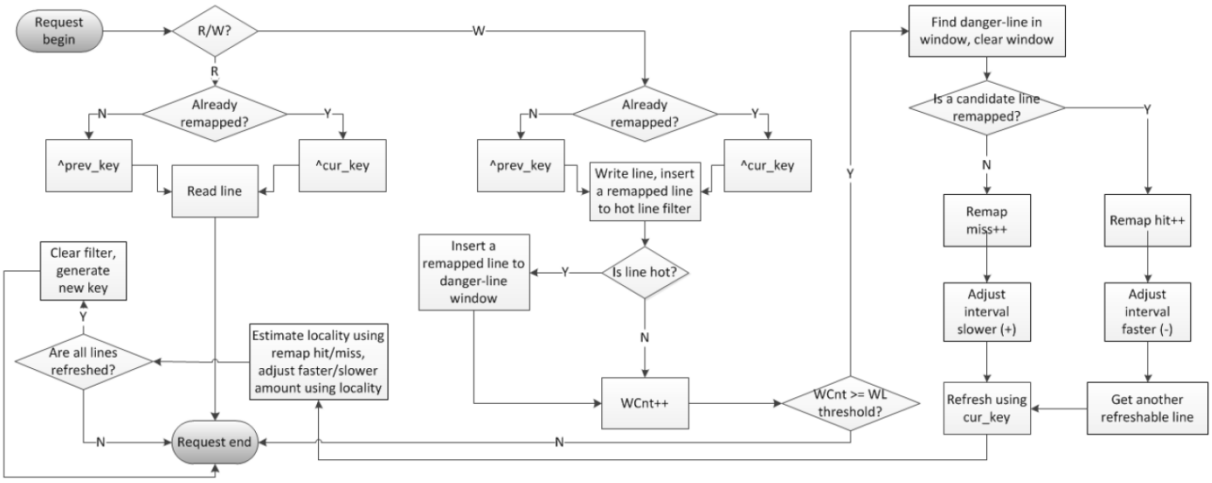
[2]. M. Grätzel, Nature 409, p575 (2001)

Wear-Leveling Algorithm for Phase Change Memory using Danger-Line First Address Randomization

Dong-gun Kim
Design Technology System Architecture Team, SK hynix Inc., Icheon, Gyunggi-Do 467-701, Korea
E-mail : donggun.kim@sk.com

Phase Change Memory (PCRAM) becomes a convincing candidate for future computer systems. It has many advantages such as non-volatility, a fast latency and high density. However, PCRAM has several disadvantages and the important one among them is limited endurance. However, conventional wear-leveling algorithm for NAND flash cannot be applied to PCRAM because PCRAM has small read/write unit and architecture for wear-leveling is not considered yet.

In this paper, we propose the advanced wear-leveling algorithm for reliability of PCRAM. To distribute write operations evenly, the proposed algorithm detects frequently written lines using 2-level filter and rescue them first with randomizing address. Also the interval of wear-leveling is dynamically adjusted using estimated locality of write patterns. This algorithm increases lifetime of PCRAM by 2.08 times than conventional algorithms with extremely concentrated attack condition.



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Identifying Redundant Inter-Cell Margins and Its Application to Technology Mapping

이유종, 심성보, 신영수
KAIST 전기및전자공학과

최신 standard cell 들은 그림 1(a)와 같이 레이아웃 양쪽에 여백 (inter-cell margin)을 내장하고 있는데, 이것은 리소그래피 과정에서 빛의 간섭현상으로 셀들 사이에 패턴결함이 생기는 것을 사전에 방지하기 위한 안전장치이다[1]. 빛의 간섭현상 유무는 레이아웃 형태에 의해 결정되므로 어떤 셀 조합간에는 여백 없이도 안전하게 리소그래피를 할 수 있는 경우가 있다. 28nm 상용 라이브러리를 가지고 다양한 셀 조합에 대해 리소그래피 시뮬레이션을 해본 결과 대략 35%의 셀 조합에 대해 여백이 불필요함을 확인할 수 있었다. 만일 설계과정에 이러한 사실을 적절히 이용할 수 있다면 칩의 면적을 줄이는데 도움이 될 것이다. 모든 셀 조합에 대해 리소그래피 시뮬레이션을 하는 것은 현실적으로 불가능한데, 다행스럽게 셀 조합의 레이아웃 패턴을 소수의 그룹으로 분류한 다음 각 그룹에 대해 시뮬레이션을 해서 모든 조합에 대해 여백의 필요유무를 사전에 테이블로 만들어 두는 것이 가능하다[2].

본 논문에서는 로직합성의 일부분인 테크놀로지 매핑 단계에서 이 사실을 이용하고자 한다. 그림 1(b)와 같이 로직이 그래프형태로 (subject graph 라고 불림) 표현되어 있을 때 인접한 노드는 레이아웃에서도 인접하게 배치될 확률이 높다. 따라서 인접한 k 개의 노드들을 그룹핑한 다음 각 그룹에 대해 여백이 최대한 줄어드는 순서를 찾고, 그 순서대로 레이아웃상에서도 배치되게 하였다. 제안하는 방법은 SIS[3] 로직합성 패키지에 구현하였고, k=7 일때 여러 테스트회로에 대해 평균 8%의 면적이 줄어드는 것을 관찰하였다.

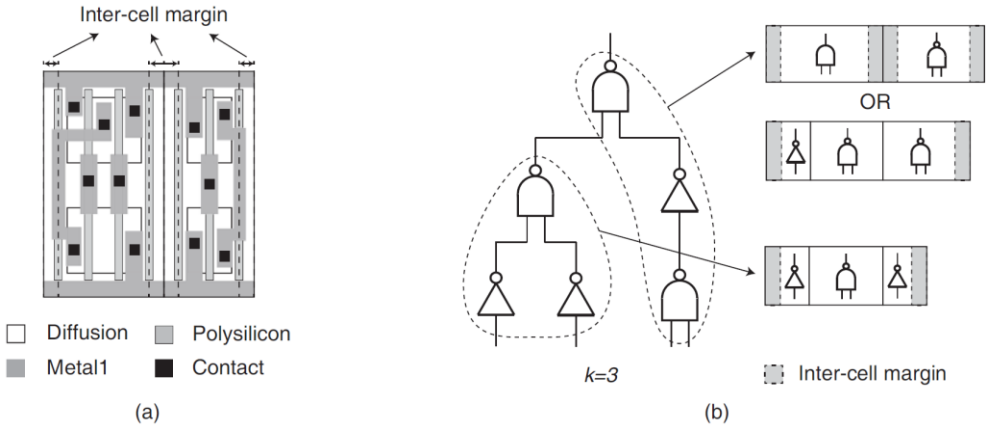

그림 1. (a) 셀간 여백을 내장한 셀 레이아웃, (b) 셀간 여백 제거를 고려한 테크놀로지 매핑.

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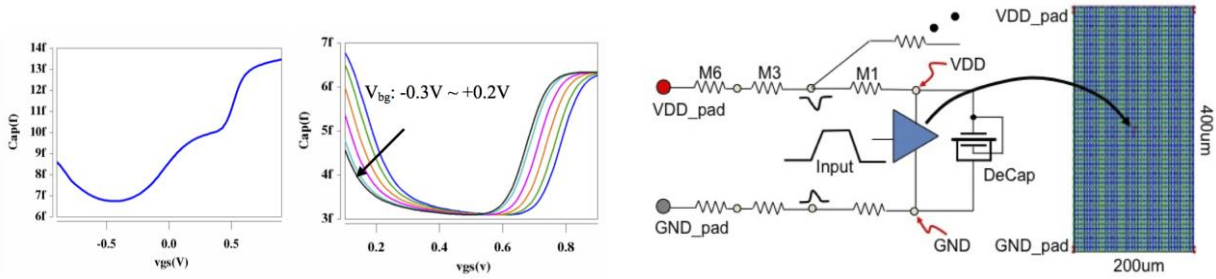
PEEC-based Dynamic IR drop Analysis with On Chip Decoupling Capacitor of the Double-Gate FinFETs

Jaemin Lee and Youngmin Kim
School of Electrical and Computer Engineering, UNIST, Ulsan 685-789, Korea
E-mail : youngmin@unist.ac.kr

As the technology node has scaled down below 32 nm, the supply voltage has decreased to 1 V and the current demands for active devices have increased. Therefore, the supply noise due to the IR drop in the power delivery network (PDN) has become a critical problem for robust circuit operation. Huge decoupling capacitors are introduced to overcome the supply voltage fluctuations [1]. In this study, we investigate a 32-nm double-gate FinFET device for a decoupling capacitor in the PDN. The circuit designers can independently control both the gates in the double- gate FinFET [2]. We compare the supply and ground noise reduction in the conventional planar 2D CMOS and in various FinFET structures in a PEEC-based [3] practical PDN and propose the best decoupling capacitor design strategy for double-gate FinFETs. The simulation results show that we can achieve an increased reduction in the supply voltage noise up to 50% by shorting the front gate and back gate together.



(a) (b)

Fig 1. (a) C-V plot of the CMOS and the FinFET at different back gate biases and (b) Power delivery network (PDN) structure with clock buffers.

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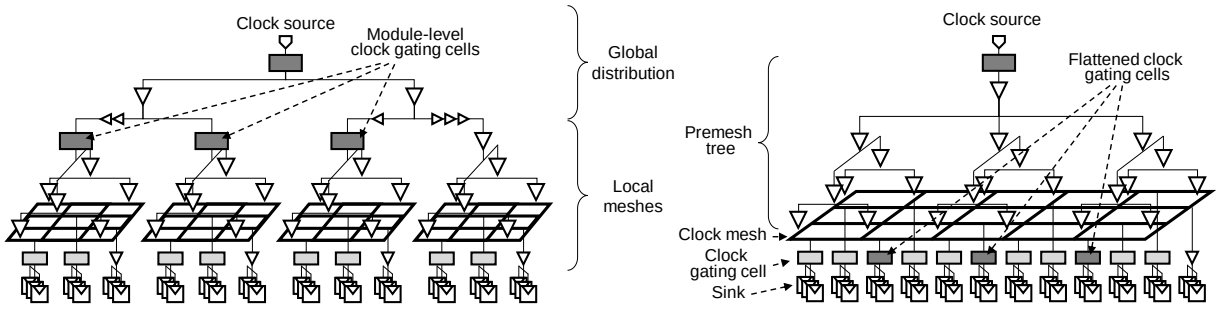
Design and Optimization of Mesh Clock Network with Multi-Level Clock Gating

Jinwook Jung, Dongsoo Lee, and Youngsoo Shin
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea

저전력 설계를 위해 주로 사용하는 clock gating 은 그림 1(a)와 같이 흔히 계층적으로 적용된다. 이런 경우에 clock mesh [1]는 모듈 수준에서 그림 1(a)와 같이 적용하는 것이 자연스러우나 복수의 mesh를 설계하는 어려움이 생긴다. 반면에 clock gating의 계층 구조를 없앤 다음 그림 1(b)와 같은 단일한 mesh 를 사용하게 되면 설계는 용이해지지만 clock gating을 보다 자주 적용할 수 없게 되므로 전력 소모 측면에서 불리하다. 본 논문에서는 이 두 가지 설계 옵션을 다양한 테스트 회로를 이용해 실험적으로 탐색해보고자 한다.

그림 1(a)와 같은 구조를 채택하는 경우, mesh 들간에 서로 중첩되지 않게 하려면 회로의 배치과정에 제한을 가해야 하고, 반면에 중첩을 허용하게 되면 mesh 에 사용되는 wire 의 길이는 늘어나지만 배치를 보다 자유롭게 할 수 있다. 이 두 가지 설계옵션도 본 논문에서 탐색해 보고자 한다.



(a) (b)

그림 1. 계층적인 구조를 갖는 multi-level clock gating 에서의 mesh clock network: (a) 복수의 mesh 를 모듈 수준에서 적용한 경우, (b) 회로 전체에 단일한 mesh 를 갖도록 clock gating 의 계층 구조를 없앤 경우.

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Synthesis of Multi-Stage Gate-Level Clock Gating

Inhak Han and Youngsoo Shin
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : ihhan@dtlab.kaist.ac.kr, youngsoo@ee.kaist.ac.kr

클럭 게이팅 방식은 크게 1 단식과 다단식으로 나눌 수 있다. 1 단식은 클럭 게이팅 셀(CGC)이 플립플롭의 클럭만 제어하는 방식이고, 다단식은 그림 1(가)와 같이 한 CGC 가 다른 CGC 와 플립플롭의 클럭을 동시에 제어하는 것이 가능한 방식이다. 게이트레벨 클럭 게이팅은 게이트레벨 넷리스트에 클럭 게이팅을 적용하는 방법으로, 1 단식과 다단식 모두에 적용이 가능한데, 본 논문에서는 2 단식 게이트레벨 클럭 게이팅을 다룬다. 게이트레벨 클럭 게이팅을 위한 합성 문제는 크게 같은 게이팅 신호를 공유하는 플립플롭 그룹들을 만드는 그룹핑 문제와 각 그룹의 게이팅 신호를 합성하는 문제로 나뉜다. 그룹핑 문제를 단순한 greedy algorithm 으로 풀면, 한 CGC 를 공유하는 플립플롭의 개수가 많아질 수 있는데, 각 플립플롭의 게이팅 신호를 모두 ANDing 한 신호가 게이팅 로직이 되기 때문에, 게이팅 로직 합성이 어려워질 수 있다. 그래서 본 논문에서는 전체 플립플롭들을 2 개씩 그룹지어서 최대 파워 이득을 얻는 maximum weight perfect matching (MWPM) [1]을 이용한다. 첫 MWPM 를 이용해서 플립플롭 그룹들을 만든 후, 더 이상의 파워 이득이 없을 때까지, 반복적으로 그룹들에 MWPM 를 적용하여 최종 그룹을 얻는다. 최종 그룹은 플립플롭 개수가 균일하여 게이팅 로직이 비교적 단순하다. 플립플롭 그룹핑을 마친 후에는 게이팅 신호를 최소의 게이트 수로 합성한다 [2]. 몇 개의 테스트 회로들에서, 2 단식 클럭 게이팅은 평균 29%, 최대 35%의 파워 감소를 보였고, 1 단식은 평균 15%의 파워 감소를 보였다.

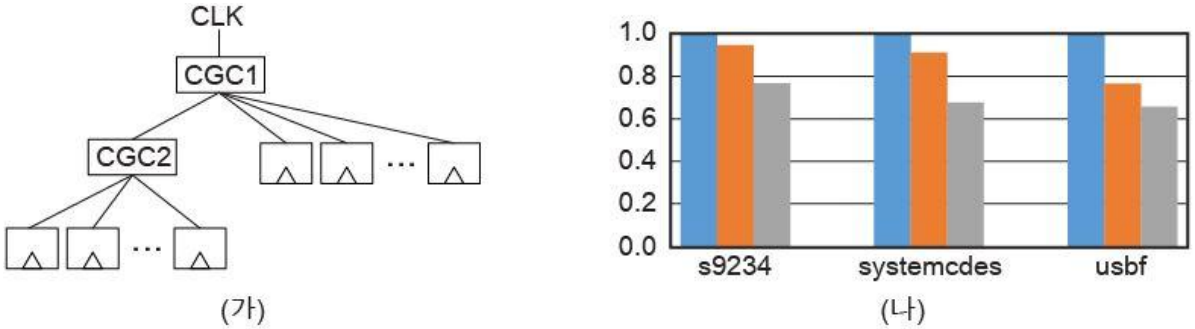

그림 1. (가) 다단식 클럭 게이팅과 (나) 원 회로 (파란색 바)와 1 단식 (주황색 바), 2 단식 (회색 바) 클럭 게이팅이 적용된 회로들의 파워 소모 비교.

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Optimized Heterogeneous 3D Networks-on-Chip for High Performance System-on-Chip Design

Michael Opoku Agyeman
School of Engineering and Built Environment, Glasgow Caledonian University, Glasgow, UK
E-mail : Michael.Agyeman@gcu.ac.uk

The design practicality of 3D NoCs face several challenges such as thermal issues, high power consumption and area of the conventional 3D router, high complexity and cost of vertical link implementation. To mitigate the performance and manufacturing cost of 3D NoCs, heterogeneous architectures have emerged to combine 2D routers and 3D routers in NoCs producing 3D NoCs with lower area and power consumption while maintaining the performance of homogeneous 3D NoCs [1]. To increase the performance, reliability while reducing the energy consumption of heterogeneous 3D NoCs. This paper presents a multistage heterogeneous architecture generation algorithm. Firstly, a power and reliability aware application mapping algorithm is proposed to generate an optimized 3D NoC dimension as well as a heterogeneous 3D NoC architecture with minimum number of 3D routers. Secondly, by exploiting the communication dynamics of the application in the newly generated architecture, a buffer redistribution approach is used to generate an optimized heterogeneous architecture. The algorithm has been evaluated and compared with existing heuristic mapping algorithms (CastNet, Onyx and Nmap), optimal mapping (branch-and-bound) and a random mapping with various realistic traffic patterns. Experimental results show heterogeneous 3D NoC architectures generated by our multistage approach have lower energy consumption and significant reduction in packet delays compared to the existing architectures.

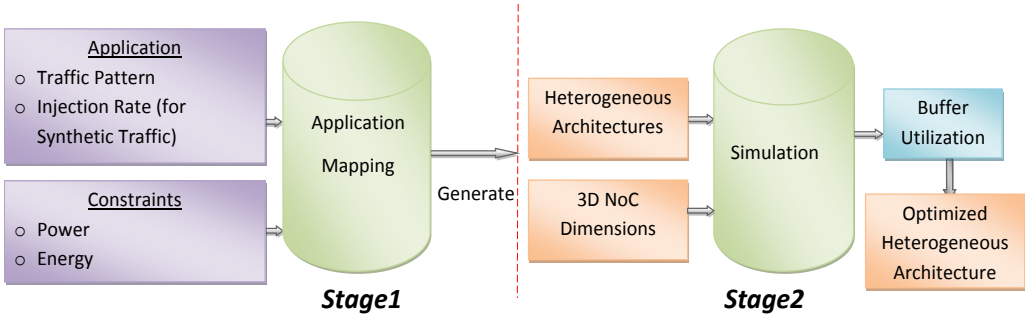

Fig 1. Multistage Optimized Heterogeneous 3D NoC Architecture Generation.

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Fault-tolerant CGRA-based Multi-Core Architecture[1]

Seungyun Sohn, Heesun Kim, and Yoonjin Kim
Department of Computer Science, Sookmyung Women's University, Seoul 140-742, Korea
E-mail : {kjkj35, khs9101, ykim}@sookmyung.ac.kr

With the increasing defect rate in semiconductor technology, there has been growing need for fault-tolerant systems that can maintain functionality in the presence of multiple failed components. Specially, such a fault-tolerance is necessary for embedded systems to be severely constrained by the harsh environment. To guarantee reliability in the embedded system, the computing engines such as embedded processsors or accelerators should be tolerant to prevent decommissioning the entire systems from a few failures. In order to implement fault-tolerant computing engines, most of researches have taken redundant modules into account – the extra modules enable system to keep its running even though the main module meets fault. Therefore, in terms of redundancy, coase-grained reconfigurable architecture (CGRA)-based multi-core architecture has been expected as a suitable solution because CGRAs include multiple processing elements and storage units that can be reconfigured. Until now, there have been a few research projects based on fault-tolerant CGRA with voter [1] or undo-retry [2]. However, they only show implementations applied with general fault-tolerant design schemes as well as their works are limited to single CGRA. Therefore, in this paper, we propose a new reliable multi-CGRA fabric for the efficient replacement of the modules driving malfuction. The proposed fabric enables exploiting the inherent redundancy and reconfigurability of the CGRA for fault-recovery.

We make use of the multi-CGRA in Fig 1 as base architecture for comparison with proposed architecture. It is composed of a general purpose processor (GPP), a DMA, four CGRAs, and

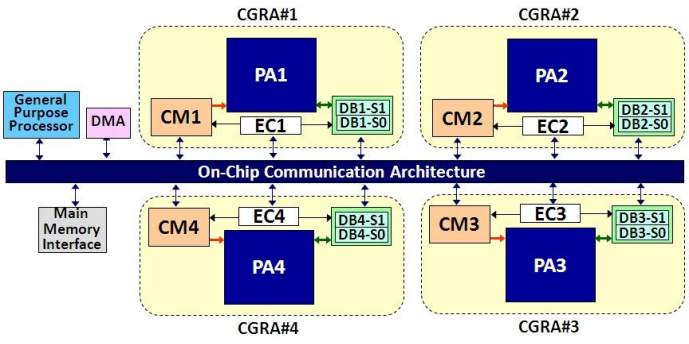

Fig 1. CGRA-based multi-core architecture.

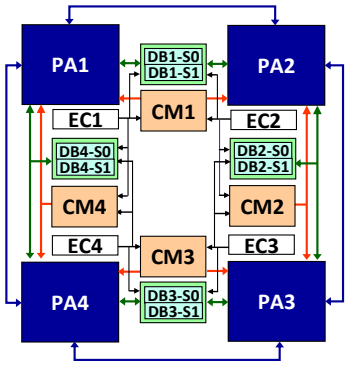

Fig 2. Ring-based sharing fabric (RSF).

[1] This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2011-0013282) and by IC Design Education Center (IDEC).

on-chip communication architecture which couples them. Single CGRA consists of PE array (PA), data buffer (DB), configuration memory (CM), and execution controller (EC). The proposed multi-CGRA fabric based on four CGRAs is shown in Fig. 2 – it is called ring-based sharing fabric (RSF). The RSF connects all of the PAs through single-cycle interconnections and a DB (or a CM) is shared by two adjacent PAs as Fig 2. Such interconnections are utilized for inter-CGRA reconfiguration that enables efficient resource utilization when faults occur - inter-CGRA reconfiguration means that use of each component is not limited to a CGRA.

In order to show the process of the fault-recovery on the RSF, we assume an example that some faults occur in the base architecture as Fig 3. In this case, only one component is broken in each CGRA but no CGRA can normally operate despite most of components are available – it is very typical case that entire system is decomissioned by a few failures. However, Fig 4 shows that the same faults occur in the RSF but it makes 3 CGRAs alive by efficient replacement of the broken modules whereas the base architecture loses all of CGRAs. Such a fault-recovery can be achived by inter-CGRA reconfiguration exploiting the inherent redundancy of the multi-CGRA.

Experimental results show that the proposed RSF shows area/delay/power overhead of up to 19%/10%/21.73% with increasing the number of CGRAs (4~16) when compared with the conventional CGRA-based multi-core architectures.

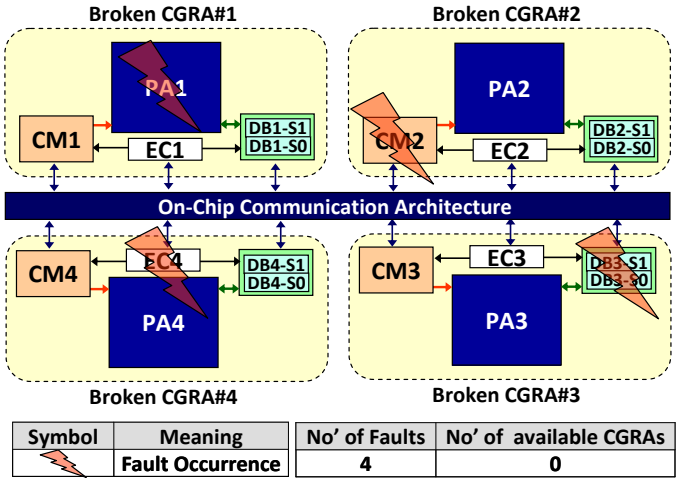

Fig 3. An example when 4 CGRAs have faults.

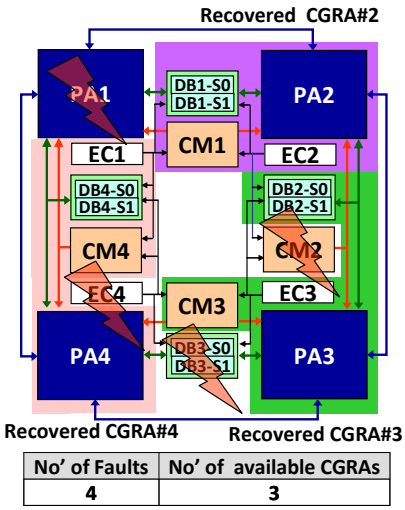

Fig 4. Fault-recovery on RSF.

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A 256-Radix Crossbar Switch using Mux-Matrix-Mux Folded-Clos Topology

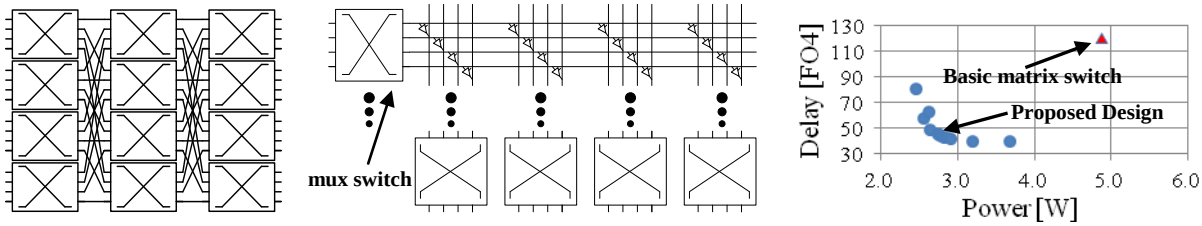
Sung-Joon Lee and Jaeha Kim

Department of Electrical and Computer Engineering, Inter-university Semiconductor Research Center

Seoul National University, Seoul, Korea

E-mail : sjlee@mics.snu.ac.kr

This paper describes a high-radix crossbar switch design with low latency and power dissipation for Network-on-Chip (NoC) applications. The reduction in latency and power is achieved by implementing the switch as a collection of low-radix switches rather than as a single high-radix switch. However, such an approach may not be straightforward to realize in ICs, since for instance, the folded-clos design in [1] with identical sub-switches may result in unequal wire lengths connecting between them. The proposed crossbar switch solves this problem by implementing the first- and third-level switches as multiplexer crossbars which is more efficient than matrix crossbars in point of area and power [2] while implementing the second-level ones as matrix crossbars as shown in Fig. 1(b). This mux-matrix-mux architecture resembles a memory design where the row decoder, memory array, and column multiplexer correspond to the first-level mux, second-level matrix, and third-level mux, respectively. In this architecture, the wire lengths become uniform and therefore their latencies are equally critical. The second-level matrix crossbar is not a full switch and the available spaces are utilized by the additional circuits necessary to introduce the hierarchy in the matrix that can further reduce the latency and power without the area penalty. The proposed 256-radix, 8-bit crossbar switch is designed in 65nm CMOS and its simulation results demonstrate 2.75W of power and 44.91-FO4 delay at 500-MHz operation which is only 56.5% and 37.1% of those of the basic matrix switch, respectively (Fig. 1(c)).



(a) (b) (c)

Fig 1. (a) Folded-clos topology in radix-16, (b) mux-matrix-mux crossbar switch architecture and (c) simulated delay-power results at 500MHz.

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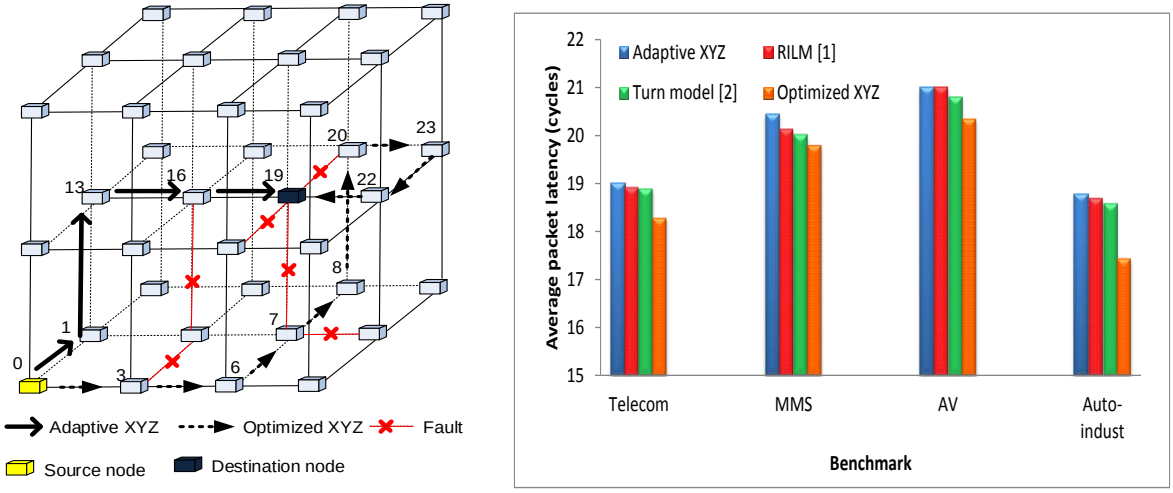
An Efficient Fault-Tolerant Routing Algorithm for 3D Networks-on-Chip

Michael Opoku Agyeman
School of Engineering and Built Environment, Glasgow Caledonian University, Glasgow, UK
E-mail : Michael.Agyeman@gcu.ac.uk

Recently three-dimensional Networks-on-Chips (3D NoCs) ranging from regular to highly irregular topologies have been realized as efforts to improve the performance of applications in both general purpose and application-specific multi-core domain. However, faults can cause high contentions in NoCs. As a solution, adaptive routing algorithms are used. On the other hand, these algorithms have high area and timing overheads due to extra logic required for adaptively. We present a novel fault-tolerant routing algorithm for emerging 3D NoC topologies. The proposed algorithm analyses the condition of the NoC resources and distance of the destination nodes intelligently reroute packets. The algorithm has been evaluated by synthetic and various real-world traffic patterns. Experimental results show that the proposed algorithm has significant reduction in packet delays (over 45%) compared to other algorithms.



(a) Proposed Algorithms (b) Average Packet Delay

Fig 1. Comparison of various fault tolerant 3D routing algorithms

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Unified Single-port Survivor Memory for High-speed Viterbi Decoder using 3-unit Packing/Unpacking-based Data Processing

Jinil Chung and Jongsun Park
School of Electrical Engineering, Korea University, Seoul 136-713, Korea
E-mail : jinil_chung@korea.ac.kr

본 논문은 비터비 디코더의 효율적인 메모리 관리를 위해 3-유닛 패킹/언패킹 기반의 데이터 처리를 갖는 새로운 구조를 제안한다. 이러한 메모리 관리 기법은 생존경로를 저장하고 역추적(TB: Traceback) 동작을 수행하는 생존경로 메모리에 적용된다. 여기서 TB 동작은 1-포인터와 M-포인터 알고리즘으로 나뉘어 지는데, 이 중 1-포인터 알고리즘은 M-포인터 알고리즘 대비 메모리 용량 및 지연 측면에서 유리하나 읽기 포인터가 쓰기 포인터 보다 최소 2 배 이상 빠르게 동작해야 하는 제약사항이 있다[1]. 이에 본 논문에서는 1-포인터 기반이면서도 동일한 읽기/쓰기 포인터 속도를 갖기 위해 생존경로 데이터 3 개를 하나의 워드로 묶은 후 3 개의 사이클 중 1 개의 사이클에서는 쓰기(WR) 동작을, 나머지 2 개의 사이클에서는 읽기(TB, DC) 동작을 수행하는 3-유닛 패킹/언패킹 기반의 데이터 처리를 적용하였다. 이렇게 함으로써 매 사이클 마다 생존경로 데이터가 들어오더라도 읽기 동작을 쓰기 동작 보다 평균 2 배 더 많이 단일포트 메모리로 처리할 수 있다. 그리고 생존경로 메모리의 워드를 생존경로 데이터의 3 개로 구성할 수 있다면 제안하는 생존경로 메모리는 단일포트 메모리 뱅크 1 개만으로도 구현이 가능하다. 다음 그림 1. (a)-(c)에서는 기존 알고리즘과 함께 제안하는 구조의 동작을 나타내었다. 그림 2 에서는 몬테 카를로 방법이 가능한 FIL(FPGA-in-the-loop) 환경을 도입하여 RTL 설계로 구현된 제안하는 구조를 갖는 비터비 디코더의 오류 정정 성능이 소프트웨어로 구현된 비터비 디코더의 것과 동일함을 확인하였다. 표 1 에서는 본 논문에서 제안하는 구조를 1-포인터와 관련된 기존 연구 결과물들[2] [3]과 함께 비교하였는데, 제안하는 구조가 읽기/쓰기 포인터 속도가 동일하면서도 적은 메모리를 차지함을 알 수 있다.

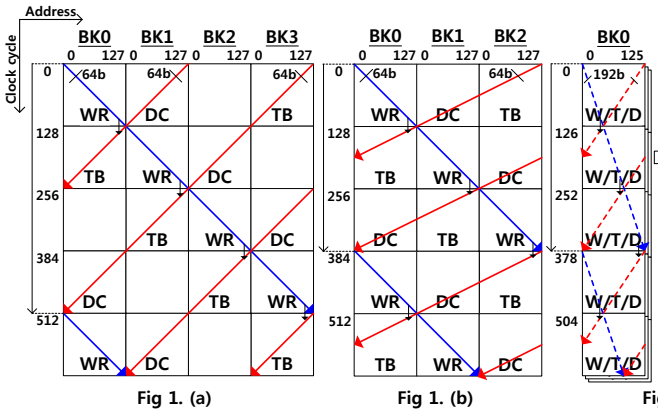


Fig 1. (a) Fig 1. (b) Fig 1. (c)

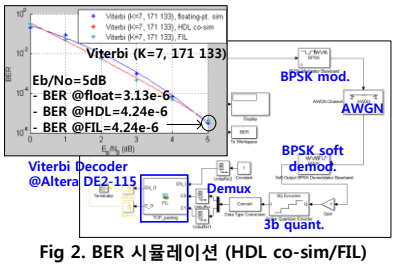


Fig 2. BER 시뮬레이션 (HDL co-sim/FIL)

Table 1. 기존 연구결과물들과 비교

K=7	[2]	[3]	proposed
# of bank	3	2	1
bank size	64b*128	64b*128	192b*126
port type	dual-port	single-port	single-port
f_{RD}/f_{WR}	1	2	1

Fig 1. 생존경로 갱신 (a) 기존 M-포인터: K=7, M=2, L=128, f_{RD}/f_{WR}=1
(b) 기존 1-포인터: K=7, L=128, f_{RD}/f_{WR}=2 (c) 제안하는 1-포인터: K=7, L=126, f_{RD}/f_{WR}=1
Fig 2. BER 시뮬레이션 (HDL co-sim), Table 1. 기존 연구결과물들과 비교

[1] G. Feygin and P. G. Gulak, IEEE Trans. Commun., vol. 41, no. 3, pp. 425–429 (1993).

[2] J. Kim and B. Kim, J. Korea Inform. Commun. Society, vol. 27, no. 5C, pp. 411-421 (2002).

[3] S.-C. Ma, IEICE Trans. Commun., vol. E87-B, no. 4, pp. 1016–1018 (2004).

Operation and modeling of select gate lateral coupling eNVM

Nam-Yoon Kim[1], Sung-Kun Park[1], In-Wook Cho[1], Kyung-Dong Yoo[1],
Eun-Mee Kwon[2], Sang-Young Kim[2]
1 *TD, Image Development Group, System IC Division, SK hynix, Cheongju*
2 *DMR, Research & Development Division, SK Hynix, Icheon-si*
E-mail : namyoon1.kim@sk.com

In area of embedded flash for system firmware coding, 2T structure including select gate(SG) for over-erase-free is generally used. Widely used EEPROM tunnel oxide(ETOX) structure with double poly needs too complicated fab processing, that result in the low logic compatibility. The other alternative can be single poly multi-time programmable(MTP) but there is demerit of low area competitive due to large capacitor area[1]. Here, the new structure of the select gate lateral coupling(SGLC) MTP cell is proposed. The SGLC MTP cell couples laterally floating gate(FG) to parallel SG playing role of control gate(CG) as well as SG. This cell uses no add mask and has CMOS compatible characteristic, moreover we achieve 1.34um^2 unit cell area much smaller than ~30um^2 of normal other MTP by replacing planar and horizontal coupling to lateral and vertial coupling. Channel hot electron(CHE) program(PGM) and band to band tunnelling(BTBT) assist hot hole injection(HHI) erase(ERS) method are used for the cell speed improvement. In order to verify this mechanism, we conduct 2D/3D TCAD simulation that shows the potential and field distribution at the time of PGM and ERS. In addition, by measuring cell PGM and ERS speed with FG to SG space size split, the cell perfomance with coupling ratio(CR) is understood more detailly. These experiments help to understand cell operation mechanism and reliability.

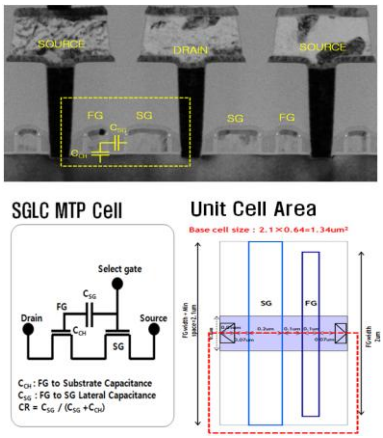


Fig 1. SGLC Structure

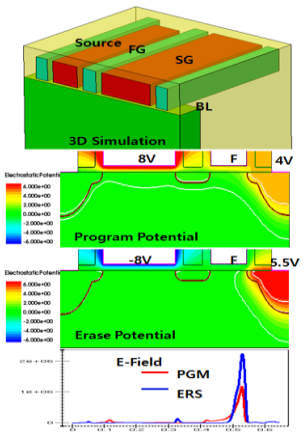


Fig 2. Simulation

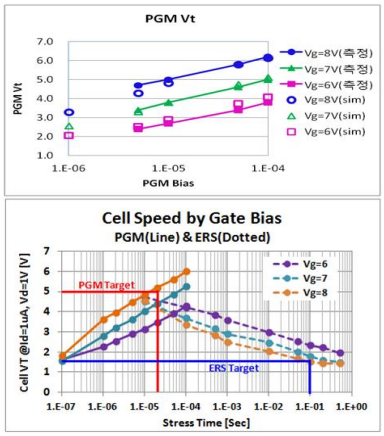


Fig 3.Cell Operation Speed

[1] C.F. Lin, C.Y. Sun, "A single-Poly EEPROM Cell Structure Compatible to Standard CMOS Process," Solid-State Electronics, vol. 51, Issue 6, pp.888-893, June, 2007.

This work was supported by the industrial strategic technology development program [10041855, Development of e-NVM (embedded non-volatile memory) analog mixed signal-based convergence process technology & IP] funded by the ministry of trade, industry & energy.

Design of new high-performance vertical NPN BJT and nLDMOS of full-featured BCD technology

Yon-Sup Pang, François Hébert, Seongmin Cho, Juho Kim, Sookjin Kwon, Yushin Ryu, Kyungho Lee, Leeyeun Hwang, Sung-Bum Park, Jung Lee, and Taejong Lee
MagnaChip Semiconductor, Corporate Engineering, Cheongju, 361-725, Korea
E-mail : yonsup.pang@magnachip.com

We present new high-performance vertical NPN BJT rated for >10V applications, integrated within a full-featured 0.18 μm BCD technology which features fully-isolated high-performance nLDMOS transistors rated for >24V applications. TCAD simulation was essentially used for developing the BCD technology. The performance of the nLDMOS is in a trade-off relation with that of the VNPN BJT. The new high-performance BJT has the maximum current gain β_{max} = 283 and the breakdown voltages, BV_{CEO} = BV_{CES} = 18.1 V, BV_{CBO} = 19.3 V and BV_{EBO} = 20 V, and uses the NDRIFT and the PBODY implants of the nLDMOS for the emitter and the base formation, respectively, without any additional masking step. The maximum current gain of our vertical NPN BJT is 10 times higher than a conventional one [1]. The breakdown voltage at zero gate voltage of the nLDMOS is 37.1 V and the specific on-resistance R_{sp} = 13.4 [mΩ-mm^2], which is compatible with the lowest one of the silicon nLDMOS published recently [2].

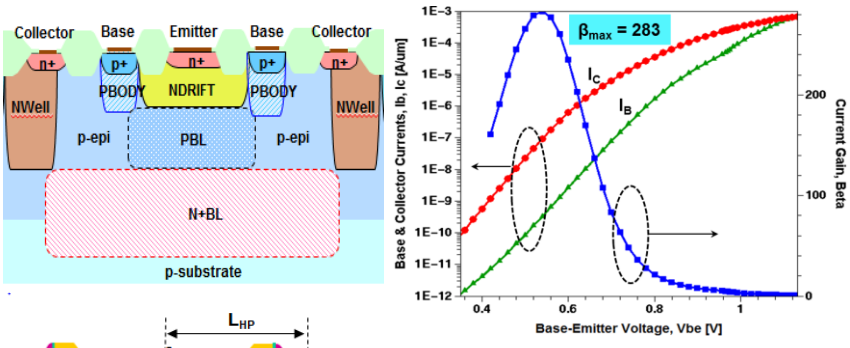


Fig. 1. Cross-sectional view of new BCD 5 V vertical NPN BJT, Gummel plot and current gain curve at V_{CE} = 5 V

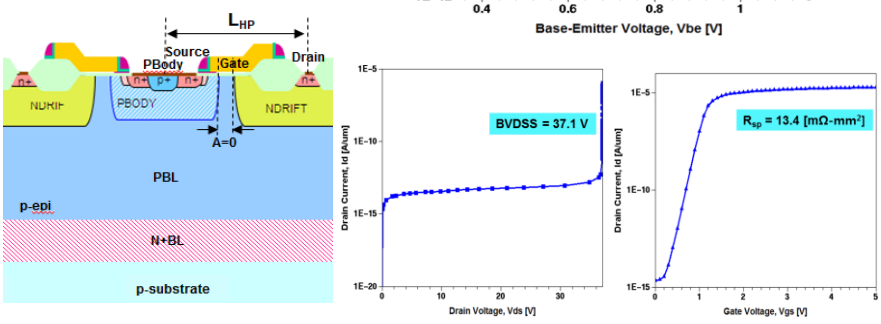


Fig. 2. Cross-sectional view of BCD 24 V high-side nLDMOS, I_D-V_{DS} curve at V_{GS} = 0 V and I_D-V_{GS} curve at V_{DS} = 0.1 V

[1] A. Andreini, et al., IEEE Trans. Electron Devices, Vol. 33, No. 12, (1986), p.2025–2030.
[2] K. Lee, et al., Proceedings of 25th ISPSD, (2013), p.163–166.

A Dual Sweep Transfer Curve Technique for Separate Extraction of Source and Drain Resistances in Advanced FETs without Substrate Contacts

Jun Seok Hwang, Hagyoul Bae, Hyunjun Choi, Jaeyeop Ahn, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim and Dong Myong Kim

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Korea

E-mail : dmkim@kookmin.ac.kr

Layout asymmetry, processing, and hot-carrier stress may cause asymmetric source (R_S) and drain (R_D) parasitic resistances in FETs. This asymmetry has invalidated many conventional methods due to incorrect assumption of $R_D = R_S$ for the extraction of device parameters [1]. Separate characterization of R_S from R_D is important in the accurate and systematic design through performance estimation and characterization of physics-related reliability mechanisms. In particular, accurate separate extraction of R_S and R_D in SOI MOSFETs is important in the modeling and characterization for practical applications. In this work, we present a convenient technique to extract R_S and R_D separately. The method, so called a dual sweep transfer curve technique, is based on the I-V models in the linear region of MOSFET's. In this technique, transfer characteristics for both forward and reverse modes in a single SOI MOSFET are employed. Experimentally extracted R_S and R_D are confirmed to be insensitive to the variations of the effective channel length, width, and mobility under the gate bias, minimizing the resistance errors generated from those parameters. The proposed technique provides a high accuracy and also, unlike other method [2], allows fast characterization in substrate contactless field effect transistors.

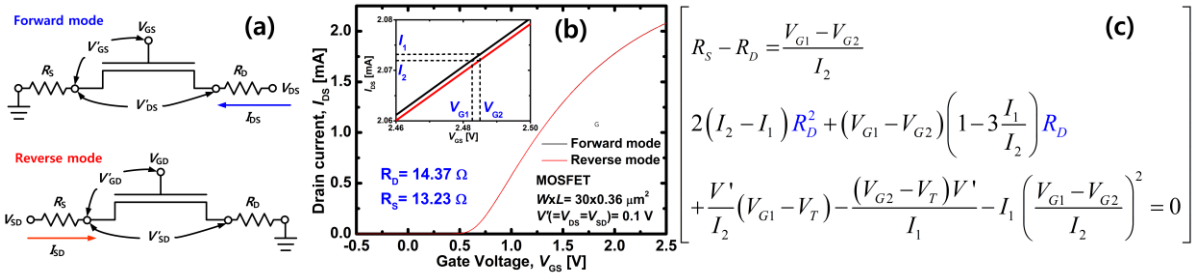


Fig 1. (a) The equivalent circuit model of SOI MOSFET, (b) forward and reverse mode characteristics in linear current-voltage graph and (c) The equations for the separate extraction of R_S and R_D.

[1] G. J. Hu, C. Chang, and Y.-T. Chia, IEEE TED, vol. ED-34, p. 2469(1987)

[2] Ja Sun Shin, Hagyoul Bae, Euiyoun Hong, Jaeman Jang, Daeyoun Yun, Jieun Lee, Dae Hwan Kim, and Dong Myong Kim, SSE, 72, p.78(2012)

Investigation of Work-Function Variation for FinFET Using a Modified RGG Concept

Hyohyun Nam and Changhwan Shin*
School of Electrical and Computer Engineering, University of Seoul, Seoul 130-743, Korea
*E-mail : {kahn0217, cshin}@uos.ac.kr

It was demonstrated in [1] that the random threshold voltage (V_{TH}) variation [*e.g.*, line edge roughness (LER), random dopant fluctuation (RDF), and work-function variation (WFV)] in sub-30-nm technology is one of the main hurdles for successfully and constantly scaling down CMOS devices according to the Moore`s Law. Above all, the WFV-induced V_{TH} variation is larger than LER- or RDF-induced V_{TH} variation in sub-30-nm process technology [2-3].

In this study, because the original ratio of average grain size to gate area (RGG) method [4] is not suitable for estimating the magnitude of WFV-induced $\sigma(V_{TH})$ in high-k/metal-gate FinFETs, we propose a modified RGG concept which can exactly and easily estimate the WFV-induced V_{TH} variation in FinFETs. It is confirmed that the WFV-induced V_{TH} variation using the modified RGG is well matched to previous simulation results [5].

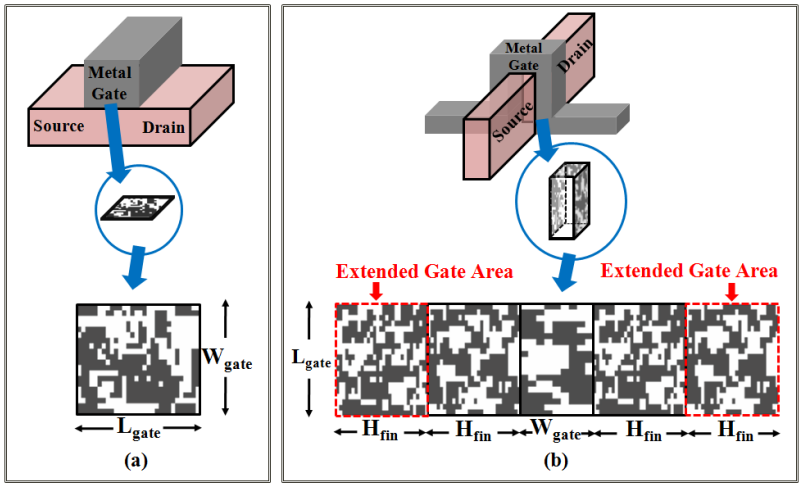


Fig. 1. The total gate area for (a) planar bulk MOSFET and (b) FinFET. Note that the total gate area should be defined as {Wgate + (4 × Hfin)} × Lgate for the FinFET and Wgate × Lgate for the

[1] A. Asenov, "Simulation of statistical variability in nano MOSFETs," in *VLSI Symp. Tech. Dig.*, 2007, pp. 86-87.

[2] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Grain-orientation induced work function variation in nanoscale metal-gate transistors – Part I: modeling, analysis, and experimental validation," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504-2514, October 2010.

[3] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Modeling and analysis of grain-orientation effects in emerging metal-gate devices and implications for SRAM reliability," in *IEDM Tech. Dig.*, 2008, pp. 1-4.

[4] H. Nam and C. Shin, "Study of high-k/metal-gate work-function variation using Rayleigh distribution," *IEEE Electron Devices Lett.*, vol. 34, no. 4, pp. 532-534, April 2013.

[5] X. Wang, A. R. Brown, B. Cheng, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *IEDM Tech. Dig.*, 2011, pp. 104-106.

Full characterization of 2T SONOS nonvolatile memory for TSC application

Taeho Lee[1], Youngjun Kwon[1], Jaegwan Kim[1], Sungkun Park[1], Inwook Cho[1], Kyungdong Yoo[1]
Youngdong Joo[2] and Seungdeok Kim[2]
[1]*TD, Image Development Group, System IC Division, SK hynix, Cheongju 361-725, Korea*
[2]*Wingcore Technology Inc, Seongnam 463-816, Korea*
E-mail : taeho2.lee@sk.com

The use of SONOS device for code storing memory can realize a low-cost, a simple process for ensuring excellent logic compatibility and superior defect tolerance properties. In the view of total chip size, the memory density over 1Mb is more advantageous to adopt 1T structure with built-in protective function against over erase, but the memory density less 1Mb is more favorable to choose 2T structure including the ability to over erase autonomously [1]. In this paper, the 2T SONOS structure has been proposed for Touch Screen Controller (TSC) application. The 2T SONOS cell provides essential properties for embedded NVM such as the full erase using the trap nitride completely, high on cell current and wide windows. We have finished a cost-effective process which is based on 90nm HV CMOS process with only three additional mask steps and compact cell size [0.29um^2]. The additional mask steps are used for formation of ONO profile and cell junctions. We have achieved high program-erase speed and good reliability in 32KB eNVM IP without special algorithms and cell array modifications.

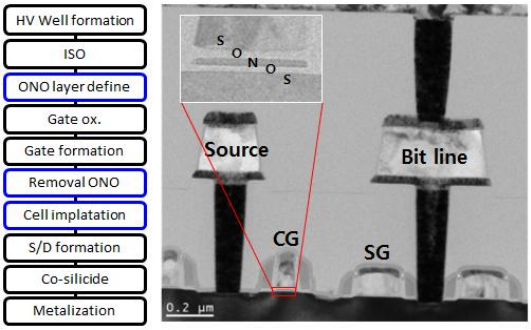


Fig1. Process flow and TEM image of 2T SONOS

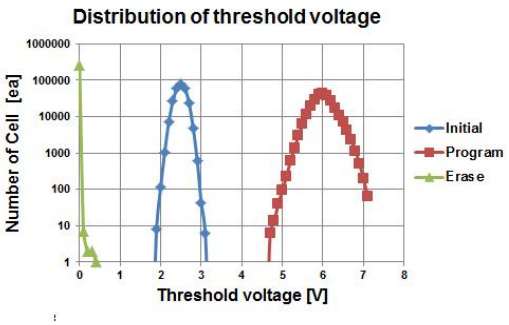


Fig2.Vth distribution on 32KB IP

[1] Jean-Michel Daga, Caroline Papaix, Emmanuel Racape, Marylene Combe, Vincent Sialelli, Jeanine Guichaoua. ―A 40ns random access time low voltage 2Mbits EEPROM Memory for embedded applications‖ IEEE, 2003

This work was supported by the industrial strategic technology development program [10041855, Development of e-NVM (embedded non-volatile memory) analog mixed signal-based convergence process technology & IP] funded by the ministry of trade, industry & energy.

Investigation of the THz Resonant Oscillation in HEMTs by Solving the Pseudo-2D Poisson Equation and the 1D Transport Equation

Sung-Min Hong[1]*, Jae-Hyung Jang[1], and Kyung Rok Kim[2]

[1]School of Information and Communications, Gwangju Institute of Science and Technology, Korea

[2]School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, Korea

*smhong@gist.ac.kr

• Abstract

In this work, we have investigated the THz resonant oscillation in field-effect transistors using the simulation approach. The 1D transport equation, which considers the time derivative of the electron current density, has been solved self-consistently with the pseudo-2D Poisson equation. It is demonstrated that the autonomous on-set of the THz resonant oscillation can be simulated by performing the conventional transient analysis.

1. Introduction

Since its potential application in various areas (for example, security, medicine, broadband communications, and so on), the generation and detection of electromagnetic radiation in the terahertz (THz) range is of great interest. [1]

It is obvious that the precise calculation of interested quantities can enhance the understanding on the subject significantly. As pointed out in [2], in many cases, an analytical description and numerical modeling of THz resonant oscillation is carried out in the framework of rather simplified models. [3] Although such models provide a good qualitative description of the physical phenomena involved, a much more detailed approach is required to enable a quantitative comparison with experimental results. Quite recently, the calculation of the THz resonant response to the externally forced gate voltage is performed by solving a 1D numerical hydrodynamic approach coupled with a pseudo-2D Poisson equation. [4] When the THz emitter is considered, the autonomous oscillation in the THz frequency range is concerned. As a preliminary investigation, we have developed a device model which can simulate the resonant oscillation properly.

The organization of the extended abstract is as follows: In Section 2, the simulation model newly implemented into our in-house device simulator is briefly explained. In Section 3, the autonomous on-set of the THz resonant oscillation is demonstrated. Finally, the conclusion is made.

2. Simulation Framework

As much as the carrier transport in the THz range is concerned, the most significant drawback of the conventional device simulation model is the lack of the time derivative of the particle current density. For conventional device simulators whose simulation frequency is below 100 GHz, it is known that the term – the time derivative of the particle current density – can be ignored without any loss of accuracy. [5] However, since the time derivative of the particle current density plays a central role in the resonant behavior, a new model is required in order to simulate the THz resonant oscillation in field-effect transistors properly.

In this work, we have implemented a new module specialized to the THz emitting high electron-mobility transistor (HEMT) into our in-house, device-circuit mixed-mode simulator. We couple the drift-diffusion equations in the transport direction (x) with the pseudo-2D Poisson equation described in [6].

$$-q\frac{\partial n}{\partial t} = -\frac{\partial J_n}{\partial x}$$

$$J_n + \tau_{jn}\frac{\partial J_n}{\partial t} = -q\mu_n n\frac{\partial \psi}{\partial x} + qD_n\frac{\partial n}{\partial x}$$

$$\epsilon_c\frac{\partial \psi}{\partial x^2} + \epsilon_s\frac{V_g - \psi}{d\delta} = q(n - N_D)$$

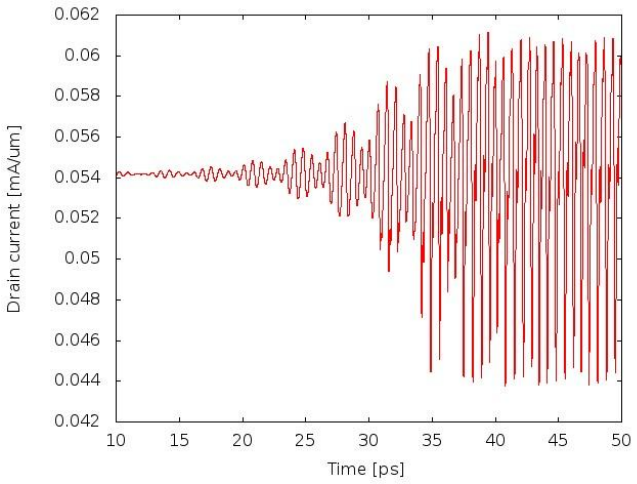
where q is the (absolute) elementary charge, n the electron density, J_n the electron current density, τ_{jn} the relaxation time of the current density, μ_n the electron mobility, ψ the electrostatic potential, D_n the electron diffusion constant. ϵ_c and ϵ_s are the dielectric constants of the channel material and the Schottky layer, respectively. d is the gate-to-channel distance, and δ is the channel thickness. The effective donor concentration in the channel is modeled as N_D.

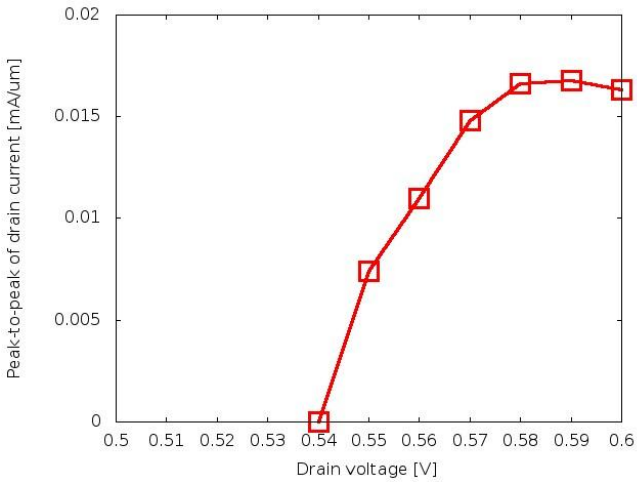
The Caughey-Thomas relation is used to describe the velocity saturation effect. The relaxation time of the current density is modeled as a constant, 0.33 ps in this work. Infinite surface recombination velocity is assumed at the source/drain contact boundaries. The contribution of holes is neglected.

3. Simulation Results

The InAlAs/InGaAs/InP HEMT structure considered in the literature [4] has been modified and simulated in this section. The gate length is 100 nm, and each of two ungated sections is 100-nm-long. An 1D real-space grid with 1 nm spacing is adopted. Uniform value of N_D is 10^{18} /cm^3. Relative dielectric constants are given by $\epsilon_c = 13.4$ and $\epsilon_s = 11.8$, respectively.

Transient analysis has been performed in a conventional way. First, the DC bias close to the target operating bias is applied to the terminals. A sudden, small change of the bias voltages to the target operating bias (typically 1 μV in this example) initiates the autonomous on-set of the THz resonant oscillation. The time step for the transient analysis is set to 1 fs. Since the terminal voltages are fixed, no fluctuation of the terminal voltage is allowed. Therefore, the drain current (per unit width) is used as an output variable. Fig. 1 shows the autonomous on-set of the THz resonant oscillation. Note that, without the time derivative of the current density, no oscillation is observed in the same structure at the same bias conditions.





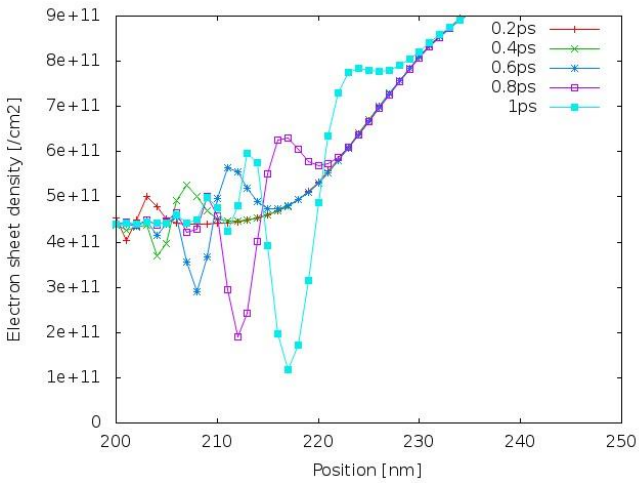
For a given gate-to-source voltage, the on-set of the THz resonant oscillation depends on the drain-to-source voltage. Increasing the drain-to-source voltage yields faster buildup of the oscillation. Fig. 2 shows the peak-to-peak value of the drain current after sufficiently long transient analysis. A clear threshold-like behavior is observed. In order to see the underlying mechanism of the resonant oscillation, at the initial solution, we intentionally apply a density perturbation at the drain-end of the gated region. (200 nm in this structure) In this case, the bias condition is fixed. Fig. 3 shows the electron sheet densities at various time instances. From the figure, it is clear that the originally-imposed small perturbation in the electron density is amplified as the time elapses.

4. Conclusion

We have developed a simplified device model which can simulate the resonant behavior of the HEMT efficiently. It is demonstrated that the autonomous on-set of the THz resonant oscillation can be simulated by performing the conventional transient analysis.

• Acknowledgment

This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009594). Sung-Min Hong's work was partially supported by



GIST College's 2013 GUP Research Fund.

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[2] H. Marinchio, G. Sabatini, C. Palermo, J. Pousset, et al., Applied Physics Letters, vol. 94, p. 192109, 2009.
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[5] C. Jungemann and B. Meinerzhagen, Hierarchical Device Simulation – The Monte Carlo Perspective, Spring-Verlag, 2003.
[6] H. Marinchio, C. Palermo, G. Sabatini, L. Varani, et al., Journal of Computational Electronics, vol. 9, pp. 141-145, 2010.

Fig. 1. Autonomous on-set of the THz resonant oscillation triggered by a small change in the gate-to-source voltage. The drain current (per unit width) is plotted as a function of elapsed time. The gate voltage is -0.2 V and the drain voltage is 0.6 V.

Fig. 2. Peak-to-peak value of the oscillating drain current (per unit width) after sufficiently long transient analysis, as a function of the drain voltage. The gate voltage is -0.2V.

Fig. 3. Electron sheet densities at various time instances after initial perturbation. The gate voltage is -0.2 V and the drain voltage is 0.6 V.

Invited paper

Scaling issues and trends of NAND flash memory

Jaeduk Lee, Youngwoo Park, and Gyoyoung Jin
Semiconductor R&D Center, Samsung Electronics, Hwaseong 445-701, Korea
E-mail : jaeduklee@samsung.com

Increasingly more scaling issues have risen as scaling down continues in NAND flash memory cell due to the intrinsic nature, more specifically the charge storage and high-voltage operation, of NAND flash cell [1]. Fig. 1 shows the scaling issues, and to solve theses issues many technical schemes have been suggested. The cell-to-cell interference [2] is being solved by changing the operation methods [3]. A solution of the E-field crowding and the narrowing of PGM/ERS V_T window is suggested by the flat-type floating gate structure. The hot-carrier disturb is being solved by the maintaining the distance between WL0 to GSL [4], and the depletion of the floating gate is suppressed by maintaining sufficient dopants in the floating gate. Comparing the conventional wrap-around floating gate cell and the flat-type floating gate cell, the former has advantages in the PGM/ERS V_T window, while the latter has advantages in the cell-to-cell interference, the E-field crowding, and the limitation of IPD thickness. However, the number of electrons in the floating gate and photo limitation are more substantial issues, which are hard to be solved easily.

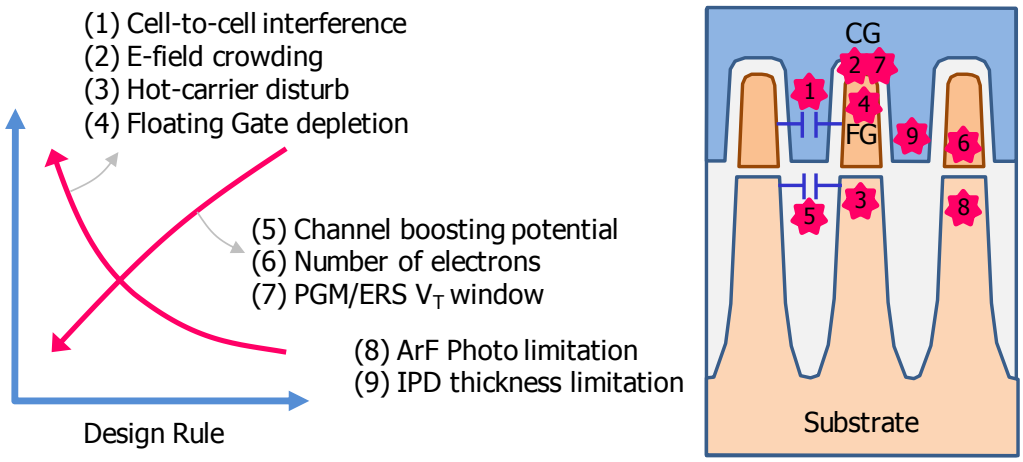

Fig 1. Scaling issues of planar NAND flash memory

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[2] Jae-Duk Lee et al., IEEE-EDL, vol. 23, no.4 , pp. 264 -266 , May 2002.
[3] Ki-Tae Park et al., IEEE JSSC, vol. 43, no. 4, pp. 919-928, Apr. 2008.
[4] Jae-Duk Lee et al., in *Proc. IEEE NVSMW*, Feb. 2006, pp. 31-33.

Towards High Performance Selector Device for 3D Stacked Cross-point Arrays

Jiyong Woo, Daeseok Lee, Euijun Cha, Sangheon Lee, Sangsu Park, and Hyunsang Hwang
Department of Materials Science and Technology, Pohang University of Science and Technology (POSTECH), Pohang 790-784, Republic of Korea
E-mail : jiyongis@postech.ac.kr

For storage-class memory applications, 3D cross-point resistive switching memory (RRAM) or Vertical RRAM (VRRAM) is essential to achieve the highest memory densities [1, 2]. To realize 3D stacking technology, the bidirectional selector device is required to suppress sneak-path currents from the neighboring cells.

In this study, to achieve a desirable selector device, the electrical characteristics of the selector device with a multilayer oxide have been systemically investigated by using various approaches such as interface engineering and by considering factors such as materials dependence. The outstanding performances such as high current density (>10^7 A/cm^2), high selectivity (~10^4), better leakage current (I_{OFF} < 100 nA) and excellent reliabilities are demonstrated by proposed multilayer oxide structure. Furthermore, we experimentally demonstrate highly promising electrical performance in the 1S-1R device that integrates a bidirectional selector with Conductive-Bridge RAM (CB-RAM). Our study opens the possibility of realizing high-performance selector devices through the incorporation of a multilayer oxide and its combinations.

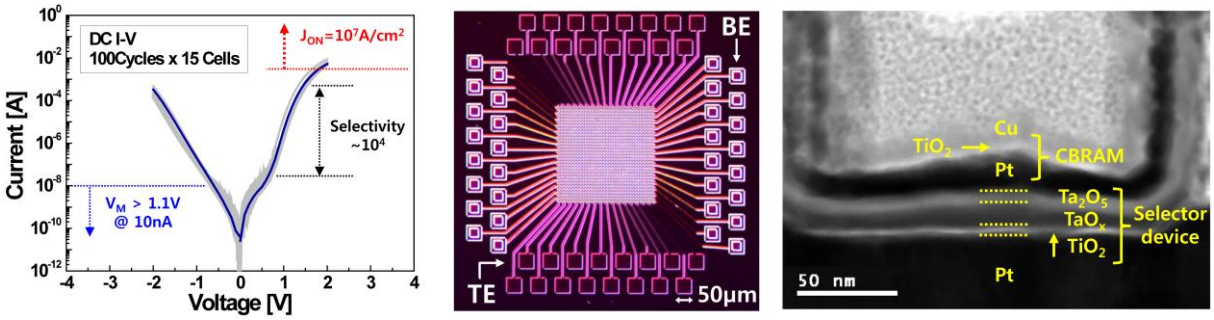

Fig 1. The selector device in nanoscale array and TEM image of the integrated device structure.

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Acknowledgement This work was supported by the Research and Development program of MOTIE/KEIT. [10039191]

A New Programming Method to Alleviate the Program Speed Variation for Three-dimensional Channel Stacked Array Architecture

Joo Yun Seo, Yoon Kim*, Sang Ho Lee, and Byung-Gook Park
Inter-university Semiconductor Research Center (ISRC) and Department of Electrical Engineering,
Seoul National University
* Flash design team, Memory division, Samsung Electronics Company Ltd.
E-mail : jooyun@snu.ac.kr

With the exploding demand for mobile devices, the market of NAND flash memory devices have increased dramatically. Accordingly, device scaling have been carried out aggresively in recent years to keep up with the demand of ultra storage capacity. However, the limitation of photo lithography techonology and interference between cells hinder further scaling. To overcome NAND scaling issues, three-dimensional (3D) stacked NAND array has been considered as a breakthrough. A number of 3D stacked NAND array architectures have been reported [1]–[4], and channel stacked array architecture is one of the representative architectures, which features single crystalline silicon channel and gate-all-around structure. Although it demonstrates its high on-current level and device scalability, there is an issue on cell size variation between layers induced by the etch slope. We investigate the effect of the cell variation on the program speed when incremental step pulsed programming (ISPP) is applied with 3D TCAD simulation. When the cross section of channel gets closer to a circle, the program speed is faster. If there is the difference of program speed among cells in different layers, it induces cell V_T variation, which increases the total program time. To reduce the total program time, a new programming method is proposed, and we achieved the result that the V_T variation among cells is alleviated.

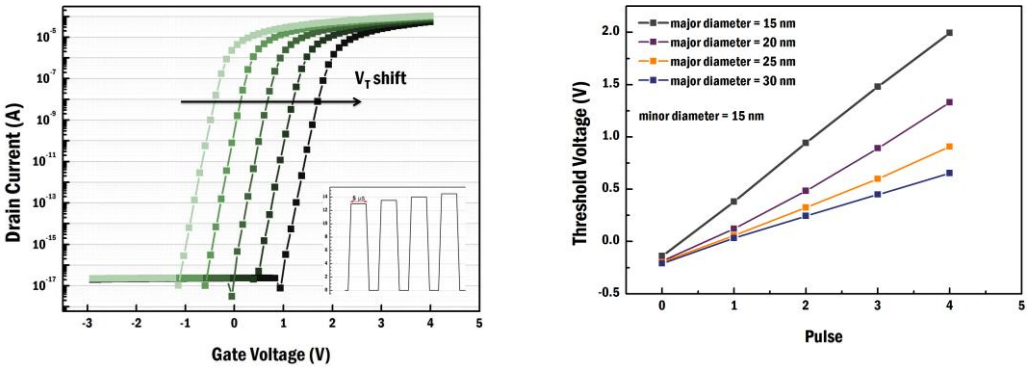

Fig 1. (left) Program characteristic when ISPP is applied (right) Program speed variation

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Acknowledgement

This work was supported by the IT R&D program of MKE/KEIT. (10035320, Development of novel 3D stacked devices and core materials for the next generation flash memory)

3차원 플래쉬 메모리를 위한 매우 얇은 다결정 실리콘 채널 층을 갖는 정션리스 플래쉬 메모리의 특성에 관한 연구

박종경 [1], 김승윤 [1], 이기홍 [2], 피승호 [2], 이석희 [1,2], 조병진 [1*]

[1] 한국과학기술원 전기 및 전자공학과, Phone: +82-42-350-3485,
Email: bjcho@kaist.edu
[2]SK 하이닉스 반도체 메모리 연구소

최근 다양한 형태의 3 차원 구조의 플래쉬 메모리에 대한 개발이 진행되고 있다 [1-2]. 3 차원 플래쉬 메모리 소자에서는 cell 사이에 highly doped junction 을 사용하는 대신 gate bias 에 의한 fringing field 를 인가하여 inter-cell region 을 inversion 시킴으로써 소자를 작동시킨다 [1]. 하지만 충분하지 못한 fringing field 와 다결정 실리콘(poly-Si) 고유의 특성으로 인해 높은 S/D 저항을 야기함으로써 read current 를 향상시키는 것이 매우 어렵다. 이에 대한 대안으로 채널/소스/드레인을 모두 n^+-doped poly-Si 을 사용하는 정션리스(junctionless) 소자가 제안되었다 [3]. Junctionless 소자는 소자를 off 시키기 위해서 채널을 완전하게 depletion 시켜야 하기 때문에 채널의 두께를 매우 얇게 형성해야 할 필요가 있다. 본 논문에서는 매우 얇은 두께를 갖는 junctionless 소자의 실제 동작 특성과 메모리 특성을 확인하기 위하여 2 ~ 7 nm 두께의 poly-Si 채널을 갖는 junctionless charge trap type flash (CTF) thin-film transistor (TFT)를 구현하였다. 구현된 소자를 통하여 얇은 poly-Si 채널에서의 transfer curve 특성과 더불어 program/erase, retention, endurance 특성과 같은 메모리 특성도 살펴보았다. 결과를 보면 2 nm 이하의 얇은 채널을 갖는 junctionless CTF TFT 소자의 경우에 우수한 transfer curve 특성과 향상된 메모리 특성을 얻을 수 있음을 확인하였다. 따라서 본 결과를 응용하면 poly-Si 채널 층의 두께를 지속적으로 scaling 함으로써 3 차원 플래쉬 메모리의 bit density 를 더욱 높일 수 있을 것으로 기대한다.

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Organic nonvolatile memory devices based on self-assembled nanomaterials

Jang-Sik Lee
Department of Materials Science and Engineering, POSTECH, Pohang, Kyungbuk 790-784, Korea
E-mail : jangsik@postech.ac.kr

Recently, active research has been carried out on organic electronic devices because of their advantages of low cost, simple fabrication processes, and flexibility in comparison to silicon-based electronic devices. Additionally, organic materials can be applied to flexible electronic devices if processed at low temperatures.[1-4]
In this work, we fabricated flexible organic memory devices based on self-assembled materials and processes. For non-volatile memory devices the charge trapping elements, here, metallic nanoparticles, were synthesized by the self-assembly and inserted in the gate dielectric layer of organic transistor devices. Good programmable memory properties were obtained in terms of memory windows, operation voltages, and reliability.[5-9] Overall, organic electronic devices were successfully fabricated on flexible plastic substrates. Detailed device fabrication processes, electrical chatactrization, and device operations will be discussed in detail.

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Flexible graphene-PZT ferroelectric field effect transistors for nonvolatile memory

Wonho Lee and Jong-Hyun Ahn

School of Electrical & Electronic Engineering, Yonsei University, Seoul, 120-749, Korea
E-mail : ahnj@yonsei.ac.kr

Recently, flexible memory devices which are the basic factors to compose the electronic device have been intensively developed for realization of the multi-functional flexible electronic systems. However, flexible nonvolatile memory devices consist of organic ferroelectrics and graphene which are intrinsically flexible have shown the limitation in their high operating voltage region and poor reliability. [1]

We investigated the flexible graphene-based ferroelectric field effect transistors (FeFETs) memory arrays with inorganic $Pt(Zr_{0.35}Ti_{0.65})O_3$ (PZT) in forms of thin ribbon structures. [2] The single layer graphene grown by CVD methods is used as a channel and PZT films formed by sol-gel methods showed a high remnant polarization (P_r) of 30 $\mu C/cm^2$ and a coercive voltage (V_c) of 3.5 V under a voltage loop over ± 11 V. The graphene-based FET with a PZT film on a plastic substrate presents an on/off current ratio of 6.7, a memory window of 6 V.

We also suggested the electrolyte treating method to suppress the anti-ferroelectric effects observed on graphene-PZT FeFETs due to charge trapping by water, impurities and defects at interfaces and non-uniform charge induction. [3,4] The devices exhibited remarkable mechanical properties and were readily integrated with plastic substrates for the production of flexible circuits. This approach suggests that graphene based FeFET with PZT films on a plastic substrate can be an alternative option for flexible nonvolatile memory device.

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Characterization of nanoscale copper-oxide resistive switching memory devices using self-assembled nano-templates

Un-Bin Han, Jang-Sik Lee
Department of Materials Science and Engineering, POSTECH, Pohang, Kyungbuk 790-784, Korea
E-mail : jangsik@postech.ac.kr

Resistive switching random access memory (RRAM) has been widely investigated for future memory device because of its advantages, for example, fast switching speed, low operation voltage, high scalability, and good endurance/data retention properties. In this study, we fabricated copper oxide-based RRAM device using anodized aluminum oxide as the template layer.[1] Among the various metal oxides, copper oxide is very attractive as a switching material in RRAM because it is relatively inexpensive and non-toxic. The copper oxide layer was employed to fabricate $Cu/Cu_xO/Cu$ RRAM device, which shows a reproducible resistive switching behavior. The resistive memory devices were characterized by atomic force microscope (AFM), field-emission scanning electron microscope and their electrical properties were directly measured using the conductive AFM and semiconductor parameter analyzer. This study provides the fabrication of highly scalable RRAM device with bottom-up process. In this presentation, detailed device fabrication and characterization using nanoscale RRAM devices will be discussed.

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Hardware Implementation of Associative Memory Characteristics

Kibong Moon, Sangsu Park, Daeseok Lee, and Hyunsang Hwang
Department of Materials Science and Engineering, Pohang University of Science and Technology, Pohang 790-784, Korea
E-mail : kbmoon@postech.ac.kr

Recently, resistive switching random access memory (ReRAM) has been considered as newly introduced element for neuromorphic applications due to its high density, low-power consumption and similarity with synapse [1, 2]. One of the important things in neuromorphic system is memory characteristics such as an associativity which means the ability to learn and remember the relationship between unrelated information. The key point of animal's learning is connection strength of synapse between neurons. We made Pt/TiN/$Pr_{0.7}C_{0.3}MO_3$ (PCMO)/Pt structure (from top to bottom) to mimic synapse behavior. TiN/PCMO based ReRAM has multi resistance state with same spike. When a negative pulse was applied to the top of a device, the current increased gradually and vice versa (fig. 1-a). Using TiN/PCMO based ReRAM having synapse characteristics, we design simple circuit which comprised of voltage adder, divider, comparator for realizing neuromorphic system of animal's learning process such as classical conditioning (fig. 1-b). We define acquisition times (T_A), learning times (T_L), respectively. The result shows that T_A increased in proportion to simultaneous applying times of V_{UCS} and $V_{NS, CS}$ with various condition (fig. 1-c). That means that memory retention increases in proportion to learning times like animal's learning system. In this research, we realize hardware implementation of neuromorphic system in the point of an associativity in memory characteristics using CMOS neuron and ReRAM synapse.

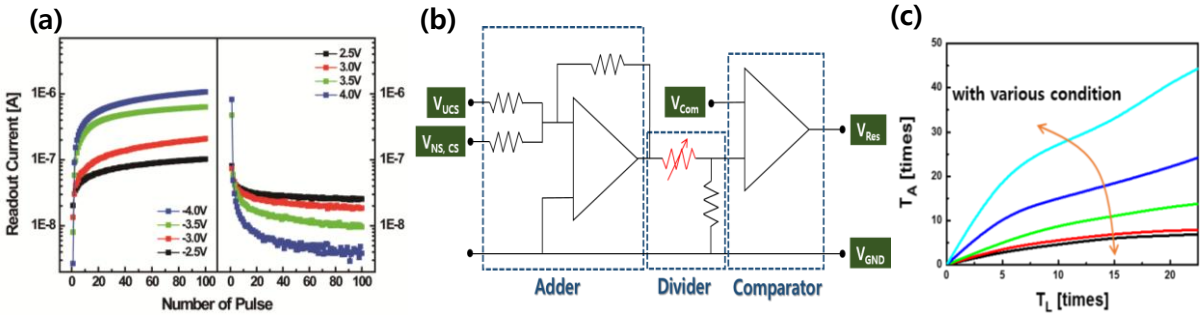

Figure 1. (a) TiN/PCMO AC characteristics, (b) circuit for realizing learning process, (c) experiment results of classical conditioning

Acknowledgement This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009460).

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Intercalation of CVD graphene for interconnects

최동철, 박재현, 김혜지, 이원준, 정종완*
세종대학교 나노신소재공학과
E-mail : jwjung@sejong.ac.kr

탄소 원자 한 층의 두께를 가지는 이차원 구조체인 그래핀은 이동도가 매우 높으며 저항이 낮고 잘 휘어지는 뛰어난 물리적, 전기적 성질을 띈다. 그래핀을 배선에 사용하기 위해서는 단층이 아닌 다층의 두꺼운 그래핀 박막이 필요한데, 이 경우 층간의 전자 상호작용에 의해 단층 그래핀의 이동도가 낮아지는 문제가 발생하며, 이를 해결하기 위해서는 그래핀 층간의 전자 결합을 억제하여야 한다. 본 연구에서는 다층 그래핀의 저항을 낮추는 것을 목표로, 다층 그래핀의 층간의 상호작용을 막아주기 위한 intercalation 연구를 진행하였다. 그래핀의 면저항(R_s)을 감소시키기 위해 FeCl3 을 층간 사이의 intercalation 물질로 사용하였다. 니켈 촉매를 이용해 단층에서 다층의 그래핀을 CVD 방법으로 성장시킨 후에 퍼니스에서 $FeCl_3$ 분말과 Ar gas flow 를 흘려주면서 $FeCl_3$ 를 층간에 침투시켜 intercalation 을 진행하였다. Intercalation 여부는 샘플의 Raman spectroscopy 를 비교하였고, 또한 면 저항을 측정하여 분석하였다. 또한 MEIS(Medium energy ion scattering spectroscopy)로 샘플의 성분분석을 통해 Fe 와 Cl 이 삽입되었음을 확인하였다.

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Development of Post-CMP Cleaning Solution for Interconnect Application

Young-Gil Seo[1], Byoung-Jun Cho[2], Manivannan Ramachandran[1], and Jin-Goo Park[1, 2, *]

Department of [1]Materials Engineering and [2]Bio-Nano Technology, Hanyang University, Ansan 426-791, Korea

[*]E-mail : jgpark@hanyang.ac.kr

During chemical mechanical planarization (CMP), copper/low-k surface would be contaminated by abrasive particles, organic materials and other additives [1]. Those contaminant needs to be removed in the subsequent cleaning process using an effective cleaning solution with a minimum material loss. In this study, a dilute amine based alkaline cleaning solution was used along with physical force in the form of megasonic energy to remove the particle and organic contaminants. Tetramethyl ammonium hydroxide (TMAH) and monoethanol amine (EA) were used as an organic base and complexing agent respectively, in the proposed solution. Also, ethanolamine acts as corrosion inhibitor in the solution. Organic residue removal was confirmed based on the contact angle measurements and X-ray photoelectron spectroscopy analysis. Electrochemical studies showed a good protection against corrosion for the proposed solution. The hybrid cleaning technology showed higher particle removal efficiency from both copper and low-k surface.

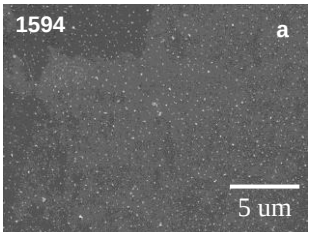
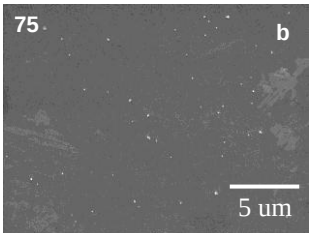
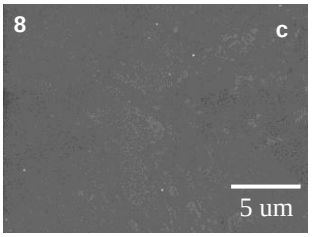
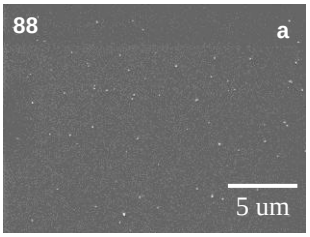
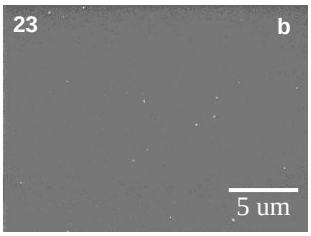
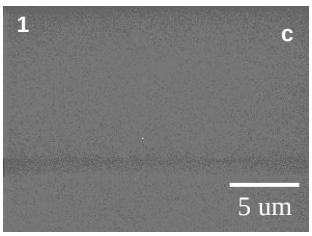
	After contamination (Before cleaning)	After cleaning w/o megasonic	After cleaning w/ megasonic
Copper			
low-k			

Fig 1. FESEM images of copper and low-k wafer

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Performance enhancement for Ag nanowire-based transparent conductor using TiO_2:Cs sol-gel

Sunho Kim[1], Sekwon Na[1], Jun-gu Kang[1], Haekyoung Kim[2], and Hoo-Jeong Lee[1]

1 School of Advanced Materials Sci. and Eng., SungKyunKwan Univ., Suwon, Korea

2 School of Materials Sci. and Eng., Yeungnam Univ., Gyeongsan, Korea

E-mail : hlee@skku.edu

Transparent conductive electrodes(TEC) have been highlighted recently for increasing demand of touch screen panels which are the key parts of smart phone. tin-doped indium oxide(ITO) is used as the TCE materials but but has the problems of high price, scarcity, and application for flexible displays.[1] Silver nanowires(Ag NWs) are one of the promising materials for replacing ITO-based TCE. But the contact resistance of pristine networked Ag NW electrodes is the point to be solved because the high contact resistance causes high sheet resistance. It is the one the serious reason which decrease the performance of Ag NWs-based TCE.[2] In this work, using TiO_2:Cs sol-gel we welded Ag NWs junctions and measured the change of sheet resistance and transmittance. The sheet resistance of TiO_2:Cs sol-gel treated films decrease without the change of transmittance. Fig. 1(b) shows the welded Ag NW network. The welded network increases the contact strength more than the pristine Ag NW network shown in Fig. 1(a).

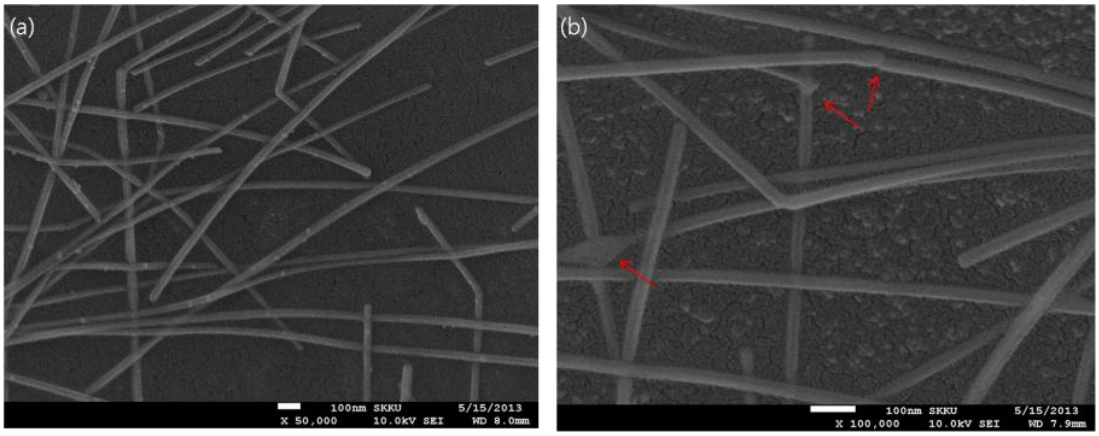

Fig.1 (a) Pristine AgNWs network. (b)Fused AgNWs network after TiO_2:Cs sol-gel treatment.

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[2] Rui Zhu, Choong-Heui Chung, Kitty C. Cha, Wenbing Yang, Yue Bing Zheng, Huanping Zhou, Tze-Bin Song, Chun-Chao Chen, Paul S. Weiss, Gang Li, and Yang Yang ACS NANO. 12, 9877

Chemical vapor deposition of molybdenum thin film for copper interconnect

Jae-Min Park, Clement Lansalot-Matras[1] and Won-Jun Lee
INAME, Faculty of Nanotechnology and Advanced Materials Engineering, Sejong University, Seoul, 143-747,Korea
[1]Air Liquide Laboratories Korea, Seoul, 120-749, Korea
E-mail : wjlee@sejong.ac.kr

Ta and TaN thin films prepared by ionized physical vapor deposition (i-PVD) technique have been used as cladding and diffusion barrier layers for copper metallization, and they are facing a scaling problem as the line width decreases beyond 20 nm. Atomic layer deposition (ALD) and chemical vapor deposition (CVD) are potential solutions to deposit highly conformal ultrathin (<2 nm) cladding/barrier layers, however, it is rather difficult to prepare Ta film by ALD or CVD. Recently, ruthenium, cobalt and molybdenum attract much interest as the materials appropriate for the direct plating of copper. To date, very little work has been done on ALD or CVD of molybdenum [1]. In the present study, we report the CVD of molybdenum thin film at low temperatures of 100–300°C using an organomolybdenum compound. The effect of substrate temperature on the characteristics of the deposited films was also investigated. The deposition is limited by surface reaction at below 100°C, whereas it is limited by mass transport at 100 °C and higher temperatures. The growth rate is ~20 nm/min at 180°C. The resistivity of the deposited film decreases as the substrate temperature increases, and the lowest resistivity of 258 μΩ·cm was obtained at the substrate temperature of 300°C.

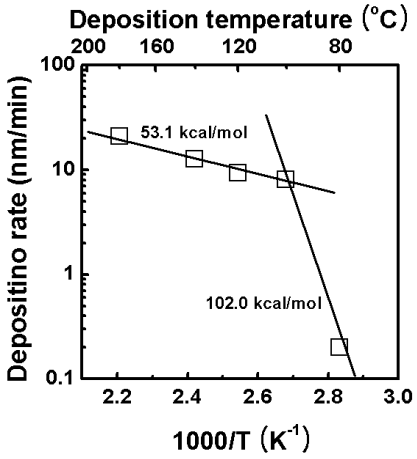

Fig. 1.The Arrhenius plot of the deposition rate of CVD molybdenum film on a SiO_2 substrate

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Atomic layer deposition of highly conformal and amorphous W-Si-N thin films using a novel metallorganic precursor and application to a diffusion barrier for advanced Cu interconnects

Jae-Hun Jung[1], Taek Mo Jung[2], Chang Gyun Kim[2], So Jeong Yeo[2], Taehoon Cheon[1,3], Sang-Kyung Choi[4] and Soo-Hyun Kim,[1,*]

[1] *School of Materials Science and Engineering, Yeungnam University, 214-1, Dae-dong, Gyeongsan-si, 712-749, Koera*

[2]*Advanced Materials Division, Korea Research Institute of Chemical Technology, Daejeon 205-600, Krea*

[3]*Center for Core Research Facilities, Deagu Gyeonbuk institute of Science & Technology, Sang-ri, Hyeonpung-myeon, Daseng-gun, Daegu, 711-873, Korea*

[4]*Center for Research Facilities, Chungnam National University,99, Daehak-ro(St), Yuseong-gu, Deajeon, 305-764, Korea*

E-mail : *Soohyun@ynu.ac.kr

Ternary and amorphous tungsten silicon nitride (WSiN) thin films were grown on thermally grown SiO_2 and TiN substrate by atomic layer deposition (ALD) using a sequential supply of a novel silicon and nitrogen-containing W metallorganic precursor of bis(1-tertbutylamino-2-trimethyl-silyl)tungsten [$W(N^tBu)_2(btsa)_2$] (Fig. 1) and H_2 plasma at substrate temperatures ranging from 250 and 450 ^oC. The typical ALD characteristics, such as self-limited film growth and linear dependency of the film growth on the number of ALD cycles, were confirmed and the growth rates on thermally grown SiO_2 substrate were 0.079 nm/cycle and negligible incubation cycle of ~5. Due to the ideal ALD growth, the step coverage of WSiN film was excellent, ~ 100 % at 25-nm width trench (Fig. 2). A very thin (~ 6 nm in thickness) ALD-WSiN film effectively prevented the diffusion of Cu into Si up to annealing at 650 ^oC.

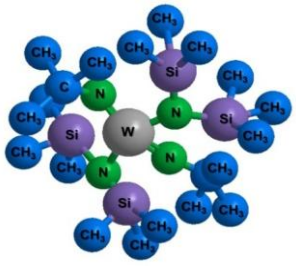

Figure 1. Molecular structure of $W(N^tBu)_2(btsa)_2$precursor

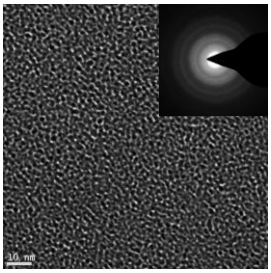

Figure 2. Plan-view TEM image

Acknowledgements

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Enhancement of thermal stability of ytterbium silicide by alloying with molybdenum

Jun-Gu Kang[1], Sekwon Na[1], Juyun Choi[1], Hyungsub Kim[1], Hoo-Jeong Lee[1,*]
1 School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, Korea
E-mail : hlee@skku.edu

In recent years, studies for rare earth silicides have received renewed attention due to needs for low resistance contact materials. Earlier works on electrical contact formation on n-Si shows that rare earth metal silicides have a low schottky barrier height on n-Si with low annealing temperature.[1] Also, Ytterbium silicide has a low electric work function among rare earth metal silicides. So, ytterbium silicides are promising materials as source/drain in N-MOSFETs.[2] Nevertheless, there are several challenges practical usage of this material, including the oxidation problem. One of the problems is the thermal stability of the silicide. In this study, we alloyed ytterbium with Mo to enhance thermal stability of ytterbium silicide. We investigated how adding Mo affects formation of silicide and its electrical properties by using Yb alloyed with Mo with different concentrations (5~10at%). Ytterbium and molybdenum were co-sputtered on a n-Si(100) substrate with a resistivity of 1 to 10Ωm using RF sputtering. To remove the native oxide, the Si substrate was dipped in a solution of 1% diluted hydrofluoric acid. Then, an ytterbium alloy film with 30nm thickness was deposited on the Si substrate by using RF sputtering. Subsequently, a TaN capping layer with 50nm thickness was deposited to prevent the oxidation. The samples were annealed in a rapid thermal annealing from 300℃ to 800℃ for 1min in N^2 ambient to form ytterbium alloy silicide. We used transmission electron microscopy(JEM-2100F) to observe silicidation and EDS for composition analysis. In addition, 4-probe point and I-V measurement system were used for electrical properties. The results indicate that oxidation at high temperatures was auppressed for alloyed sample, suggesting improvement in thermal stability due to the Mo addition. In addition, our thorough materials characterization disclosed that sluggish diffusion of Mo slowed down the overall reaction, which helped improve the thermal stability.

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Cu electroless deposition on the Ta substrate through Pd activation assisted by ultrasound

Kanghoon Kim[a], Taeho Lim[b], Kwang Hwan Kim[b], Hyunjoon Lee[a], Jae Jeong Kim[b], and Oh Joong Kwon[a]

[a]*Department of Energy and Chemical Engineering, Incheon National University, Incheon, 406-772, Korea*

[b]*School of Chemical and Biological Engineering, Seoul National University, Seoul, 151-744, Korea*

E-mail : ojkwon@incheon.ac.kr

For the formation of Cu thin film using electroless deposition, Pd activation with small size and narrow size distribution is required. In order to synthesize small Pd particle, we adopted a sonochemical method in Pd activation step. Sonochemical method is an effective way to synthesize a nanoparticle[1,2].

Experimental was composed of three steps such as an oxide etching, a Pd activation with the assistance of ultrasound, and a Cu electroless deposition. PVD-Ta (7 nm)/Si was used as a substrate, and K_2PdCl_6 and NH_4OH were used as a Pd precursor and a reducing agent. In doing sonochemical reduction, various experimental parameters were firstly optimized, and Cu thin film was obtained at the optimized condition. Figure 1. shows the Cu film which has a thickness of 44.96 nm and the resistivity of 3.37 μΩ · cm. The characterization of Cu film was carried out with a field emission scanning electron microscope (FE-SEM), an X-ray diffraction (XRD), and an atomic force microscopy (AFM). Finally, the gap-filling was performed on 80 nm pattern wafer.

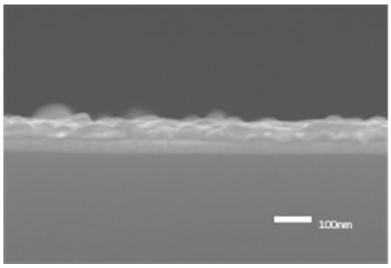

Fig 1. FE-SEM image of the Cu thin film obtained on the Ta substrate activated by sonochemically deposited Pd.

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[7]

[8] Chang-myeon Lee, Jun-Mi Jeon, Hong-kee Lee

[9] Treatment & Plating Technology Center, Technology Application Department, Incheon Regional Division, Korea Institute of Industrial Technology

[10] E-mail : cmlee@kitech.re.kr

[11]

[12] Currently, research on copper electroless plating with palladium activation on various diffusion barriers for metallic interconnects of semiconductor devices is being conducted. Since there is no need for a seed layer for electroless deposition, it is possible to build copper interconnects with uniformity and excellent characterization without poor step coverage. Despite these strengths, the copper interconnect technique for semiconductors using an electroless plating process shows various limits such as high electrical resistivity, void formation in interconnects, and poor adhesion strength. A low thickness of the diffusion barrier due to reduced trenches restricts the surface treatment through etching processes, and incurs problem in that the copper film is easily excoriated by the diffusion barrier. In order to solve these problems, a variety of studies for enhancing the adhesion strength of copper electroless films have been conducted.[1~2] In spite of detailed studies, not much is known about the effect of complexing agents in the copper plating solution on the adhesion strength between a copper film and a diffusion barrier. In this research, the influence of typical complexing agents, Rochelle salt (potassium sodium tartrate) and EDTA (Ethylenediaminetetraacetic acid), was investigated in regard to the adhesion strength, and the causes were examined through structural analysis with XRD.

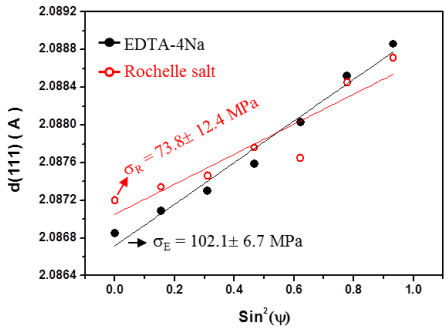

Fig1 d(111) versus $\sin^2\psi$ plots for electroless Cu deposits obtained using EDTA and Rochelle's salt as a complexing agents, respectively.

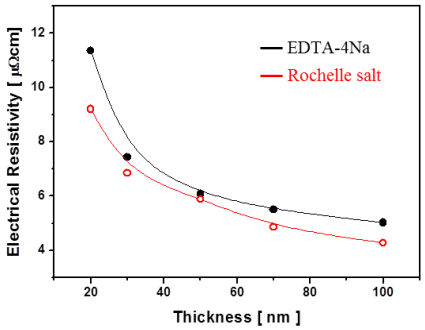

Fig.2 Variation of electrical resistivity of electroless Cu deposits obtained using EDTA and Rochelle's salt as a complexing agents as a function of thickness

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A Study on the improvement of Adhesion for the direct electroless copper plating

Jin-Young Hur, Chang-Myeon Lee, Ho-Nyun Lee, and Hong-Kee Lee
Heat Treatment & Plating Technology Center, KITECH, Korea
E-mail : isedang@kitech.re.kr

Recently, electroless copper plating has been used as seed layer for electro deposition on the insulating materials and currently, magnified as all wet process which allows direct deposition that could be performed for super conformal gap-fill not having seed layer but with ELD only. At this point, deoxidation and activation for Ta is the process which must be considered preferentially and weightily. This process is the biggest influence on adhesion. Particularly, this study researched about the optimization of the deoxidation Ta process intensively[1]. Substrate used 10nm thickness of Ta. After IPA cleaning, etching process was carried out and then dipping in electroless copper electrolyte was performed prior to applying 10mA/cm^2 of DC. To practice deoxidation, the method of dipping in the mixture of HF 1vol% and HNO_3 1.5vol%, or mixture of NaOH 3vol% and H_2NO_2 1vol%, or mixture of TMAH 3vol% and H_2O_2 1vol% was applied. In addition to that, (1N H_2SO_4) the coulometric reduction method(CRM) was also fulfilled. The experimental results demonstrate that removal works well during the treatment with mixture of NaOH and H2O2 at 50℃ for 5min and mixture of TMAH and H2O2 at 50℃ for 7min, providing Tainoxide/Ta value of 0.18. The treatment with mixture solution of HF 2.0vol% and HNO3 2.0 vol% RT at 10~15 min, proposed Tainoxide/Ta value of 0.22. 1N H2SO4, 0.1mA CRM method is that showed Tain oxide/Ta good the effect values 0.185(Rz is 0.517nm). In order to improve adhesion, It is considered to be favorable to have uniform and rough surface, even if the rate is not fast enough[2].

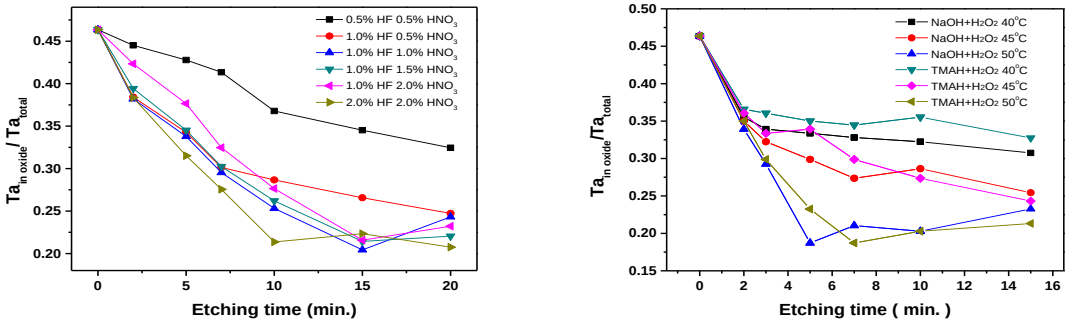

Fig 1. Effect of Ta deoxidation for the catalyst free copper direct plating process

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Verilog-A를 이용한 STT-MRAM 셀의 매크로 모델링

김경민, 유창식
한양대학교 전자컴퓨터통신공학과
E-mail : csyoo@hanyang.ac.kr

본 연구는 자기 터널 접합 (Magnetic Tunnel Junction, MTJ) 기반의 스핀 전달 토크 (Spin Transfer Torque, STT)의 Short Pulse Read (SPR) 특성과 process variation 에 따른 MTJ 의 특성변화를 그림 1. (a)와 같이 모델링 하였다. 우선 SPR 특성을 반영하기 위해 MTJ 에 흐르는 전류량에 따라 자화상태가 변하는 시간이 다른 특성을 이용 하였다. 또한 지속적인 SPR 동작시, 일어나는 읽기 방해 (read disturbance) 현상을 자화의 세차운동 특성을 통해 모델링 하였다 [1]. 다음으로 process variation 에 따른 MTJ 변화의 모델링을 위해서 [2]의 실험 결과를 참고하여 random parameter 값을 적용하였다. 제안된 모델링을 검증하기 위해 그림 1. (b)와 같이 회로를 구성하여 시뮬레이션을 했다. 그림 1. (c)는 정상적인 읽기 (SPR 동작) 또는 쓰기 동작 과정에서 process variation 에 따른 switching time 이 변하는 것을 보여준다. 또한, 그림 1. (d)에서는 지속적인 SPR 동작의 전압 크기와 duty ratio 에 따라 읽기 방해가 일어나는 시간이 다른 것을 보여준다. 시뮬레이션 결과에서 보여지듯이 제안된 모델링은 MTJ 의 random 한 특성을 반영하므로 MTJ 의 주변 회로를 설계할 때 도움을 준다.

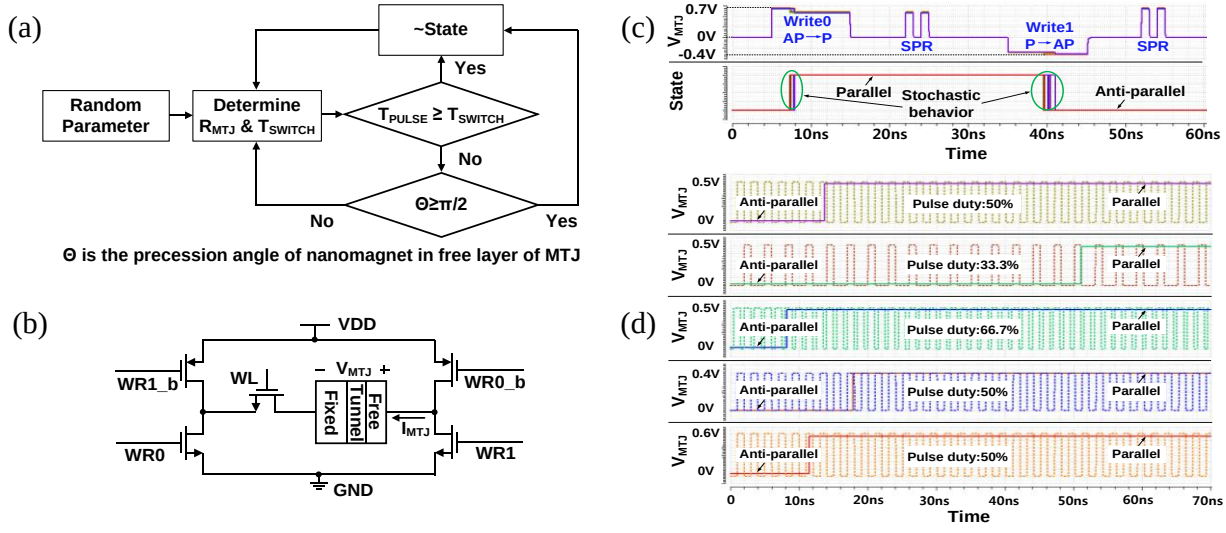

그림 1. MTJ 의 (a) 제안된 모델링, (b) 검증회로, (c)-(d) 시뮬레이션 결과

[1] A. Raychowdhury et al., IEEE, Device Research Conference (2010).
[2] Y. Zhang et al., IEEE, Transactions on magnetics, 49, 7 (2013)

본 연구는 산업통상자원부 및 한국산업기술평가관리원의 산업융합원천기술개발사업 (정보통신)의 일환으로 수행하였음. [10044608, 10nm 급 STT-MRAM 의 MTJ 신뢰성 모델링 및 신뢰성 불량에 강인한 회로 기술 연구]

Study on Physical Mechanism on the Positive Bias Stress-Induced Degradation of Amorphous InGaZnO Thin-Film Transistors with Density-of-States Based Characterization

Chunhyung Jo, Hyeongjung Kim, Sungwoo Jun, Dong Jae Shin, Kyung Min Lee, Jaeman Jang, Jaewook Lee, Juntae Jang, Sungju Choi, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim [a)]

School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

[a)]E-mail : drlife@kookmin.ac.kr

In active matrix organic light emitting diode displays (AMOLEDs), amorphous oxide semiconductor-based thin film transistors (TFTs) operate as current drivers at the turn-on state (gate-voltage $V_{GS}>V_T$ and drain-voltage $V_{DS}>0$) for a long frame time, and the electrical stability of the driving TFT is very important to guarantee the image quality of the AMOLED. Most previous publications draw attention to the charge trapping as a dominant mechanism, although some observations favoring a defect creation under high positive bias [1]. However, the charge trapping and the creation of defect states near the channel/dielectric interface do not offer a sufficient physical explanation on the instability mechanism. In this work, the instability mechanism of amorphous InGaZnO (a-IGZO) TFTs under a positive bias stress (PBS) was systematically investigated. In particular, we pointed out a variation of the subgap density-of-states (DOS) as the most probable physical mechanism on the degradation of the carrier transport characteristics [2]. Moreover, the PBS effect was examined by both capacitance-voltage (C-V) and current-voltage (I-V) measurement in order to systematically characterize the degradation mechanisms quantitatively.

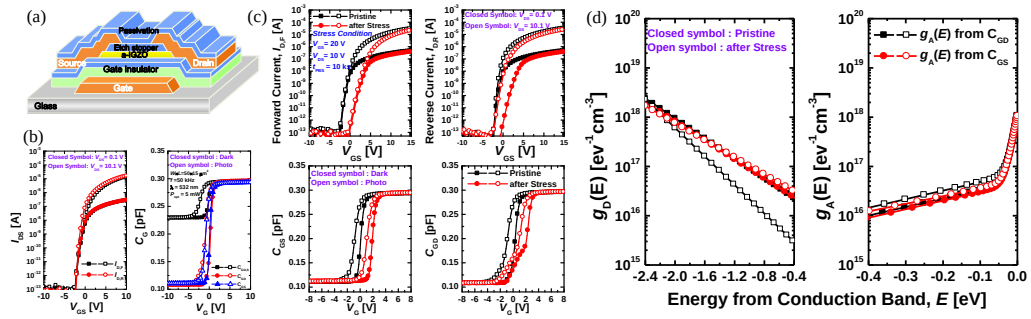

Fig 1. (a) Schematic of the a-IGZO TFTs, (b) *I-V* curve at V_{DS}=0.1, 10.1 V ($I_{D,F}$, $I_{D,R}$) and C-V curve under dark and photonic states ($C_{GD,S}$, C_{GD}, C_{GS}), (c) PBS time evolution (t_{PBS}) of *I-V* and *C-V* curve characteristics, (d) t_{PBS} of subgap DOS.

[1] R. B. M. Cross and M. M. De Souza, IEEE International Reliability Physics Symposium, pp. 467-471 (2007).

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Degradation and Breakdown of MgO Magnetic tunnel junction

Jungmin Lee, Chulmin Choi, Kyuhyun Gil and Yunheub Song
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : yhsong2008@hanyang.ac.kr

A reliability of a magnetic tunnel junction (MTJ) based on a CoFeB with an MgO tunnel barrier was evaluated by constant voltage stress and interval stress. In particular, we focused on its dependence on the barrier thickness, junction size, polarity of the applied voltage. The results suggest that the breakdown voltage strongly depends both on the polarity of the applied voltage. It was found that a negative bias application, which corresponded the electron tunneling from the top electrode to the bottom one, provided a larger resistance drift compared with the negative bias in a voltage stress with a constant time and an interval. The reduction of the resistance drift in the positive bias application is attributed by surface roughness and crystalline of MgO barrier. Furthermore, a breakdown modeling for the MgO barrier was carried out in aspect of the "*E*" and "1/*E*" models through the stress tests. As a result, we found that an interface condition of the MgO layer played a very important role in the reliability of a barrier for the CoFeB/MgO/CoFeB MTJs. This study will be helpful in understanding the degradation and breakdown of Magnetic tunnel junction.

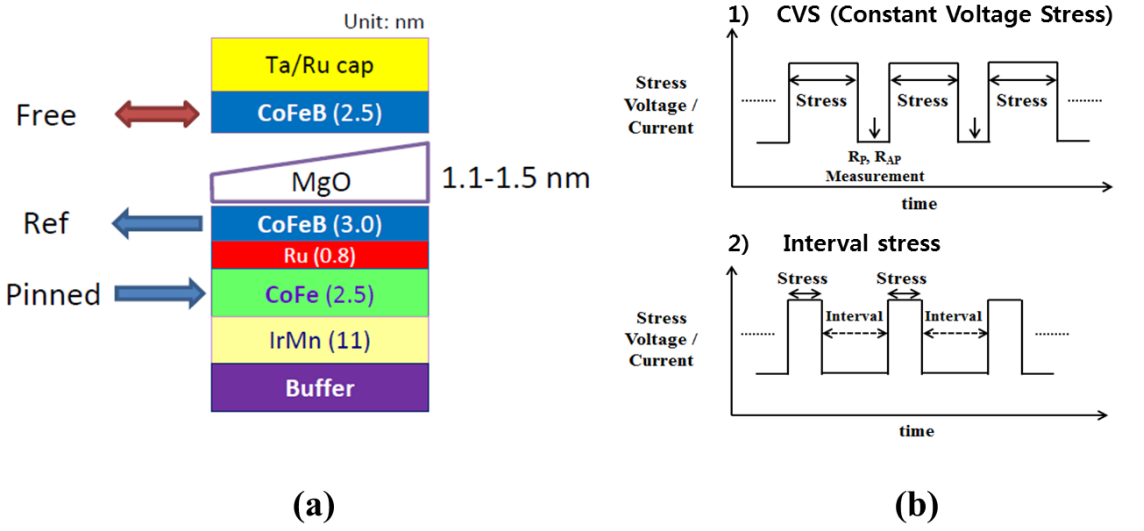

Fig 1. (a) Schematic illustration of MgO barrier based MTJs using CoFeB. (b) Timing diagram of Constant voltage and interval stress.

Substrate doping concentration dependence of electron mobility enhancement in uniaxial strained (110)/<110> nMOSFETs

Wookyung Sun, Sujin Choi and Hyungsoon Shin
Department of Electronics Engineering, Ewha Womans University, Seoul 120-750, Korea
E-mail : hsshin@ewha.ac.kr

As device dimensions shrink, the enhancement of carrier mobility by strain has been investigated to improve device performance. We investigated the substrate doping concentration dependence of strain-enhanced electron mobility in (110)/<110> nMOSFETs using one-dimensional self-consistent Schrödinger-Poisson solver. The electron mobility model includes coulomb (μ_{coul}), phonon(μ_{ph}), and surface roughness (μ_{sr}) mobility. To consider the physical mechanism of mobility enhancement in strained nMOSFETs, we take the intravalley and intervalley phonon scattering into account [1]. Our simulation results shows excellent agreement with the experimental data taken from [2]. It is found that the relative occupancy of sub-valleys is the major factor to determine the electron mobility enhancement induced by strain. Our calculation x propose that the strain-induced electron mobility enhancement on the (110)/<110> can be increased at high substrate doping concentration. It is a contrast to (100)/<110>. Conclusively, the results of this paper should be helpful in understanding the strain-induced elecetron mobility characteristic and advantageous for strain-induced high electron mobility.

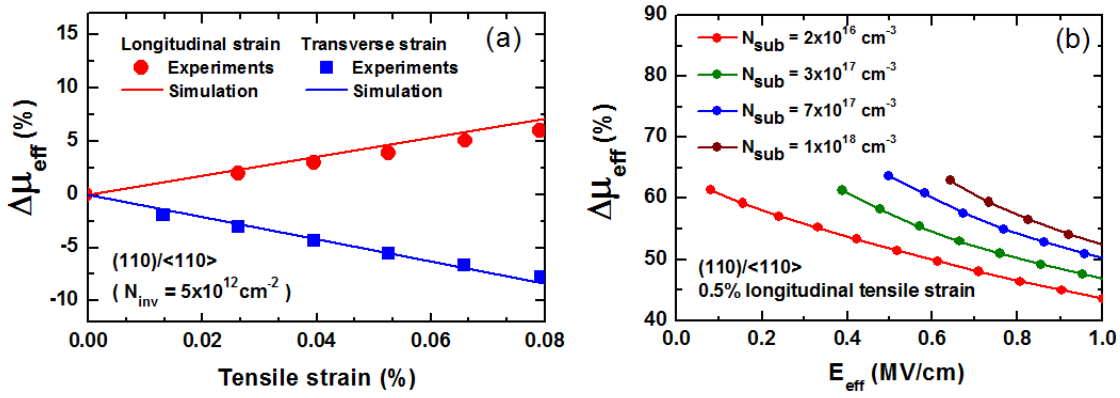

Fig 1. Strain induced electron mobility enhancement in the (110)/<110> (a) with various strain condition and (b) with various substrate doping concentration

[1] S. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, J. Appl. Phys., 80, 1567 (1996).
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Influence of the poly-Si/SiO_2 interface traps on the program/erase characteristics of 3D SONOS NAND Flash memories

Jeongsu Lee[1], Seonjun Choi[2], and Seung-Beck Lee[1,2,3]

Department of Nanoscale Semiconductor Engineering[1], Department of Electronic Engineering[2], and Institute of Nano Science and Technology[3], Hanyang University, Seoul 133-791, Korea

E-mail : sbl22@hanyang.ac.kr

Recently, three dimensionally integrated structures were reported as a candidate to solve the planar 2D integration density issues. However, including Bit Cost Scalable (BiCS) Flash memory [1], physical mechanisms of reliability issues for the 3D Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) device are not fully understood yet. Among them, poly-Si/SiO2 interface traps are recognized to have impact on program/erase (P/E) operation and vice versa. A well-known generation proceses of interface trap is that depassivation of hydrogen (H) or deuterium (D) at the Si-SiO_2 interface which were dangling bonds initially[2]. In this study, we simulated a single SONOS cell with constant channel interface trap density varies from $1X10^{10}$ cm^{-2} to $3X10^{12}$ cm^{-2} to verify its effect on V_{th} variation and memory window. As a result, increased interface trap density affects both initial V_{th} and memory window of programmed cell. Maximum initial Vth difference was about 3.2 V and maximum memory window difference at fully programmed state was about 1.4 V showing memory performance degradation with increasing interface trap density.

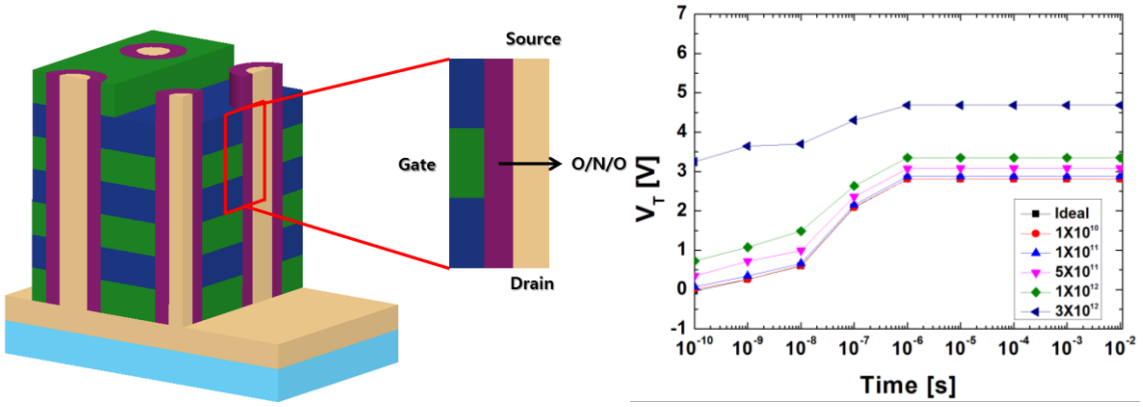

Fig. 1. Simulated structure and its program characteristics (V_{pgm} = 20 V) of a SONOS cell.

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Electrical characteristic variations of FinFETs dependent on the fin shape

Ju Tae Ryu, and Tae Whan Kim

Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea

E-mail : twk@hanyang.ac.kr

Scaling-down process of the planar memory devices face has been extremely challenging due to interent problems of short channel effects, leakage currents, process variations, and reliability degradations. FinFET devices have been particularly attractive because of excellent performance about scaling-down devices [1, 2]. Electronic devices by using a FinFET structures have been suggested due to the scale-down advantages of logic processors and static random access memories. Even though some studies concerning the effect of the fin width, the gate length, and the silicon on insulator substrate have been performed, few investigations on the effect of the gradient fin shape of the electrical characteristics for the FinFETs have been reported.

This paper presents data for the shape effects of the fin side wall on the electrical charateristics of the FinFET. The electrical characteristics of the FinFETs were simulated to optimize the device performance by using the three-dimensional technology computer-aided design tools taking into account a multi-orientation mobility model. The gradient angle of the fin side wall was varied to investigate the effect of the shape of the fin side wall on the electrical characteristics of the FinFETs. The performance of the n-channel FinFET was investigated by using the distribution of on-current, the threshold voltage, and the subthreshold swing. While the gate length, gate width, fin thickness, and fin height used in this simulation are fixed, the gradient angles were changed. The upper surface orientation of the fin was different from its side surface orientation. The variation of the electron mobility on the fin side was significantly increased by the variation of the fin shape. The electrical characteristics of the FinFETs become deteriorated with decreasing on-current level and increasing subthreshold swing. The degradation mechanisms of the performance for the FinFETs were analyzed by the vertical electric field and the electrical potential of the fin side region.

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2013-016467).

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Demonstration of neuron spike model using memristive MTJ element

Sungmin Hwang, Dong Ik Suh, Junwoo Lee, and Wanjun Park
Department of Electronic Engineering, Hanyang University, Seoul 151-747, Korea
E-mail : wanjun@hanyang.ac.kr

Neuromorphic architecture has been proposed as an alternative approach for after-era of current IC technology with adoption of neural functions based on functional combination of synapse and neuron for the recognition, learning, and conjecture. The memristive device has been demonstrated for the basic device element since it achieves the analog synaptic functions. Magnetic tunnel junction (MTJ) is a candidate of the memristive element with bi-state switching characteristics determined by the magnetization aligning direction of two ferromagnetic layers which are separated by an insulator. In this paper, we propose a simple circuit system composed of 1-transistor and 1-MTJ as a device element for generating the function of action potential firing in the spiking neuron model. We also emulate the neural spiking signal by modeling and simulation with development of MTJ macro-model for SPICE. Current researches in this area are limited so far, only for realizing artificial synaptic function, but the proposed device is expected as a device element for generating artificial neural function which is applicable to a new form of computing comprehensive neural network.

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Device design of Short Channel Tunneling Field-Effect Transistor for Low Standby Power Application

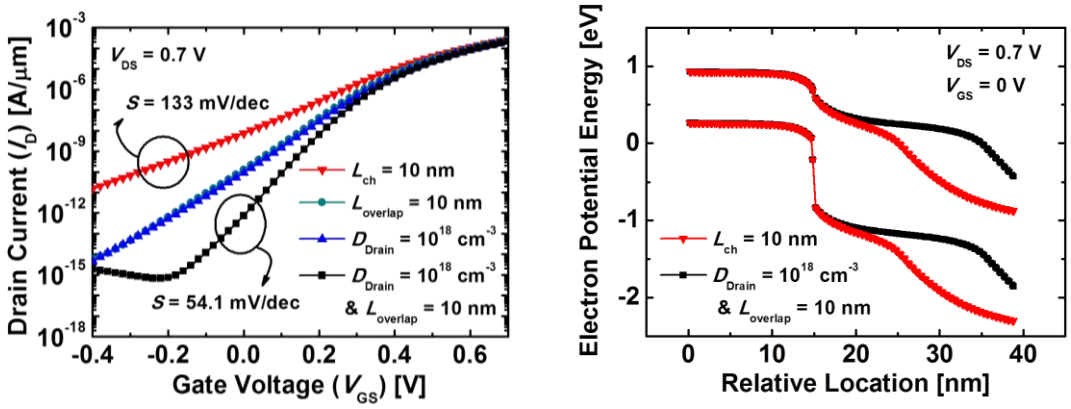
Hye Rim Eun[1], Young Jun Yoon[1], Jae Hwa Seo[1], Hee-Sung Kang[1], Eou-Sik Cho[2], Seongjae Cho[2], Jung-Hee Lee[1], and In Man Kang[1*]

[1]*School of Electronics Engineering, Kyungpook National University, Buk-gu, Daegu 702-701, Republic of Korea*

[2]*Department of Electronics Engineering, Gachon University, Seongnam, Kyunggi-do 461-701, Republic of Korea*

[*]E-mail : imkang@ee.knu.ac.kr

Tunneling field-effect transistors (TFETs) are promising low standby power (LSTP) device because of precipitous subthreshold-swing (S) and low off-state current (I_{off}) [1]. However, as the channel length of TFET is decreased down to 10 nm, TFETs having short channel below 10 nm showed high S above 60mV/dec and I_{off} due to drain induced barrier thinning (DIBT). In this work, we designed a short channel TFET by using device simualtion ATLAS to overcome these drawbacks [2]. The proposed TFET consist of Ge source, GaAs channel and GaAs drain for high current performances. The GaAs channel length (L_{ch}), total gate length (L_g) and drain-overlap length ($L_{overlap}$) are 10 nm, 20 nm, and 10 nm, respectively. Fig. 1 (a) shows transfer curves of short channel TFET having various structures. TFET having drain overlap structure and low drain doping achieves S below 60 mV/dec without change of on-state current (I_{on}). The drain-overlap structure and low drain doping can form large tunneling barrier width in channel by suppressing DIBT, as shown in Fig. 1 (b). It has been confirmed that the short channel TFET having low drain doping and drain-overlap structure has strong potential by achieve steep S and low I_{off} for LSTP operation.



(a) (b)

Fig. 1. (a) Transfer curves and (b) Energy-band diagrams of various short channel TFET.

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Simulation of the installation process of solid-state drives to improve their mechanical reliability

Jinwoo Jang, Yusuf Cinar, Juyub Lee, and Gunhee Jang
Department of Mechanical Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : ghjang@hanyang.ac.kr

Recently, solid-state drives (SSDs) have attracted a lot of attention due to its high performance and small volume compared to hard disk drives(HDDs). SSDs have been exposed to various mechanical impacts, such as bending, vibration and thermal cycling during installation, trasportation or operation. Especially, installing SSDs to device by hand could result in solder joint crack(SJC), due to considerable bending motion of SSDs. In this study, we investigated the installation process of SSDs into device to reduce the stress of solder joints. The experimental method as shown in Fig.1 has been developed to measure the force, moment and strain of SSDs in the installation process. The finite element (FE) model of the SSD has been developed to simulate the installation process. To validate the FE model, the natural frequencies and modes were calculated and compared with experimental modal testing. FE simulation has also been conducted to calculate strain and stress of a solder joint. Calculated strain values from the FE model were also compared with the experimental ones. Finally, appropriate installation condition to reduce the stress of solder joint has also been proposed. This study will contribute to understand the installation condition of SSDs in order to improve the mechanical reliability of SSDs.

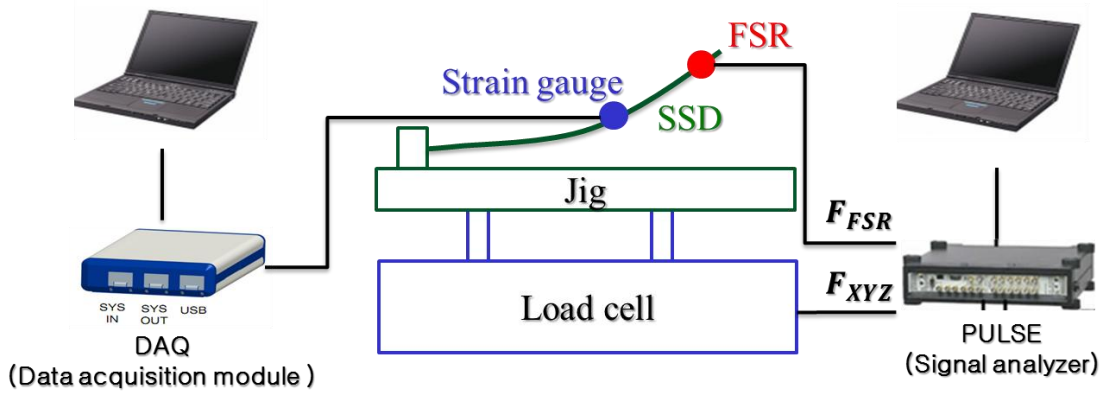

Fig 1. Experimental setup to measure installation condition data

Theoretical study on Organic Light Emitting Diodes With Micro-cavity Structure

Young-Wook Hwang, Hyeon-Gi Lee, and Tae-Young Won
Department of Electrical Engineering, Inha University, Incheon 402-751, Korea
E-mail : twon@inha.ac.kr

A structure with two reflective interfaces is ususally called a micro-cavity. In this paper, we report a numerical study on the electronic-optical properties of the organic light emitting diodes (OLEDs) with micro-cavity structure. OLEDs are made up of N,N'-bis(3-methylphenyl)-N,N'-bis(phenyl) benzidine (TPD) as a hole trasport layer (HTL) and tris(8-hydroxyquinolinato)aluminum (Alq3) as an electron transport layer (ETL). Additionally, we employ the reflectors which consists of the a thick metal mirror on one side and a distributed Bragg reflector(DBR) on the other side for micro-cavity effects. The DBR comprise a combination of layer with refractive index difference. Our simulation revealed that the insertion of the bottom mirror play a critical role in the emission property. Compared with the non-cavity device, we can observe the device with a cavity structure has a narrower spectrum and the chromaticity is changed. The modification results in enhanced emission compared to the conventional devices.

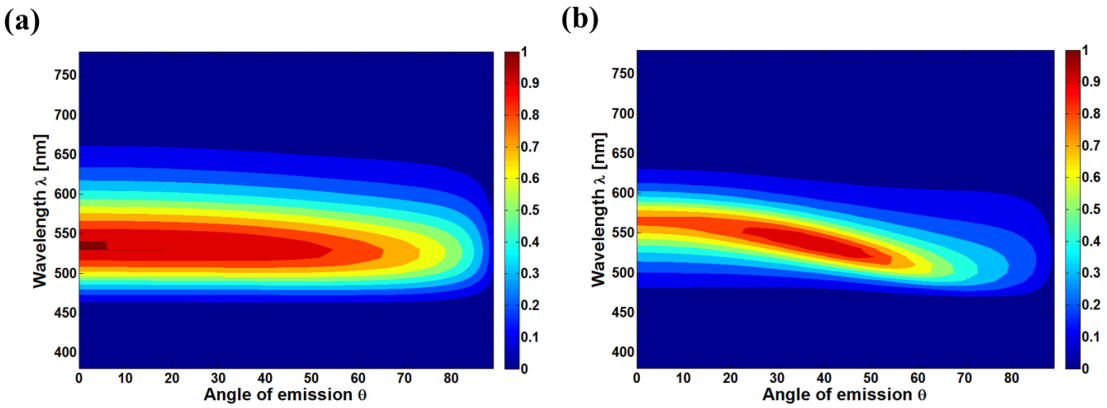

Fig.1 (a) Calculated the angular emission spectra of the conventional OLED (without DBR). (b) Calculated the angular emission spectra of the enhanced OLED (with DBR)

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The enlargement of process window by using source optimization

Du Hyun Beak, Jin Phil Choi, Tony Park, Young Seog Kang, and Hun Hwan Ha
Samsung Electronics Co., Ltd, San #16, Banwol-Dong, Hwasung-City, Gyeonggi-do, Korea
E-mail : dh.beak@samsung.com

We report that the process margin at critical layers with low DoF (depth of focus) and low EL (exposure latitude) can be effectively enlarged by using source optimization (SO) [1].
Recently, we are suffering from the low process margin in semiconductor industry. This is inevitable and natural since process window margins are getting smaller as design rule shrinks down.
In this paper, the source optimization is performed for the purpose of the process window enlargement. Usually, the DOE (diffractive optical element) has been employed to generate the illumination source at photo lithography equipment. However, it is found that the freeform source can make larger process window than DOE without any mask layout changes. The result shows the DoF margin improvement around 8% and EL improvement over 20% can be achieved by source optimization [2].
The source optimization gives the novel method to get larger process margin without any changes such as mask, stacks and so on, and will be helpful to understand the relations between illumination source and optical lithography.

Keywords: source optimization, source mask optimization, process window, freeform source

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Computational study on Behaviors of Carrier in OLED devices with thin CuPc layer

Hyeongi Lee, Youngwook Hwang, and Taeyoung Won
Department of Electrical Engineering, Inha University, Incheon, Nam-gu, Korea
E-mail : twon@inha.ac.kr

We discussed on behaviors of carrier in OLED device which has the thin CuPc layer for hole injection layer (HIL). We used Alq_3 (Tris (8- hyroxyquinolinato) aluminium) for electron transfer layer, S-DPVBi (4,4'-bis (2,2'- diphenylvinyl) -1,1'- spirobiphenyl) for Emission layer and S-TAD (2,2′,7,7′-tetrakis-(N,N-diphenylamino)-9,9′-spirobifluoren) for hole transfer layer. After we varied lowest unoccupied molecular orbital (LUMO) and highest occupied molecular orbital (HOMO) of thin CuPc Layer, we compared simulation results of each device. We determined four OLED devices for our simulation. Device A is the tri-layer device which doesn't have HIL. Device B is the device which HIL has 5.3 eV of HOMO level and 3.8eV of LUMO level. Device C is made by varing LUMO level of HIL to 3.0eV. Finally, we varied HOMO level of HIL as 5.4 eV. This device also used for Device D in our simulation. In this paper, we simulated carrier injection, transportation and recombination of these four devices. Thereby we showed the effect of HIL, as well as we demonstrated that the characteristic of these devices has been improved by a thin layer of CuPc between the anode and HTL.

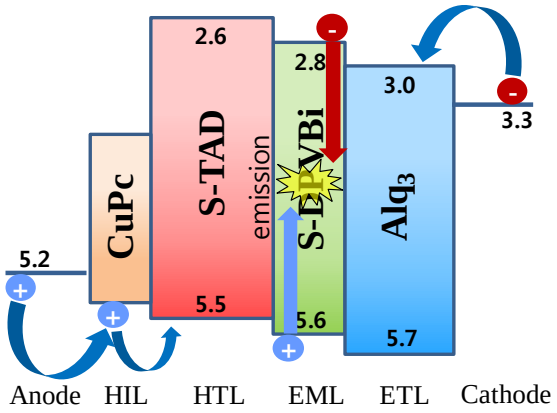

Fig 1. Four layer OLED

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Constant current stress-induced instability of the top-gate IZO TFTs for AMOLED displays

Sungju Choi, Jaeman Jang, Hyeongjung Kim, Juntae Jang, Jaewook Lee, Chunhyung Jo, Sungwoo Jun, Kyung Min Lee, Dong Jae Shin, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim[a)]

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul, 136-702, KOREA

[a)]E-mail : drlife@kookmin.ac.kr

Motivated by that a real mass production of oxide thin-film transistor (TFT)-driven active-matrix organic light-emitting diode (AMOLED) displays began very recently [1], the instabilities of *n*-channel oxide TFTs induced by applying the positive gate/drain voltage (V_{GS}/V_{DS}) need to be understood. On the other hand, the top-gate structure showed potential for high performance [2-4]. However, details on positive V_{GS}/V_{DS} stress-induced degradations of the oxide TFTs driving AMOLED displays have been seldom investigated. Here we investigated the constant current stress (CCS)-induced long-term instability of indium-zinc-oxide (IZO) TFTs not only by consolidating all of the experimental *I-V*, *C-V*, and device simulation but by paying a special attention to the difference between forward and reverse read-out (*I-V* sweep with switching source and drain). It was found that the CCS-induced degradation of threshold voltage (ΔV_T) and subthreshold swing (ΔSS) was larger in reverse rather than in forward read-out. Related mechanism was most likely to be the hot carrier generation followed by the electron trapping localized in drain edge. The difference between top-gate and bottom-gate structure was also addressed in perspective of CCS instability. Our results are expected to be useful for optimizing TFT structure for AMOLED era.

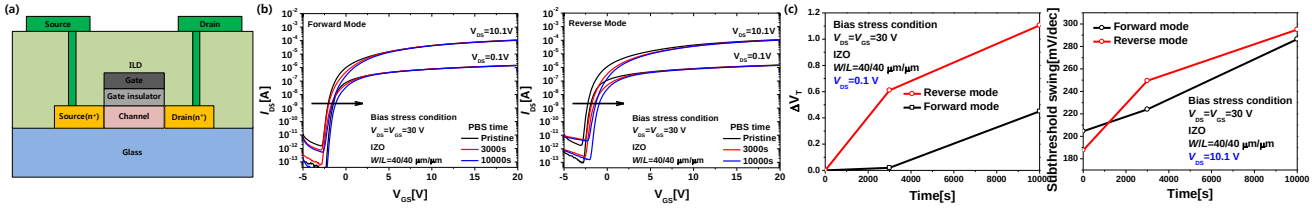

Fig 1. (a) Schematic of top gate a-IZO structure, (b) The forward and reverse transfer curves according to stress time, and (c) ΔV_T, *SS* vs. time characteristics of a-IZO TFTs.

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다층 PCB 휨 거동 예측을 위한 패턴 모델링 및 해석기법 개발

김도형 [1], 주성준 [1], 이준희 [2], 곽동옥 [2], 김학성 [1,3]*

1. *Department of Mechanical engineering, Hanyang University, Seoul 133-791, Korea*
2. *Memory Division, Samsung Electronics, Hwasung 445-701, Korea*
3. *Institute of Nano Science and Technology, Hanyang University, Seoul 133-791, Korea*

*E-mail : kima@hanyang.ac.kr

최근 스마트폰, solid state disk (SSD), multimedia card (MMC) 제품 등의 고집적형 반도체 제품 시장 비중이 커지고 있어 반도체 제품의 집적화와 고밀도 패키징 기술 개발의 필요성이 대두되고 있다. 이를 위해 인쇄회로기판 (printed circuit board: PCB)은 점점 얇아지고 있고, 공정 중에 사용되는 온도는 더 높아지게 되면서 PCB 는 최대한 휨을 억제하도록 요구되고 있다. PCB 의 휨은 제조 공정 중 구성요소들간의 부적합한 결합과 연결의 실패를 일으킬 수 있고, 추후 공정 과정에서도 조립의 어려움과 장기 신뢰성 저하 등 심각한 품질상의 문제점들을 야기하기 때문이다 [1]. 본 연구에서는 기존 다층 PCB 기판 휨 해석의 주요 어려움이었던 구리패턴의 기하학적 복잡함과 소재의 점탄성 물성을 고려하면서도 정확한 휨을 예측할 수 있는 모델링 및 해석 기법을 제안하였다. 이를 위해 각 구리패턴의 가상 물성 테스트를 통한 패턴 별 등가물성 라이브러리화가 수행되었으며, 해석 프로그램의 서브루틴을 개발하여 축 방향에 따라 달라지는 점탄성 물성을 구현하였다. 이를 통해 실제 공정 열 이력에서의 2 층 PCB 의 휨 해석을 수행하였고 실험 결과와 유사한 휨 양상을 성공적으로 예측 할 수 있었다. 이 연구에서 제안한 방법은 다양한 패턴 및 공정상의 PCB 휨 문제를 위한 설계 개선에 활용될 수 있으리라 기대된다.

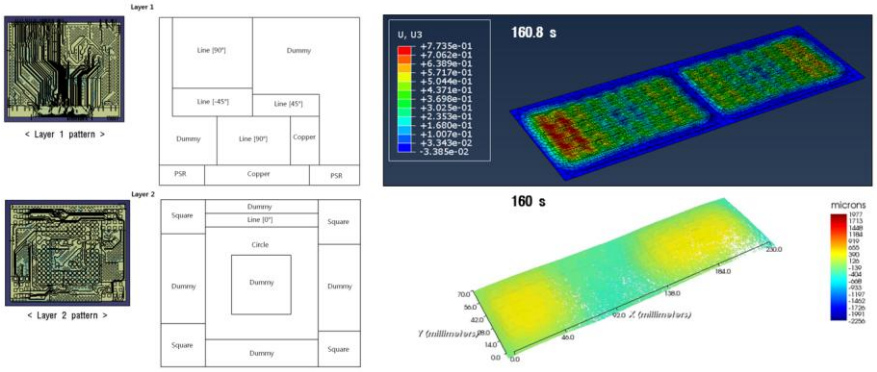

Fig 1. Equivalent modeling of PCB pattern area and warpage analysis.

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Design and Analysis of Gate-recessed Double Heterojunction AlGaN/GaN Field-Effect Transistor

Hye Su Kang[1], Jae Hwa Seo[1], Young Jun Yoon[1], Hwan Gi Lee[1], Gwan Min Yoo[1], Young Jae Kim[1], Sung Yoon Kim[1], Sung Yun Woo[1], Hee Bum Roh[1], Hye Rim Eun[1], Seongjae Cho[2], Jung-Hee Lee[1] and In Man Kang[1,*]

[1]*School of Electronics Engineering, Kyungpook National University, Daegu, 702-701, Korea*

[2]*Department of Electronics Engineering, Gachon University, Seongnam, Kyunggi 461-701, Korea*

[*]E-mail : imkang@ee.knu.ac.kr

These day, various of the GaN-based transistors have been studied and purposed. The superior characteristics such as wide bandgap, high electron velocity, and polarization field makes GaN-based transistors as a essential elements in high-power, high-temperature, and high-frequency electronic applications [1-2]. In addition, due to a two-dimensional electron gas (2DEG) which is formed by AlGaN/GaN heterojunction has a high electron mobility and current drivability, the AlGaN/GaN heterojunction devices are one of the most common devices in GaN-based transisotor technology. In this works, the gate-recessed double heterojunction (DH) AlGaN/GaN field-effect transistor (FET) is designed and analyzed by technology computer-aided design (TCAD). In Fig. 1, the purposed device which has a double 2DEG layer and gate recessed structure is demonstrated. The double 2DEG layer formed by AlGaN/GaN DH structure ensure the increase of current drivability. And the gate-recess sturcture suppress the degradation of threshold voltage (Vt). For the comparison of device characteristics, the AlGaN/GaN based HEMT, MOS-HFET, and DH MIS-FET are also designed and analyzed.

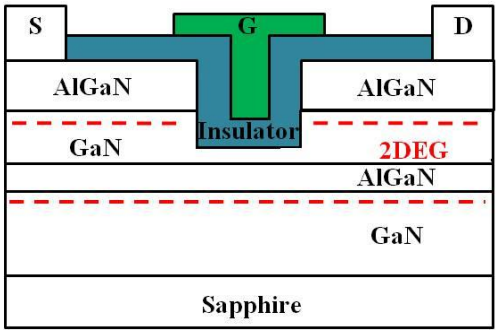

Fig 1. Schematics of the gate-recessed DH AlGaN/GaN FET

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Pixel Circuit with a-IGZO TFT for AMOLED

Jae-Pyo Lee[1], Kyeong-Min Yu[1], Jin Nyoung Jang[2], MunPyo Hong[2] and Byung Seong Bae[1]
[1]*Dept. of Display Engineering, Hoseo University, Asan, Chungnam 336-795, Korea*
[2]*Dept. of Display and Semiconductor Physics, Korea University, Sejong, Korea*
E-mail : bsbae3@hoseo.edu

This paper proposes a threshold voltage compensation pixel circuit for active-matrix organic light emitting diode (AMOLED) using amorphous indium-gallium-zinc-oxide thin-film transistors (a-IGZO-TFTs) [1-5]. Oxide TFT is an n-channel TFT; therefore, we optimized the circuit for the n-channel TFT characteristics. The proposed pixel circuit was verified using circuit analysis as well as circuit simulations. The proposed circuit could compensate for the threshold voltage variations of drive TFT in AMOLED. Using the proposed pixel circuit, threshold voltage compensation was achieved.

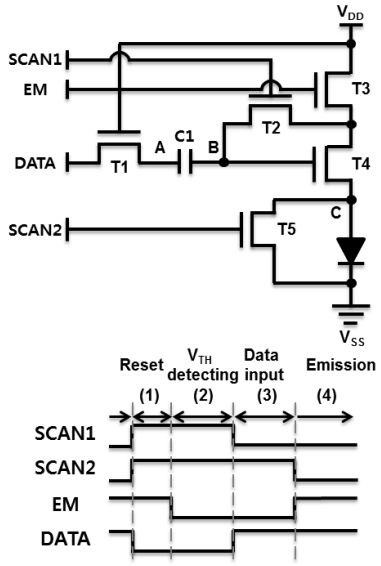

Fig 1. Proposed pixel circuit with a timing diagram

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[2] C. L. Lin, W. Y. Chang, and C. C. Hung, IEEE Electron Device Lett., 34, 1166 (2013).
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Effect of gate/drain voltage configuration on electrical degradation of the bottom-gate In-Ga-Zn-O thin-film transistors driving AMOLED displays

Hyeongjung Kim, Jaeman Jang, Jaewook Lee, Chunhyung Jo, Sungwoo Jun, Kyung Min Lee, Dong Jae Shin, Juntae Jang, Sungju Choi, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim[a)]

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul, 136-702, KOREA

[a)]E-mail : drlife@kookmin.ac.kr

Very recently, active matrix organic light emitting diode (AMOLED)-centered future displays driven by oxide thin-film transistors (TFTs) have become very close to their real commercialization [1, 2]. Therefore, a fundamental understanding of degradation mechanisms of amorphous In-Ga-Zn-O (IGZO) TFTs driving AMOLED display backplanes becomes indispensable for the high-frame rate displays with 3-D visual effects.

In this paper, we analyzed electrical degradations of the bottom-gate IGZO TFTs driving AMOLED and investigated the effect of voltage (V_{GS}/V_{DS}) configuration on instability details. Used method was consolidating all of the measured forward/reverse I-V, separately measured C-V (C_{GS}/C_{GD}), and device simulation. It was found that the widely observed positive threshold voltage shift (ΔV_T) was attributed to the local trapping of electrons and its main position could be either near source or near drain by the competition between vertical and lateral electric field, in other words, with very sensitive dependency of V_{GS}/V_{DS} configuration.

Our results can give a physical insight on the pixel circuit optimization of oxide TFT-driven AMOLED displays.

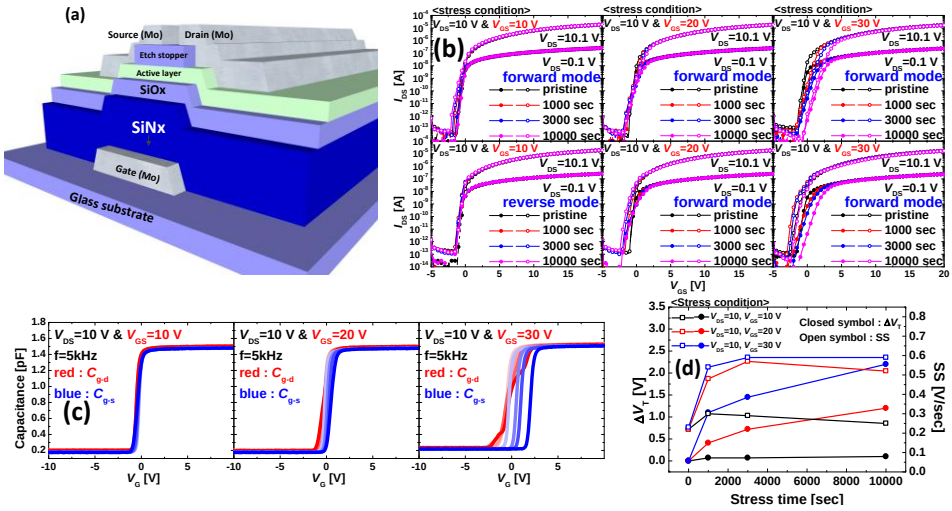

Fig 1. (a) a-IGZO TFTs structure. (b) Forward and reverse mode of transfer curve. (c) $C_{g\text{-}d}$ and $C_{g\text{-}s}$ curves. (d) ΔV_T and SS according to stress time.

[1] W.-J. Nam et al., SID symposium digest, p. 243 (2013)
[2] C.-Y. Chen et al., SID symposium digest, p. 247 (2013)

A Two-Step Set Operation for Reliability of ReRAM with Triple-layer ReRAM

Sangheon Lee, Daeseok Lee, Jiyong Woo, Euijun Cha and Hyunsang Hwang
Department of Materials Science and Engineering, POSTECH, Pohang, 790-784, Republic of Korea
E-mail : hwanghs@postech.ac.kr

For the first time, we demonstrated filament controllability by a two-step set operation based on triple-layer ReRAM. Hence, we report a highly reliable memory switching of a triple-layer structure based on resistive switching memory devices by inserting an additional binary metal oxide layer. The inserted oxide layer in the triple-layer can act as a filament controlling factor with the two-step set operating for reliable resistive switching. Compared with the bi-layer structure, the three layers of the two-step set operation showed excellent uniform V_{set}, V_{reset}, high-resistance state (HRS), and low-resistance state (LRS). Furthermore, the device exhibited excellent memory reliability such as endurance and retention for non-volatile memory (NVM) applications.

The resistive switching random access memory (ReRAM) has been considered as next generation NVMs to solve the scaling limit and for low power operation of the conventional Flash memory [1]. Since 2004, the unipolar type ReRAM with a single-layer, which uses a binary metal oxide, has been extensively studied as active layers for resistive switching owing to its advantages in terms of CMOS compatibility and immunity against thermal and chemical damages [2]. Furthermore, a bi-layer structure was reported as a filamentary bipolar switching ReRAM device for more reliable switching uniformity [3]. It can retain its conductive filament shape for data retention, because it can readily form and dissolve the filament using reactive metal on switching layer. Although various bi-layer ReRAMs have been investigated and the switching variability has improved, ReRAM still retain non-uniform resistive switching parameters such as V_{set}, V_{reset}, high-resistance state (HRS), and low-resistance state (LRS). To mitigate this problem, we demonstrated that the filaments made of two metal oxide layers, namely, hafnium (HfO_x) and tantalum oxide (TaO_x), can be accurately controlled by their different filament formation and dissolution abilities. Highly improved memory performance of the Pt (TE)/Ti/HfO_x/TaO_x/Pt (BE) (250 nm device size) devices was achieved by a two-step filament formation in HfO_x and TaO_x with different filament formation and dissolution abilities. Compared with the Pt/Ti/HfO_x/Pt structure, the inserted TaO_x in the triple-layer can act as a filament controlling layer. Hence, the main concern of the resistive switching fluctuation is significantly mitigated by adopting the triple-layer ReRAM. It is attributed to two filaments formation of HfO_x and TaO_x, which induces stepwise set operation for excellent reliability.

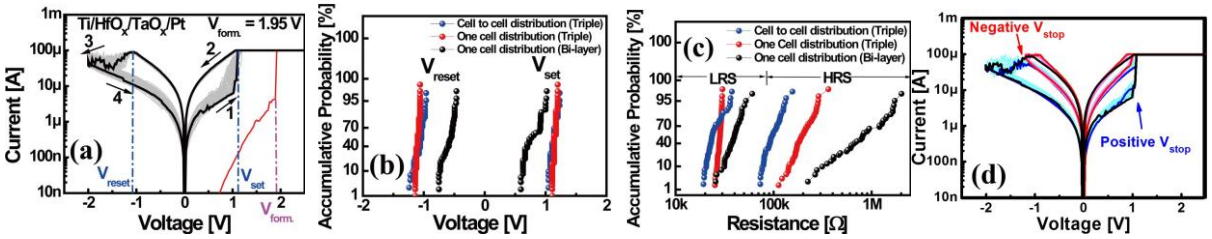

Fig 1. (a) Typical I-V curves of bipolar switching ReRAM in 250 nm via-hole structure (b) and (c) switching distributions (d) The direct evidence of two filament formation in HfO_x and TaO_x.(Blue: In case of only HfO_x filament formation, Red: In case of only TaO_x filament dissolution)

Reference

[1] R. Waser, and M. Aono, "Nanoionic-based resistive switching memories", in Nat. Mater. 6, 833, (2007)

[2] I. G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D. -S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U. I. Chung, and J. T. Moon, "Highly scalable non-volatile resistive memory using simple binary oxide driven by assymetric unipolar voltage pulses", IEEE Int. Electron Devices Meet. pp 587, (2004)

[3] K. Aratani, K. Ohba, T. Mizuguchi, S. Yasuda, T. Shiimoto, T. Tsushima, T. Sone, K. Endo, A. Kouchiyama, S. Sasaki, A. Maesaka, N. Yamada, and H. Narisawa, "A novel resistance memory with high scalability and nanosecond switching", IEEE Int. Electron Devices Meet. pp 783 (2007)

Acknowledgement This work is supported by the R&D program of Ministry of Knowledge Economy.

Investigation of the Deposition of Sb-Te Phase Change Film inside the Trench Structure by the Screen Remote Plasma-Enhanced Atomic Vapor Deposition

Jin Hwan Jeong, Su Bin An, and Doo Jin Choi*

Department of Material Science and Engineering, Yonsei University, 262 Seong Sanno, Seodaemun-gu , Seoul 120-749, Korea

E-mail : drchoidj@yonsei.ac.kr

Recently, phase change random access memory (PCRAM) has attracted a lot of attention as the candidate for next generation memory [1]. However, high operational power consumption is the critical issues of PCRAM. To solve this issue, trench-structure cells have been investigated to minimize thermal energy loss and thermal cross-talk among adjacent memory cells [2]. Though many advangate as low deposition temperature, relatively fast deposition and good film quality, application of plasma deposition to small trench strucutre is at a disadvantage because of its low step coverage. In this research, a new screen remote plasma-enhanced atomic vapor deposition technique was studied for increasing gap fill ability of Sb-Te phase change film. We set a metallic mesh between the plasma region and the substrate to generate a plasma sheath of ions and an energy filter for the control of the activation state of the injected precursors and the deposition of a fine structure. With consideration of a model of the plasma sheath, the gap fill ability of the films was evaluated and we expect this research to provide a new deposition methode for the fine control of step coverage.

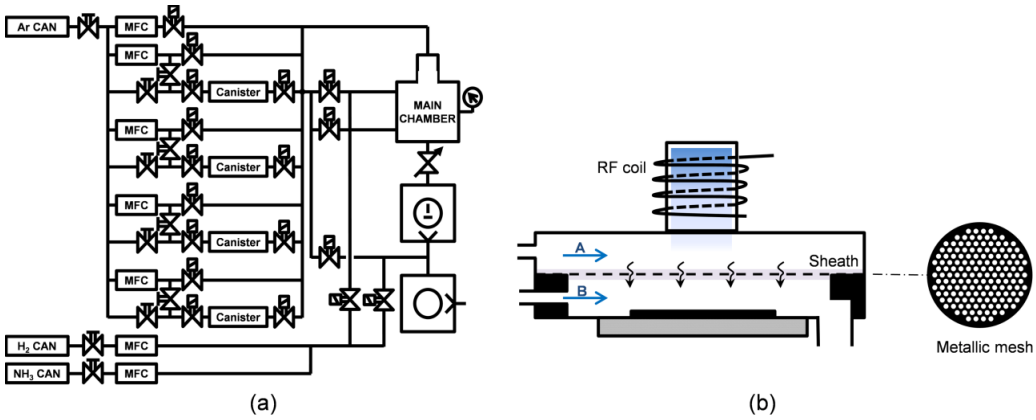

Fig 1. The schematic diagram of (a) the multi-channel PEAVD system and (b) the reaction chamber with metallic mesh

[1] R. Bez, IEDM. Int. Electron. Devices Meeting, 5.1.1 (2009)

[2] A. Pirovano, A.L. Lacaita, A. Benvenuti, F. Pellizzer, S. Hudgens, and R. Bez, IEEE. Int. Electron. Devices Meeting, 699 (2003)

Bipolar resistive switching of $Ge_2Sb_2Te_5$ and $Ge_2Sb_2Te_7$ thin films without involving obvious phase change

Sijung Yoo, Taeyong Eom, Taehong Gwon, and Cheol Seong Hwang*

Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea.

*E-mail : cheolsh@snu.ac.kr

Ge-Sb-Te ternary system is one of the most widely known for PCRAM (Phase Change Random Access Memory) materials among chalcogenide materials. However, shortcomings such as high power consumption for RESET process have been the obstacle for its application to the PCRAM. Recently, resistive switching in GeSbTe system without obvious phase change was reported [1], shedding a new light on the possibility of overcoming such demerits of conventional PCRAM.

In this study, the bipolar resistive switching of GeSbTe system was examined and the mechanism of the switching was proposed. The crossbar type devices with Ti/$Ge_2Sb_2Te_x$/Pt (x=5 or 7) stack with various active area (from 16 to 100 μm^2) were fabricated in order to demonstrate bipolar resistance switching behavior of GeSbTe ternary system. Tellurium-rich ($Ge_2Sb_2Te_7$) composition was adopted to demonstrate the effect of excess Tellurium on device operation in comparison with conventional $Ge_2Sb_2Te_5$ composition. Typical bipolar resistive switching with high R_{HRS}/R_{LRS} was observed while unipolar switching was not possible for both compositions. Both compositions showed almost identical switching characteristics except that the forming voltage is decreased as Tellurium concentration increases. HRS (OFF-State) current showed linear dependence of electrode area while LRS (ON-State) did not, which implies the filamentary nature of this resistive switching phenomenon. LRS conductivity showed a semiconducting behavior ($d\sigma/dT > 0$), suggesting that the conducting filament was composed of semiconducting elements. Taking these observations into consideration, the filamentary bipolar switching of GeSbTe system can be attributed to formation and rupture of the conducting filament composed of Tellurium by migration of Tellurium atoms under high electric field. High resolution transmission electron microscopy confirmed this hypothesis.

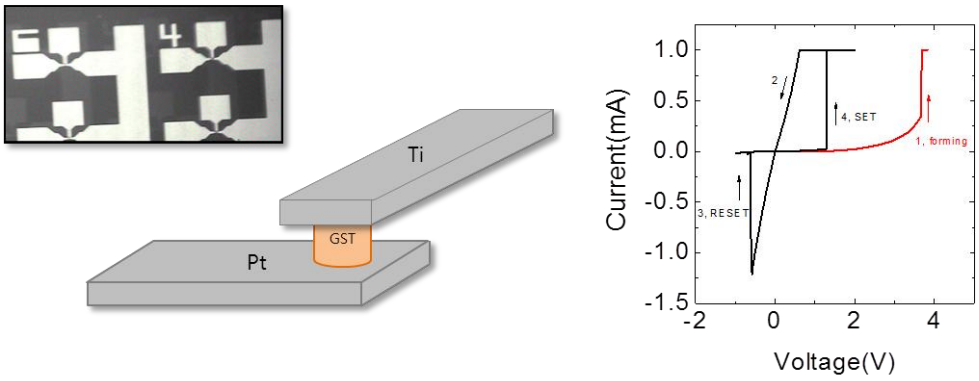

Fig 1. The crossbar type device and its I-V characteristic

[1] R. Pandian et al., Adv. Mater., 19, 4431 (2007)

Improvement of unipolar resistive switching characteristics in Al/$Ge_{0.5}Se_{0.5}$/Pt structure by using Ag nanocrystals

Jang-Han Kim, Ki-Hyun Nam, Won-Ju Cho, and Hong-Bay Chung
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail : hbchung@kw.ac.kr

Recently, resistance change random access memory (ReRAM) has become a promising candidate for next-generation nonvolatile memory (NVM) applications due to its potential for replacement of flash memory. The resistive switching effect observed from various materials, such as binary metal oxide, and chalcogenide materials. Among them, chalcogenide based ReRAM devices that exhibits the bipolar resistive switching (BRS) properties due to formation and dissolution of the Ag or Cu filament in the chalcogenide layer were already reported. In this paper, the unipolar resistive switching (URS) charateristics in the Al/$Ge_{0.5}Se_{0.5}$/Pt structure have been investigated. In addtion, we acheived the uniformity improvement of BRS properties in $Ge_{0.5}Se_{0.5}$ thin film with embedded Ag nanocrystals (NCs) between the Al top electrode (TE) and the $Ge_{0.5}Se_{0.5}$ active layer. Stable DC endurance (> 100 cycles) and high data retention (>10^4 sec.) properties were achieved from the Al/NCs/$Ge_{0.5}Se_{0.5}$/Pt structured ReRAM devices.

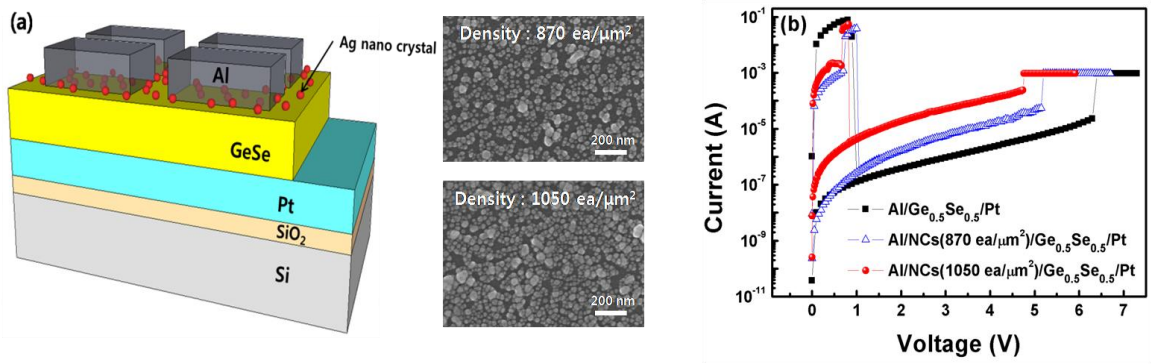

Fig 1. (a) Schematic view of the Al/NCs/$Ge_{0.5}Se_{0.5}$/Pt ReRAM device and the SEM image of Ag NCs. (b) The URS *I-V* characteristics according to the changes in the density of the Ag NCs.

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Fabrication of solution processed Al-doped HfO_x ReRAM

Jung-Hoon Park, Jang-Han Kim and Won-ju Cho
Department of Electronic Materials Engineering, Kwangwoon Univ., Seoul, Korea
E-mail : chowj@kw.ac.kr

최근, 저항 변화 메모리 (resistance random access memory, ReRAM)는 단순한 구조, 고집적성, 저 소비전력, 우수한 retention time 같은 장점을 통해 현재 사용되는 메모리의 물리적 한계를 극복할 수 있는 차세대의 비 휘발성 메모리로써 큰 주목을 받고 있으며, 특히 TiO_2, Al_2O_3, HfO_2 및 Ta_2O_5 등과 같은 이원계 산화물을 이용한 ReRAM 연구가 활발하게 진행되고 있다. 이러한 이원계 산화물의 스위칭 메카니즘으로 필라멘트의 생성과 소멸에 의한 모델이 스위칭 특성을 설명하기에는 가장 적합하지만, 아직까지 스위칭 전압, 저항 분포의 불안정성 같은 문제로 인하여 차세대 메모리로써의 응용이 제한되고 있다. 이러한 문제를 개선시키기 위한 방법으로 이원계 산화물에 대한 금속 삽입, 이온 도핑, 이중 층 구조를 이용하는 방법들이 연구되고 있다. 특히, 이온 도핑의 경우에는 필라멘트의 형성 에너지를 감소시켜 소자의 안정성이 향상되는 것이 보고되고 있다[1]. 그러나 기존의 도핑 방법의 경우에는 도핑 과정에서 많은 공정상의 어려움이 있으며 공정 시간과 비용이 소모된다는 문제점이 있다. 따라서, 공정시간과 비용을 감소시키기 위하여 도핑이 용이한 용액 공정을 이용한 Al-doped ReRAM 을 제작하여 특성을 평가하였다. 그 결과, 매우 우수한 endurance (>100 cycles) 특성 및 안정한 스위칭 동작 (V_{set} : 0.95 V, V_{reset} : −1.18 V, HRS : 10.9 kΩ LRS :0.36 kΩ)을 가지면서 신뢰성이 우수한 ReRAM 을 제작할 수 있었다. 따라서, 도핑이 간단하고 소자의 제작이 용이한 용액공정으로 이온 도핑된 ReRAM 을 제작한다면 차세대 비 휘발성 메모리로써의 적용이 가능할 것이라 생각된다.

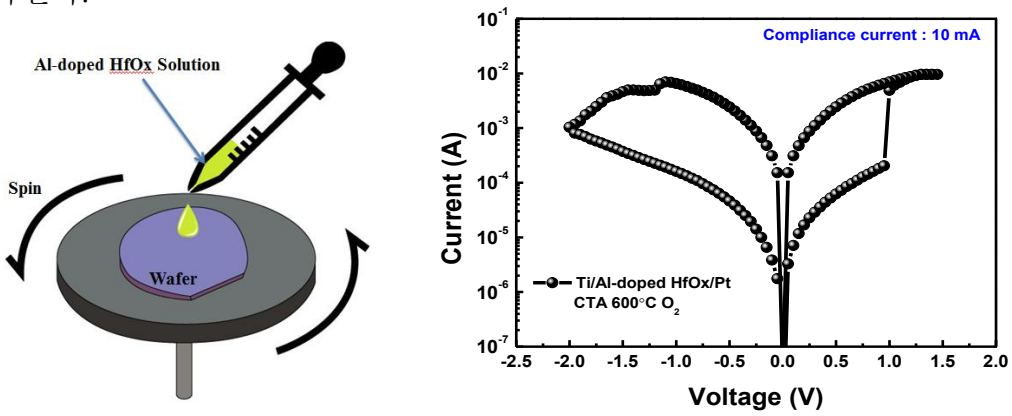

Fig 1. Al-doped HfOx solution process and electrical characteristics

[1] Ching-Shiang Peng, Wen-Yuan Chang, Yi-Hsuan Lee, Ming-Ho Lin,a Frederick Chen, and Ming-Jinn Tsai Electrochemical and Solid-State Letters, 15 (4) H88-H90 (2012)

Acknowledgment

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Characteristics of resistive switching depending on localized conducting filaments

Yeon Soo Kim, Sangik Lee, Jihoon Jeon, Chansoo Yoon, Taejun Oh, Keundong Lee,YoonSeung Nam, Bae Ho Park

Department of Physics, Konkuk University, Seoul 143-701, Republic of Korea

E-mail : baehpark@konkuk.ac.kr

Resistive switching (RS) attracts numerable interests because of its intriguing physical phenomena and great potential applicable semiconductor industry. However, mechanism of uni-polar RS which is explained usually with formation and rupture of filaments is still controversial because of the difficulty of evident observation on study. In this work, we deposited NiO thin film by using reactive DC magnetron sputter on conventional Pt substrate at 500℃. Our study consists of two parts: Using atomic force microscopy (AFM) and electrical measurements by using Agilent 4156B semiconductor parameter analyzer.

We fabricated nano-patterns on NiO thin film by conventional E-beam lithography technique. The conducting filaments in NiO thin film were formed by conducting AFM tip with applying voltage. we kept vacuum ambient during formation of filaments to reduce oxidation effects around air. All nano-patterns are categorized by the number of filament. As-formed filaments are confirmed by current mapping image and current-voltage (I-V) data with current AFM (C-AFM) mode. After depositing Pt top electrode on patterns, which filaments have already formed, by DC magnetron sputtering, electrical characteristics of patterns were measured with Agilent 4156B semiconductor parameter analyzer in probe station. We will show the relation of I-V data with changing number of filaments in each pattern.

Switchable Schottky diode and resistive switching characteristics in Mn-doped ZnO thin films

YoonSeung Nam, ChanSoo Yoon, JiHoon Jun, SangIk Lee, KeunDong Lee, TaeJoon Oh, GwangTaek Oh, and Bae Ho Park*

Dept. of Division of Quantum Phases and Devices, Konkuk University, Korea

E-mail : namssak@nate.com

We investigated the asymmetric current-voltage (I-V) characteristics and accompanying unipolar resistive switching of pure ZnO and Mn(1%)-doped ZnO (Mn:ZnO) films sandwiched between Pt electrodes. After electroforming, a high resistance state of the Mn:ZnO capacitor revealed switchable diode characteristics whose forward direction was determined by the polarity of the electroforming voltage. Linear fitting of the I-V curves highlighted that the rectifying behavior was influenced by a Schottky barrier at the Pt/Mn:ZnO interface. Our results suggest that formation of conducting filaments from the cathode during the electroforming process resulted in a collapse of the Schottky barrier (near the cathode), and rectifying behaviors dominated by a remnant Schottky barrier near the anode.

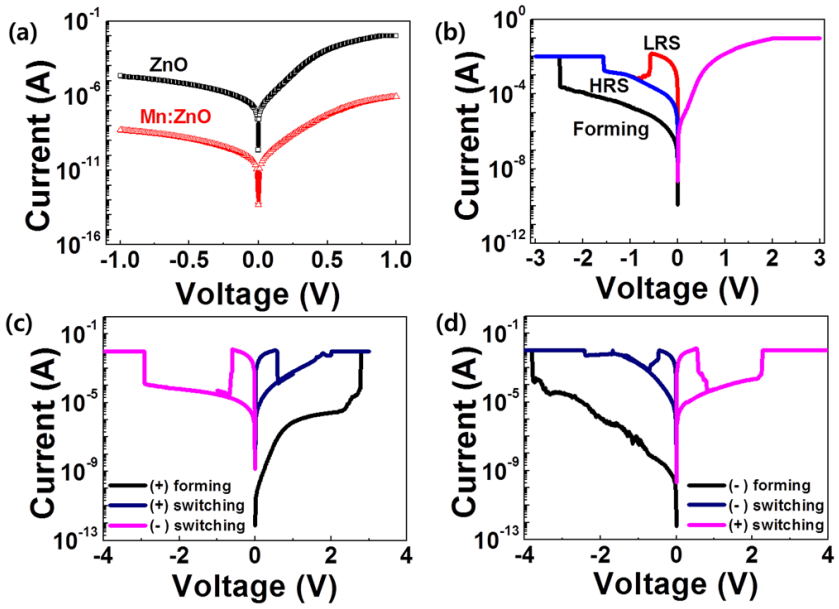

FIG. 1. (a) Low voltage I-V characteristics of Pt/ZnO/Pt and Pt/Mn:ZnO/Pt capacitors. (b)-(d) Unipolar resistive switching behaviors of (b) Pt/ZnO/Pt capacitors, and Pt/Mn:ZnO/Pt capacitors after applying (c) positive and (d) negative forming voltages

Effect of Non-lattice Oxygen Concentration on Non-linear Resistive Switching Characteristic of HfO_2 films

Jonggi Kim, Yongjae Kim, Kyumin Lee and Hyunchul Sohn
Department of Materials Science & Engineering, Yonsei University, Seoul 120-749, Korea
E-mail: hyunchul.sohn@yonsei.ac.kr

The effect of electrode and deposition methods on non-linear interfacial resistive switching of HfO_2 was studied. The operating current in HfO_2 based device was increased with negatively increasing the heat of formation energy in top electrode [1].lso, it was investigated that the operating current in HfO_2 based device was changed with deposition methods of O_3 reactant ALD, H_2O reactant ALD and dc reactive sputtering, resulting the magnitude of the operating current and on/off ratio in order of HfO_2 films deposited by dc reactive sputtering, H_2O reactant ALD, and O_3 reactant ALD. Non-lattice oxygen concentration, which is closely related to oxygen vacancies [2], was increased in order of Pt, TiN, and Ti top electrodes and in order of O_3 reactant ALD, H_2O reactant ALD, and O_3 reactant ALD, and dc reactive sputtering deposition method. From all results, non-lattice oxygen concentration in ultra-thin HfO_2 films play a crucial role in the operating current and memory states (LRS & HRS) in the non-linear interfacial resistive switching.

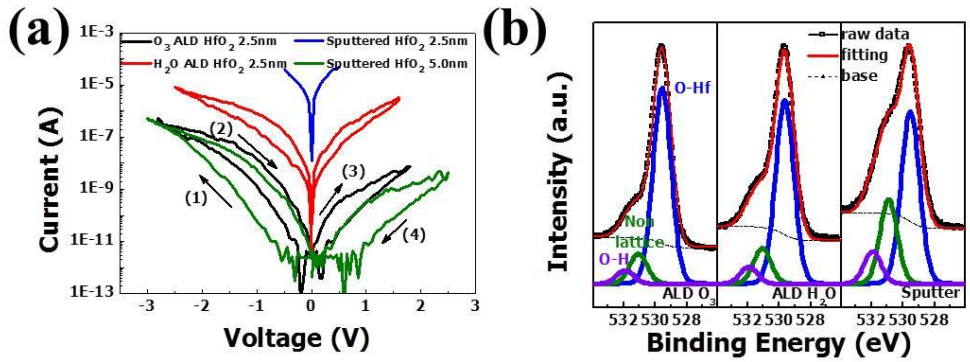

Fig 1. (a) Non-linear switching and (b) non-lattice oxygen concentration of HfO_2 with deposition methods

[1] I. Barin, F. Sauert. E. Schultze-Rhonhof, and W. S. Sheng, Thermochemical Data of Pure Substances II, Wiley-VCH Verlagsgesellschaft, Weinheim, Germany, 1989.
[2] John C. C. Fan and John B. Goodenough, J. Appl. Phys. **48**, 3524 (1977).

Non-linear Resistive Switching Characteristic based on ZnSe Selector for Eliminating Sneak Current in Cross-bar ReRAM Device

Youngjae Kim, Jonggi Kim, Yoonki Min, and Hyunchul Sohn
Department of Materials Science & Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : hyunchul.sohn@yonsei.ac.kr

The non-linear characteristics of ON states are important for the application to the high density cross-point memory industry because the sneak current in neighbor cells occurred during reading, erasing, and writing process[1]. K_w of above 40 in ON states, which is the writing current @ V_{write}/the current @ $1/2V_{write}$, was required in cross-point ReRAM memory industry. The high current density non-linear IV curve of ZnSe selection device was shown and the ALD HfO_2 switching device has the linear properties of ON states and the compliance current of 100uA. To evaluate the performance of the selection device, we connected it to HfO_2 switching device in series. All of the bias was applied with respect to the top electrode of the selection device, whereas the bottom electrode of the RRAM was grounded. In the cross-point application, $1/2V_{write}$ and $-1/2V_{write}$ were applied to the word-line and bit-line, respectively, which were connected to the selected cell, and a zero bias was applied to the unselected word-lines and bit-lines. The current @ $1/2V_{write}$ of the unselected cells was blocked by the selection device, thus eliminating the sneak path and obtaining a writing voltage margin. Using this method, the writing voltage margin was analyzed on the basis of the memory size and K_w of 49 in ON states in ZnSe selector – HfO_2 resistor device was shown. Also, the great reliability such as retention and endurance was shown. From all results, the key factors on non-linearity of ON states in non-linear resistive switching of 1S1R device were also invevestigaed in comparison with simulation and real data.

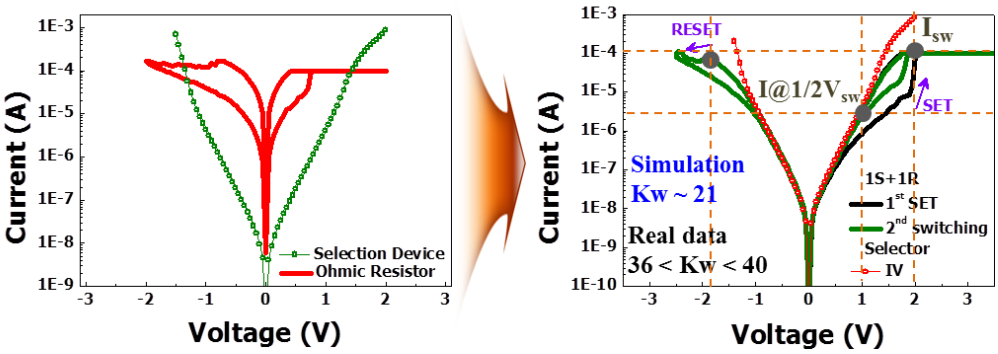

Fig 1. Simulation and real I-V data of Selection device + linear resistive switching device

[1] Seong-Geon Park, et al., Electron Devices Meeting (IEDM), 2012 IEEE International

Influence of trap states on transport and photoresponse of resistive switching Pt/Nb:STO Schottky junctions

Yoonjung Kim*, Haeri Kim, and Dong-Wook Kim†
Department of Physics, Ewha Womans University, Seoul 120-750, Republic of Korea
E-mail: dwkim@ewha.ac.kr

Pt/Nb-doped $SrTiO_3$ (Nb:STO) single-crystal Schottky junctions exhibit bipolar resistive switching (RS) behaviors. The switching mechanism is under debate, in spite of the simple device structure. Alteration of Schottky barrier height (SBH) has been suggested as a major origin by many researchers. Instead, trap-mediated tunneling conduction has been proposed as an alternative mechanism. Transport of the junction showed distinct behavior under dark and illuminated conditions. Such results might be signatures of the interfacial trap states, which capture and release the carriers to the trap states. The trapping and detrapping processes could induce reversible change in the interface potential profile, resulting in the bistable resistance states. This study will provide us with clues to understand how the trap states contribute to the RS mechanism of the metal/oxide Schottky junctions.

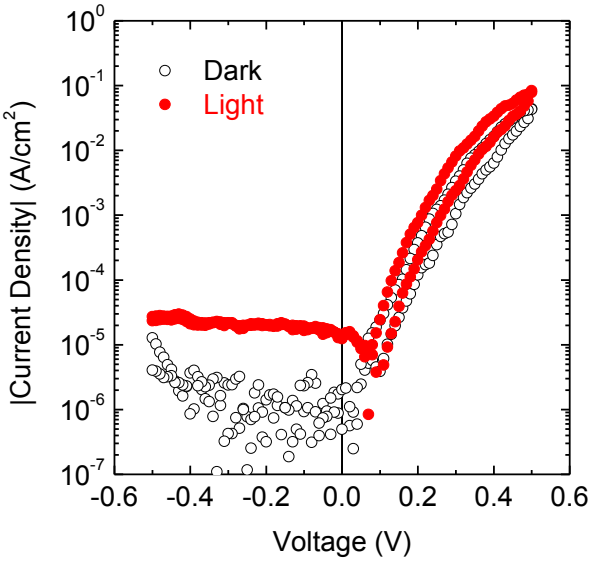

Fig 1. RS characteristics in dark and light

Non-lattice oxygen ion driven negative differential resistance behavior for the future ReRAM applications

Yoon Cheol Bae [a], Ah Rahm Lee [a], Gwang Ho Baek [a], Je Bock Chung [a], Won Bae Koo [b] and Jin Pyo Hong [a, b*]

[a]*Division of Nano-Scale Semiconductor Engineering, Hanyang University, Seoul, 133-791, Republic of Korea*

[b]*Research Institute for Natural Science, Novel Functional Materials and Devices Laboratory, Department of Physics, Hanyang University, Seoul 133-791, Republic of Korea*

E-mail : jphong@hanyang.ac.kr

Resistive switching behaviors observed in various oxide materials have attracted considerable attention because of the simple metal/oxide/metal sandwich structures of these materials and their potential applications in next-generation nonvolatile memory devices (NVMs) [1-2]. This study examined the oxygen ion drift-based resistive switching features of TiO_x/ TiO_y bi-layer homo-junctions. The TiO_x/TiO_y bi-layer structure has a difference oxygen chemical composition in each layer. X-ray photoelectron spectroscopy (XPS) measurements were carried out before and after electro-forming to determine the role of non-lattice oxygen content. Variation of the oxygen ion content in the TiO_2 layers resulted in changes in the on/off ratio and increased the non-lattice oxygen content. A possible switching mechanism based on oxygen ion content is discussed.

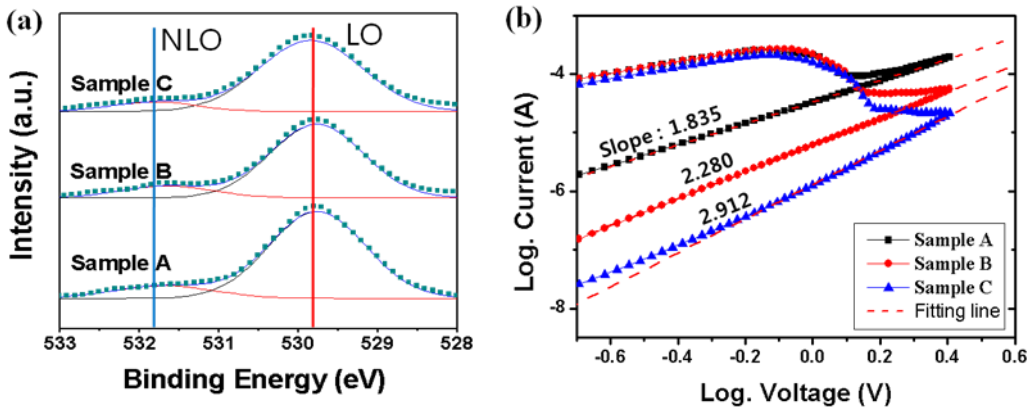

Fig 1. (a) Oxygen 1s XPS spectrum of initial samples A, B and C, and (b) I-V curve of reset process in bipolar resistive switching behavior.

[1] R. Waser, Aono, Nat. Mater. 6 (2007) 833.

[2] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, Nat. Nanotechnology 3 (2008) 429.

TiO_xN_y electrode interface-driven dual-resistive switching behaviors of Pt/ Ta_2O_{5-x}/TiO_xN_y cell for the future ReRAM applications

Ah Rahm Lee[1], Yoon Cheol Bae[1], Gwang Ho Baek[1], Je Bock Chung[1], and Jin Pyo Hong[1,2]

[1]*Division of Nano-Scale Semiconductor Engineering, Hanyang University, Seoul, 133-791, Republic of Korea*

[2]*The Research Institute for Natural Science, Novel Functional Materials and Devices Lab, Department of Physics, Hanyang University, Seoul 133-791, Republic of Korea*

E-mail : jphong@hanyang.ac.kr

Recently, several group reported the resistive switching (RS) cells exhibiting the coexistence of filamentary and interfacial RS in single memory cell [1]. However, the underlying nature of resistive switching and the conductive transport in the ReRAM is still arguable and unclear [2]. Therefore, further studies are necessary for finding the key parameters required for the realization of a ReRAM device. This work reports the dual-resistive switching features in simple $Pt/Ta_2O_{5-x}/TiO_xN_y$ cells that display typical bipolar switching behaviors. The initial resistive switching direction was clockwise due to a reaction of the TiO_xN_y electrode with migrated oxygen ions under bias. In addition, the typical current sweeping indicated the appearance of negative differential resistance (NDR) region just before the reach of typical set step, corresponding to the occurrence of the other sneak resistive switching hysteresis. The difference between two switching modes is discussed.

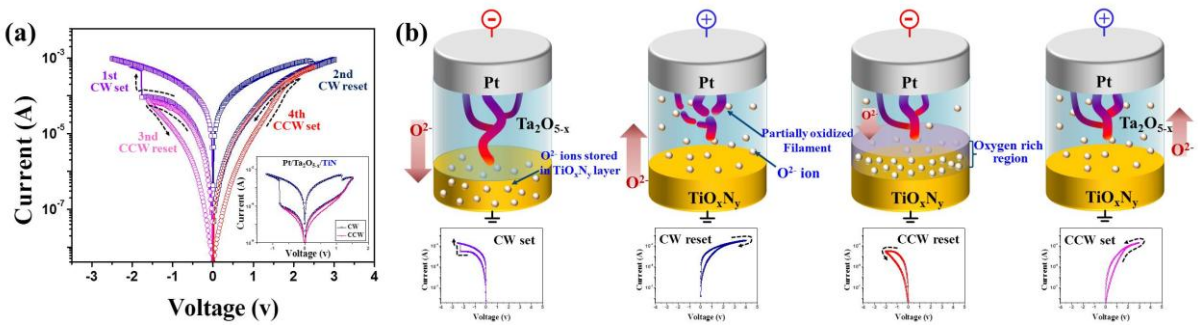

Fig 1. (a) Dual-resistive switching curves with a first CW set (purple line), second CW reset (blue line), third CCW reset (pink line), and fourth CCW set (red line). (b) Possible pictures of dual-resistive.

[1] R. Muenstermann, T. Menke, R. Dittmann, G. Staikov, and R. Waser, Adv. Matter. 22, 4819 (2010).

[2] R.Waser, R. Dittmann, G. Staikov, and K. Szot, Adv. Matter. 21, 2632 (2009).

Area-efficient, Power-efficient Program Voltage Generator for 3D Solid State Drive with NAND Flash Memories

Youngil Kim[1], Sungwook Choi[2], and Sangsun Lee[1,*]

[1]*Depart. Nanoscale Semiconductor Engineering, Hanyang University*

[2]*Flash Design Team, Flash Development Division, SK Hynix Semiconductor Inc.*

E-mail :[1]rlayi84@hanyang.ac.kr, [2]sungwook.choi@skhynix.com, [1,*]ssnlee@hanyang.ac.kr

There is growing demand for high performance, highly reliable and low power solid-state drives (SSDs). The typical SSD consists of several NAND flash memories, DRAMs and a NAND controller. Since the reduction of planar NAND feature cell size is somewhat limited, so the use of through-silicon-vias (TSVs) and three-dimensional (3D) NAND technology has become a key topics. In this respect, the design of the area-efficient peripheral circuit is becoming more important. Recently, many researchers have proposed various strategies to improve the area-efficient and power-efficient peripheral circuit of the high voltage generator for the 3D-SSD. Two main approaches have been proposed: modifying the charge pump to improve the area-efficiency and power-efficiency [1], and using the boost converter for area-efficiency and power-efficiency, and fast rising time performance [2].

In this work, a single inductor multi output (SIMO) boost converter or power supply supplies the external power of 12V and 5V to all NAND chips, in order to reduce the charge pump stage of each NAND chip. As a result, the power consumption and area overhead of the charge pumps are greatly reduced. Also, we propose the new scheme of the high voltage switch for using an external high voltage of 12 V without a breakdown issue. Additionally, we propose a new scheme of the high voltage linear regulator using an external high voltage of 5 V, and we propose a fast transient response active mode VDC using an NMOS pass element and external high voltage of 5 V.

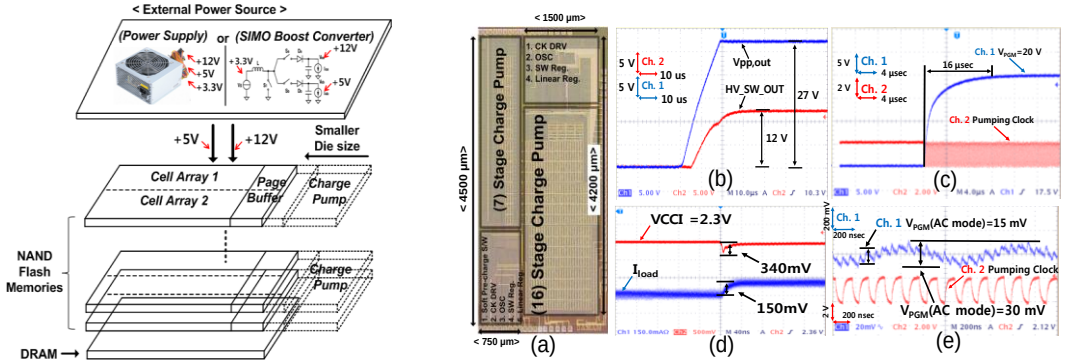

Fig 1. The proposed Program Voltage Generator using external power.

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[2] K. Ishida, Ken Takeuchi, ISSCC 2009, Feb. 10 (2009).

Selective etching of MTJ materials using CO/NH3 gas mixture in pulse-biased inductively coupled plasmas

Minhwan Jeon, and Geunyoung Yeom
SKKU Advanced Institute of Nano Technology (SAINT), Sungkyunkwan University, Suwon, Gyeonggi 440-746, Republic of Korea
E-mail : gyyeom@skku.edu

Recently, magnetic random access memory (MRAM) has made prominent progress in memory performance and has brought a bright future for the next-generation nonvolatile memory owing to its faster access time, higher storage density, lower operating voltage, and infinite rewrite time as compared with conventional RAM devices [1-2]. In particular, spin transfer torque (STT)-MRAM has been investigated extensively owing to the possibility in an attempt to overcome the scaling limit of MRAM devices. For the mass storage in addition to high-capacity nonvolatile MRAM devices, the dry etch process of this multilayer MTJ material is one of the most important processes owing to the difficulty in the formation of volatile compounds between ferromagnetic materials and etch gases, and therefore, the difficulty in the etching of MTJ materials.

In this study, an RF pulse-biasing technique has been applied in the etching of MTJ materials, such as CoFeB and MgO, and W has been used as one of the hard mask materials and its effect on the etch characteristics was investigated in an ICP system using a CO/NH3 gas mixture.

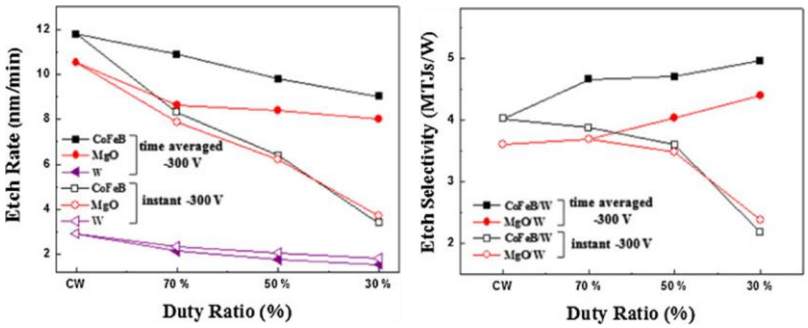

Fig 1. Etch characteristics of MTJ-related materials and W as a function of pulse duty percentage at a fixed DC bias voltage of -300 V.

[1] Y. Otani, H. Kubota, A. Fukushima, H. Maehara, T. Osada, S. Yuasa, and K. Ando: IEEE Trans. Magn. 43 (2007) 2776
[2] G. Muller, T. Happ, M. Kund, G. Y. Lee, N. Nagel, and R. Sezi: IEDM Tech. Dig., 2004, p. 567.

The study of scalable three-dimensional NAND flash structure using edge fringing field

Hyungjun Yang, Gaehun Lee, and Yunheub Song
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : yhsong2008@hanyang.ac.kr

Recently, various 3D NAND flash structure have been proposed to keep bit density and reduce bit cost[1,2]. We propose the scalable three-dimensional (3-D) NAND flash structure with fully surrounding charge storage using edge fringing field which is evaluated by TCAD simulation to study program characteristics. We confirmed that our structure has the program threshold voltage about 5 V during the program voltage of 18 V at 1ms when the oxide thickness is 10 nm between nitride and control gate, which is competitive with program characteristics of conventional 3D NAND structures[1,2]. Also, the structure is expected to have smaller effective cell size compared to conventional 3D NAND structures since structure with horizontal ONO layer reduces the size of contact hole. As a result, the proposed structure is one of the candidates of Terabit 3-D vertical NAND flash structure with lower bit cost and design scalability.

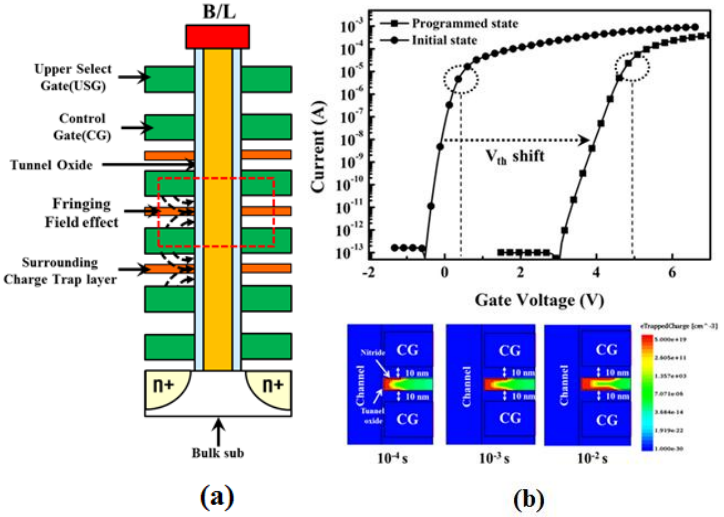

Fig 1. The (a) cross section schematic and (b) Id-Vg program characteristic and the status of stored electron depending on programming time

[1] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, and A. Nitayama, Symp. VLSI Tech. Dig., 2007, p. 14.
[2] J. Jang, H. S. Kim, W. Cho, H. Cho, J. Kim, S. I. Shim, Y. Jang, J. H. Jeong, B. K. Son, D. W. Kim, K. Kim, J. J. Shim, J. S. Lim, K.-H. Kim et al, Symp. VLSI Tech. Dig., 2009, p. 136.

Current-induced synchronized switching of magnetization

Soo-Man Seo[1], Jung-Hwan Moon[1], Seung-Jae Lee[1], and Kyung-Jin Lee[1,2]
[1]*Department of materials science and engineering, Korea University, Seoul, Korea*
[2]*KU-KIST Graduate school of converging science and technology, Korea University, Seoul, Korea*

E-mail : kj_lee@korea.ac.kr

Spin-polarized current can exert torque on magnetization via spin-transfer torque (STT) [1,2]. If spin-polarized current is sufficiently large, current-induced magnetization switching can be realized. From the application point of view, decrease of switching current without loss of thermal stability is one of the important issues. However, in perpendicular magnetic tunnel junction (p-MTJ), both switching current and thermal stability are directly coupled to magnetic anisotropy energy, thus it is impossible to pull apart the switching current and thermal stability. Recently, it is theoretically predicted that CiSS (Current-induced Synchronized Switching) structure allows low switching current and high thermal stability compared to conventional p-MTJ [3]. In this work, we assumed another top pinned layer (Fig. 1(a)) and investigated switching current (Fig. 1(b)) with varying saturation magnetization (M_s) of top pinned layer. Further details such as distribution of switching current and thermal stability factor will be discussed in presentation.

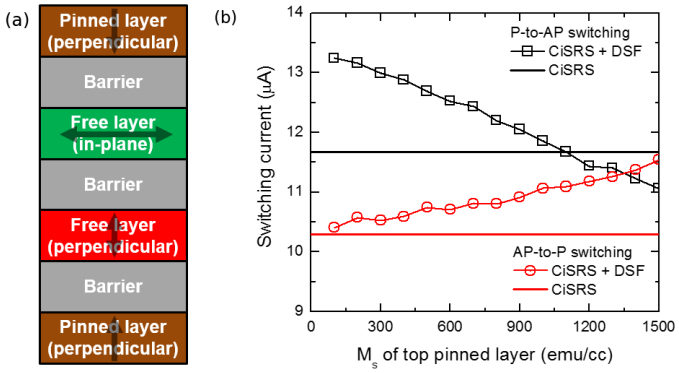

Figure. 1 (a) Schematic structure of CiSS with top pinned layer. (b) Effect of M_s on switching current.

[1] L. Berger, J. Appl. Phys. **55**, 1954 (1984); **71**, 2721 (1992).
[2] J. C. Slonczewski, J. Magn. Mag. Mater. 159,
[3] S.-M. Seo and K.-J. Lee, Appl. Phys. Lett. **101**, 062408 (2012).

Ge 기판의 S 처리를 이용한 charge –trapping type 소자의 메모리 특성 연구

Myungwan Lee, Yong Chan Jung, Sejong Seong, In-Sung Park and Jinho Ahn*
Department of Materials Science and Engineering, Hanyang University, Seoul, Korea
E-mail : jhahn@hanyang.ac.kr

최근, NAND flash 의 device 가 scaling down 되면서 기존의 floating gate type memory(FGT)는 인접 cell 간의 간섭 정도가 증가하여 동작전압 제어가 어려워지고 coupling ratio 가 감소하는 등의 문제점이 있다. Charge-trapping type memory(Metal gate/Blocking oxide/Charge trap layer/Tunnel oxide/Si)는 FGT 의 문제점을 해결한 방식이며 charge trap lyer 에 전자를 저장하므로 FGT 에 비해 전하 저장의 안정성 측면에서 장점을 지닌다. Charge trap layer 로 Si_3N_4 을 대체하여 최근에는 HfO_2 등의 high-k 물질을 적용하여 큰 전도대 오프셋과 높은 trap 밀도를 얻을 수 있어 더 큰 trap charge 를 기대할 수 있다. 기존 Si 기판 대신 Ge 기판을 사용하면 전자와 홀의 mobility 가 높아 동작속도를 개선할 수 있다. 그러나 Ge 기판 표면의 native oxide 는 다수의 dangling bond 를 발생시켜 결함이 적은 계면을 만드는 passivation 기술이 필요하다. Passivation 방법에는 NH_3 처리, nitride layer, Si layer, sulfur 처리(S-passivation)등이 있다. 그 중 sulfur 용액인 $(NH_4)_2S$ 를 이용한 S-passivation 기술은 native GeO 를 GeOS 로 변화시켜서 결함을 제거한다. 본 연구에서는 S-passivation 기술을 이용하여 결함이 줄어든 GeOS 박막을 형성하여 tunnel layer 로 사용하고자 하는데 목적이 있으며 $(NH_4)_2S$ 처리시의 용액 속에 포함된 $(NH_4)_2S$ 의 농도를 변화시키면서 메모리 특성을 살펴보았다.

그림 1(a)는 본 연구에서 제안한 charge trapping type 메모리소자의 구조를 나타낸 것이다. 그림 1(b)는 $(NH_4)_2S$ 농도에 따른 C-V 곡선을 나타낸 것이다. $(NH_4)_2S$ 농도에 따라서 C-V 곡선의 kink, stretch out 특성이 바뀌며, 메모리 window 도 바뀐다. $(NH_4)_2S$ 10% 이상에서는 약 2.5V 메모리 window 를 가지는데 이는 0%에 비해서 약 0.5V 정도 window 가 늘어난 값이다. 계면 특성은 15% 농도 이상에서 크게 개선되었다. 즉, $(NH_4)_2S$ 처리로 생긴 GeOS 막이 passivation 기능을 수행하면서 동시에 메모리 window 를 넓혀주는 tunnel layer 로도 기능하고 있다.

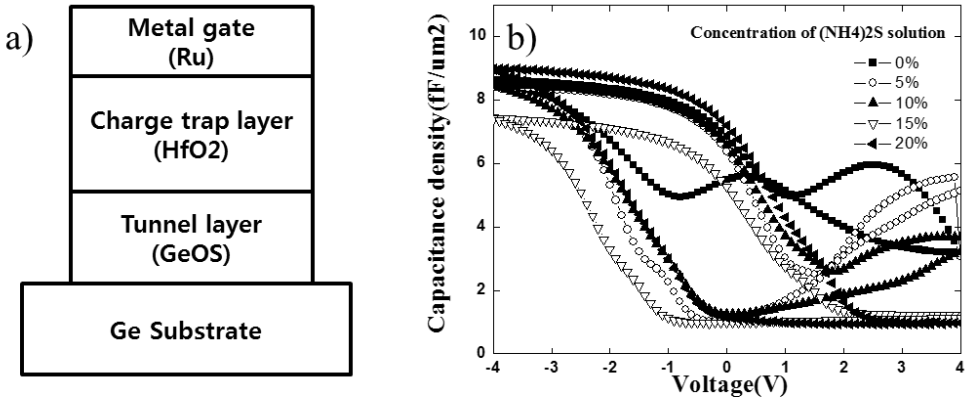

Fig 1. a) Schematic of charge-trapping type device and b) its C-V curves with $(NH_4)_2S$ treatment

Improved reliability of RRAM by optimizing pulse shape to minimize current overshoot

Jeonghwan Song, Daeseok Lee, Jiyong Woo, and Hyunsang Hwang
Department of Materials Science and Engineering, Pohang University of Science and Technology, 77 Cheongam-ro, Nam-gu, Pohang, Gyeongbuk, Republic of Korea
E-mail : hwanghs@postech.ac.kr

Recently, resistive random access memory (RRAM) has been intensively studied as a promising candidate for next-generation non-volatile memory [1]. In this study, we proposed the optimized pulse shape to minimize current overshoot in a typical RRAM device with W/Zr/HfO_2/TiN structure. The transient response during SET and RESET processes directly show the current overshoot [Fig. 1(a)]. The current overshoot in SET process has severe effects on variability of low resistance state (LRS) [2]. The current overshoot in RESET process can change the state of RRAM cell from high resistace state (HRS) to LRS when repeatedly applied. It means that the current overshoot in RESET process can cause HRS failure. Therefore, suppressing the current overshoot in SET and RESET processes as low as possible will improve the variability and endurance of RRAM device in its operation. The current overshoot can be minimized by increasing rising or falling time (dt), according to $I_C=C\times dV_C/dt$. Thus, the rising time of SET pulse and the falling time of RESET pulse are increased by 900ns compared with 100ns in that of conventional rectangular pulse [Fig. 1(b)]. By the proposed SET and RESET pulse shapes, the variability of LRS was significantly improved [Fig. 1(c)] and the endurance was also improved more than 10^3 times compared to those of conventional rectangular pulse [Fig. 1(d)].

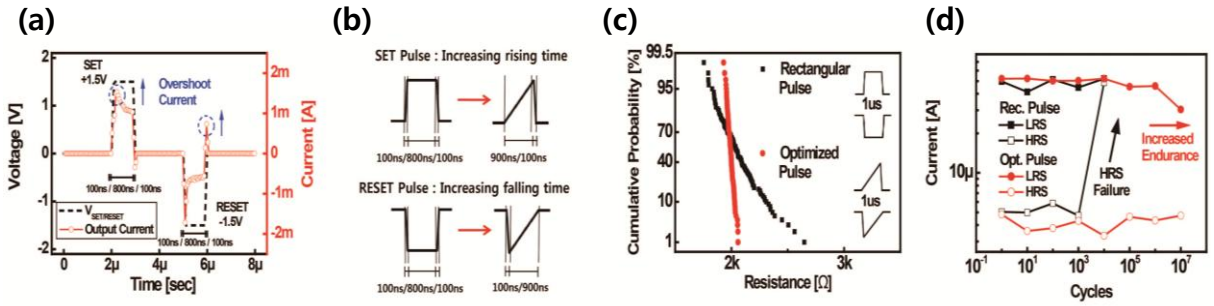

Fig 1 (a) Transient response, (b) Proposed pulse shape and Comparisons of (c) cumulative probabilities of LRS resistance and (d) endurance with rectangular pulse and optimized pulse

Acknowledgement This work was supported by the R&D program of MOTIE/KEIT. [10039191]

References [1] R. Waser et al., Adv. Mater. 21, 2632 (2009). [2] X. Guan et al., IEEE Trans. Elec. Dev. 59, 1172 (2012).

Real-time PRBS chaser

Seok-Min Ye, Deog Kyoon Jeong
Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-747, Korea
E-mail : mppiero5@snu.ac.kr

Recently, as complexity of system grows up, calibration and recalibration states are used to acheive low power architecture. Realtime update of timing adjustment and equalizer coefficient uses much power. So usually in these state, not only timing recovery but also equalizing should be done. Just for the timing recovery, simple data pattern can be used, but for the equalizing, variety data pattern should be promised. In this situation, PRBS pattern data is used often for ease sync between transmitter and receiver. In other words, because PRBS pattern uses FSM, receiver can reset the state machine in digital domain and receiver can recognize what is right and wrong. This FSM can be synthesized easily in digital domain and can be organized as full rate architecture because FSM uses only one synchronized clock. But in sub-rate, typical FSM cannot be implemented. For example in the PRBS7,. XOR of the 6th and 7th FF output becomes to input of the 1st FF such as Fig.1 When implemented in half-rate, simple diagram such as Fig.2 can be used and in quater-rate, Fig.3 can be used. Furthurmore, Fig.4 is final implemented result. In this way, variety kinds of PRBS chaser can be implemented in sub-rate.

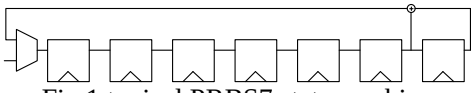

Fig.1 typical PRBS7 state machine

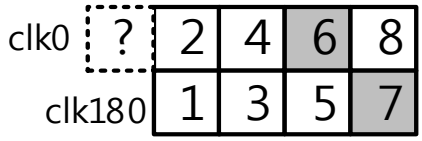

Fig.2 half-rate diagram example

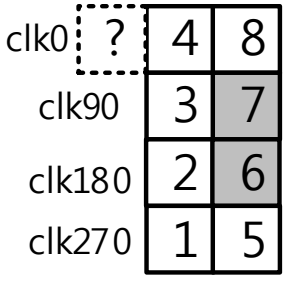

Fig3. quarter-rate diagram example

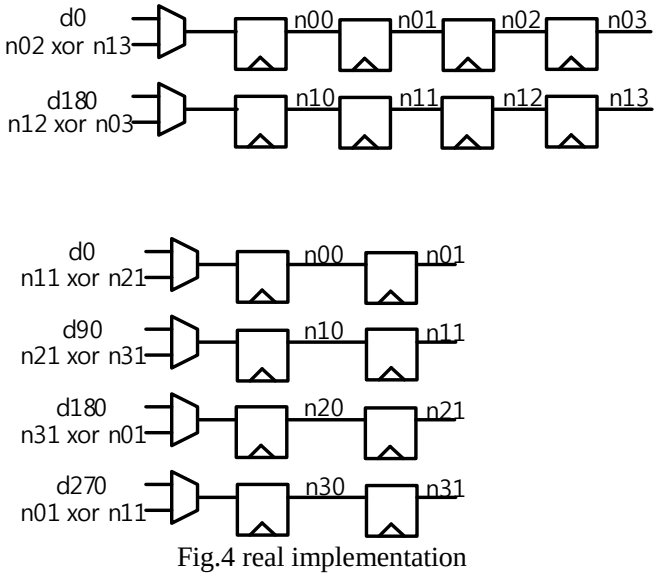

Fig.4 real implementation

High-Accuracy differential Voltage Amplifier Operating At Wide DC Input Voltage

Tae-Ho Kim, Jae-Mun Oh, Jong-Hyun Yoon, Jin -Won Mok, Jong-Ho Park, Jae-Hyun Shim, Seong-Yong Kim and Byung-Do Yang
Graduated School of Semiconductor Engineering, Chungbuk University, Cheongju, 361-763, Korea
E-mail : bdyang@cbnu.ac.kr

This paper proposed a high-accuracy differential voltage amplifier operating at wide DC input voltage. Most transistors are low voltage transistors for high performance and small area. These transistors are destroyed by the applied high voltage. The proposed differential voltage amplifier protects the low voltage transistors by inserting high voltage transistors in the high-voltage applied nodes. Also, it achives high-accuracy at DC 6 ~ 60V input voltage. The proposed circuit was implemented in a 0.35 ㎛ BCDMOS process.

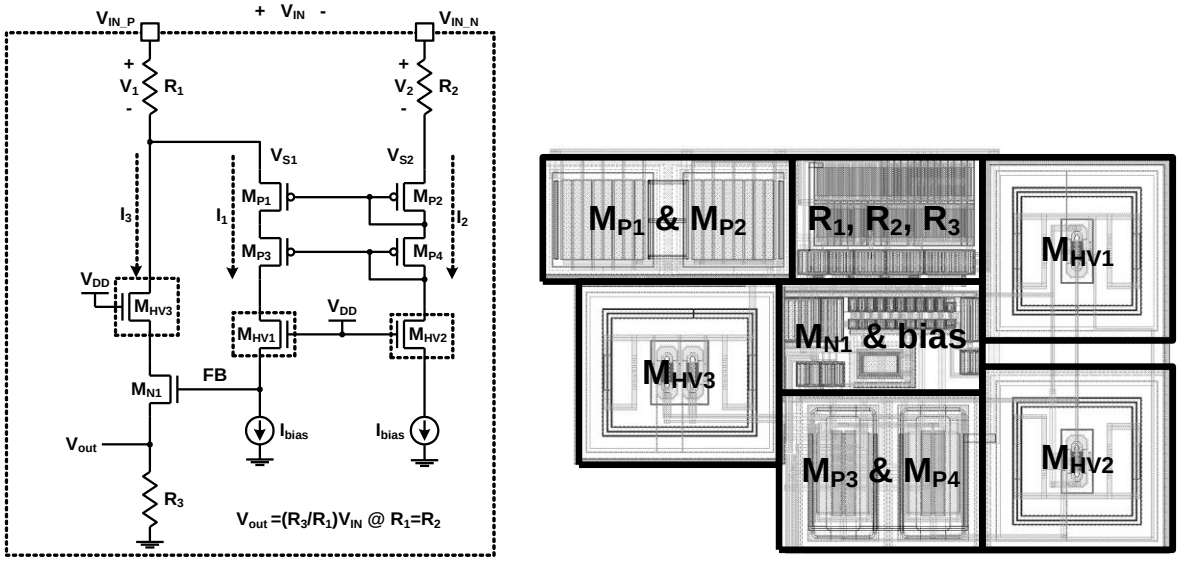

Fig 1. Proposed circuit and its layout

[1] Jianbin Lin, Huihui Cheng, Jianli Xing, ASID. 177-179 (2011)

Circuit for Preventing Negative Oscillation of Power-Switch with Wide DC Input voltage

Seong-Yong Kim, Jae-Mun Oh, Jong-Hyun Yoon, Jin -Won Mok, Jong-Ho Park, Jae-Hyun Shim, Tae-ho Kim and Byung-Do Yang
Graduated School of Semiconductor Engineering, Chungbuk University, Cheongju, 361-763, Korea
E-mail : bdyang@cbnu.ac.kr

This paper proposed a circuit for preventing negative oscillation of power switch with wide DC input voltage. In a integrated chip, negative oscillations cause serious damages on chip circuit. The negative oscillation commonly occur when driver circuits are driving power-switches. Easy way to prevent negative oscillations is driving a power switches slowly. However, slow power-switch driving causes slow chip's operation and low the power efficiency. The proposed technique optimizes the driving speed according to the wide range of supply voltage(6 ~ 60V). Thus, fast power-switching is possible without the negative oscillation. The proposed circuit was implemented in a 0.35 ㎛ BCDMOS process.

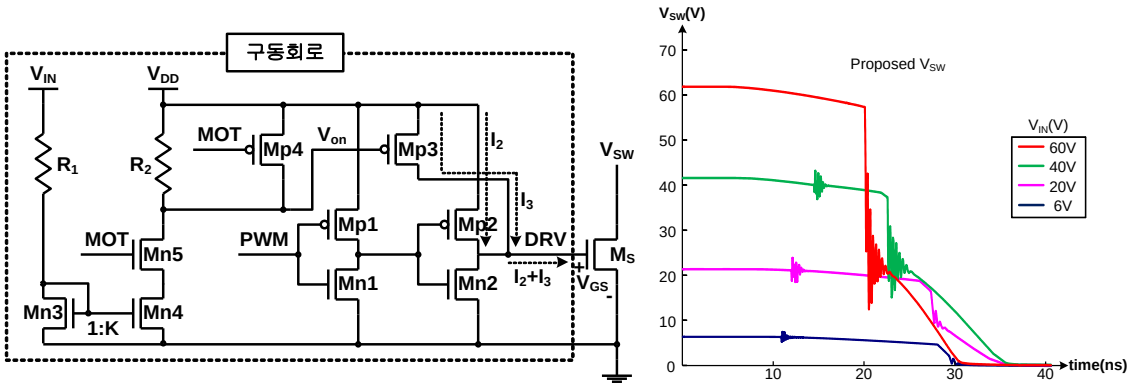

Fig 1. Proposed circuit and its simulation waveform

[1] Zhiliang Zhang, Eberle, W., Zhihua Yang, Yan-Fei Liu, Sen, P.C., TPEL, 653-666 (2008)

Dual-Mode CMOS Image Sensors for Depth Acquisition and Motion Detection

Kwang-Hyun Lee[1], Yibing M. Wang[2], Hongyu Wang[2], Seunghoon Lee[1], Dong-Ki Min[1], Seokyong Hong[1], Sung-Jae Byun[1], Hyunil Byun[1], Jungbin Yun[1], Deokha Shin[1], Yohwan Noh[1], Wanghyun Kim[1], Ilia Ovsiannikov[2], and Taechan Kim[1]

[1]*Image Development Team, System LSI, SEC, Yongin-si, Gyeonggi-do, Korea*

[2]*Samsung Semiconductor, Inc. 2 N Lake Ave, Suite 230, Pasadena, CA 91101, USA*

E-mail : khyun7.lee@samsung.com

Gesture recognition is becoming more and more popular for user interface in computer and mobile devices. With one single image sensor, gesture can be recognized by motion detection using 2D image sensors, but the conventional 2D approach requires a frame memory for consecutive frames to be compared, and large data bandwidth for decision making. It also increases system latency and power consumption. In this paper, we propose and fabricate a dual-mode CMOS image sensor, which can perform dual functions including depth acquisition and motion detection, in a 90nm backside-illuminated (BSI) CIS process. The sensor has a 720 x 528 pixel array with the pixel pitch of 7um. It works as a typical time-of-flight (TOF) sensor having two taps with column-parallel 10-bit ADCs for 3D imaging, but it just compares two-tap pixel outputs with only 1-bit ADC for the motion detection to reduce power consumption. With this new sensor, we achieve power consumption of 8.5mW at 30 fps in motion detection mode. Such sensors may be used as proximity sensors in mobile devices. In addition, the design can be further extended to RGBZ sensor which mixed color and TOF pixels in a single array.

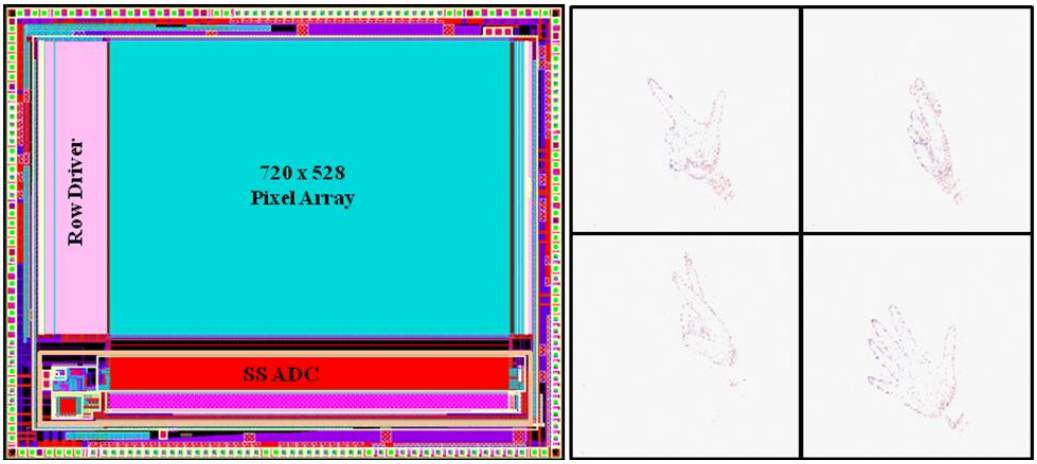

Fig 1. Chip layout and hand-gestured images captured from a video clip.

A Replica-driving Technique for High Performance SC Circuits

[1]Chang-kyo Lee, [2]Wan Kim, [2]Hyun-wook Kang, [1]Jung-hwan Choi, [2]Seung-Tak Ryu

[1]Memory Division, Samsung Electronics, Suwon, Korea

[2] Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon, Korea

E-mail : ck1980.lee@samsung.com

This paper proposes a replica driving technique to implement low-power high-performance switched-capacitor (SC) amplifiers which are used in a filter, S/H and MDAC. The reduced swing range problem arising from the source-follower (SF) output stage [1, 2] is resolved by a simple switched-capacitor (SC) level shifter, without additional supply or static buffer and the output driving capability is ensured by using a class-AB output stage as shown in Fig 1. A prototype 12bit 150MS/s pipelined ADC including the reference driver was designed for concept proof in a 65nm CMOS process. The ADC consumes 92.4mW including the reference drivers at a 1.2V supply. The measured INL and DNL are 0.5 LSB and 1.5 LSB, respectively. The SNDR and SFDR are 58.2dB and 73.6dB at 150MS/s with an 8.3MHz input.

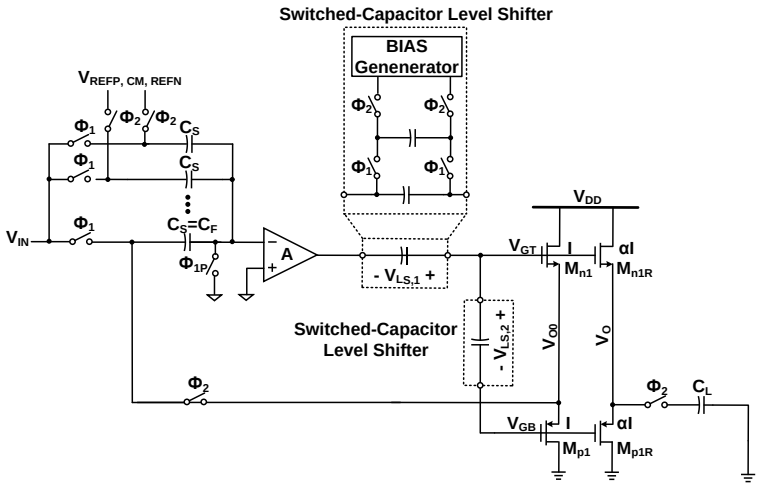

Fig 1. Switched Capacitor (SC) Residue Amplifier with Replica Driving Technique

[1] Wei-Hsuan Tu, Tzung-Hung Kang, "A 1.2V 30mW 8b 800MS/s Time-interleaved ADC in 65nm CMOS," in IEEE Symp. On VLSI Circ. Dig. Tech. Papers, Jun. 2008, pp72-73.

[2] H. Yu, S.W.Chin, B.C.Wong, "A 12b 50MSPS 34mW Pipelined ADC," in Proc. IEEE CICC, Sept. 2008, pp297-300.

A High Gain and Small Size Comparator Array for Laser Radar Receiver

[1,2]Jongsun An, [1]Joo-Young Choi, [2]Bongki Mheen, and [1]Choul-Young Kim
[1]*Department of electronics engineering, Chung Nam national University, Daejeon 305-764, Korea*
[2]*Electronics and Telecommunication Research Institute(ETRI),*
218 Gajeong-ro, Yuseong-gu, Daejeon, 305-700, KOREA
E-mail : jsan@cnu.ac.kr

A 2 × 4 comparator array composed of transimpedance amplifer(TIA) as a preamplifier and comparator with Hysteresis. The 2 × 4 Comparator array is designed and simulated in a 0.18um CMOS process, and provieds 79dBΩ trans-impedance gain, 148MHz -3dB bandwidth for a 0.5pf photodiode capacitance and 8.8mW power consumption for 1.8V supply voltage.The comparator has been integrated in a core size of only 30 × 35um^2 . The comparator detect 2uA input current from APD(avalanche photo diode).

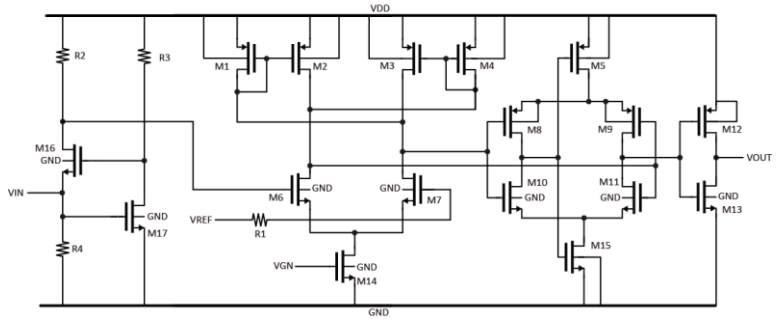

Fig 1. Comprator schematic

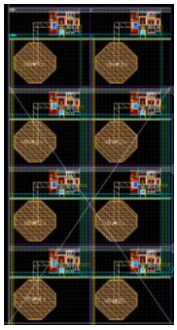

Fig 2. 2 × 4 Arrray Comprator Layout

[1] S.M. Park, “CMOS Transimpedance Amp-lifiers for Gigabit Ethernet Applications”, Journal Title, ICCT(Publisher Name), vol. 43, no. 4, pp.16-22, 2006.
[2] 민봉기, “대면적 검출기 기반의 시각안전 레이저 레이다 시스템 기술,” 제 6 회 군수용 초고주파부품 워크샵, 2013,10, p.147.

A 16-channel CMOS transimpedance amplifier array for PSL systems

Xiao Ying, Hanbyul Choi, Seung-Hoon Kim, and Sung Min Park
Department of Electronics Engineering, Ewha Womans University, Seoul 120-750, Korea
E-mail : xy880328@hotmail.com, smpark@ewha.ac.kr

Recently, the laser detection and ranging (LADAR) systems have become very attractive for the applications of three-dimensional image processing such as for the usage of unmanned vehicles. This paper presents a linear read-out integrated circuit (ROIC) with an 16 x 1 multi-channel transimpedance amplifier(TIA) array for panoramic scan LADAR(PSL) systems which measure the time difference between the light source and the reflected signals, and hence accomplishing the distance measurements [1]. The signals coming into the TIA array vary from $2\mu A_{pp}$ to $20\mu A_{pp}$ in amplitude, depending upon the reflectance of a target. Therefore, the sensitivity of each TIA in the array should be very high and also the linearity should be guaranteed to avoid the overlapping of signals especially when a minimum detectable signal ($2\mu A_{pp}$) is followed by a large $20\mu A_{pp}$ signals in a consecutive sequence with only one unit-interval (UI) apart.

The post-layout simulations of the 16-channel TIA array in 0.18μm CMOS demonstrate the transimpedance gain of 76.7dBΩ, the bandwidth of 1.06GHz with 0.56dB peaking around the -3dB frequency, the noise spectral density of 6.41pA/sqrt(Hz) corresponding to -28dBm sensitivity for 10^{-12} BER and 0.6A/W responsivity, the signal-to-crosstalk ratio of 43dB, and the power dissipation of 17.3mW from a single 1.8-V supply

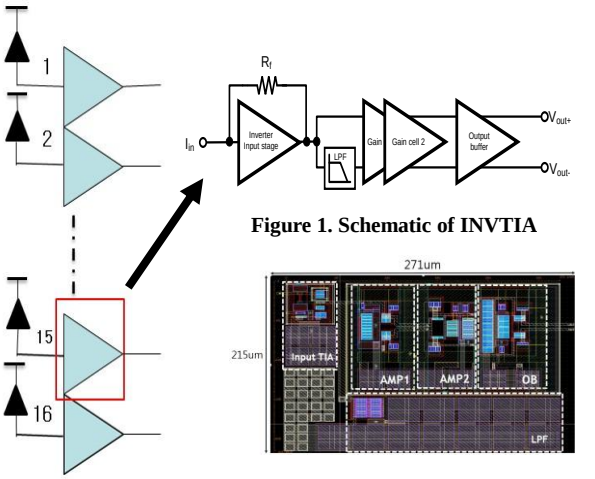

Figure 1. Schematic of INVTIA

Figure 2. Layout of INVTIA

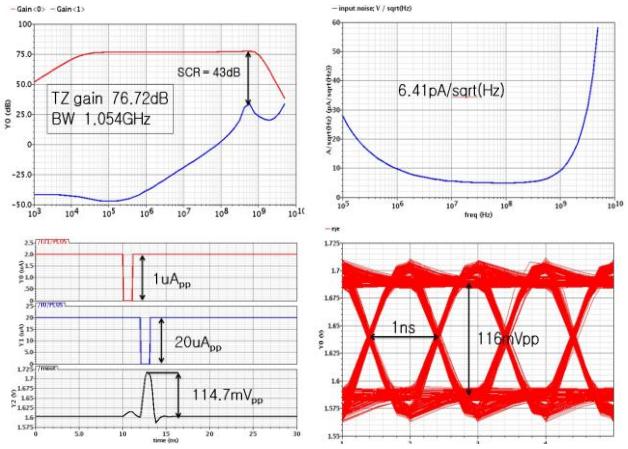

Figure 3. Post-layout simulation results

[1] S. G. Kim et al., "A 1.8Gb/s/ch 10mW/ch -23dBCrosstalk Eight-Channel Transimpedance Amplifier Array for LADAR Systems", IEEE ISOCC, in press (2011).

LED구동 회로용 온도 히스테리시스를 갖고 있는 고온 탐지기 회로

김영기, 황재연
안양대학교 정보통신공학과 대학원
E-mail : kimyg@anyang.ac.kr, wodusking@anyang.ac.kr

많은 에너지의 작용과 반작용, 순환은 온도에 영향을 끼친다. 온도는 모든 것들의 원자와 분자의 단계까지 영향을 준다. 특히 고온은 반도체와 전자회로에 전기신호와 소자들에게 열전자로 인해 열 잡음을 일으키며 열폭주와 같은 예상치 못한 동작을 일으키고 반도체가 파괴될 수도 있다. 고온에서 회로가 정지하도록 신호를 주고 식었을 때 다시 가동하도록 디지털 신호를 주는 고온 탐지기가 필요하다.

본 논문에는 BJT 가 흘리는 전류가 온도에 따라 증가하는 성향을 이용하여 고온 탐지기회로를 Magnachip 0.35um CMOS 공정으로 PAD 를 제외한 103 um * 56 um 크기로 그림 1 과 같이 설계, 제작, 측정하였다. 본 논문의 탐지기 회로는 그림 2 과 같이 고온 검출부, 증폭부, 온도 기준 전환부로 나뉘어 있다. 고온 검출부에서는 온도에 따라 변하는 BJT 의 전류에 따라 증폭부에서 전압으로 검출하여 출력하게 된다. 증폭부에서 0 으로 인식되는 온도까지 올라가면 온도기준 전환부로 신호를 전달하여, 고온 검출부의 BJT 전류를 더 증가 시키도록 전환한다. 증가된 BJT 전류가 증폭부에서 1 로 인식될때까지 온도가 내려가야 다시 출력이 1 로 돌아오며, 온도 기준 전환부가 BJT 의 전류를 다시 감소시키게 된다. 하강된 온도에서는 전류를 더 감소시켜도 증폭부에서 1 로 인식하는 정상상태가 된다. 온도에 따른 출력의 히스테리시스는 3.3V 1mA 에서 그림 3 과 같이 85℃와 48℃로 측정되었다.

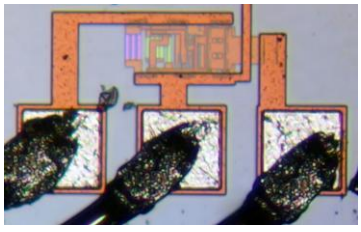

그림 1. 제작된 고온 탐지기

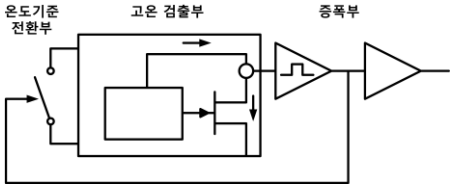

그림 2. 고온 탐지기 구성도

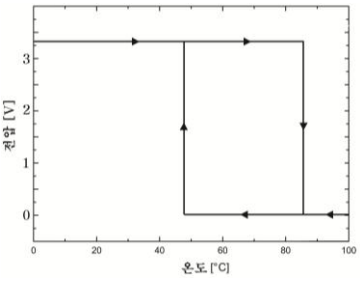

그림 3. 온도에 따른 출력 값 측정 결과

[1] Phillip E. Allen, Douglas R. Holberg. CMOS Analog Circuit Design. Third Edition. p161 (2012).

Cu_2Te as back contact layer in CdS/CdTe solar cell

ShinHaeng Cho, SangSu Kim, MinHyuk Park, and JinKi Hong
Department of Applied Physics, Korea University, ChungNam 339-800, Korea
E-mail : jkhongjkhong@korea.ac.kr

Cu_2Te is a promising candidate of back contact material on CdTe based solar cell. 600Å thick Cu_2Te and Cu films were deposited on CdS/CdTe solar cells by use of thermal evaporation method. Subsequent annealing was carried out under several conditions of temperature. A single phase of Cu_2Te is produced by annealing at 180 ℃. Barrier height of the contact between Cu_2Te (or Cu) and CdTe layer and hole density nearby the contact were obtained from current-voltage and capacitance-voltage characteristics. Figure 1 displays the curves of current density versus bias voltage (*J-V*). The rollover effect increases gradually as temperature decrease, which can be characterized by turning current, J_t. J_t is defined by the current in a *J-V* curve where a rollover takes place (see the inset of Fig. 1). J_t obtained from experimental *J-V* curves are shown in Fig. 2. Φ_b of the Cu_2Te and Cu device are 0.41 and 0.43 eV, respectively, which are determined from the theoretical curve. Φ_b reported by other groups belong to the range of 0.35~0.45 eV, which supports our results are reasonable ones. The hole density nearby the contact in our device is 6×10^{15} cm^{-3}, and conversion efficiency reaches 12%. The barrier height of the Cu_2Te device is less than that of the Cu device, which is one of the evidence showing promising possibility of Cu_2Te material for application to CdTe based solar cell.

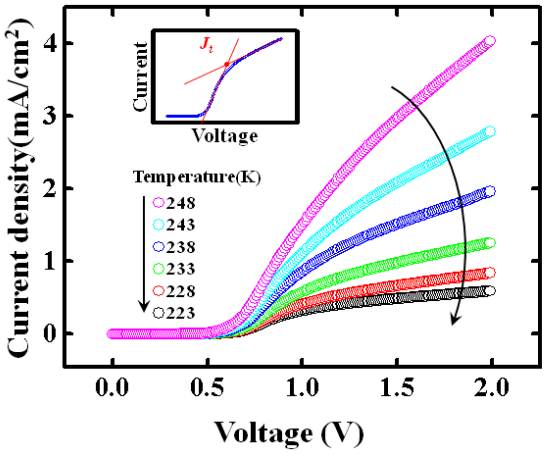

Figure 1: Current density versus bias voltage for Cu_2Te/CdTe/CdS/ITO device for various temperature. The inset shows the definition of turning current, J_t.

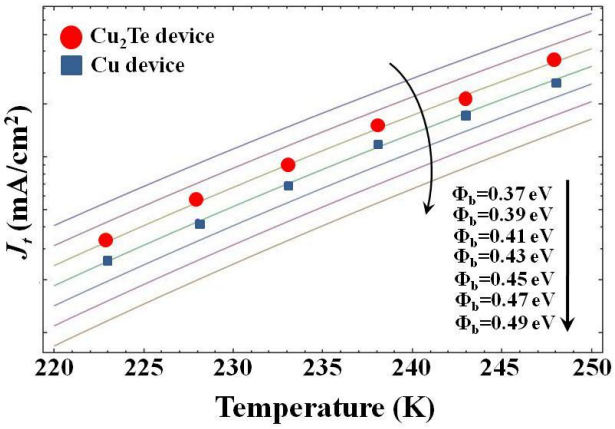

Figure 2: Turning current density as a function of temperature. Solid lines are theoretically calculated ones where Φ_b is used as a parameter. The curves of Φ_b=0.41 and 0.43 eV well simulate the experimental ones.

Photovoltaic and electrical characterization of $Cu(In,Ga)Se_2$ thin film solar cells

Ji Eun Kim, Yunae Cho, and Dong-Wook Kim

Department of Physics, Ewha Womans University, Seoul 120-750, Korea

E-mail : jekim12@ewhain.net

Chalcopyrite thin film based solar cells is in the limelight research interest due to their high efficiency and low cost. Copper indium gallium diselenide (CIGS) solar cells consist of several polycrystalline thin films deposited by several growth techniques. Analysis of their optical and electrical properties can provide us valuable information regarding further enhencement of the energy conversion efficiency. In recent days, there has been intensive research effort to prepare CIGS thin films by solution-based process. However, in-depth electrical characterizations and analyses have not been carried out. In this regard, understanding roles of the defects in solution-processed CIGS thin films is a very important research subject. We studied photovoltaic characteristics and the temperature dependence of transport behaviors. In particular, we investigated the complex admittance of the devices as means to deduce the energy distribution of traps. We could reveal major recombination processes in the cells. Also, we could identify dominant trap states, influencing the temperature-dependent admittance spectra.

Flat and thin heat dissipation method for high power device

Seok-Hwan Moon[1], Kyu-Ho Lee[1], Soo-Hyun Hong[1], Sang-Choon Ko[1],
Chi-Hoon Jun[1], Jae-Kyoung Mun[1], Hyung-Man Lee[2]
1 GaN Power Device Research Department, ETRI, Daejeon, Korea
2 KETI, Seongnam, Korea
E-mail : shmoon@etri.re.kr

Elevated temperatures is one of the disadvantages of a high power device. To reduce the temperature, we may consider a material with high thermal conductivity at the chip level, and a passive or active type heat dissipation device at the module level[1]. In this study, a flat and thin passive type dissipation solution, operated by a vapor-liquid phase change heat transfer mechanism, was investigated for application to the module and system. The flat heat dissipation device has a flat shape, making it easy to thermally contact with a heat source in comparison to the conventional circular type[2]. A heat dissipation device with 2 mm thickness and 40 mm width was designed and fabricated. Also, a variety of total lengths was considered. Through the results, based on the temperature difference between the heat input and heat dissipation parts, we were able to obtain a reliable heat dissipation solution with thermal resistance lower than 2 ℃/W. The results also indicated the heat dissipation device has some operational limitations in total length. The device is recommended to operate with a total length shorter than 250 mm.

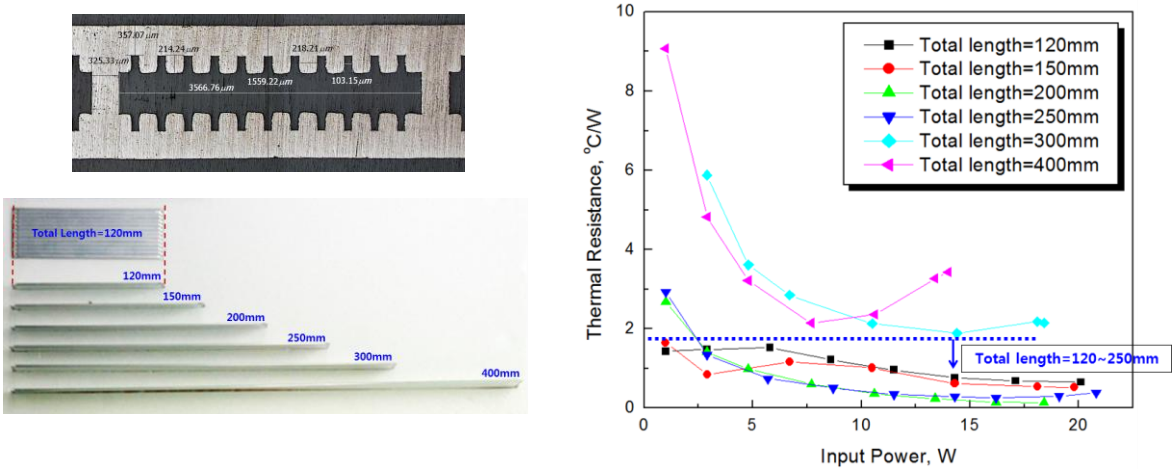

Fig 1. Flat heat dissipation device and its thermal experimental data

[1] A Wang, M J Tadjer and F Calle, “Simulation of thermal management in AlGaN/GaN HEMTs with integrated diamond heat spreaders,” Semicond. Sci. Technol. 28, 8pp (2013)
[2] S.H. Moon, G. Hwang, and H.T. Lim, “Development of a Flat-Plate Cooling Device for Electronic Packaging,” ETRI Journal, Vol.33, No.4, pp. 645–647 (2011)

Photo-thermal current in $SrRuO_3$ thin film device

Ji Ho Sung, Jin Hong Lee, and Moon-Ho Jo
Advanced Materials Science, POSTECH, Korea
E-mail : jihosung@postech.ac.kr

In general, seebeck coefficient(thermo-power) is a measure of the energy dependence of the DOS(density of state) at the fermi level(E_F). The DOS(at E_F) of transition metal oxides is predominated by heavy d-electrons, therefore, the conduction electrons are expected to be localized strongly.[1] Correlated transition metal oxide material, strontium ruthenate($SrRuO_3$) is known to be metallic itinerant ferromagnet and is also known for its widespread utility as a conducting electrode in oxide heterostructures. However, its thermoelectric properties have scarcely been reported until now. Here, we demonstrated that the $SrRuO_3$ thin film is responsible for photo-thermal electric current properties by scanning photocurrent microscopy. We estimated the seebeck coefficient of $SrRuO_3$ with measured photocurrent and also provide the temperature and optical power dependence. This study suggest that scanning photocurrent microscopy can be a useful tool for understanding thermoelectric properties of materials and also suggest the transition metal oxides including strontium ruthenate as a potential thermoelectric material. [2]

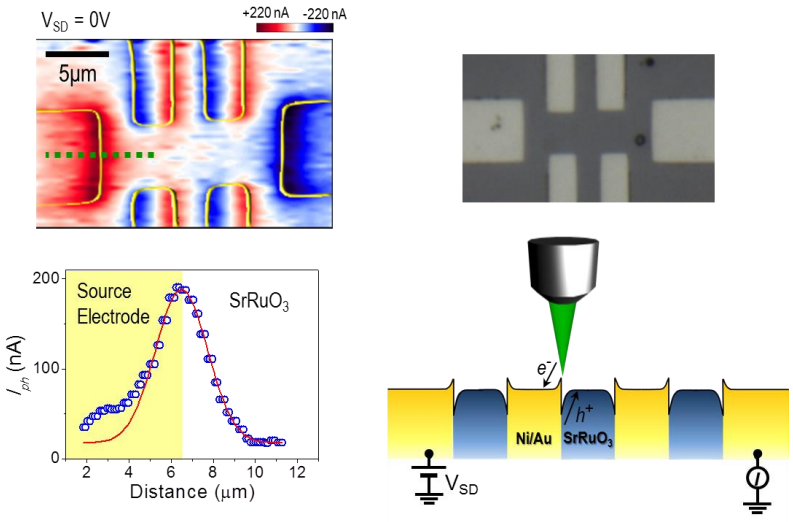

Fig 1. $SrRuO_3$ thin film device and its photothermal current

[1] Hiromichi Ohta et al., Nat. Mater. 6, 129 (2007).
[2] M. Buscema, et al., Nano Lett. 13, 358 (2013)

Estimating Electrical and Optical Properties of 1D Metal Grid Transparent Electrode on SiO_2 substrate

Kilbock Lee, Jinho Ahn
Department of Material science & Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jhahn@hanyang.ac.kr

Metal-based TCE is one of the promising candidates as a next-generation transparent electrode because of flexibility, low costs and the highest electrical conductivity at room temperature.[1,2] We investigated the transmission behavior of 1-dimensional metal grid on SiO_2 substrate using a simulation tool. 1D silver and aluminum grid exhibit low sheet resistance and very high transparency in visible region. The metal grid in 500 nm and 1 μm linewidth demonstrates uniform transparency over a wide range of visible wavelength corresponding to the opening ratio of the structure and low sheet resistance similar to the bulk resistivity of materials. To compare the properties of different structures, two types of figure of merit were estimated. 1 μm-linewidth Ag grid yields the best figure of merit (FoM), which shows a high ratio of the electrical conductance and the optical conductance (σ_{dc}/σ_{opt}) of 1123 in 95 % OR structure and Haacke's figure of merit (ϕ_{TC}) of 7.3×10^{-2}. This study will be helpful in understanding the transmission behavior of 1-dimensional metal grid and will also provide guideline for the design of metal grid transparent electrode for optoelectronic devices.

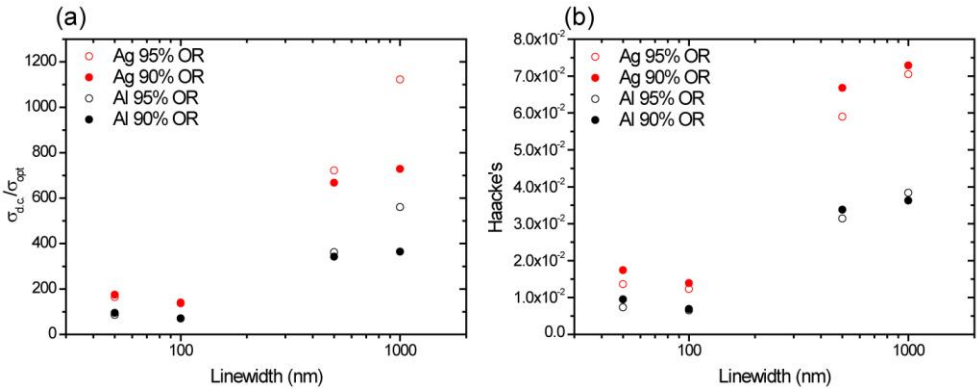

Fig 1. FoM(figure-of-merit) values of metal grid with various width and structure

[1] Klaus Ellmer, Nat Photon **6** (12), 809 (2012).
[2] David Hecht, Liangbing Hu, and Glen Irvin, Advanced materials (Deerfield Beach, Fla.) **23** (13), 1482 (2011).

Characterization of degradation in Cu(In,Ga)Se_2 photovoltaic modules under accelerated damp heat

Dong-Won Lee[1,2], Yong-Nam Kim[2], Chi-Hong Park[3], Kyung-Eun Park[3], and Won-Ju Cho[1*]

[1]*Department of Electronic Materials Engineering, Kwangwoon University, Korea*
[2]*Material Testing Center, Korea Testing Laboratory, Seoul 152-718, Korea*
[3]*Solar Cell Laboratory, LG Innotek Co., Ltd., Osan 447-705, Korea*
E-mail : chowj@kw.ac.kr

Long operational lifetime, reliability and stability of PV modules are crucial for their success as a source of renewable energy. To ascertain a long-term stability of PV modules, several types of accelerated tests have been employed. An important tool in the qualification of solar cell modules is the damp heat test, where modules are placed in a high temerature (85^{o}C) and humidity (85%) environment [1]. In this paper, to clarify causes for the degradation of CIGS PV moduels, the damp heat stability of modules is investigated. After damp heat test, PV modules showed decreased open-circuit voltage (V_{oc}), fill factor (*FF*), and efficiency and exhibited a discoloration phenomenon around the edge. To clarify the reason for the degradation of V_{oc}, *FF*, and efficiency, a failure analysis on the degraded PV modules was carried out. After exposure to damp heat, the degradaiton behaviors of CIGS PV modules are suggested based on the relationship among the electrical properties of AZO layer, CIGS layer and Mo layer. In addition, to clarify the effect of moisture on degradation of CIGS PV modules, we conducted depth profiling and chemical bonding analysis using X-ray photoelectron spectrometer (XPS) and Fourier transform infrared (FT-IR) spectrometer, respectively.

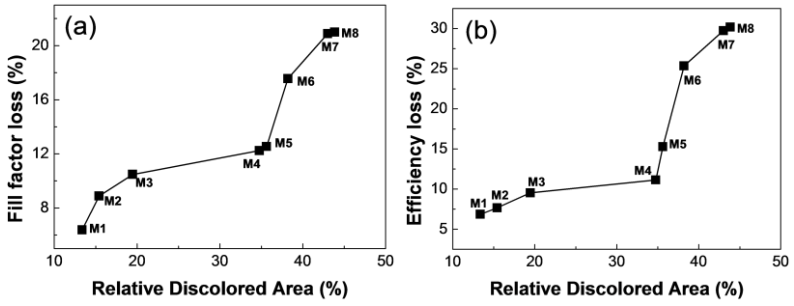

Fig 1. (a) Fill factor and (b) efficiency loss as a function of relative discolored area of CIGS PV modules.

[1] P.F. Carcia, R.S. McLean, and Steven Hegedus, Sol. Energy Mater. Sol. Cells 94, 2375 (2012).

Changes in the characteristics of Cu(In,Ga)Se_2 photovoltaic modules under various accelerated environmental tests

Dong-Won Lee[1,2], Yong-Nam Kim[2], Chi-Hong Park[3], Kyung-Eun Park[3], and Won-Ju Cho[1*]

[1]*Department of Electronic Materials Engineering, Kwangwoon University, Korea*
[2]*Material Testing Center, Korea Testing Laboratory, Seoul 152-718, Korea*
[3]*Solar Cell Laboratory, LG Innotek Co., Ltd., Osan 447-705, Korea*
E-mail : chowj@kw.ac.kr

Cu(In,Ga)Se_2 (CIGS) has a major potential as a semiconductor material for thin film photovoltaic devices. This is because of its appropriate band gap and high absorption coefficient and outstanding electro-optical properties [1]. Recently, CIGS-based photovoltaic (PV) modules have been widely fabricated for their high conversion efficiency and good performance. However, for their success as a source of sustainable energy as well as the successful commercialization, the long-term stability and performance reliability of CIGS PV modules are important issues. To ensure the long-term stability and reliability of CIGS modules, the degradation behaviors of CIGS cells under various accelerated degradation tests, as well as the damp heat test, should be investigated. In this study, the reliability and stability of CIGS modules under various degradation accelerated tests were preferentially investigated. After performing the various accelerated stresses, the CIGS modules showed a decrease in P_{max}. To explain the degradation mechanism of CIGS modules, the failure analysis of CIGS modules was performed. Through the connection between electrical properties and structural properties, the causes of the degradation of CIGS modules under various degradation accelerated tests were clarified.

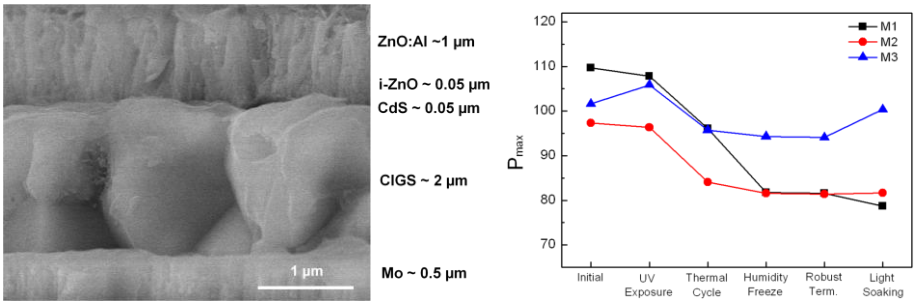

Fig 1. CIGS solar cell and P_{max} changes of CIGS modules after various accelerated degradation tests.

[1] N.G. Dhere, Sol. Energy Mater. Sol. Cells 91, 1376 (2007).

Ga-Doped ZnO Nanorods Using an Aqueous Solution Method for a Piezoelectric Nanogenerator

Su-HyunYoon, Sang-Woo Kim
School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon 440-746, Republic of Korea
E-mail : kimsw1@skku.edu

Mechanical energy has a high potential for self-powered electronic devices. Wurtzite-structured nanomaterials have been regarded as potential applicants for piezoelectric nanogenerators which can change mechanical energy into electricity, due to their special semiconducting and piezoelectric properties. In this paper, we report on the growth of Ga-doped ZnO (GZO) nanorods and examine the performance of nanogenerators fabricated from undoped ZnO (UZO) nanorods, low Ga-doped ZnO (LGZO) nanorods, and high Ga-doped ZnO (HGZO) nanorods. A nanogenerator combined with LGZO nanorods demonstrated a current density of 1.2 μA/cm², an enhancement over the 0.4 μA/cm² and 0.7 μA/cm² current densities of nanogenerators combined with UZO and HGZO nanorods, respectively.

High-Performance of P-type Polymer Hybridized ZnO Thin Film Piezoelectric Nanogenerator

Sung-Soo Kwak[1)], Keun Young Lee[1)], Sang-Woo Kim[1)2)]

[1)] *Sungkyunkwan University (SKKU), School of Advanced Materials Science & Engineering, 2066 Seobu-Ro Jangan-gu, Suwon, Gyeonggi-do, 440-746, KOREA*

[2)] *SKKU Advanced Institute of Nanotechnology (SAINT), School of Advanced Materials Science & Engineering, 2066 Seobu-Ro Jangan-gu, Suwon, Gyeonggi-do, 440-746, KOREA*

Enhancing the output power of a nanogenerator is essential in applications as a sustainable power source for wireless sensors and microelectronics. We report here a novel approach that greatly enhances piezoelectric power generation by introducing a p-type polymer layer on a piezoelectric semiconducting thin film. Holes at the film surface greatly reduce the piezoelectric potential screening effect caused by free electrons in a piezoelectric semiconducting material. Furthermore, additional carriers from a conducting polymer and a shift in the Fermi level help in increasing the power output. Poly(3-hexylthiophene) (P3HT) was used as a p-type polymer on piezoelectric semiconducting zinc oxide (ZnO) thin film, and phenyl-C61-butyric acid methyl ester (PCBM) was added to P3HT to improve carrier transport. The ZnO/P3HT:PCBM-assembled piezoelectric power generator demonstrated 18-fold enhancement in the output voltage and tripled the current, relative to a power generator with ZnO only at a strain of 0.068%. The overall output power density exceeded 0.88 W/cm3, and the average power conversion efficiency was up to 18%. This high power generation enabled red, green, and blue light-emitting diodes to turn on after only tens of times bending the generator. This approach offers a breakthrough in realizing a high-performance flexible piezoelectric energy harvester for self-powered electronics

Two-Dimensional Vanadium-Doped ZnO Nanosheet-Based Flexible Direct Current Nanogenerator

Tae Yun Kim, Manoj K Gupta, Sang-Woo Kim
Advanced Institute of Nanotechnology, Sungkyunkwan University, Suwon 440-746, Korea
E-mail : kimsw1@skku.edu

Growth of two-dimensional (2D) nanosheet have attracted tremendous attention owing to their fascinating physics, unique properties and potential applications in future electronics. Herein, we report the direct growth of high crystalline piezoelectric 2D vanadium doped ZnO nanosheet (NS) on flexible and transparent polymer substrate coated with ITO. We fabricated transparent and flexible nanogenerator (NG) based on 2D V-doped ZnO NS. We found that, the morphologies of ZnO nanostructures changed completely from vertically aligned nanorods to vertical nanosheet network due to vanadium doping. X-Ray diffraction and high resolution transmission electron microscopy (HR-TEM) studies confirm the wurzite structure and preferred c-axis orientation of V-doped ZnO NS. The piezoelectric and ferroelectric properties of ZnO NS were measured using PFM. The piezoelectric output voltage and current were measured from fabricated nanogenerator under vertical compressive force. This work opens up a new avenue for miniaturization of self-powered nanodevices and nanosystems and also promises new form of 2 dimensional based nanogenerator for multifunctional applications.

Stretchable Piezoelectric-Pyroelectric Hybrid Energy Harvester based on P(VDF-TrFE)

HongJoon Yoon[1)], and SangWoo Kim[1), 2)*]

[1)] *School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 440-746, Korea*

[2)] *SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University, Suwon, 440-746, Korea*

E-mail : yoonhj@skku.ac.kr

One of piezoelectric material showing pyroelectric property is poly(vinylidenefluoride -co-trifluoroethylene) [P(VDF-TrFE)] polymer which has been extensively studied and reported as a promising energy harvester taking advantage of ambient sources, for example mechanical energy generated from all movements and thermal energy. It is consequently favorable to convert both forms of energy from a single cell of nanogenerators(NG) that shows significant power output performance and also can be utlized in numerous applications such as wearable communication devices, electronic textile, and biomedical devices. Micro-patterned polydimethylsiloxan(PDMS) -carbon nanotubes(CNTs) composite made the NG device truly stretchable and flexible, and also served as a robust electrode on the bottom side of the device.[1,2] Instead of using metal electrodes, graphene nanosheets which have excellent flexibility and high thermal conductivity are functioned as a top electrode since a rapid temperature gradient should be realized. It is foreseeable that the micro-patterning process increases durability of devices and stable performance even after a number of stretch-and-release cycles. NG described as follows based on piezoelectric and pyroelectric effects measured its electric and mechanical properties under certain strains and thermal gradients. With this promising technology, we believe conversion of ambient sources that might be negligible into practical and usable electric energy is possible.

[1] S. Ghosh, I. Calizo, D. Teweldebrhan, E. P. Pokatilov, D. L. Nika, A. A. Balandin, W. Bao, F. Miao, C. N. Lau, Appl. Phys. Lett., 92, 151911 (2008).

[2] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, C. N. Lau, Nano Lett., 8, 902 (2008)

Microstructure and electrical property of Si/Carbon Fiber hybrid structure

Eulyong Chae, Heedo Na and Hyunchul Sohn*
Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : eychae@yonsei.ac.kr

Due to increasing need for energy issues, various electronic applications have been developed until now. Among them, solar cells have been considered the best candidates for addressing energy problems. Particularly for various applications, carbon fiber, material consisting of fibers about 5-10 μm in diameter and composed mostly of carbon atoms, has been almost exclusively used due to its superior properties such as high strength, low weight, high temperature tolerance, low thermal expansion, and high electrical property to other materials. We suggest new paradigm that low cost and high electrical property based carbon fiber is integrated with semiconductor process technology. Carbon fiber based solar cell has some effective benefits over traditional wafer based or thin film devices related to electrical effects, lightweight, flexible property, new charge separation mechanisms, and cost[1]. Therefore, it is used in a myriad of different applications such as flexible or wearable devices. To apply the hybrid structure consisting of carbon fiber and silicon layer to solar cell, microstructure and electrical properties of the hybrid structure should be investigated first. In this study, we analyzed the microstructure and electrical properties of silicon layer on carbon fiber for carbon fiber based solar cell. For this study, we designed a jig for analyzing electrical property of carbon fiber and measured it several times. Intrinsic silicon layer on carbon fiber was deposited by plasma-enhanced chemical vapor deposition (PECVD) according to its deposition time. Then, photo and dark current of silicon layer on carbon fiber were measured by I-V measurement using designed jig, and result in general characteristics of schottky diode. Also, microstructure of this hybrid structure was observed by scanning electron microscopy (SEM).

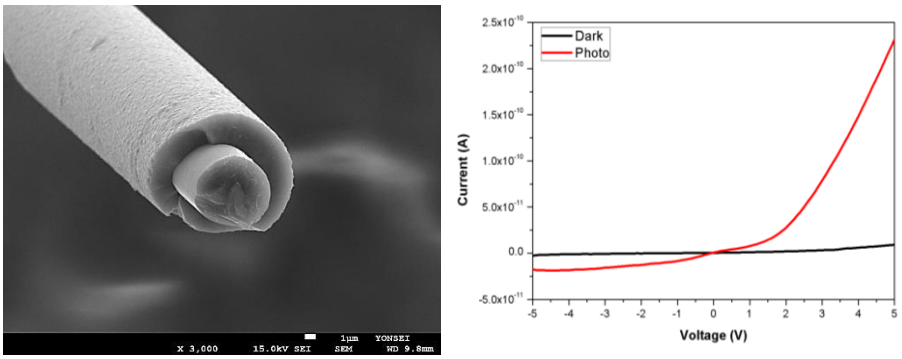

Fig 1. Microstructure and I-V characteristic of Si/Carbon Fiber hybrid structure (dep. time:180s)

[1] Wenjun Xu, Seungkeun Choi and Mark G. Allen, Georgia Institute of Technology, 2010, IEEE

A 60/120 GHz Push-push Voltage Controlled Oscillator in 65 nm CMOS Technology

Namhyung Kim, Jongwon Yun, and Jae-Sung Rieh

School of Electrical Engineering, Korea University, Seoul 136-713, Korea

E-mail : jsrieh@korea.ac.kr

The paper proposes a 60/120 GHz push-push voltage controlled oscillator (VCO) in 65-nm CMOS technology. The circuit offers V-band and D-band output, and can be used in D-band phase locked loops (PLL) [1].

The core of the VCO is based on a push-push LC cross-coupled structure, and blocking capacitors (C1 and C2) are added in front of the varactors to linearize the tuning behavior of the VCO [2] . The total size of the implemented circuit including pads is 690 × 460 μm^2.

The circuit was fabricated using Samsung 65-nm CMOS technology. The output frequency varies from 116.5 GHz to 118.4 GHz. The measured output powers are around -1 dBm and -21 dBm for V-band and D-band respectively. The phase noise is measured through the frequency divider chain, and the estimated phase noise is -90.6 dBc/Hz at 1 MHz offset from the 118 GHz output. The VCO draws 24 mA from a 1.5 V voltage supply, including output buffers.

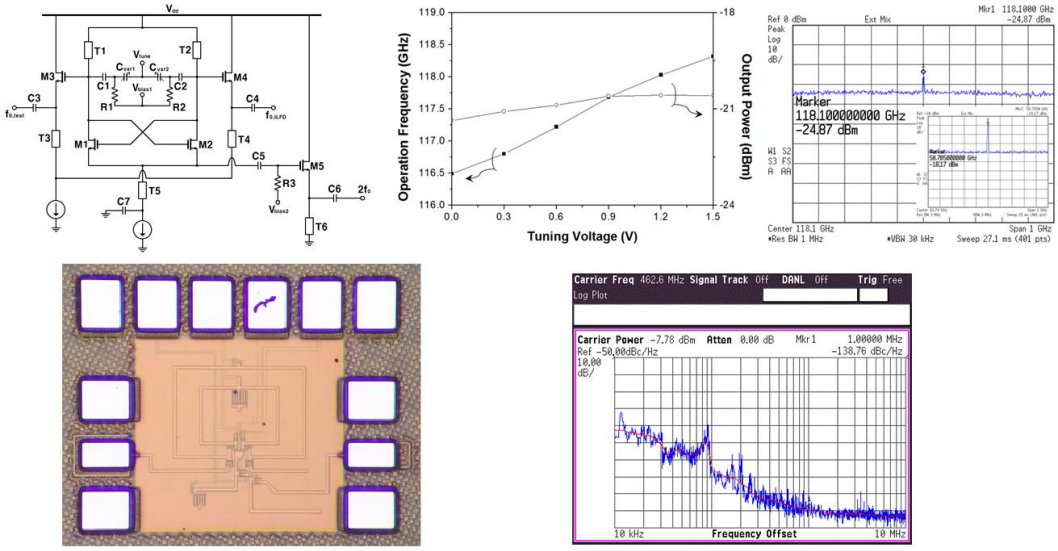

Fig 1. Schematic, chip photo and measurement results

[1] K.-H. Tsai and S.-I. Liu, "A 104-GHz Phase-Locked Loop Using a VCO at Second Pole Frequency," IEEE Transactions on Very Large Scale Integration Systems, vol. 20, pp. 80-88, 2012.

[2] N. Kim, Y. Oh, and J.-S. Rieh, "A 47 GHz LC Cross-Coupled VCO Employing High-Q Island-Gate Varactor for Phase Noise Reduction," IEEE MWCL, vol. 20, pp. 94-96, 2010.

A 60 GHz Injection-Locked Frequency Divider in 65 nm CMOS Technology

Namhyung Kim, Jongwon Yun, and Jae-Sung Rieh

School of Electrical Engineering, Korea University, Seoul 136-713, Korea

E-mail : jsrieh@korea.ac.kr

The paper proposes a 60 GHz injection-locked frequency divider (ILFD) in 65-nm CMOS technology. The circuit can be used in high operation frequency phase locked loop (PLL) [1, 2].

The circhit was designed based on a LC cross-coupled structure with a tail injection. To increase the operation range with frequency tuning, additional varactors are included in the core of the ILFD. The varactors also help to degrade the Q-factor of the tank, leading to a locking range improvement [3]. Another effort to increase the locking range was made by increasing the ratio between the injection and the oscillation currents.

The circuit was fabricated using Samsung 65-nm CMOS technology. The measured locking range was around 3.5 GHz for a fixed varactor state with an injection power level of around -1 dBm. With extra varactor tuning, an operation range over 5 GHz was obtained with the input frequency of around 30 GHz. The ILFD core and the buffer draw 6 mA and 4 mA from a 0.8 V and 1 V supply, respectively, leading to a total DC power consumption of 8.8 mW.

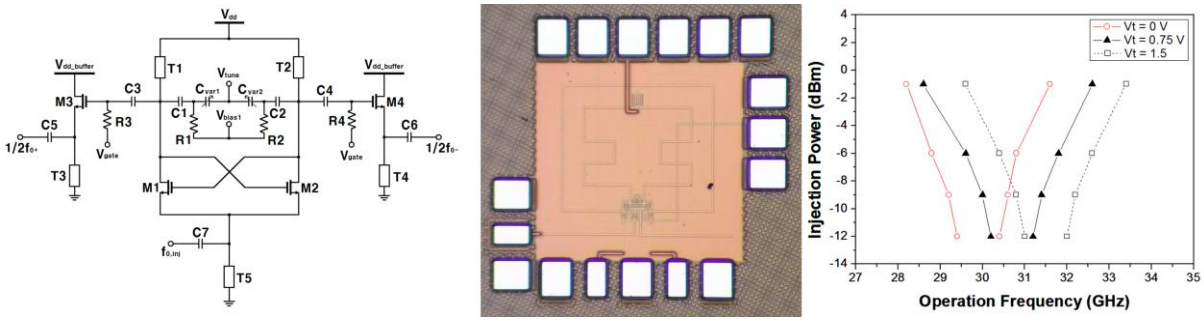

Fig 1. Schematic, chip photo and measured locking range

[1] K.-H. Tsai and S.-I. Liu, "A 104-GHz Phase-Locked Loop Using a VCO at Second Pole Frequency," IEEE Transactions on Very Large Scale Integration Systems, vol. 20, pp. 80-88, 2012.

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[3] B. Razavi, "A study of injection locking and pulling in oscillators," IEEE Journal of Solid-State Circuits, vol. 39, pp. 1415-1424, 2004.

A 5 GHz Phase Locked Loop in 0.11-μm CMOS Technology

Namhyung Kim, Jongwon Yun, and Jae-Sung Rieh
School of Electrical Engineering, Korea University, Seoul 136-713, Korea
E-mail : jsrieh@korea.ac.kr

The paper demonstrates a 5 GHz phase locked loop (PLL) with a LC cross-coupled voltage controlled oscillator (VCO) developed in 0.11-μm CMOS technology. The designed PLL can be used in 5 GHz wireless communication systems [1-3].

The PLL is composed of a 5-GHz LC cross-coupled VCO, 8-stage static divider chain, a PFD and a charge pump with an on-chip loop filter. The total size of the implemented system including pads is 1.16×0.96 mm^2.

The circuit was fabricated using Dongbu 0.11-μm CMOS technology. The measured tuning range of the PLL is from 4.89 to 5.02 GHz. Figure 3 shows the measured spectrum when the PLL is in locked state. At this state, the maximum power level of the reference spur is about 45 dB lower than the PLL output signal f0. The VCO and dividers including other digital block draws 9 mA and 20 mA from a 1.2 V and 1.5 V voltage supply, respectively.

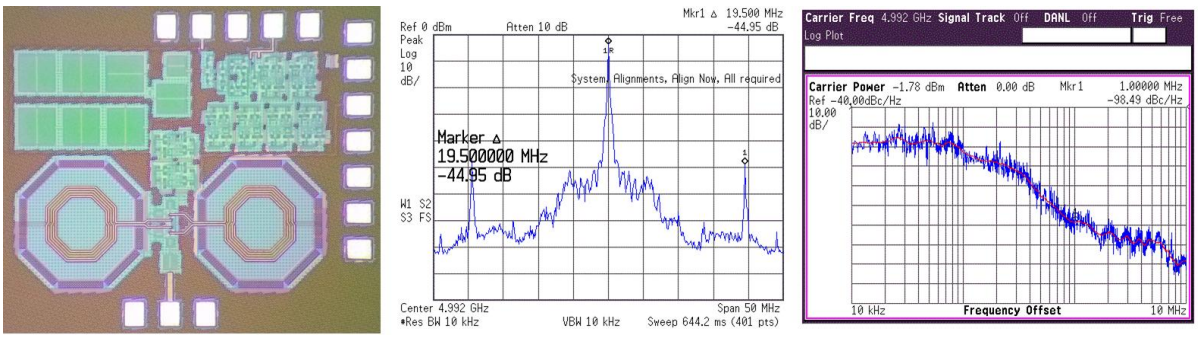


Fig. 1 Chip photo and its measurement results

[1] H. R. Rategh, H. Samavati, and T. H. Lee, "A 5 GHz, 32 mW CMOS frequency synthesizer with an injection locked frequency divider," in IEEE VLSI Circuits Symposium, 1999, pp. 113-116.

[2] H. Samavati, H. R. Rategh, and T. H. Lee, "A 12.4 mW CMOS front-end for a 5 GHz wireless-LAN receiver," in IEEE VLSI Circuits Symposium, 1999, pp. 87-90.

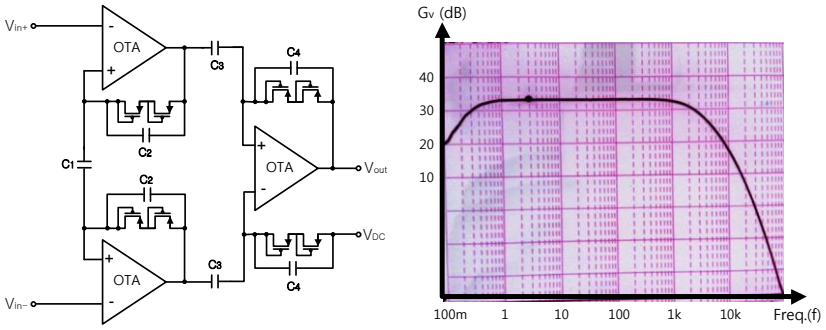
[3] C. Quemada, J. Mendizabal, J. Presa, I. Adin, J. Legarda, and G. Bistue, "A CMOS frequency synthesizer with selfbiasing current source for a 5-GHz wireless LAN receiver," in IEEE Personal, Indoor and Mobile Radio Communications Symposium, 2004, pp. 1886-1890 Vol.3.

A Low-Power Low-Noise CMOS Instrumentation Amplifier for Versatile Biopotential Signal Acquisition

최종환, 이욱준, 신현철
광운대학교 전파공학과 고속집적회로 및 시스템 연구실
E-mail : cjhwan86@kw.ac.kr

인간의 건강한 삶에 대한 관심이 증가함에 따라서 IT 융합 의료기기에 대한 관심이 크게 성장하고 있다. 특히, U-healthcare 사회의 실현을 위해 휴대가 가능한 다기능 복합형 생체 신호 측정용 의료기기들이 개발되고 있다. 의료기기의 소형화 추세에 따라 뇌파 측정 등의 생체 신호 측정용 기기를 하나의 칩으로 구현하고 있는 추세에 있다.

이러한 추세에 발맞춰 본 논문에서는 일반적으로 5 ㎷ 이하에 존재하는 생체신호인 심전도, 근전도, 뇌파를 단일 칩으로 측정할 수 있는 시스템의 맨 앞단에서 생체 신호를 1 차적으로 증폭하는 역할을 하는 저전력 계측용 증폭기 설계 결과에 대하여 기술하였다. 그림 1(a)는 일반적으로 사용되는 3 Op-Amp 를 이용한 계측증폭기 구조를 사용하였다. 그림 1(b)는 Signal Control Analyzer (HP3564A)에 의해서 측정된 결과이다. 전체 대역폭은 0.15 Hz ~ 2 kHz 으로 일반적인 생체신호의 대역폭인 0.5 Hz ~ 1 kHz 를 포함하고 있으며, 전체 전압이득은 34 dB 로 측정되었다. 설계된 생체신호 측정용 저전력 저잡음 증폭기는 CMOS 0.18 ㎛ process 에 의해서 제작되었으며 전체 대역폭은 다양한 생체신호를 증폭하기 적합하도록 설계되었다. 전체 소모 전류는 저전력 설계에 의해 4 ㎂의 측정 결과를 얻었으며, 6.2 ㎶ rms 의 Input-referred RMS noise 값을 얻을 수 있었다.



(a) (b)

그림 1.(a) 설계된 계측증폭기 (b) 측정결과

• 감사의 글

본 연구는 한국연구재단 기초연구사업(2012038649), 대학 IT 연구센터 지원사업 (NIPA-2013-H0301-13-1013) 및 IDEC MPW 의 지원으로 수행되었음.

[1] 최종환, 신현철 "다양한 생체 신호 수집을 위한 저전력 저잡음 CMOS 계측 증폭기," 2012 년 대한전자공학회 SoC 학술대회, pp. 20, 광운대학교, 2012 년 4 월 21 일.

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A 1 W, 68 % PAE Stacked RF Power Amplifier Using 0.18-μm SOI CMOS

Jung-Lin Woo, Sunghwan Park, and Youngwoo Kwon
Department of EECS and INMC, Seoul National University, Seoul 151-747, Korea
E-mail : woocr421@gmail.com

The efficiency of RF Power Amplifier (RFPA) directly affects the battery time in wireless handset application, because RFPA is the most power consumer in the RF front end. Therefore, highly efficient RFPA is strongly demanded. In this work, 2-stage CMOS stacked RFPA is demonstrated. To overcome the breakdown limit of CMOS FET, stacked FET configuration is widely used for CMOS RFPA. Fig. 1 (a) shows the schematic of designed 2-stage RFPA. Triple stacked FET is used for both driver and power stage. The size of power cell driver stage is 20mm and 2mm respectively. The overall efficiency of stacked PA is heavily depends on the size of power cells. At a first glance, large power cell looks appropriate choice for stacked configuration because it will lead lower dc power dissipation from the knee voltage hence enhance the output power and efficiency. However, parasitic capacitances from over-sized FET disturb the in-phase voltage combining; result in degradation of overall efficiency. This trade-off relation can be solved by charging acceleration capacitor on the each node of common gate FET(CM2, CM3)[1]. Fig. 1 (b) shows measured performance of 2-stage stacked RFPA using 840MHz carrier frequency CW mode with 3.4V supply voltage. The maximum output power reaches 29.8dBm with 68% PAE and 75% power stage drain efficiency. This excellent efficiency performance shows potential for fully integrated CMOS envelope-tracking transmitter.

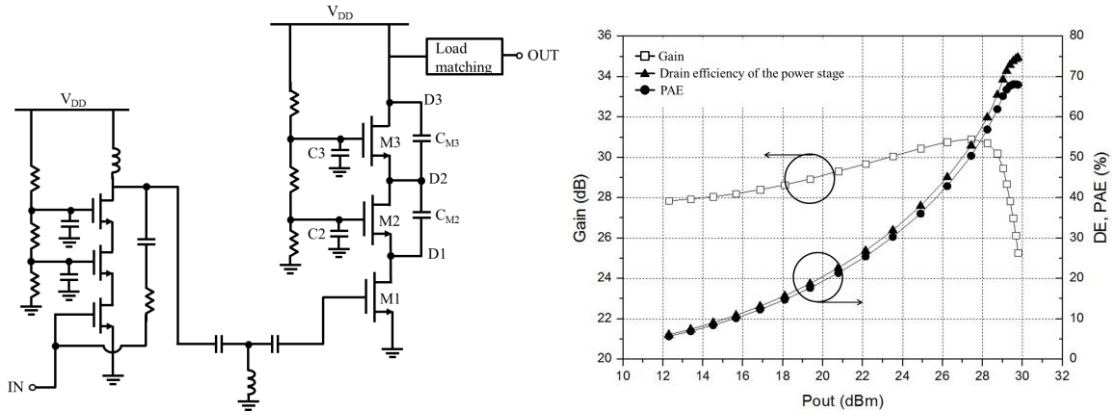


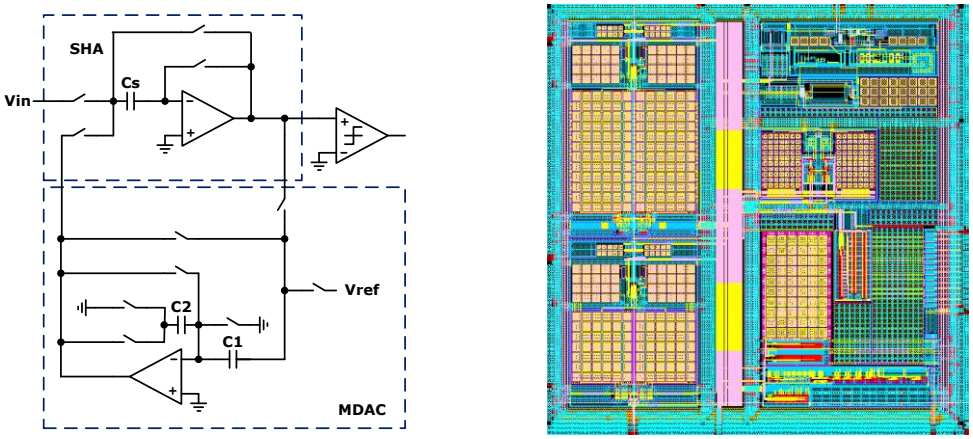
Fig 1. (a) Schematic of designed 2-stage RFPA. (b) Measured performance of the 2-stage RFPA

[1] O. Lee, J. Han, K. An, D. Lee, K. Lee, S. Hong, and C. Lee, "A Charging Acceleration Technique for Highly Efficient Cascode Class-E CMOS Power Amplifiers," IEEE Journal of Solid-State Circuits, Vol. 45, No. 10, pp. 2184-2197, Oct. 2010.

A 14-b Ratio-Independent Algorithmic ADC

Seunghuen Song, Kichang Jang, Chulkyu Park, and Joongho Choi
Department of Electrical and Computer Engineering, University of Seoul, Seoul 130-743, Korea
E-mail : jchoi@uos.ac.kr

Ratio-independent technique for algorithmic analog-to-digital converter is presented. This technique is suitable for achieving high resolution overcoming mismatch limit between sampling capacitors caused by process variation. The performance of the conventional algorithmic analog-to-digital due to capacitor mismatch is improved by modifying arrangement of capacitor switching with four phase clock scheme. Accurate signal multiplication that is required by conversion is realized through multiplying digital-to-analog converter. Charge summing and multiplying can be performed with capacitors that occupy a small die area. Switch errors generated in the circuit are minimized by fully differential circuit implementation and delayed non-overlap clocks. The algorithmic A/D converter was fabricated in a 0.13-μm CMOS technology. It achieves 70.2 dB SNDR at a sampling rate of 1.92 kHz and showed power consumption of 706μW. The active die area is 1 x 1 mm^2.



(a) (b)

Fig. 1. (a) Architecture of the ratio-independent algorithmic A/D converter.
(b) Layout of the A/D converter.

[1] Li, P.W, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. 19, pp. 828-836, Dec. 1984.
[2] Kichang Jang, "A Low Power 13-Bit Analog Front End for Mobile Battery Monitoring Applications," *Proc. IASTED* 2008 Conference, pp.89-92, Aug. 2008.

Designed Opamp Sharing SDM with FDPA(Feedback Delay Path Addition) Technique

Euihoon Jung, Kisang jung, Jaebung Kim, and Seongik Cho
Div. of Electronic & Information Engineering, Chonbuk National University, jeonju 561-756, Korea
E-mail : euihoon@jbnu.ac.kr

SDM(Sigma-Delta Modulator)에서 보다 높은 SNR을 얻기 위한 방법으로 OSR을 높이는 방법, 적분기의 개수를 늘려서 차수를 증가시키는 방법, 양자화기의 bit수를 높이는 방법 등이 있다. 하지만 적분기의 개수를 늘려 차수를 증가시키거나 양자화기의 bit수를 증가시키면 전력소모와 면적이 커지게 된다. 따라서, 연산증폭기를 공유하고, 적분기의 개수를 증가시키지는 않지만 전달함수를 증가시켜 SNR을 높이는 방법을 제안한다. 제안한 구조는 SDM의 잡음 특성을 개선하고자 STF와 NTF에 (Z+1)의 극점을 추가하였다. NTF에 (Z+1)의 극점을 추가하면 NTF의 크기는 신호 대역 내에서 1/2로 줄어들어 SNR이 7dB 증가한다. 제안한 구조는 비교기 출력을 DF/F을 이용하여 디지털 피드백 패스만을 사용하는 방법을 제안한다. FDPA 기법을 이용한 제안한 구조는 전력 소모를 낮추기 위해 적분기 하나로 구현하였고, 클록의 종류가 단순화 되어 회로 구현이 간단하다. 0.18um CMOS 공정을 이용하여 신호대역폭 20KHz, 샘플링 주파수 2.56MHz에서 실험하였고, 그 결과 전력 소모는 220uW이고 SNR은 81dB이다.

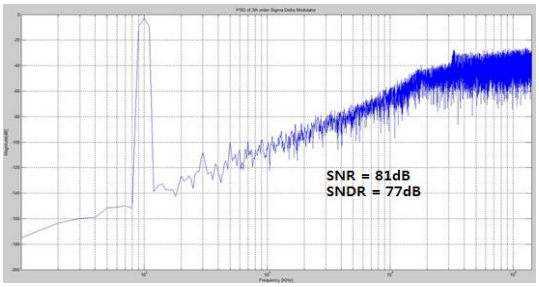


Fig 1. SNR of simulation result

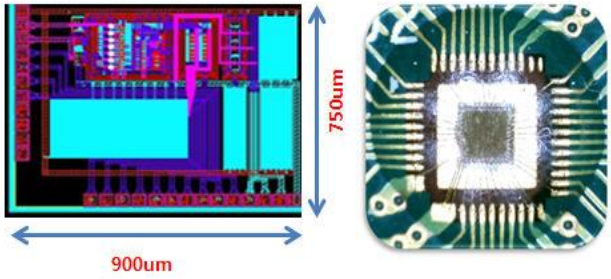


Fig.2 Chip layout and COB photo

[4] Daisuke Kanemoto, Toru Ido and Kenji Taniguchi, “A 7.5mW 101dB SNR Low-Power High-Performance Audio Delta-Sigma Modulator Utilizing Opamp Sharing Technique,” SoC Design Conference(ISOCC), 2011 Internatioanl, pp. 66-69. 2011

[5] Chuan-Hung Hsiao, Wei-Lin Chen, Chih-Cheng Hsieh, “A 0.8V 80.3dB SNDR Stage-Shared Sigma-delta Modulator with Copper-Embeded Switched-Opamp for Biomedical Application,” IEEE Asian Solid-State Circuits Conference, IPEC. 2012. 6522673, pp. 253-256. 2012

Design and Implementation of BPSK Modem in 0.35 um CMOS Process

Cheolmin Ahn, Youngsik Kim
Department of Information and Technology, Handong Global University, Pohang 791-708, Korea
E-mail : adsums@hgu.edu

Modern wireless communication systems could be classified by the data rate and cover range. In the wide area network, the larger cover range and higher speed are main concerns, but a near link with medium speed system is much focused on its power consumption. In such a near/medium link, the amplitude modulation schemes have been widely used to improve the power efficiency [1]. However, it is well-known that AM has poorer noise immunity and spectral efficiency compared with a phase-shift keying (PSK) [2]. For this reason, binary phase-shift keying (BPSK) is still widely used in wireless communication such as WPAN (Wireless Personal Area Network) [3]. The structure of designed BPSK modem is shown in Fig 1. The data rate of designed BPSK modem is 40 kb/s and the chip rate is 600 kchip/s. BPSK modem is implanted with VHDL and implemented with 1P5M 0.35 um CMOS process.

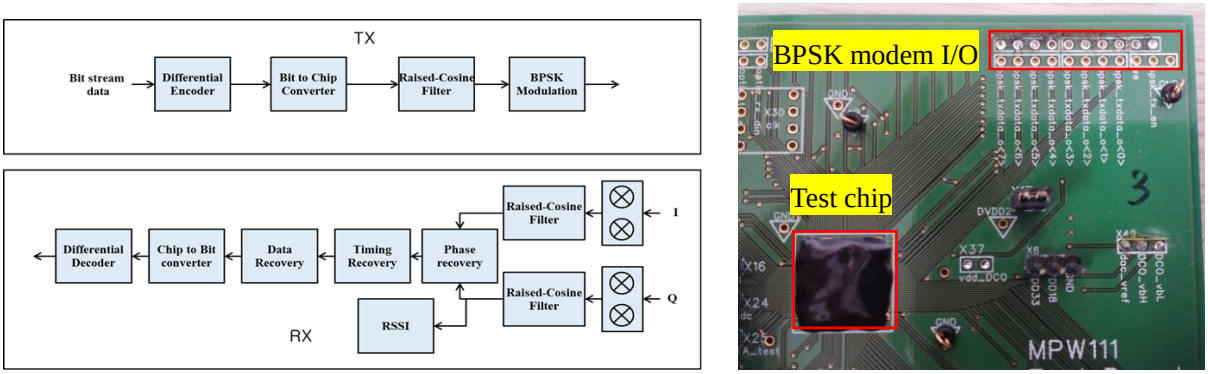


Fig 1. Block diagram of BPSK modem and the test PCB for BPSK modem

[1] D. C. Daly and A. P. Chandrakasan, “An energy-efficient OOK transceiver for wireless sensor networks,” IEEE J. Solid-State Circuits, vol.42, no. 5, pp. 1003–1011, May 2007.
[2] B. Sklar, Digital Communication Fundamentals and Applications. Upper Saddle River, NJ: Prentice-Hall, 2001.
[3] IEEE Std. 802.15.4-2003, ‘Wireless medium access control and physical layer specifications for low-rate wireless personal area networks’ IEEE Press, New York, 2003

Vibration Induced Self-startup for Dual-source Energy Harvesting Interface

Young-Sub Yuk, Hui-Dong Gwon, Sung-Won Choi and Gyu-Hyeong Cho
Department of Electrical Engineering, KAIST, Daejeon, Korea
E-mail : bvtop@kaist.ac.kr, wings@kaist.ac.kr, swon0927@kaist.ac.kr

This paper presents self-startup technique in a battery-free boost converter for energy harvesting interface from both static and vibration energy sources. The vibration-induced self-startup process provides intermittent supply to the controller until the boost converter completely wakes up. Fig.1 shows the proposed scheme for the self-startup using TEG and PZT. This system starts to wake up whenever VDX exceeds the MOV of 650mV. The control circuit powered intermittently controls the boost converter to transfer energy from V_{IN_TEG} to C_{Load} via the inductor L. By this operation, V_{OUT} increases gradually and eventually the body diode of M4 turns on. Then, the leakage current from V_{OUT} to V_{DX}, i_{leak}, helps V_{DX} not to decrease below some level. Eventually, when BV by voltage doubler exceeds the threshold of M4, the V_{DX} is strongly defined by V_{OUT}. Then, the starting up procedure is completed by providing constant supply to control circuit. After the self-starting sequence has been completed, the energy from PZT also harvested as well as from TEG. Fig 2 shows the measurement waveform for the proposed self-startup technique. Fig 2 (a) shows the V_{OUT} according to the various TEG voltages and the PZT sinusoidal output voltage is $1V_{pp}$. The minimum voltage for startup is 240mV for TEG when PZT sinusoidal output is 1Vpp. Fig 2 (b) shows the V_{OUT} and V_{DX} when the self-startup occurs. As the proposed concept at Fig 1, when the V_{DX} exceeds the M.O.V, the V_{OUT} is increased by the energy from TEG.

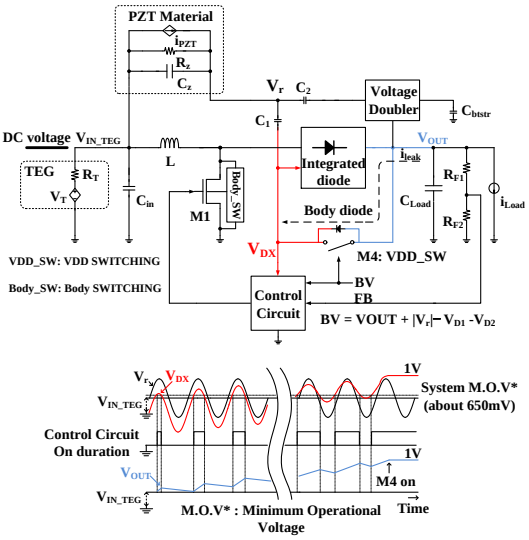


Fig. 1. A proposed self-startup scheme for dual-source energy harvesting interface

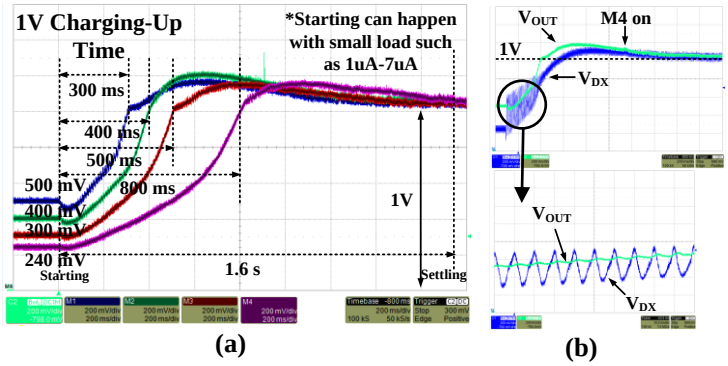


Fig. 2. Self-startup waveform: (a) V_{OUT} according to various TES's voltage and (b) V_{DX} with V_{OUT} voltage at 500mV TEG's voltage

[1] Y. K. Ramadass and A. P. Chandrakasan, "An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," IEEE ISSCC Dig. Tech. Papers, pp. 296-297, Feb. 2009.
[2] Y. K. Ramadass and A. P. Chandrakasan, "A batteryless Thermoelectric Energy-Harvesting Interface Circuit with 35mV Startup Voltage," *IEEE ISSCC. Dig. Tech. Papers*, pp 486-487, Feb 2010.

A 2.4μW 400nC/s Constant Charge Injection for Wirelessly-Powered Electro-Acupuncture

Hyungwoo Lee, Yongsu Lee, and Hoi-Jun Yoo
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST)
E-mail : hwlee@eeinfo.kaist.ac.kr

An invasive medical treatment using electro-acupuncture has received more attention recently. To improve subject's convenience, a multi-channel wirelessly-powered EA system [1], [2] was proposed. However, the safety issue correlated to balanced charge intensity [3] was not considered. In this paper, a hybrid frequency-drift compensation mechanism is presented so that injected charge should be stable over time. It was regulated by APF calibration loop.

Fig.1 shows the structure of the proposed constant charge injector (CCI) based on APF calibration loop. It consists of: 1) diode protection, 2) frequency-drift compensation including clock generator, and 3) an auxiliary control logic.

The measurement result shows that the proposed APF in CCI provides supply voltage dependency of 0.2Hz/V. It is sufficiently stable for inject-able charge intensity of 399.33-400.45nC/s. The proposed CCI is expected to be safer and lower power consumption than the previous APW stimulator [1], [2]. This work was supported by the IDEC.

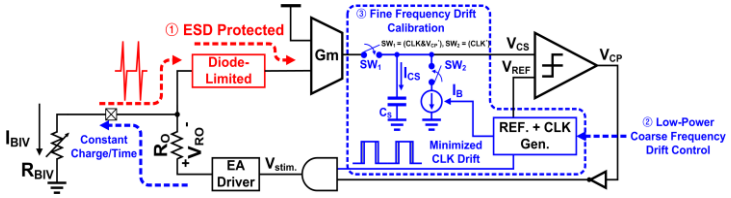


Fig 1. The proposed constant charge injector (CCI)

incorporates adaptive pulse-width frequency-drift (APF) calibration

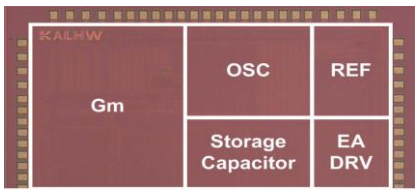


Fig 2. Chip photograph

[1] K. Song, S. Lee, and H.-J. Yoo, IEEE ISCAS, May 2010.
[2] K. Song, L. Yan, S. Lee, J. Yoo, and H.-J. Yoo, IEEE TBioCAS 2011.
[3] C. David Lytle, Brenton M. Thomas, Edward A. Gordon and Victor Krauthamer, The Journal of Alternative and Complementary medicine, vol.6, 2000.

An ANN-Searching Processor for Full-HD 30fps Video Object Recognition

Gyeonghoon Kim, Jinwook Oh, Dongjoo Shin, and Hoi-Jun Yoo
Department of EE, KAIST, Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea

An approximate nearest neighbor (ANN) searching is an essential function in object recognition [1]. ANN-searching stage becomes the main bottleneck in object recognition process due to increasing database size and massive dimensions of keypoint descriptors. In this paper, a high throughput ANN-searching processor is proposed for high-resolution (Full-HD) and real-time (30fps) video object recognition. The proposed ANN-searching processor adopts, both inter-frame cache architecture and zeroless locality-sensitive-hashing (zeroless-LSH) algorithm as a hardware-oriented approach and a software-oriented approach, respectively, to reduce the external memory bandwidth required in nearest neighbor searching. A 4-way set associative on-chip cache has a dedicated architecture to exploit data correlation in frame level. Zeroless-LSH minimizes data transaction from external memory in vector-level. The proposed ANN-searching processor is fabricated as a part of object recognition SoC using a 0.13μm 6 metal CMOS technology and it achieves 62,720 vectors/sec throughput and 1,140GOPS/W power efficiency, which are 1.45x and 1.37x higher than the state-of-the-art respectively, enabling real-time object recognition for Full-HD 30fps video streams.

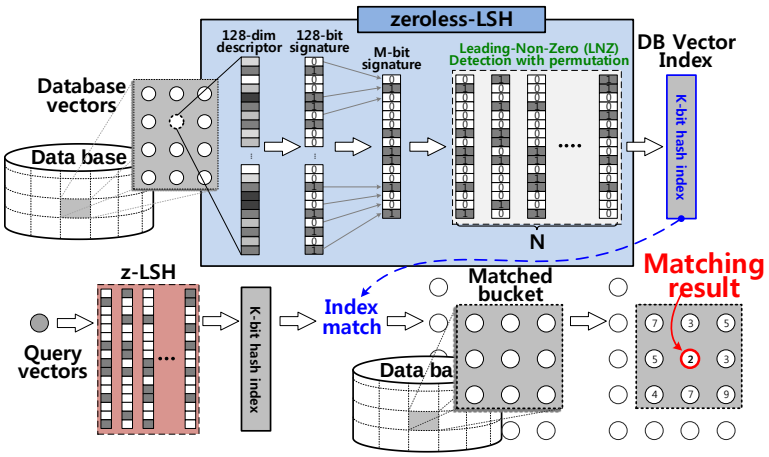


Fig 1. Zeroless locality-sensitive hashed algorithm

[1] Adnoni, A., "Near-optimal hashing algorithms for approximate nearest neighbor in high dimensions," Proceedings of the 47th Annual IEEE Symposium on Foundations of Computer Science, pp. 459–468, 2006.

This work was supported by the IDEC.

채널간 전류 오차를 보상하는 PLL구조를 이용한 Current regulator의 설계

임을수, 황인철
강원대학교 전기전자공학과
E-mail : eslim@kangwon.ac.kr

LED 특성상 전류-광출력의 관계가 선형이므로 LED driver IC 에는 CR(current regulator)를 이용해 전류를 조절한다. 하지만 LED 공정 특성상 채널간의 전류의 mis-match 가 발생한다. 이것은 채널간 광출력의 불균형을 만들게 되어 보상이 필요하다. 그리하여 PLL 구조를 이용한 새로운 CR 제안한다. 그림 1 은 CR 의 상세한 회로도 이다. S1, S2 가 동시에 턴온되며 채널전류(M1)는 M3 에 1/1200 의 비율로 on-chip current sensor 를 통해 전류를 센싱하고 CVG(Current to Voltage pulse Generator)를 통해 센싱된 전류를 전압의 펄스로 바꾼다. 그리고 내부에서 기준전류에 의해 만들어진 전압펄스와 센싱 펄스를 비교하여 결과적으로 PLL 과 같이 PFD 로 비교하여 charge pump 에서 출력을 gate 전압으로 보상하여 결과적으로 출력전류를 보상한다. Linear regulator 와 비교하면, 센싱 저항을 제거하여 CR 의 효율을 높이고 각 채널간 전류를 300mA 이내에서 5mA, 1.6% 이내의 오차의 측정결과를 보인다.

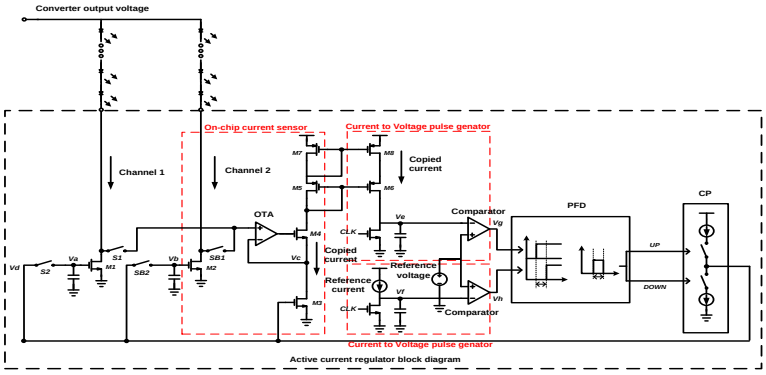


Fig 1. 제안하는 Current regulator 의 블록도.

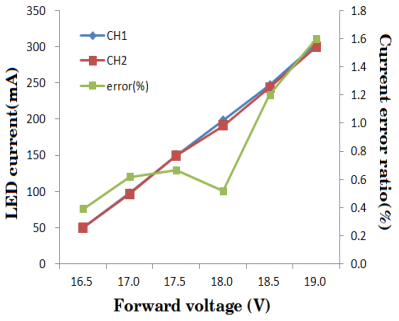


Fig2. 채널간 전류오차 측정결과

"This work was supported by the IDEC" and "This research was supported by the MSIP, Korea, under the C-ITRC support program supervised by the NIPA(NIPA-2013-H0401-13-1002)"

[1] Chen, C. C., C-Y. Wu, and T-F. Wu. "LED back-light driving system for LCD panels." *Applied Power Electronics conference and Exposition, 2006. APEC"06. Twenty-First annual IEEE, 2006*

[2]*http://ledlight.osram-os.com/wp-content/uploads/2010/05/AppGuideCurrentDistributioninParallelLEDStrings.Web_.pdf*

[3] Rao, S., Khan, Q., Bang, S., Swank, D., Rao, A., McIntyre, W.,&Hanumolu, P. K. (2011). "A 1.2-A Buck-Boost LED Driver With On-Chip Error Averaged Sense FET-Based Current Sensing Technique. Solid-State Circuit, IEE Journal of, 46(12), 2772-2783

H^+ Ion-sensitive Transistor based on Gated Lateral Bipolar Junction Transistor (GLBJT)

Hyeon-Ji Yun*, Hyun-Min Jeong**, Hyurk-Choon Kwon**, and Shin-Won Kang†
*Department of Sensor and Display Engineering, Kyungpook National University, Daegu, Korea
**,†School of Electronics Engineering, College of IT Engineering, Kyungpook National University, Daegu, Korea
†E-mail : swkang@knu.ac.kr

Lateral Bipolar Junction Transistor (GLBJT) was reported in the late 1960s [1]. The GLBJT of p-channel transistor implemented by n-well CMOS technology is shown in Fig. 1 [2]. The proposed device fabricated in a standard 0.13-μm CMOS logic process, which is provided by Samsung Electronics Co., Ltd. via the Integrated Circuit Design Education Center Multi-Project Wafer (IDEC-MPW). The device can be operated on multiple modes, including a typical MOSFET mode, a typical BJT mode, and a MOSFET-BJT hybrid mode. The operational modes can be switched using the gate bias and base current (I_B) supply. The propose of this study is to demonstrate that the GLBJT using MOSFET-BJT hybrid mode makes the electrochemical sensor avaliable and the characteristics of this device can be adaptable in pH measurements. As shown in Fig. 2, the sensitivity of the proposed sensor for hydrogen-ion were approximately 5.1 μA/pH, 9.7 μA/pH, and 7.4 μA/pH, for acid, alkaline, and total pH range, respectively.

Acknowledgments

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (NO. 2008-0062437). This work was supported by Samsung Electronics Co., Ltd. and the IDEC

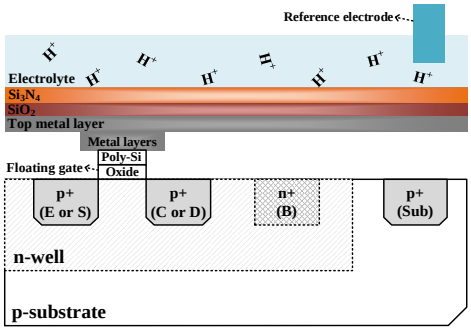


Fig 1. Schematic of GLBJT for H^+ ion detection

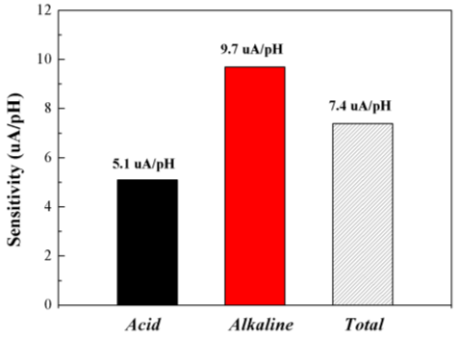


Fig 2. Acid, alkaline, and total sensitivity using GLBJT

[1] H. C. Lin, J. C. HO, R. R. Iyer, and K. Kwong, IEEE Trans, Electron Devices, vol. ED-16, no. 11, pp. 945-951, Nov. 1969.

[2] H. C. Kwon, D. H. Kwon, K. Sawada, and S. W. Kang, IEEE, Electron Device Lett, vol. 29, no. 10, pp. 1138-1141, Oct. 2008.

A Hough Transform-Based Line Detection Accelerator

Jeong-Rok Lee, Hyeon-Sik Son, Kyeong-ryeol Bae, and Byungin Moon
School of Electronics Engineering, Kyungpook National University, Daegu 702-701, Korea
E-mail : bihmoon@knu.ac.kr

The Hough transform for line detection is widely used in many machine vision applications due to its robustness against data loss and distortion [1]. However, it is not appropriate for real-time embedded vision systems, because it has inefficient computation structure and demands a large number of memory accesses. Thus, there have been some researches and developments for the implementation of hardware accelerators for line detection but they are only about line detection using FPGA devices which have constraints in cost and performance. On the other hand, there are few researches and developments for ASIC implementation of line detection accelerator. So, we developed a Hough transform-based line detection accelerator ASIC for low-power and small-area implementation. We improved the conventional voting scheme of the Hough transform, and then we applied this scheme to our Hough transform hardware architecture so that it can provide real-time performance with less hardware resource [2]. This scheme reduces computation overhead of the voting procedure by using correlation between adjacent pixels and by increasing reusability of vote values. The proposed hardware architecture maximizes its throughput by computing and storing vote values for many adjacent pixels in parallel. After FPGA verification of the proposed Hough transform architecture, it was implemented in an ASIC through IDEC MPW with M/H 0.18 μm technology.

Specifications	
Gate count	560,000
Frequncy	27 MHz
SRAM	46 SRAMSs of 1120 × 8
die size	4.5 mm × 4 mm
Package	LQFP 208

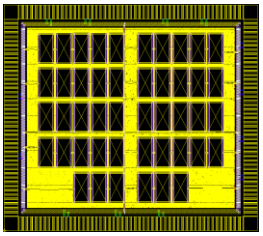


Fig 1. Specification, layout and package of the Hough transform ASIC

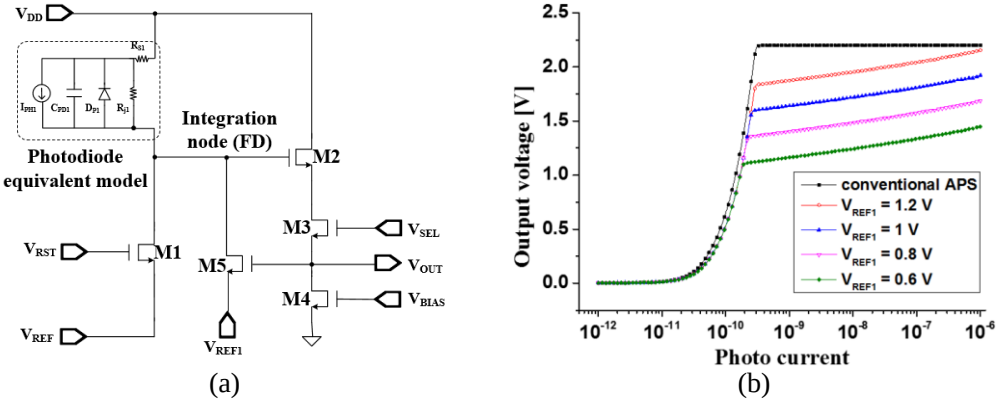
[1] C. T. Ho and L. H. Chen, “A high speed algorithm for line detection,” Pattern Recognition Lett., vol. 17, no. 5, pp. 467-473, May 1996.
[2] J. Lee, K. Bae, B. Moon, “A Hardware Architecture of Hough Transform Using an Improved Voting Scheme,” J. Korea Inform. Commun. Soc. (KICS), vol. 38A, no. 9, 1892, pp. 773–781, sept. 2013.

Wide dynamic range CMOS Linear-Logarithmic active pixel sensor

Sung-Hyun Jo[1], Myunghan Bae[1], Minho Lee[1], Jeongyeob Kim[2], Byoung-Soo Choi[1],
Pyung Choi[1] and Jang-Kyoo Shin*[1,2]
[1]*School of Electronics Engineering, College of IT Engineering, Kyungpook National University*
[2]*Department of Sensor and Display Engineering, Kyungpook National University*
1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Korea
E-mail : jkshin@ee.knu.ac.kr

In the complemetary metal-oxide semiconductor (CMOS) image sensors (CISs), pixel size has continuously been scaled down using sub-micron CMOS process and thus the operation voltage has been reduced. However, the sensitivity and dynamic range of the active pixel sensor (APS) is decreased because of the reduction in the photo-detection area and supply voltage. Various approaches have been proposed to achieve high-sensitivity and wide dynamic range. Conventional logarithmic sensors operating in the sub-threshold region suffer from low sensitivity at low light intensity. The quality of the resulting output image of the logarithmic sensor is degraded by mismatches between the individual pixels in each sensor [1].

In this work, we propose a new approach of wide dynamic range CMOS APS based on feedback mechanism [2]. The proposed APS has advantages to allow improvements in both the dynamic range and the sensitivity. The designed circuit is being fabricated by using 0.18μm 1-poly 6-metal standard CMOS technology.



(a) (b)

Fig 1. The proposed APS. (a) Schematic, (b) variation of the output voltage with the photocurrent as a function of reference voltage (V_{REF1}).

[1] Dileepan Joseph and Steve Collins, Journal of Transactions on Instrumentation and Measurement, vol. 51, no. 5, pp. 996-1001, 2002.

[2] Sung-Hyun Jo, Hee Ho Lee, Myunghan Bae, Minho Lee, Ju-Yeong Kim, Pyung Choi, Jang-Kyoo Shin, Journal of sensor science and technology, Vol. 22, No. 4, pp. 256-261, 2013.

Design of Analog-Digital Signal Processing Circuit for γ-ray Detection

You Mi Kwon[1], Hee-Sung Kang[1], Ji-Hyun Kim[1], Soo-Jin Yu[1], Ju-Yeung Kim[1], Minho Lee[1], Young-Kyu Kwon[2], Deok-Hwan Hyun[3], Jung-Hee Lee[1] and Yong Soo Lee[1*]

[1)]School of Electronics Engineering, Kyungpook National University, Daegu
[2)]Department of Electronics Engineering, Uiduk University, Gyeongju
[3)]Department of Electrical Energy and Electronic Engineering, Gyeongju University, Gyeongju

**E-mail : leesoo@femtoline.com*

Nuclear explosion emits gamma ray, electromagnetic pulse (EMP) as well as X-ray in advance of thermal and air blasting shock wave. This energy generates electron-hole pair (EHP) in semiconductor devices of the electrical systems. Excessive amount of EHP results in current which might go beyond the limits of the system and ultimately destroy the system [1-2]. Gamma ray detector circuit senses initial gamma ray radiation and raise a signal to protect and avoid the sensitive systems from being destroyed. This paper presents the design and implementation of the gamma ray detection circuit. The system consists of two parts. One is 2 latches which set the event indicating output signals and the other is comparator block which comprises of 13-bit comparator as well as 2 counters. Input signal from the gamma ray sensor turns ON the two SR latches that directly set two output signals. One of the output of latches is nuclear event flag (NF) signal, which indicates the nuclear event has occurred and this signal gets reset by an external input signal. The other output of the latch is nuclear event output (NO) signal which turns OFF the power switches of the system under protection. By doing this we expect that fatal impact of the radiation on the system will be avoided. Before layout, operation of the system was checked with Altera Quartus system. Figure 2 shows the block diagram of the system. Proper operation of the system was confirmed with Quartus system. Clock input of the system is 1 [MHz] to assure a fast response time from the sensor input to NO output. Counter resolution was 13-bit to accommodate wide range of the NO signal duration. Fig. 1 and 2 shows the layout of the chip and the measurement results of the completed chip. 1 [MHz] clock was used as a clock frequency. NO signal duration was changed with a reference value which was supplied externally. We confirmed proper operation of the system as we expected.

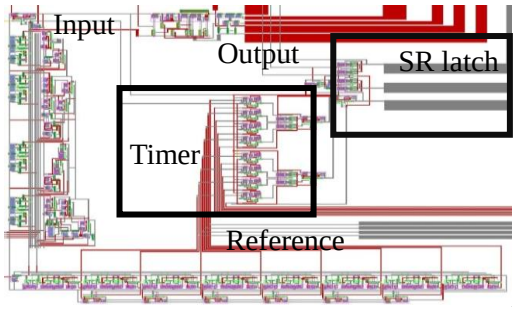


Fig. 1: Layout of signal processing circuit

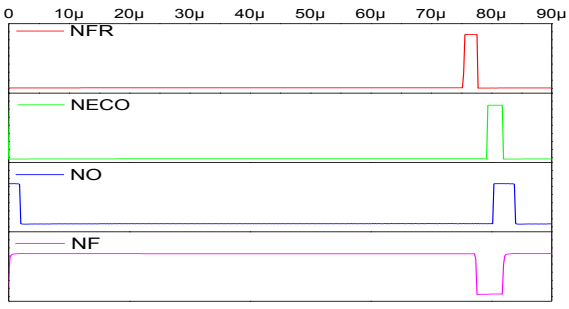


Fig. 2: The measurement result of input-output

[1] R.C. Baumann, IEEE Trans. Dev. Mat. Rel., 1, 17 (2001)

[2] M. Tavani, A. Argan, A. Paccagnella, A. Pesoli, F. Palma, S. Gerardin, M. Bagatin, A. Trois, P. Picozza, P. Benvenuti, E. Flamini, M. Marisaldi, C. Pittori, and P. Giommi, Nat. Hazards Earth Syst. Sci., 13, 1127 (2012)

320MHz ~2.2GHz 32분주 다이나믹 D-플립플롭 디바이더

정재상, 하정완, 김창우
경희대학교 전자전파공학
E-mail : jungjs21@khu.ac.kr

디바이더는 모든 시스템에서 주파수 분주 역할을 하는 회로이다. 통신시스템이 점차 고주파로 개발됨에 따라 디바이더 역시 GHz 대의 고주파 동작을 요구하게 되었다.
이 논문은 통신시스템에서 필수적으로 사용되는 PLL 의 주파수 분주를 위해 설계되었다.
L-Band 대역 동작을 기점으로 설계하였으며 TowerJazz 0.18-um RFCMOS 공정을 이용해 설계하였으며 170 x 95-um^2 의 크기를 가진다.
D-플립플롭에서 흔히 발생하는 전하공유(charge sharing)과 글리치(glitch) 현상을 줄이기 위해 다이나믹 구조를 선택하였으며 Q-bar 를 D-input 에 피드백을 통하여 2 분주 신호를 만들어내도록 했다. 그림 1. 은 다이나믹 D-플립플롭을 이용한 디바이더이며 총 5 단의 2 분주 회로를 통하여 32 분주 디바이더를 설계하였다. 그림 2, 3. 은 320 MHz 와 2.2 GHz 클럭에서의 32 분주 측정결과를 나타낸다.

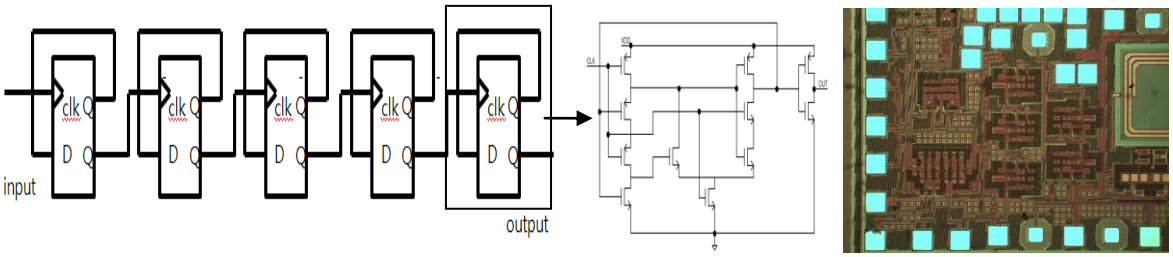


그림 1. 다이나믹 D-플립플롭을 이용한 32 분주 디바이더

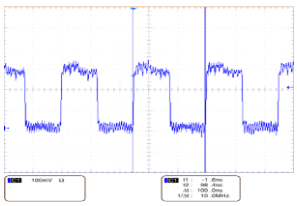


그림 2. 320MHz 측정결과

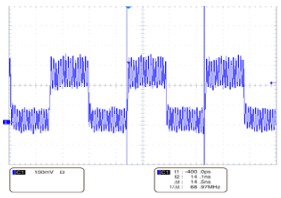


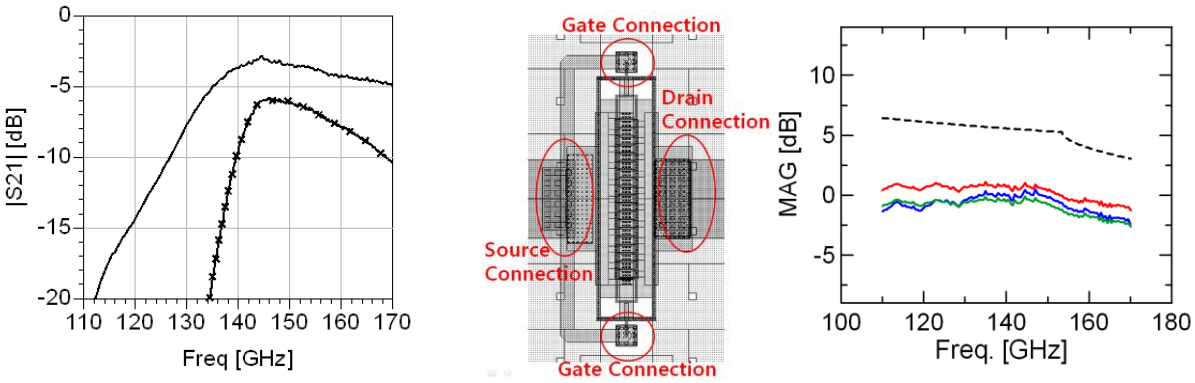
그림 3. 2.2GHz 측정결과

[1] Sung-Hyung Yang, “A CMOS dual-modulus prescaler based on a new charge sharing free D-flip-flop” ASIC/SOC Conference, 2001. Proceedings. 14th Annual IEEE international.

Understanding CMOS Amplifier Design Issues in D-band by Fabricating Conventional Amplifier

S.H. Choi, K.J. Lee, and M. Kim
School of Electrical Engineering, Korea University, Seoul, 136-701, Korea
E-mail : hyperleonheart@hotmail.com

Conventional CMOS common-source amplifier is fabricated and measured to understand the design issues in D-band. Although standard CMOS 65nm technology is known to provide f_T and f_{MAX} over 200GHz, it is hard for a single amplifier to obtain positive gain because of device parasitics[1]. Fabricated amplifier is desined using non-linear model provided by process. All of passive structures are EM simulated except internal device parasitics. Simulation expects a single amplifier to present 2.2 dB peak |S21|, while calculated |S21| from measurements is only -0.75dB(Fig1(a)). The difference between simulated and measured |S21| for the amplifier circuit is occurred from internal device parasitic components, which degrade the device performance more than expected(Fig1(b)). Further opimization for device-to-signal line interconnection is required to minimize deivce parasitics.



(a) (b)

Fig 1. (a)Actual peak |S21| for a single amplifier assumed to be about -0.75dB by comparing single(solid) and 5-stage(cross) amplifier. (b)Device layout including device-to-signal interconnection structure and its MAG measurement results from different die chips(bold) with simulated one(dashed).

[1] S.T Nicolson et al., “A 1.2V, 140GHz Receiver with on-die antenna in 65nm CMOS”, in proc. IEEE RFIC Symp., May 2008, pp.229-232

Low Area / Power Viterbi Decoder Enabled by Logic Compatible eDRAM

Woong Choi, Gyuseong Kang and Jongsun Park
School of Electrical Engineering, Korea University, *Seoul 136-713, Korea*
E-mail : peregrinus@korea.ac.kr

Viterbi decoder is one of the most widely used component in digital communications and storage devices. Although several in-depth studies of its VLSI implementation are carried out over the last decades, scope of embedded memory is excluded from those previous works [1]. In the Viterbi decoder design, SRAMs occupy large fraction of chip area and play a crucial role in power consumption. Accordingly, to reduce the area and power consumption of Viterbi decoder, we focus on the scope of embedded memory with two point of views. First, the gain cell based embedded DRAM (eDRAM) [2] is exploited to substitute the conventional SRAM. Second, the Viterbi-specific memory architecture is also addressed to further reduce its unnecessary overhead. By replacing the SRAM with application-specific eDRAM as embedded memories of Viterbi decoder, the chip area and power consumption can be reduced 28% and 52%, respectively.

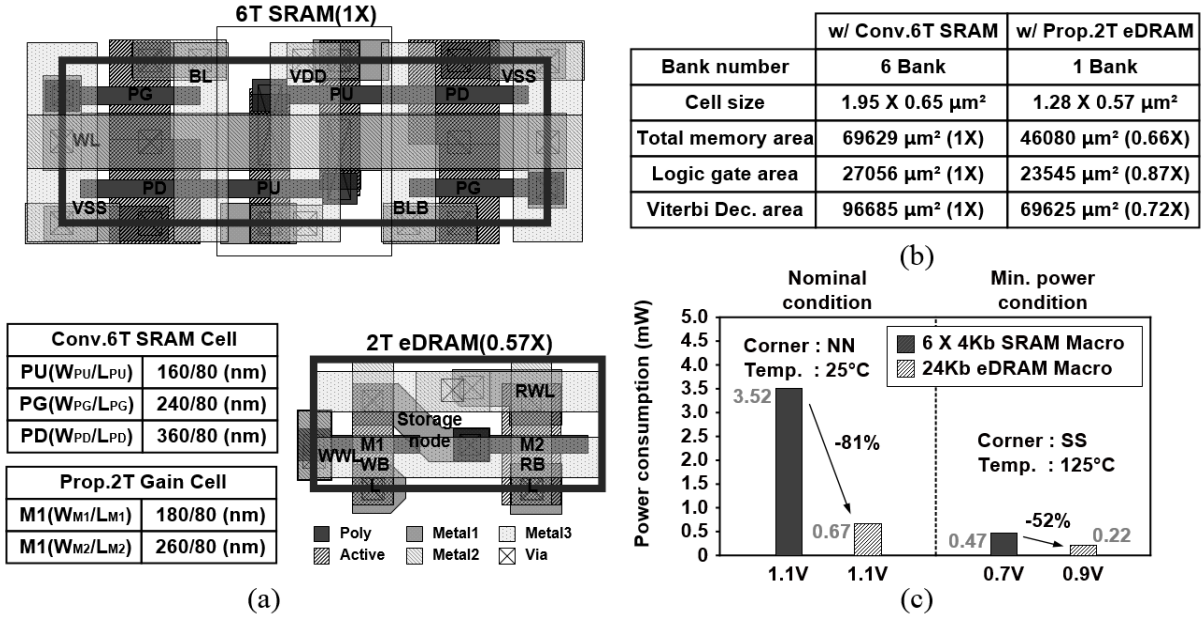


Fig. 1. (a) Bit-cell layout. (b) Area comparison. (c) Power comparison

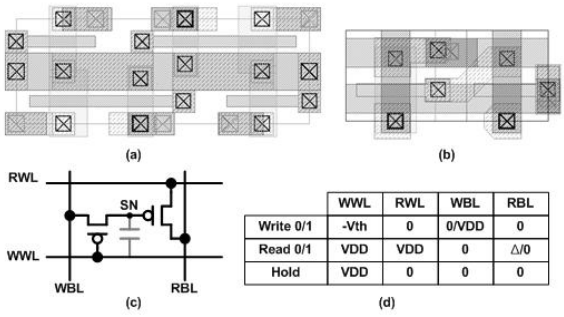
[1] I. Habib et al., "Design Space Exploration of Hard-Decision Viterbi Decoding: Algorithm and VLSI Implementation", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol 18, no. 5, pp 794–807, 2010.

[2] D. Somasekhar et al., "2 GHz 2 Mb 2T Gain Cell Memory Macro With 128 GBytes/sec Bandwidth in a 65 nm Logic Process Technology", IEEE Journal of Solid-State Circuits, vol 44, no. 1, pp 174–185, 2009.

Low Area FFT Processor with Logic Compatible Embedded DRAM

Gyuseong Kang, Woong Choi, and Jongsun Park
School of Electrical Engineering, Korea University, *Seoul 136-713, Korea*
E-mail : ntmouse@korea.ac.kr

Orthogonal frequency division multiplexing (OFDM) system is one of the popular schemes for digital communication due to high spectral efficiency and robustness against multi-path fading channel. In OFDM, fast Fourier transform (FFT) is essential function block for modulating or demodulating sub-carriers which are orthogonal to each other. In FFT processor, embedded memories and complex multipliers occupy more than 50% area and power dissipation [1]. In order to reduce power and area, many FFT architectures and algorithms are researched to optimize computation. But there are few improvements for memory. For optimal FFT memory design, we replace SRAM with embedded dynamic memory (eDRAM) which is based on gain-cell and can be implemented with common logic block unlike conventional 1T1C DRAM [2]. eDRAM has smaller cell size and less static power dissipation than SRAM but the data is available only within retention time.



	WWL	RWL	WBL	RBL
Write 0/1	-Vth	0	0/VDD	0
Read 0/1	VDD	VDD	0	△/0
Hold	VDD	0	0	0

	FFT w. SRAM	*FFT w. eDRAM*
No. of Cell Tr	6	2
Cell size	4.32um^2	1.88um^2
Overall FFT area	0.325mm^2	0.178mm^2

Fig 1. (a) 6T SRAM layout (b) 2T eDRAM layout (c) 2T eDRAM diagram
(d) 2T eDRAM voltage characteristic (e) Chip Result (f) FFT with 2T eDRAM layout

[1] Y.-W. Lin et al., "A dynamic scaling FFT processor for DVB-T applications", *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2005-2013, Nov. 2004.
[2] D. Somasekhar et al., "2 GHz 2 Mb 2T Gain Cell Memory Macro With 128 GBytes/sec Bandwidth in a 65 nm Logic Process Technology", *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 174-185, Jan. 2009.

Varification of Low Power and Ultra High Speed On-Chip CMOS Temperature Sensor

Jiwoong Jang, Jinse Kim, Reum Oh, Man Young Sung
Department of Electrical Engineering, Korea University, Seoul 136-713, Korea
E-mail : semicad@korea.ac.kr

Recently, the degree of integration of IC increases the heat generated per unit chip area has increased. So the on-chip CMOS temperature sensors have been proposed due to low standby current, the small overhead chip size and fast sensing time[1]. But the conventional on-chip CMOS temperature sensors have needed a current or voltage bias circuit which is complex to design and needs large power consumption in need of standby current. Therefore, this paper presents low power and ultra high speed on-chip temperature sensor only using two ring-oscillators which have different channel length, counters and TDC(time to digital converter). The inverter with the long channel length has a large delay variation. In the contrast, the inverter with the short channel length has a small delay variation[2]. The proposed temperature sensor is designed using dong-bu 0.11μm CMOS process and has 70bits digital output code. Effective resolution was 1.43℃ from 0℃ to 100℃ and its chip area was only 0.035mm^2. Test board is measured from 30℃ to 60℃. Power consumption is 30μW and sensing speed is 800Ksamples/s at 1.2V operation voltage in operation temperature.

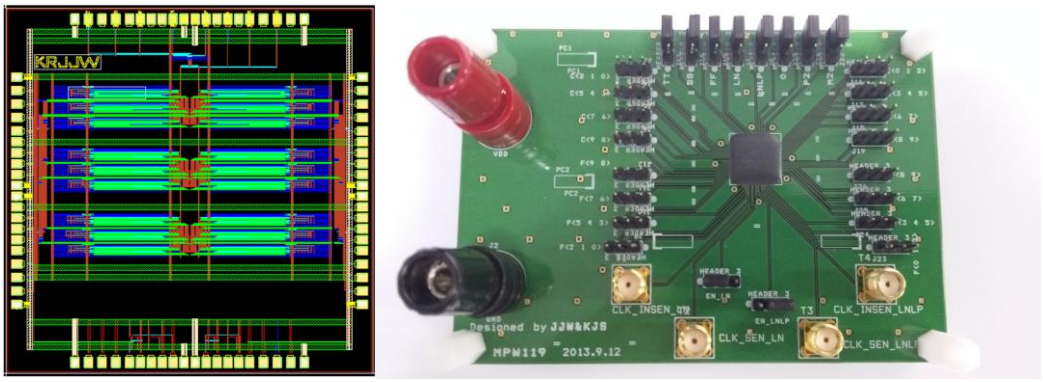


Fig 1. Figure of the full chip Layout and the test board.

[1] Poki Chen, C.-C, Chen, C.-C. Tsai, and W.F. Lu, "A time to digital converter based CMOS smart temperature sensor", IEEE J. Solid State Circuits, Vol. 40, no. 8, pp. 1642-1648, Aug. 2005.
[2] Jiwoong Jang, Jinse Kim, Reum Oh, Man Young Sung, "All digital on-chip temperature sensor using dual ring-oscillators", 20th ICECS 2013, pp. 12, 2013.

A 6-Level Signaling Driver for High Speed Interface

Tae-Hoon Lee, Seong-Ju Lee, Suki Kim

School of electrical engineering

Korea University

llth123@korea.ac.kr, _korea_@korea.ac.kr, skim@korea.ac.kr

Inter Symbol Interference (ISI) caused by non-linear frequency response of a channel, is a huge problem in a high speed transmission, that damage signal integrity. So equalization technique is needed to compensate ISI. However speed of transmission and process technology make limit to equalization. In this situation, multi level signaling can be solution. In this paper, 6-level signaling driver is suggested.

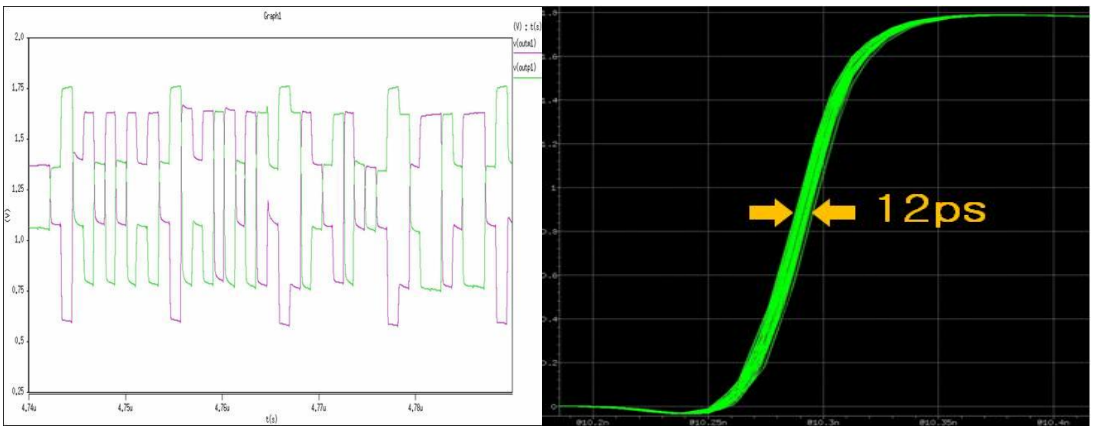


Fig 1. Simulated output of interface

[1] Behzad Razavi, Design of Analog CMOS Intergrated Circuits, McGRAW-Hill, pp.109, pp. 506, 2001.

[2] David Lee et. Al, " A VLSI Controller for Active-Matrix LCDs'"in *Proc. Int. Solid-State Circuits Conference Dig. Tech. Paper*, Feb.1994, pp. 156-157

Acknowlegement : This work was supported by IDEC

Design of a successive approximation registered ADC with a modified capacitor switching method

Jung-Min Lee, and Jong-In Song
School of Information and Communications, Gwangju Institute of Science and Technology (GIST),
1 Oryong-dong, Buk-gu, Gwangju, Republic of Korea 500-712
Email: jisong@gist.ac.kr

A current-to-voltage converter and a successive approximation registered (SAR) analog-to-digital converter (ADC) with a modified capacitor switching method for touch sensor applications are presented. In graphene touch sensor using piezoelectric effects, current of graphene patterns is proportional to the touch pressure applied to the piezoelectric material. Therefore, current-to-voltage converter and analog-to-digital converter to detect and quantize current magnitude are needed. The current-to-voltage converter, implemented using a current mirror, has wide input range and good linearity. The SAR ADC showed an average switching energy smaller that of SAR ADCs that use the conventional switching process by 75%. The SAR ADC has 8-bit resolution and 200-kHz detection speed. The measured spurious free dynamic range (SFDR) was 55.30-dB and signal to noise and distortion ratio (SNDR) was 44.73-dB at the input frequency of 10.32-kHz. The circuit was designed by Cadence Spectre simulation and fabricated by the Hynix Magnachip 0.18 μm CMOS technology. The power consumption is 0.58 mW at 1.8V dc supply. Total area is 0.296 mm^2.

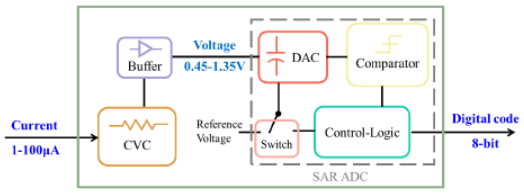


Fig. 1 Schematic block diagram of the CVC and SAR for touch sensor applications

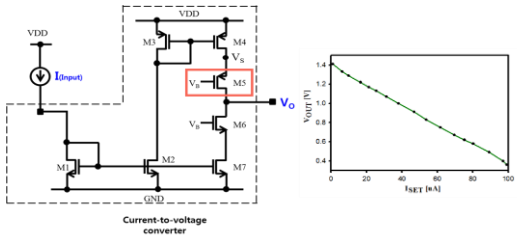


Fig.2 Circuit diagram of current-to-voltage converter

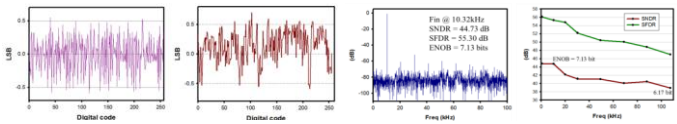
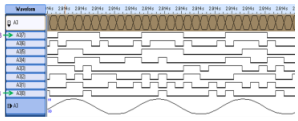


Fig.3 Measurement result of SAR ADC



	Simulation	Measurement
0.49V	01000101	01000110
0.91V	10000001	10000000
1.3V	10111001	10111000

Fig.4 The PCB board for testing chip and transient result of SAR ADC

[6] D. Draxelmayr.”A 6b 600MHz 10mW ADC array in digital 90nm CMOS,” in IEEE ISSC Dig. Tech. Papers, Feb. 2004, p. 264-527.

[7] J.H.Park, C.K.Hagn, and H.D. Yoon,”Implementation of Current-to-Voltage Converter with Wide Dynamic Range and Its Applicaiont,”in SoC Design Conference (ISOCC), 2009, pp.500-503.

[8] J. Park, H.-J. Park, J.-W.Kim, S.Seo, and P.Chung,”A 1mW 10-bit 500KSps SAR A/D Converter,”in Proc. 2000 IEEE Int. Symp. Circuits and Systems, 2000, vol. 5, 2000, pp. 581-584.] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, Nat. Nanotechnol. 6, 147 (2011).

A Chopper-Stablized Current-Feedback Instrumentation Amplifier with a Tunable Gain and Low-cutoff Frequency for EEG Acquisition Applications

Chung-Jae Lee, and Jong-In Song
School of Information and Communications, Gwangju Institute of Science and Technology (GIST),
1 Oryong-dong, Buk-gu, Gwangju, Republic of Korea 500-712
Email: jisong@gist.ac.kr

A chopper-stabilized current-feedback instrumentation amplifier (CFIA) for EEG acquisition applications is presented. The proposed design includes an AC-coupled CFIA and a switched-capacitor (SC) integrator. By using an appropriate chopper modulation technique in both input and output stages of the CFIA, 1/f noise is reduced. An input-referred noise power spectral density (PSD) of 60 nV/√Hz is obtained. The SC integrator was employed to control the low cutoff frequency of the CFIA by adjusting the sampling frequency of the SC integrator. Simulation results show that the proposed amplifier provides a common mode rejection ratio (CMRR) of 111 dB. The low cutoff frequency was determined within a range from mHz to a few Hz depending on the switching frequency of the SC integrator and the high cutoff frequency was approximately 600 Hz. The total power dissipation of the CFIA was 2.35 µW. The proposed design was simulated with the Samsung 0.13 µm standard CMOS process.

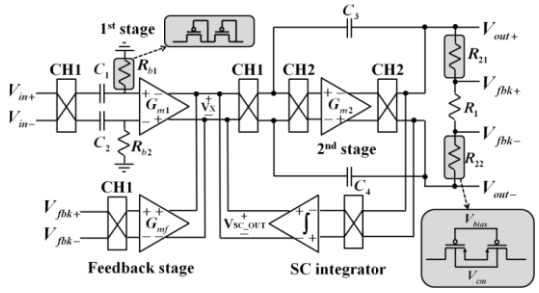


Fig.1 Circuit diagram of the designed amplifier

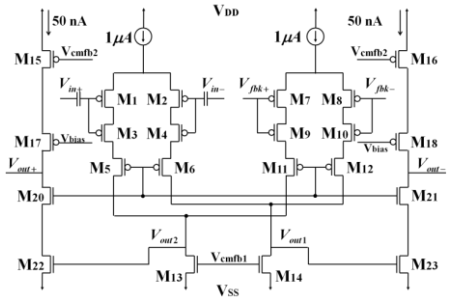


Fig.2 Schematic of the 1st, feedback, and 2nd stages

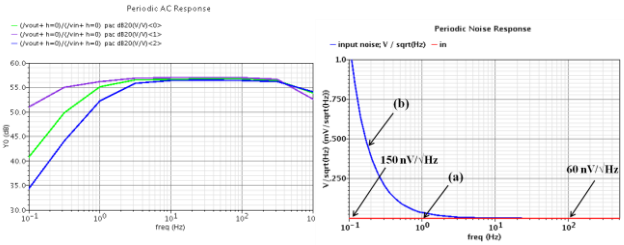


Fig.3 (a) Simulated PAC analysis of the amplifier showing tunable low cutoff frequency, (b) Pnoise analysis with chopping and without chopping

Table 1: Summary of amplifier performance

	This work	[6]	[7]	[9]
Year	2012	2011	2007	2008
Gain (dB)	36-57	65	41	48
Low cutoff frequency (Hz)	Tunable	0.25	Tunable	0.5
High cutoff frequency (Hz)	600	1.1 k	120	Tunable
Input noise PSD (nV/√Hz)	60 (at 100 Hz)	51	100 (at 100 Hz)	53-57 (at 100 Hz)
Input referred noise(µV)	0.61 (0.1-100Hz)	0.73 (0.1-100Hz)	0.98 (0.05-100Hz)	0.59 (0.5-100Hz)
Supply current (µA)	2.35	2.65 (CFIA) / 3.45 (total)	1.1	2.3
Supply voltage (V)	1	1	1.8	3

Rong Wu, K. A. A. Makinwa, J. H. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1mHz 1/*f* noise corner and an AC-coupled ripple-reduction loop," . IEEE J. Solid-State Circuits, vol.44, no.12, pp.3232-3243, Dec. 2009.

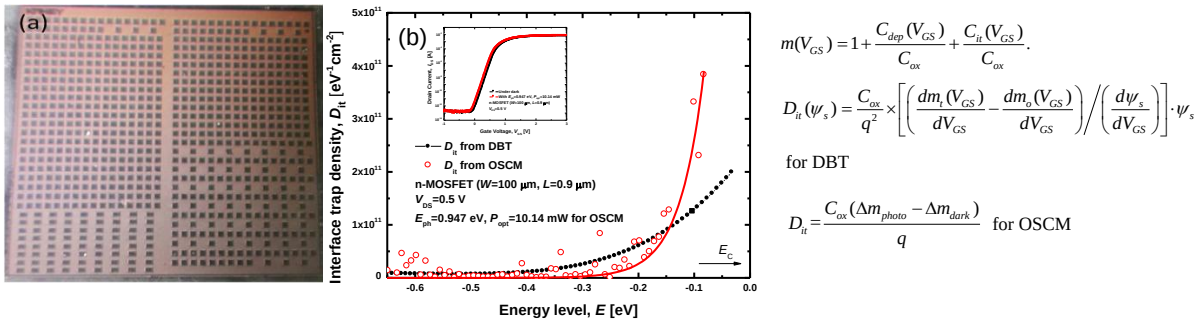
J. F. Witte, J. H. Huijsing, K. Makinwa, "A current-feedback instrumentation amplifier with 5 µW offset for bidirectional high-side current sensing," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2769-2775, Dec. 2008.

R. R. Harrison, and C. A. Charles, "A low-power low-noise CMOS amplifierf for neural recording applications," IEEE J. Solid-State Circuits, vol. 38, no. 9, pp. 958-965, June 2003.

Characterization of Interface States based on the Sub-bandgap Photonic Subthreshold Current in MOSFETs

Jungmin Lee, Jun Seok Hwang, Jaeyeop Ahn, Hyunjun Choi,
Hagyoul Bae, Sungwoo Jun, Jinsu Yoon, Sung-Jin Choi, Dae Hwan Kim and Dong Myong Kim
School of Electrical Engineering, Kookmin University, Seoul 136-702, South Korea
E-mail : dmkim@kookmin.ac.kr

With the scaling down of metal-oxide-semiconductor field-effect transistors (MOSFETs) for higher performance and higher integration density, the interface state density (D_{it}) become one of the most important issues. Therefore, it is necessary to characterize the energy distribution of D_{it} over the energy band-gap ($E_V<E<E_C$) for improvement of the reliability and the performance of devices. For accurate extraction of D_{it}, we employed the differential body factor technique (DBT) and optical subthreshold current method (OSCM) [1]-[2]. Through these methods, we confirmed the energy distribution of D_{it} near the conduction band in n-channel MOSFETs. For extraction of D_{it}, we applied to n-channel MOSFET with $N_A=1\times10^{17}$ [cm^{-3}], t_{ox}=3.9 [nm] and $W \times L=100 \times 0.9$ [μm^2]. Also, we employed an optical source with E_{ph}=0.947 [eV], $\underline{P}_{opt}$=10.14 [mW] for a sub-bandgap photonic excitation. As shown in Fig.1, the energy distribution of D_{it} near the conduction band was experimentally obtained to be $D_{it}=10^{10}\sim10^{11}$ [$cm^{-2}eV^{-1}$].



$$m(V_{GS}) = 1 + \frac{C_{dep}(V_{GS})}{C_{ox}} + \frac{C_{it}(V_{GS})}{C_{ox}}.$$

$$D_{it}(\psi_s) = \frac{C_{ox}}{q^2} \times \left[\left(\frac{dm_t(V_{GS})}{dV_{GS}} - \frac{dm_o(V_{GS})}{dV_{GS}} \right) \Big/ \left(\frac{d\psi_s}{dV_{GS}} \right) \right] \cdot \psi_s$$

for DBT

$$D_{it} = \frac{C_{ox}(\Delta m_{photo} - \Delta m_{dark})}{q}$$ for OSCM

Fig.1 (a) n-channel MOSFET device used for experiment. (b) The distribution of D_{it} obtained from DBT and OSCM for n-channel MOSFET with $W \times L = 100 \times 0.9$ [μm^2].

This work was supported by the IDEC.

[1] D. Yun, etc., *IEEE Electron Device Lett.*, 1206-1208 (2011).
[2] M. S. Kim, etc., *IEEE Electron Device Lett.*, 101–103 (2004).

Oscillation RF-DC Converter for Wireless Energy Harvesting

Jihoon Lee, Wonjae Jung, Hyobin Jung, Yoonjae Nam, Donggyun Yoo, Yongki hur and Junseok Park
School of Electronical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : cz8700@kookmin.ac.kr

Recently, increase effort to IT devices charging by wireless power transmission and harvesting. Especially, microwave energy transmission and harvesting techniquies is studied for increase distance of energy transmission. These microwave energy harvester consist of rf-dc converter, super-capacitor and dc-dc converter[1]. The greater part of these studies are development of low power dc-dc converter for improve dc-dc conversion efficiency[2]. Using 915MHz, 3W microwave energy transmitter, energy harvester accept -15dBm(159mVp-p) at 15m distance. Input power is too low to charging the super-capacitor and have long charging time. In this paper, rf-dc converter with L, C oscillation impedance matching circuit for high voltage to charging super-capacitor. Two main rectifier is used for proof proposed concept, one is one stage ring rectifier and the other is 2stage villard rectifier. When super-capacitor charged to 1.8V, dc-dc converter into active mode. Proposed rf-dc converter output voltage is about 6.4V at 1k ohm load of villard rectifier, 5V at 1k ohm load of ring rectifier. The rang of input power for charging super-capacitor at 1.8V is -16dBm to 20dBm. And rf-dc conversion efficiency is about 95.5% at 10dBm inputed.

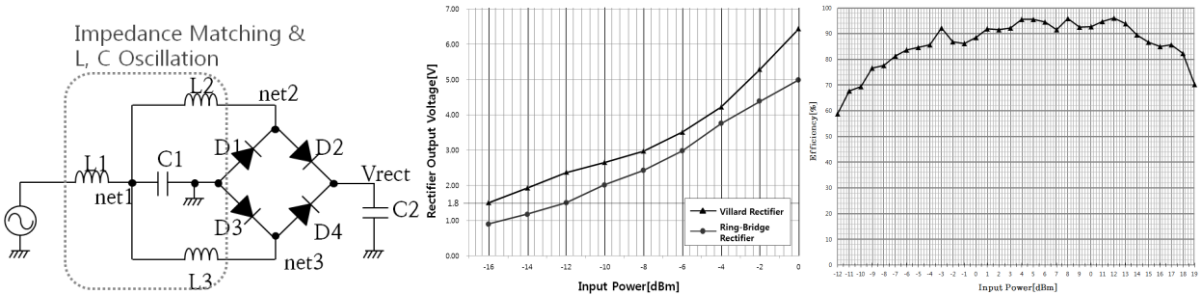


Fig 1. L, C oscillation rectifier and output voltage and efficiency of rf-dc converter

[1] Yuan Rao, “An Input-Powered Vibrational Energy Harvesting Interface Circuit With Zero Standby Power”, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 26, NO. 12, pp. 3524-3533, 2011
[2] Yuan Rao and David P.Arnold, "Input-Powered Active AC/DC Converter with Zero Standby Power for Energy Harvesting Applications", Power Electronics, IEEE Transactions on Vol.26, Issue 12, pp 635-3533, 2011.12

An Active Switching DC-DC Converter for wireless energy harvester

Jihoon Lee, Wonjae Jung, Hyobin Jung, Snaggu Yoon, Donggyun Yoo, Yongki Hur and Junseok Park
School of Electronical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : cz8700@kookmin.ac.kr

For a few decades, various techniques have been studied for wireless energy harvesting. This paper aims to develop a los power dc-dc converter with active switch for improve conversion efficiency of rf energy harvesting techniques. Rf energy harvester consist of rf-dc converter, super-capacitor and dc-dc converter[1-2]. Once super-capacitor charged enough to operate dc-dc converter, generated enable signal and dc-dc converter into active mode. Proposed dc-dc converter consist of low power oscillstor, boosting switch, active switch, and storage-capacitor. Low power oscillator using triangular wave form and compare with reference voltage. Oscillator turned on and off boosting switch. Boosting voltage rectified by diode and charging the storage-capacitor. When storage-capacitor charged to 3.8V active switch is turned on. Otherwise dis-charged to 3.6V active switch turened off. Oscillator using triangular wave current consumption is 2uA at active mode. And active switch current consumption is 0.9uA. In this paper, active switching dc-dc converter was fabricated in a Magnahynix 0.18um CMOS process. Input voltage range is 0.8V to 1.8V and output range is 3.0V to 5.8V. Conversion efficiency is about 90.8% at 50mA load current.

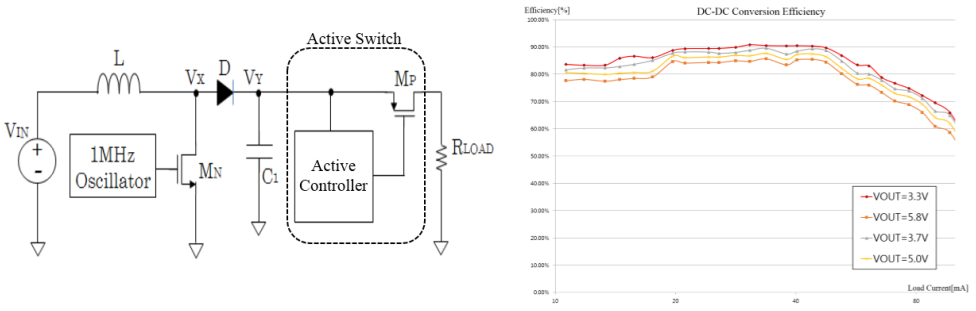


Fig 1. Active switching dc-dc converter and conversion efficiency

[1] Yuan Rao, “An Input-Powered Vibrational Energy Harvesting Interface Circuit With Zero Standby Power”, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 26, NO. 12, pp. 3524-3533, 2011

[2] Yuan Rao and David P.Arnold, "Input-Powered Active AC/DC Converter with Zero Standby Power for Energy Harvesting Applications", Power Electronics, IEEE Transactions on Vol.26, Issue 12, pp 635-3533, 2011.12

A Design of High Efficiency Microwave Wireless Power Acceptor IC

Jihoon Lee, Wonjae Jung, Hyobin Jung, Anggu Yoon, Yoonjae Nam, Yongki hur and Junseok Park
School of Electronical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : cz8700@kookmin.ac.kr

Wireless power transmission technology has been studied variety. Recently, wireless power transmission technology used by resonance and magnetic induction field is applied to various fields. However, magnetic resonance and inductive coupling are have drawbacks - power transmission distance is short. Microwave transmission and accept techniques have been developed to overcome short distance. However, improvement in efficiency is required. This paper, propose a high-efficiency microwave energy acceptor IC(EAIC). Suggested EAIC is consists of RF-DC converter and DC-DC converter[1][2]. Wide Input power range is -15 dBm ~ 20 dBm. And output voltage is boosted up to 5.5 V by voltage boost-up circuit. EAIC can keep the output voltage constant. Available efficiency of RF-DC converter is 95.5 % at 4 dBm input. And DC-DC efficiency is 94.79 % at 1.1 mA load current. Fully EAIC efficiency is 90.5 %.

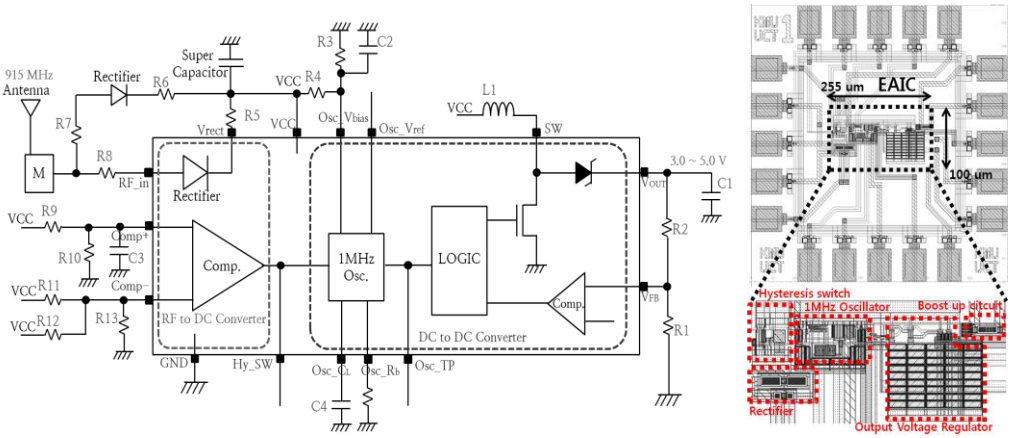


Fig 1. Energy acceptor block diagram and layout

[1] Yuan Rao and David P.Arnold, "Input-Powered Active AC/DC Converter with Zero Standby Power for Energy Harvesting Applications", Power Electronics, IEEE Transactions on Vol.26, Issue 12, pp 635-3533, 2011.12

[2] Yuan Rao, “An Input-Powered Vibrational Energy Harvesting Interface Circuit With Zero Standby Power”, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 26, NO. 12, pp. 3524-3533, 2011

A Design of Up-Down Converter for WCDMA Repeater

Hyo-Bin Jung, Won-Jae Jung, Sang-Kyu Kim, Se-Mi Lim, Ji-Hoon Lee, Kyu-Hyun Nam, Jun-Seok Park

School of Electrical Engineering, Kookmin University, Seou , Korea

E-mail : epicjung@kookmin.ac.kr

This paper is proposed Up/Down converter at SKT BAND5(Up RF 1950MHz, Down RF 2140MHz) band and fabricated in SiGe 0.18um technology. Proposed Up/Down converter can be adoptable to all WCDMA service in Korea. Up converter consist of active double balanced mixer, buffer, PTAT and LO buffer and down converter consist of semi-active type double balanced mixer and LO buffer, mixer buffer.[1] Apply for multi-band, off-chip matching circuit is implemented. In this paper, supply voltage is 3.3V, down converting mixer have low gain, and designed semi-active type mixer because of higher linearity than active mixer.[2] 1950MHz up converting gain is 12.5dB, OIP3 is 21dBm at -6.5dBm output. 2140MHz up converting gain is 14.5dB, OIP3 is 35dBm at 5.5dBm output. LO input is 2070MHz for up 120MHz, down 70MHz.

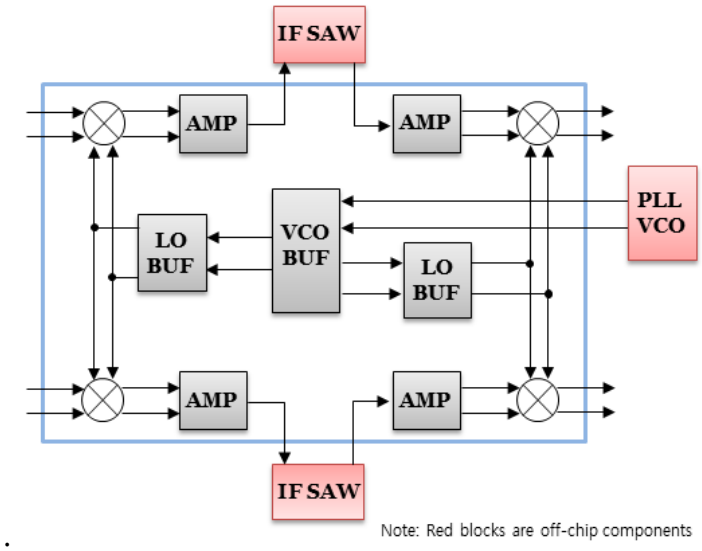


Fig 1. WCDMA Repeater System block diagram

[1] Behzad Razavi, “RF Microelectronics” 1997

[2] Joohwa Kim, James F. Buckwalter “ Straggered gain for 100+ GHz Broadband Amplifier”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL.46, NO.5, MAY 2011

A Design of Transceiver for Advanced UHF band RFID Reader

Hyo-Bin Jung, Won-Jae Jung, Sang-Kyu Kim, Se-Mi Lim, Ji-Hoon Lee, Kyu-Hyun Nam, Jun-Seok Park

School of Electrical Engineering, Kookmin University, Seou , Korea

E-mail : epicjung@kookmin.ac.kr

A Fully integrated UHF Band Direct-Conversion transceiver for mobile RFID system is presented. A direct-conversion UHF Band transceiver for international RFID Standards(ISO18000-6 Type B and C, and EPC Golbal C1 Gen2).[1] The transceiver consists of a low noise amplifier, a down-conversion mixer, a band pass filter, and programmable gain amplifier (PGA) for RX path; and a power amplifier, an up-conversion mixer, a low-pass filter, and a PGA for TX path. In addition, the fractional N PLL is integrated to cover different frequency standards for different nations. The transceiver meets the dense reader environment specifications.[2] Power consumption is about 90mA@1.3V.

This transceiver is developed with a 0.13um technology for UHF band RFID Reader system.

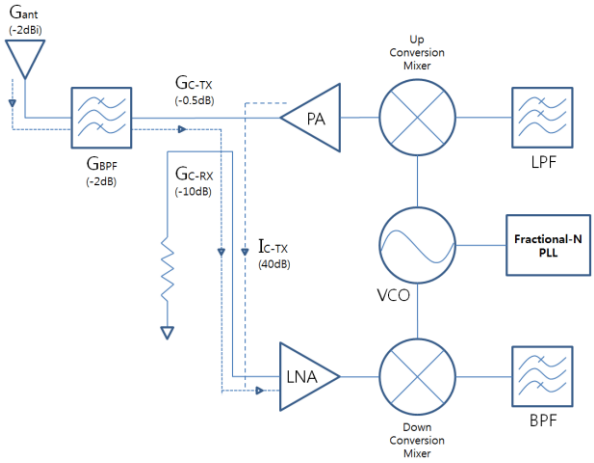


Fig 1. UHF Band RFID Reader Block Diagram

[1] EPC global EPCTM Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860MHz~960MHz Version 1.0.7

[2] Scott Chiu, Issy Kipnis, Marc Lyer, Jan Rapp, David Westberg, Jonas Johansson, peter Johansson “A 900MHz UHF RFID Reader Transceiver IC, ISSCC, vol.42, no.12(2007)

16-channel LED Driver IC for Full-Color LED Display

Hyobin Jung, Wonjae Jung, Sanggu Yoon, Yoonjae Nam, Donggyun Yoo and Jun-Seok Park
School of Electronical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : epicjung@kookmin.ac.kr

This paper proposes the 16-channel LED Driver IC for Full color LED display system. The proposed LED driver IC in this paper can flow independent current of temperature and supply voltage in each channel. [1] Current flow in the channel can be configurable via an external resistor. LED brightness is adjusted to 12-bit PWM(Pulse Width Modulation) and 8-bit DC(Dot Correction). [2]A real-time monitoring of IC temperature (130℃/150℃) and LED status (open/short) is provided by LED driver IC and the user can receive warning and get information on problems. A 16-channel LED driver IC is produced using 0.35 um BCD process and the size is 2.5mm x 2.5mm. In this paper, channel current characteristic and channel current control function were measured in order to verify a embodied 16-channel LED driver IC by producing a single IC test board.

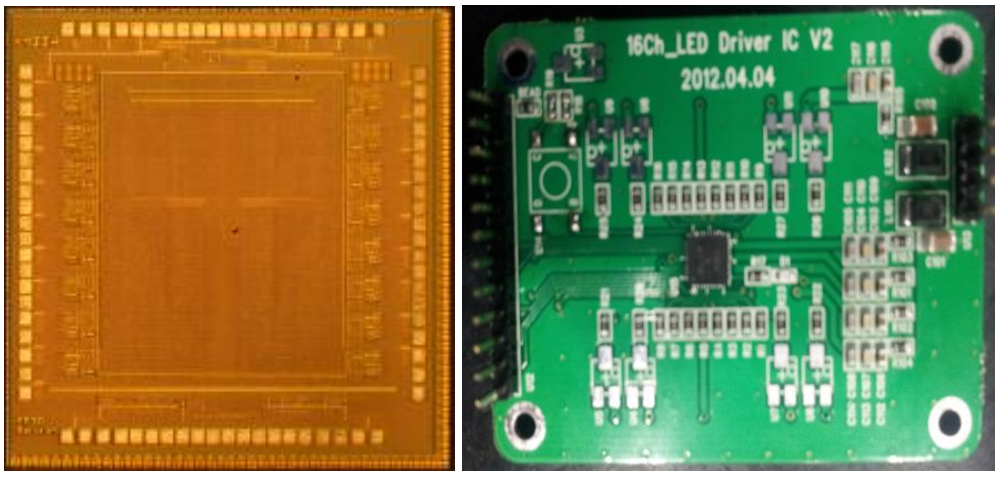


Fig 1. 16-channel LED Driver IC and Test board

[1] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", MCGrawHill, pp. 246-290, 2001
[2] M. Day and T. Saab, "TLC5940 dot correction compensates for variations in LED brightness", Analog Applications Journal, pp. 21-24, 2005.

A Design of Wideband Programmable Gain Amplifier(PGA) for LTE Repeater System

Hyo-Bin Jung, Jun-Seok Park
School of Electrical Engineering, Kookmin University, Seoul , Korea
E-mail : epicjung@kookmin.ac.kr

A programmable gain amplifier (PGA) is fabricated a 0.18um technology for LTE Repeater System. Proposed PGA consist of three stage; PGA1, PGA2 and PGA3. Each gain of PGA1 stage is 0/7/12, 0/3/6, 0/1/2dB, overall PGA gain is 20dB and each gain controlled by 6-bit SPI(Serial Parallar Interface) control. Gain step is made by collector and emitter resistance ratio of common emitter structure. PGA current is controlled by PTAT. Especially, BJT base current controlled by variation of beta of BJT using off-chip dc bias circuit. Each three PGA stage current consumption is about 25mA and total current consumption is about 75mA at 3.3V supply voltage. Resolution of PGA gain is 1dB step. Post layout simulation and measurement have similar result. Noise figure of PGA is 6.78dB at maximum gain, 17.67dB at minimum gain. Gain flatness of PGA improved 0.5dB at 20MHz to 150MHz band by connect MIM capacitor at negative and positive of each gain step.

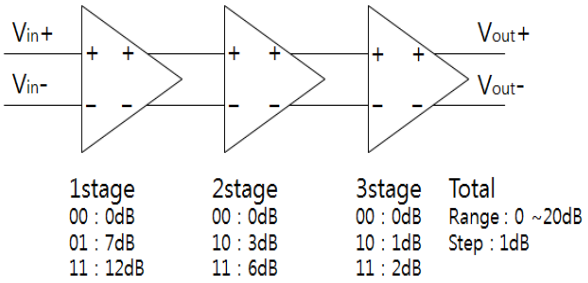


Fig 1. PGA Gain step and Block

[1] Joohwa Kim, James F. Buckwalter " Straggered gain for 100+ GHz Broadband Amplicifer", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL.46, NO.5, MAY 2011
[2] Calvo B, Sanz M.T, Celma S, "Low=voltage low-power CMOS Programmable Gain Amplifier" ICCDCS.2006

A 10-bit 10-MS/s Asynchronous Successive Approximation Register ADC using MOM Capacitive DAC

Yeon-Ho Jeong, Sang-Min Park, and Young-Chan Jang
Department of Electronic Engineering, Kumoh National Institute of Technology, Gumi 730-701, Korea
E-mail : ycjang@kumoh.ac.kr

Recently, asynchronous successive approximation register (SAR) analog-to-digital converters (ADCs) with the feature of low power consumption have become popular for mobile applications and display applications as an alternative to the pipelined ADCs[1-2]. In this paper, a 10-bit 10-MS/s asynchronous SAR ADC with a digital-to-analog converter (DAC) using a metal-oxide-metal (MOM) capacitor is proposed. The designed asynchronous SAR ADC with a rail-to-rail input range consists of a SAR logic, a comparator, and a DAC using a MOM capacitor, as shown in Fig 1. The settling time of the DAC is critical in the total conversion time of the asynchronous SAR ADC which is determined by the delay time of the DAC, comparator, and SAR logic. In this work, the DAC is implemented by using a MOM capacitor to reduce the input capacitor load and the settling time. Actually, the MOM capacitor is implemented by using a metal 4 in the process with 6 metal layers. Fig 2 shows the chip photograph of the implemented ADC. The designed asynchronous SAR ADC is fabricated using a 0.18-μm CMOS process with a 1 V supply. The active area and power consumption are 0.301 mm^2 and 0.61 mW. The measured SNDR is 54.2 dB at the analog input frequency of 101.12 kHz.

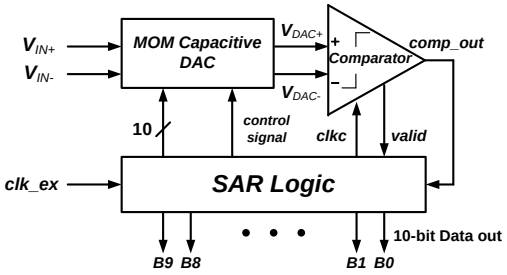


Fig 1. Architecture of asynchronous SAR ADC

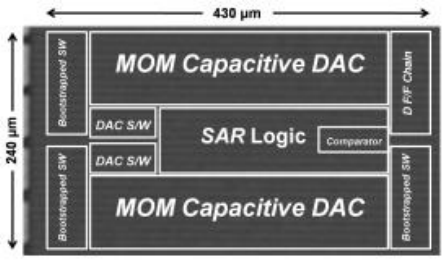


Fig 2. Chip photo

[1] S. H. Cho, J. K. Lee and S. T. Ryu, "A 550-uW 10-b 40-MS/s SAR ADC With Multistep Addition-Only Digital Error Corrections," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1881-1892, Aug., 2011.
[2] P. Harpe, C. Zhou, and X. Wang, "A 30fJ/Conversion-Step 8b 0-to-10MS/s Asynchronous SAR ADC in 90nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 388-389, Feb. 2010.

2조 동선에서 500 Mbps 이더넷 전송이 가능한 물리적 부호계층의 설계

전 성 배, 박 해 원, 정 해
금오공과대학교 전자공학과
E-mail : hchung@kumoh.ac.kr

본 논문은 4 D (Dimension) PAM-5 (Pulse Amplitude Modulation)로 전송하는 1000Base-T 를 SERDES (Serialize and De-serialize)기법을 이용해서 2 조 동선으로 500 Mbps 로 전송하는 방법을 구현한다. 이것을 500Base-T 라 하고, 500BASE-T 의 구조는 그림 1 과 같다 [1],[2]. 500Base-T 는 1000Base-T 의 계층 구조에서 RAS (Rate Adaptation Sublayer)와 S&S (SERDES and Synchronization) Sublayer 가 필요하다. RAS 와 S&S Sublayer 사이에 있는 PCS 계층은 62.5 MHz 로 동작하도록 설계하고, RAS 계층과 500Base-T PCS (Physical Coding Sublayer) 사이의 인터페이스를 0.5GMII 라 지칭한다. 본 논문에서는 500Base-T 의 PCS 와 RAS 그리고 S&S sublayer 를 구현한다. 그리고 GMII 와 0.5GMII 간의 속도차이의 문제를 해결하기 위해 FC (Flow Control)를 구현한다 [3]. 500BASE-T 는 0.13 ㎛ MPW (Multi Project Wafer)공정으로 진행되었으며, 공급 전압 3.3 V 에 최대 125 MHz 에서 동작하도록 설계되었다. 사용된 게이트 수는 78,000 개이며, RAS 의 버퍼는 '1504x10' 크기의 DPSRAM (Dual Port Static Random Access Memory)을 사용하였다. PCS 의 인코딩과 디코딩에 사용되는 테이블은 각각 '640x9'와 '512x12' 크기의 VROM (Virtual Read Only Memory)을 사용하였다.

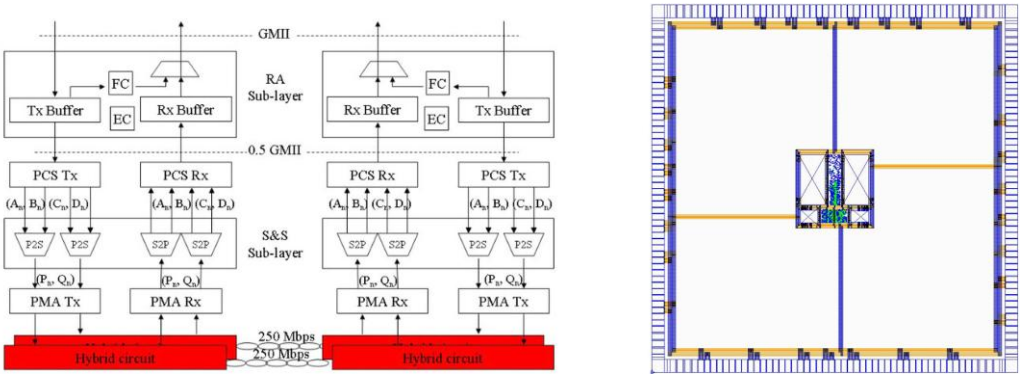


그림 4. 500BASE-T 의 구조와 layout

1.IEEE std. 802.3 Section3, "Part 3: Carrier Sense Multiple Access with Collision Detection Access Method and Physical Layer Specification," Approved 26, Dec. 2008.

2. 정해, 전성배, 김진희, 박형진, "2 조 UTP 를 이용한 500BASE-T 의 구현," 한국통신학회논문지 제 36 권 제 10 호, pp.1150-1158, 2011.

3. IEEE std. 802.3 Section 2 Annex 31B, "MAC Control Pause Operation," Approved 26, Dec. 2008.

A CMOS CONDUCTOMETRIC READOUT CIRCIT DESIGN USING SINGLE-WALL CARBON NANOTUBE SENSOR ARRAYS

JongHo Park*, Cheolhwan Lim**, Sujith S Dermal**, Sungyong Jung** and Hoon-Ju Chung*
*School of Electronic Engineering, Kumoh National Institute of Technology, Gyeongbuk 730-701, Korea
**Electrical Engineering Department, The University of Texas at Arlington, TX 76019, USA
E-mail : hjchung@kumoh.ac.kr

This study is aimed to develop a readout circuit for single-wall carbon nanotube (SWNT) sensor arrays with enhanced sensitivity, which can be used to analyze volatile organic compounds (VOCs) [1]. The reason we focus on VOCs is that even low concentration of VOCs may cause negative effects to human beings such as discomfort, irritation and disease [2]. The nanowire sensor is classified as conductometric sensor whose output is current. Besides, the SWNT sensor arrays with 16 different selectivities are adopted. For those reasons, one 4bit multiplexer and two amplifiers are utilized as shown in Figure 1. The MUX consists of 16 complementary switches and a 4:16 decoder designed with CMOS logic gates. The operational amplifiers are used for a trans-impedance amplifier (TIA) and an inverting amplifier because the output of TIA equals to -IINRF. To achieve high gain and wide output swings, a three stage OP-AMP was designed as well as to have good linearity over the input range of 1 μA to 100 μA current variation. The circuits were fabricated in 0.35 μm CMOS process. The measurement results illustrate that DC response of the readout circuit is highly linear. Also, the total power consumption is 6.07 mW. In this study, it is proved that the conductometric readout circuit with a broad input range and low power consumption can be utilized to monitoring toxic substances in the environment.

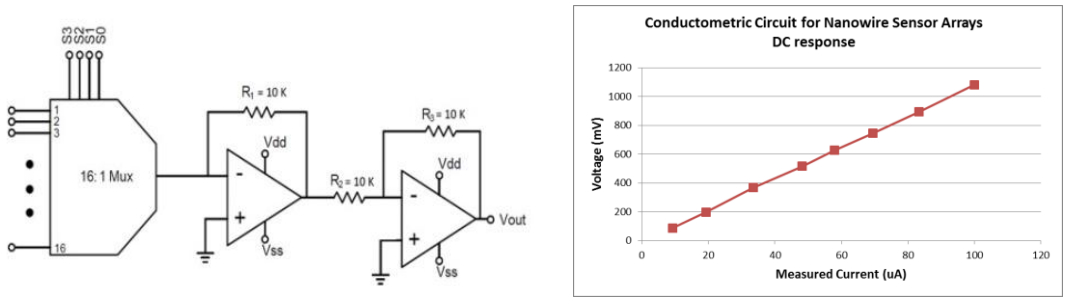


Fig 1. Readout circuit and measurement results

[1] Shirsat, M. D., Sarkar, T., Kakoullis Jr, J., Myung, N. V., Konnanath, B., Spanias, A., & Mulchandani, A., The Journal of Physical Chemistry C, 116 (5), 3845-3850 (2012).
[2] Chunrong Jia, Stuart Batterman, Christopher Godwin, Atmospheric Environment, 42 (9), 2083-2100 (2008).

On-Chip Spectral Analyzer

Woo-Hun Hong, Byeong-Ho Kang, Kyung Ki Kim
School of Electronic and Electrical Engineering, Daegu University, 712-714, Korea
E-mail : blackcat3313@live.daegu.ac.kr, kissme0905@live.daegu.ac.kr, kkkim@daegu.ac.kr

The Fast Fourier Transform (FFT) algorithm is widely used as a standard tool to carry out spectral analysis because of its computational efficiency. However, the presence of multiple tones frequently requires a fine frequency resolution to achieve sufficient accuracy, which imposes the use of a large number of FFT points that results in large area and power overheads [1][2]. In this paper, an alternative FFT method will be developed for on-chip spectral analysis of multi-tone signals with particular harmonic and intermodulation components. Figure 1 visualizes the proposed built-in calibration (BIC) approach that is the target application for the presented FFT realization. The test chip to be fabricated contains a low-noise amplifier, ADC and the FFT engine for initial characterization of the circuit blocks and measurement approach. The on-chip spectral analyzer was fabricated with CMOS 0.11μm process as shown in Fig. 2. The experimental results indicate that the chosen combination of a 10-bit ADC and a 16-point FFT in this example is suitable to accurately determine the third–order intermodulation (IM3) components of ≤ 50 dBc as shown in Fig.2.

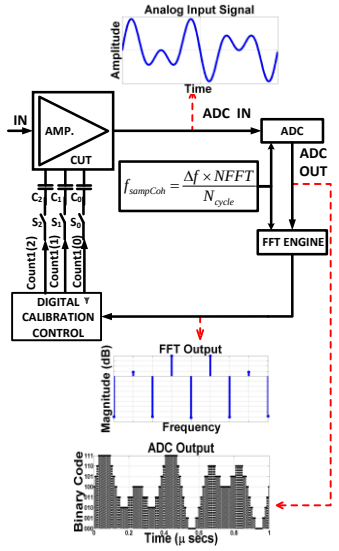
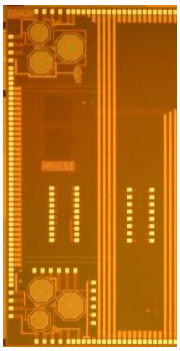
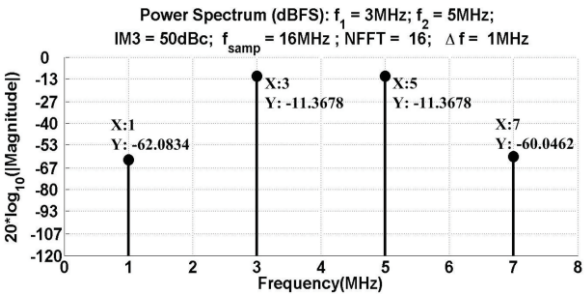


Fig 1. On-chip BIC approach with spectral testing.



(a)



(b)

Fig. 2. (a) Die photo of the CMOS neuron, (b) Output spectrum from post-layout simulation, showing the two test tones (f_1=3 MHz, f_2=5 MHz) and their IM3 products at 1 and 7 MHz.

[1] M. Onabajo, J. et. al. ,"An on-chip loopback block for RF transceiver built-in test," IEEE Trans. Circuits Syst. II, Exp., vol. 56, no. 6, pp. 444–448, Jun. 2009.

[2] H. Shin, J. Park, and J. A. Abraham, "Spectral prediction for specification-based loopback test of embedded mixed signal circuits," J. Electron. Test., vol. 26, no. 1, pp. 73–86, Jan. 2010.

An 8b 2GS/s Time-Interleaved Folding-Interpolation ADC with Self-Calibration

Donggwi Choi, Daeyun Kim and Minkyu Song

Dept. of Semiconductor Science Dongguk University, Seoul, Korea

E-mail : mksong@dongguk.edu

Nowadays, in many applications such as Radio Detecting and Ranging(Rader), communication system and signal equipment, 8-bit A/D converter(ADC) with high sampling rate are required[1]. There have been many ADC researches to meet high sampling speed operation. In this paper, an 1.2V, 8b, 2GS/s Time-Interleaved Folding-Interpolation ADC with Self-Calibration.

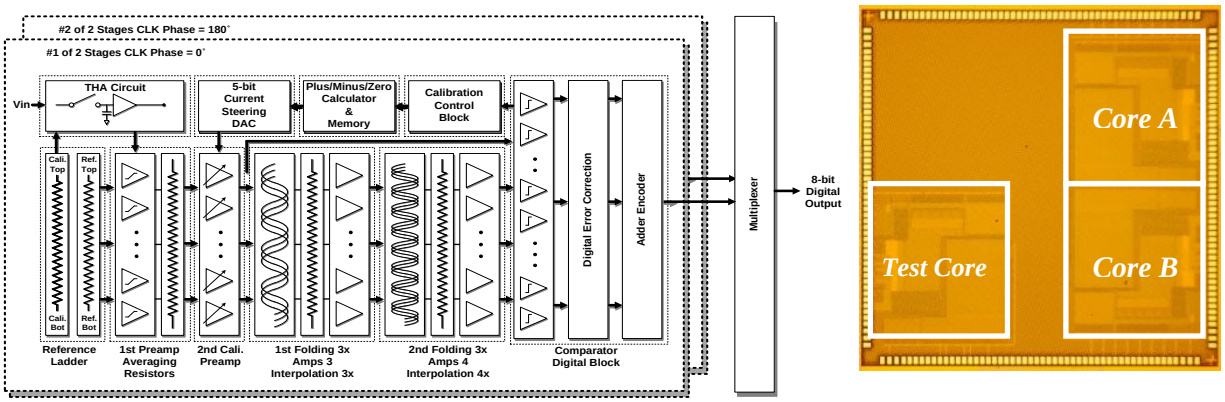


Fig.1 Architecture of the proposed A/D converter &Chip photo

The chip has been fabricated with a 1.2V 0.13um 1-poly 6-metal CMOS technology. The effective chip area is 5.78mm^2 and power dissipates about 900mW including calibration engine at 1.2V power supply. Fig.1 shows Block diagram and chip photo. The Post-Layout Simulation Result of ENOB(effective number of bit) is 6.3bit and SNDR is 39.67dB. In this test, fin=500MHz and fs=2GHz.

ACKNOWLEDGMENT

This work was supported by the IC Design Education Center (IDEC).

[1] 17th IEEE International Conferenceon,pp.110-113,201 C. C. Hsu *et al.*, “An 11-b 800-MS/s time-interleaved ADC with digital background calibration,” in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2007,pp. 464–465, (also Slide Supplement).

A CMOS Image Sensor based on a Cyclic ADC with a Digital Logarithmic Counter

Kyungtae Kim, Daeyun Kim and Minkyu Song
Department of Semiconductor Science, Dongguk University, Seoul, Korea
E-mail : mksong@dongguk.edu

Nowadays, CMOS Image Sensor (CIS) is used in camera phone, surveillance camera, medical applications and system of automobile. So CIS become a part of our daily life. Recently, as demand of CIS had merits of low power, inexpensive production cost, small area and high conversion speed is being increased in the IT market, market of CIS is becoming larger than Charge-Coupled Device (CCD). Conventionally, Single Slope ADC (SS-ADC) is used in CIS so as to convert analog signal to digital data [1]. But the higher resolution is, the longer A/D conversion time of CIS based on SS-ADC is considerably. Thus, in this paper, CIS based on Cyclic ADC had high A/D conversion time in the high resolution is proposed. Picture of the chip is Fig. 1. In this paper, proposed CIS based on Cyclic ADC will improve that conventional CIS based on SS-ADC that has demerit of low A/D conversion time in the high resolution. So in high resolution, CIS based on Cyclic ADC that had high A/D conversion time will be used in many applications with image sensor [2].

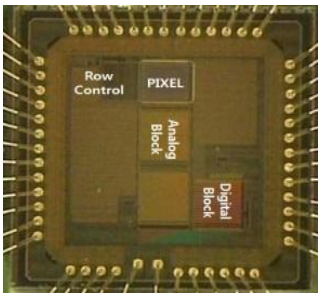


Fig. 1 Photograph of the proposed CIS

ACKNOWLEDGMENT

This work was supported by the IC Design Education Center(IDEC)

[1] Nayeon Cho, et al., "A VGA CMOS Image Sensor with 11-bit column parallel single-slope ADCs" Soc Design Conference(ISOCC), 2010 International, pp. 25-27, 22-23 Nov. 2010.

[2] Kazuya Kitamura, et al., "A 33-Megapixel 120-Frames-Per-Second 2.5-Watt CMOS Image Sensor With Column-Parallel Two-Stage Cyclic Analog-to-Digital Converters" Electron Devices, IEEE Transactions on, Vol.59, No. 12, pp. 3426-3433, 26 Dec. 2012.

6-bit 1GS/s Fully Differential Current Steering DAC

GeunYeong Park, ChaeYeol Lim and MinKyu Song
Dept of Semiconductor Science, Dongguk Univ-Seoul, Seoul 100-715, South Korea
E-mail : mksong@dongguk.edu

The current-steering structure has been widely used in high speed DACs[1]. Because current-steering type is more advantageous than voltage-steering type in the sampling speed. But this structure has disadvantages that output range limited.

Proposed 6-bit DAC is composed of n-type current cells and p-type current cells. The properties of these current cells are described in [2]. Current cells of each type make up 2+3 thermometer DAC. Signal is generated by the decoder 2+3 and this signal control switch of current cell. The p-MOS current cells make GND to $V_{DD}/2$ output, and the n-MOS current cells make $V_{DD}/2$ to V_{DD} output. Consequently, total output V_{pp} can full swing.

The chip has been fabricated with a 0.11um 1-poly 6-metal CMOS technology. The effective chip area is 0.46mm^2(740um x 450um). In Post-Layout-Simulation, the simulated result of SNR is 37.80dB and ENoB is 5.98-bit, when Fin=500MHz at Fs=1GHz.

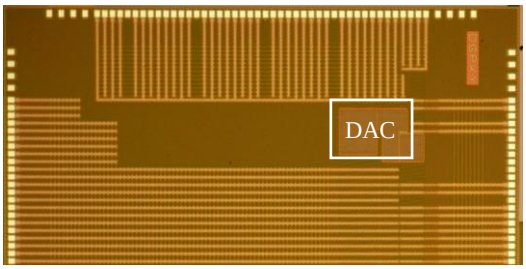


Fig 1. Picture of fabricated chip

ACKNOWLEDGMENT

This work was supported by the IC Design Education Center(IDEC)

[1] Tao Chen and Georges G. E. Gielen, “A 14-bit 200-MHz Current Steering DAC With Switching-Sequence Post-Adjustment Calibration” IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 42, NO. 11, NOVEMBER 2007

[2] Xu Wu et al, “A 130nm CMOS 6-bit Fully Nyquist 3 GS/s DAC” IEEE JOURNAL OF SOLID-STAGE CIRCUITS, VOL. 43, NO.11, NOVEMVER 2008.

An Implementation of H.264 Decoder with Reference Frame Access Optimization

Eunchong Lee, Youngsuk Kang, Donggil Kang, Jeongwoo Yoo and Youpyo Hong
Division of Electronics and Electrical Engineering, Dongguk University-Seoul, Seoul 100-715, Korea
E-mail: yhong@dgu.edu

For many years, H.264/AVC is a video compression standard that has been widely adapted in many consumer, broadcasting, and telecommunication applications. Motion compensation is a large part of the external memory bandwidth for H.264/AVC decoding. The concept of the new MC architecture is to store in sram as many reference pixel as possible in a single external memory access. Assume that the macroblock divided into sixteen 4*4 sub-blocks which can be accessed individually or as a group. We call such a group of blocks can be read by a single-burst access the window. First, all the blocks are broken into 4*4 sub-partitions in one macroblock. Second, define left edge by smallest motion vector from all broken sub-partitions. Once it has determined left edge, a right edge by the addition of burst-8 length. As the window area is defined based on horizontal ranges, there can be rows where no sub-blocks reference pixel data. So, the row addresses checked with valid pixel data and stored in row address list for all the sub-blocks included. Once the left, right edge and valid row addresses are defined, burst-read is initiated.

The experimental results indicate that motion compensation is proposed, reduce about 50% the cycles per MB compared to simple sequential reference block unit data access.

Sequence	QP	Bit rate (Mbps)	Simple access	Window
Flower	**15**	**6.62**	1,460	542
	25	**2.8**	1,147	508
	35	**0.74**	827	483
Foreman	**15**	**4.31**	1,733	611
	25	**0.9**	917	541
	35	**0.22**	641	488

Table 1. AVERAGE MEMORY ACCESS CYCLES PER MB

[1] Yu Li Qu, Yun He,"Memory Cache Based Motion Compensation Architecture for HDTV H.264/AVC Decoder", Proc. Int. Symp. Circuits and Systems , Jun, 2007
[2] Tzu-Der Chuang, Lo-Mei Chang, Tsai-Wei Chiu,Yi-Hau Chen, and Liang-Gee Chen,"BandWidth-efficient Cache-Based Motion Compensation Architecture with DRAM-friendly data Access Control ", Proc. Int. Conference. Speech and Signal Processing, April, 2009
[3] Xianmin Chen, Peilin Liu,and Jiayi Zhu," Block-Pipelining Cache for Motion Compensation in High Definition H.264/AVC Video Decoder ", Proc. Int. Symp. Circuits and Systems, 2009

GPS/Galileo를 동시 지원하는 멀티밴드 저전력 65-nm CMOS RF 수신기

최치훈 [1], 최준우 [2], 김민수 [1], 남일구 [1]
[1] 부산대학교 전기공학과, [2]SK 하이닉스 Mobile 개발본부
E-mail : milkyway0829@gmail.com

GNSS (Global Navigation Satellite System)는 인공위성을 이용하여 위치, 속도, 시간 정도를 사용자에게 제공하는 목적으로 개발되어 군사용 뿐만 아니라 민간용 분야에서도 널리 사용되고 있다 [1]. 현재 GNSS 분야는 미국의 GPS (Global Positioning System)이 거의 독점하고 있는 가운데 유럽을 중심으로 순수 민간용 서비스를 목적으로 Galileo 프로젝트가 진행되어 약 30개의 인공위성을 이용하여 GPS보다 약 3배의 정확도를 제공하려고 한다. 향후 시장에서는 GPS와 Galileo 수신기가 혼재되어 사용될 것이다. 따라서 두 시스템을 동시에 지원할 수 잇는 RF 수신기가 필요하다. 본 논문에서는 GPS와 Galileo를 동시에 수신할 수 있는 L1/L2/L5/E5 등의 멀티밴드 수신기를 위한 저전력 CMOS RF 수신기를 제안하고 설계하였다.

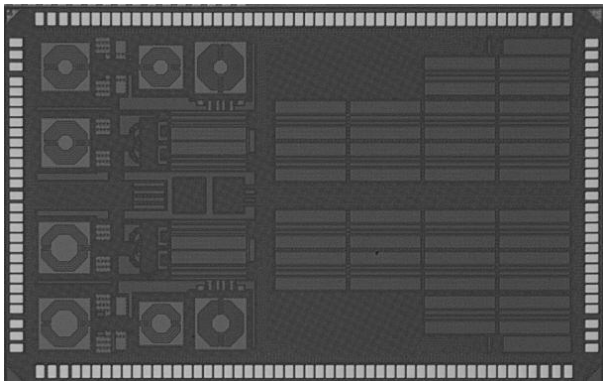


그림 1. 구현한 GPS/Galileo 수신기

표 1. 측정 성능 정리

지표	성능
동작전류 (L1/L5 동시)	25 mA @ 1.2 V
동작온도	-40 ~ 85 °C
동작주파수	1176.45 ~ 157542 MHz
잡음지수	2.5 dB
PLL 위상잡음	-110 dBc @ 1 MHz
PLL lock time	50 μsec
레퍼런스 주파수	13 ~ 40 MHz

* 이 논문은 2010 년도 정부(교육과학기술부)의 재원으로 한국연구재단의 기초연구사업 지원을 받아 수행된 것임 (NRF-2010-0013733). 칩 제작은 IDEC MPW 지원을 받은 것임.

[1] 이형수, 조상현, 고진호, 남일구, "L1/L5 밴드 GPS/Galileo 수신기를 위한 0.13 um 3.6/4.8 mW CMOS RF 수신 회로, 대한전자공학회 하계종합학술대회, 2008, pp. 421-422.
[2] J. Ko et. al., "A 19-mW 2.6-mm2 L1/L2 dual-band CMOS GPS receiver," IEEE J. of Solid-State Circuits, vol. 40, no. 7, pp. 1414-1425, July 2005.

A 1-4Gb/s All Digital CDR

Isak Hwang and Jinwook Burm

Dept. of Electronics Engineering, Sogang University,
35 Baekbeom-ro, Mapo-gu, Seoul 121-742, Korea, +82-2-714-6205
E-mail : burm@sogang.ac.kr

High speed serial links are widely used in SATA, HDMI 1.1, USB 2.0 and so on. A serial link has some advantages of reducing the link power and the number of cable. Thanks to these advantages, data signals area often transmit using high speed serial links. Clock and data recovery (CDR) circuits are very important block in high speed data serial link. From the received data signal, data and clock signal is recovered by CDR circuits. The conventional CDR is based on a charge-pump phase-locked loop (CPPLL). However, as CMOS process scales down, the design of analog CPPLL encounters many challenges. To overcome these problems, All-digital CDR have been reported. Here we implement the high speed All-digital CDR. This CDR is implemented using 0.13-μm CMOS technology. An all-digital CDR (ADCDR) is presented. ADCDR is composed of half-rate BBPD (Bang-Bang Phase Detector), frequency acquisition part, delta-sigma modulator, APGC (Adaptive Proportional Gain Controller), DCO (Digitally Controlled Oscillator), DCR (Digitally Controlled Resistor) and other control circuits. It uses a half-rate architecture as it relaxes the required clock frequency of ADCDR.

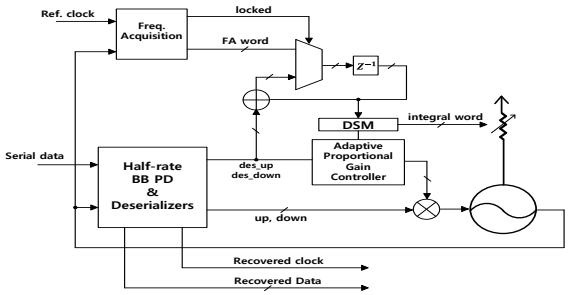


Fig 1. Architecture of ADCDR

BBPD detects the phase different between the recovered clock and reference clock. The DCO separately controlled by the proportional and integral paths generates half-rate 4-phase clocks. Using BBPD, frequency acquisition part, DCR gets digital code that controls VDD of DCO. In this way

the oscillation frequency of DCO is changed 0.5GHz ~ 2GHz. And the AGPC adjusts the proportional gain based on Up and Down signals within 10 de-serialized phase error to control the tracking bandwidth of CDR. By controlling the proportional gain actively, it decouples the trade-off between bang-bang jitter and tracking bandwidth. A delta-sigma modulator improves the resolution by dithering. Fig. 2 shows the simulation result of ADCDR. It recovers 4-Gb/s random bit stream and clock. Fig. 3 is the chip photograph of ADCDR.

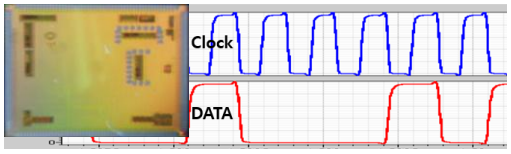


Fig 2. Simulation result of ADCDR Fig 3. Chip photograph

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CMOS rectifier circuit for Piezoelectric Energy Harvesting Device

Dongjae Han, Seunghwan Song and Kwang-Seok Yun*
Department of Electronic Engineering, Sogang University, Seoul 121-742, Korea
E-mail : ksyun@sogang.ac.kr

Sustainable operation of battery powered mobile devices is a key challenge of environmental energy harvest [1]. A vibrating piezoelectric device is one of the environmental energy harvesting devices. A piezoelectric device differs from a typical electrical energy source in that it is a capacitive source rather than an inductive source, and its output voltage varies according to the mechanical source [2]. In this paper, we investigate an efficient CMOS switching rectifier circuit that is optimized for a piezoelectric energy harvester with low frequency output voltage and high output resistance. The circuit consists of a basic CMOS rectifier and 2 switch blocks to compare the voltage levels of input source and output capacitance [3]. Each terminal of the voltage source is connected to CMOS full-wave rectifier and a switch block. If the magnitude of input source voltage is higher than the voltage of output capacitance, the full-wave rectifier starts to charge the capacitor by increasing the output voltage until the value reaches to the input voltage level. Two switch blocks always operate in complementary modes, which is advantageous for low power operation of the circuit high energy transfer efficiency. Total 6 circuit modules are implemented in single die to handle multi-phase energy harvesting application. This study will be helpful in designing the electrical equivalent model of the piezoelectric devices, and will give more issues of optimizing the power transfer efficiency of piezoelectric devices.

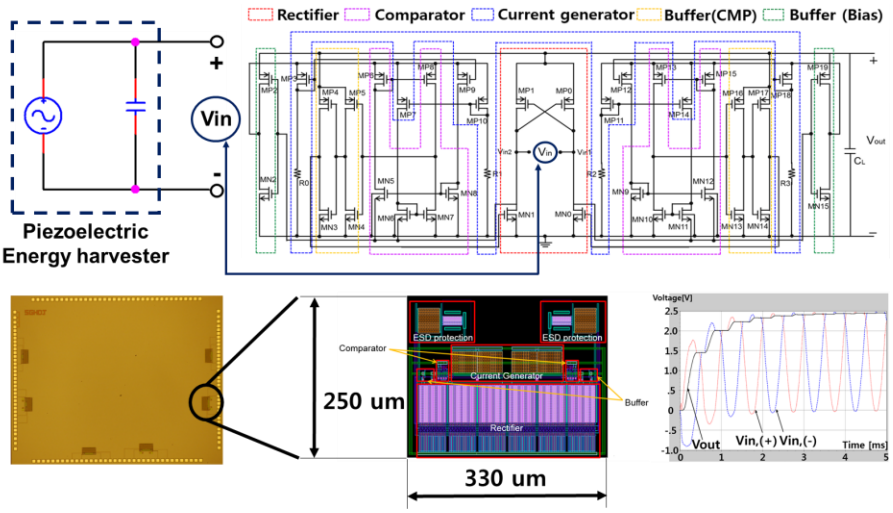

Fig 1. Circuit and layout of the proposed rectifier and its simulation result at 2.5V sinusoidal source.

[1] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, M. Srivastava, IEEE Press 64 (2005).
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94 GHz Resistive Mixer

Jihoon Kim, Hongjong Park, Sangho Lee, and Youngwoo Kwon
Department of EESC and INMC, Seoul National University, Seoul 151-747, Korea
E-mail : j7h7@snu.ac.kr

A 94 GHz CMOS Resistive Mixer is presented using 65nm CMOS process. we have optimized the layout of the unit CMOS transistors to minimize the parasitic capacitances and resistances. Full-wave EM-based layout-dependent scalable transistor model developed by the authors was used for this purpose [1]. To minimize parasitic losses which are serious at high frequencies, we adopted not only scaled-down 65 nm CMOS technology but also IF matched transistor size and symmetric transistor structures. These adoptions contribute to reducing conversion loss at 94 GHz by 2~3 dB. Fig. 1 (a) shows the circuit schematic of the resistive mixer developed in this work. Fig. 2 represents measured conversion loss according to an RF frequency at a fixed IF frequency of 1 GHz. It is based on a conventional resistive mixer topology utilizing the nonlinearity of the drain-source resistances modulated by the LO signal. It shows 8.8~9.2 dB of conversion loss from 87 to 94 GHz of RF frequencies with LO power below 7.6 dBm. The circuit has been implemented using 65nm CMOS technology with 1 poly and 8 metals including 3 μm-thick analog metals and active area of the chip is only 0.38 mm x 0.43 mm.

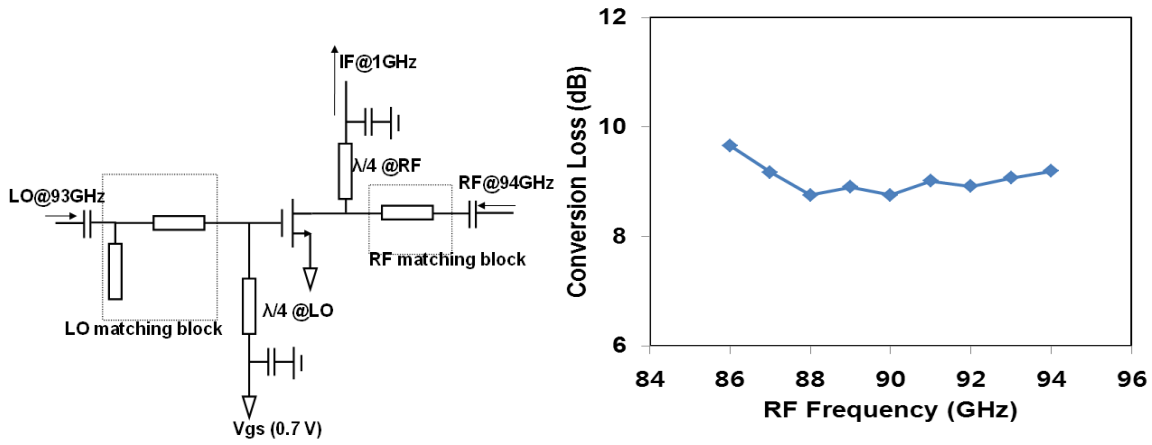


Fig 1. (a) Schematic of the 94GHz resistive mixer (b) Measured conversion loss versus RF frequencies at fixed IF frequency (1GHz) under RF power = -5dBm and LO power = 5.5 ~ 7.6 dBm

[1] W. Choi, G. Jung and J. Kim et al., "Scalable Small-Signal Modeling of RF CMOS FET Based on 3-D EM-Based Extraction of Parasitic Effects and Its Application to Millimeter-wave Amplifier Design," IEEE Trans. Microw. Theory Tech., Vol. 57, No. 12, pp. 3345-3353, Dec. 2009.

V-band Low Noise Amplifier for 60GHz WPAN Applications

Hongjong Park, Sangho Lee, and Youngwoo Kwon
Department of EECS and INMC, Seoul National University, Seoul 151-747, Korea
E-mail : park.hongjong@gmail.com

Recently, V-band radio is gathering much attentions for next-generation wireless personal area networks (WPANs). High attenuation at 60GHz band is well suited to be used to short-range applications, and high-data rate is supported with V-band radio system [1]. Traditionally, millimeter-wave MMIC is fabricated on expensive III-V semiconductor technologies, which has advantage on device performance. In this paper, the V-band low noise amplifier (LNA) is designed and fabricated by standard 65nm CMOS process, which is low-cost and domestic. Size and layout type of transistor is optimized to high MAG at V-band frequencies. Full wave EM simulation and high frequency modeling of the transistors and the transmission lines is performed to estimate the behavior at V-band frequencies. To get the broadband characteristic, each stage is matched at different frequencies, and double stub matching topology is used. Fig. 1 (a) and (b) are simulation and measurement results. Fabricated chip has 3dB bandwidth of 49GHz to 58GHz, fractional bandwidth 16.3%, with peak gain 10.3dB.

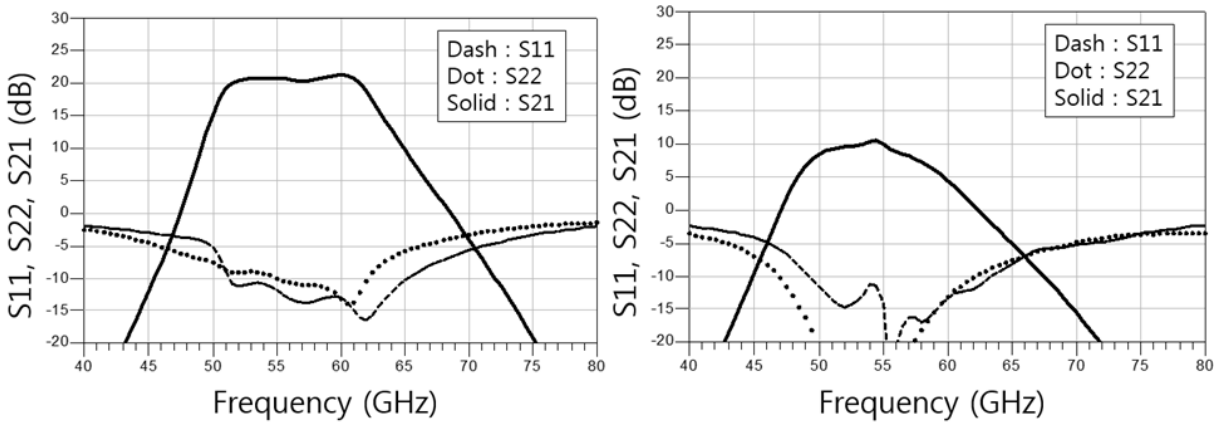


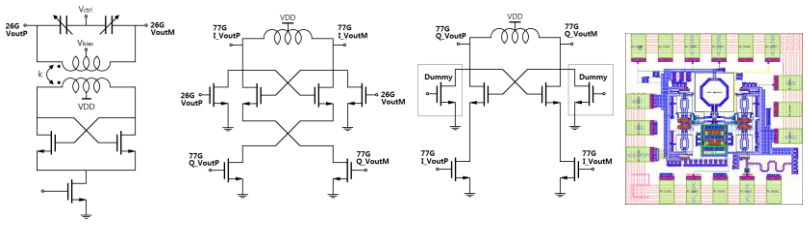
Fig 1. (a) Simulated performance of 3-stage LNA. (b) Measured performance of the 3-stage LNA

[1] I. Ju, Y. Kim, S. Lee, S. Song, J. Lee, C. Cheon, K.-S. Seo, and Y. Kwon, "V-band beam-steering ASK transmitter and receiver using BCB-based system-on-package technology on silicon mother board," IEEE Microw. Wireless Compon. Lett., vol.21, no. 11, pp. 619-621, Nov. 2011.

26-GHz VCO와 주파수 3 체배기를 이용한 77-GHz QVCO 설계

송재훈, 남상욱
서울대학교 뉴미디어 통신공동연구소
doritos43@ael.snu.ac.kr

최근 무선 통신 및 레이더 시스템 응용에 있어서 고성능 VCO 와 IQ 신호 처리를 위한 QVCO 개발이 중요한 이슈가 되고 있다. 그림 1(a)는 트랜스포머 커플링을 이용한 26-GHz VCO 의 회로도이다. 일반적인 경우 바랙터 컨트롤 전압의 조정 범위를 0~V_{DD} 라고 할 때, center-tapped 트랜스포머를 이용하여 바랙터 양 단의 전압 바이어스를 $V_{DD}/2$ 로 두어 바랙터 컨트롤 전압 에 따른 주파수 조정 범위를 최대화 하고, 선형적인 주파수 조정 특성 또한 얻을 수 있는 구조를 사용하였다 [1]. 그림 1(b)는 설계된 QVCO 의 회로도이다. 26-GHzVCO 의 출력 전압의 3 차 조화 성분을 이용하여 3 체배하는 방식으로, 77-GHz 근처에서 발진하는 IQ 발진기에 26-GHzVCO 의 출력 전압을 병렬로 주입-잠금 (Injection-Locking)하여 77-GHz IQ 신호를 발생시키는 QVCO 이다 [2]. 전체 회로 설계는 기 측정된 트랜지스터 모델과 레이아웃에서 발생한 기생 성분들을 포함한 full EM-시뮬레이션으로 설계 하였다. 시뮬레이션 결과는 표 1 에 나타나 있다.



(a) (b) (c)

그림 1. 26-GHz VCO (a)와 77-GHz QVCO (b) 회로도 및 레이아웃 (c)

	26G VCO	77G QVCO
주파수 조정범위 (GHz)	25.6~ 26.4	76.7~ 77.3 (잠금범위)
위상 잡음 @1MHz	-105.6 dBc/Hz	-
출력 전력	-	2.3dBm (버퍼 출력)
소모 전력	18 mW	50 mW

표 1. Full-EM 시뮬레이션 결과

ACKNOWLEDGEMENT

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A CMOS Integrated Carbon Nanotube Biosensor Array with AC Measurement Capability

Seok Hynag Kim, Jin-Hong Ahn and Young June Park
Department of Electrical and Computer Engineering, Seoul National University,
Seoul 151-744, Republic of Korea

The Carbon nanotube (CNT) sensors have been considered to be the most promising candidate for label-free detection of DNA or biomolecules due to their high conductivity, small size, high strength, and stability in harsh chemical environments comparing with the other reported biosensors such as silicon nanowire sensors.

A new CNT-based electrical DNA biosensor system was reported by our group, which consists of gold (Au) nanoparticle-decorated CNT network on top of concentric Au electrodes [1]. Recently, we suggested AC measurement methods which apply an electrical pulse bias between the electrical channel, to which the probe molecules are attached [2], and found that this method provides two important improvements: (i) the interaction rates between the probe and target molecules are significantly improved reducing sensing time, and (ii) the selectivity has been improved because the dynamic motion of the probe molecules could suppress undesired binding events with nonspecific molecules. In this paper, we propose a CMOS integration method of AC measurement system, which can provide AC measurement capability of array type sensors.

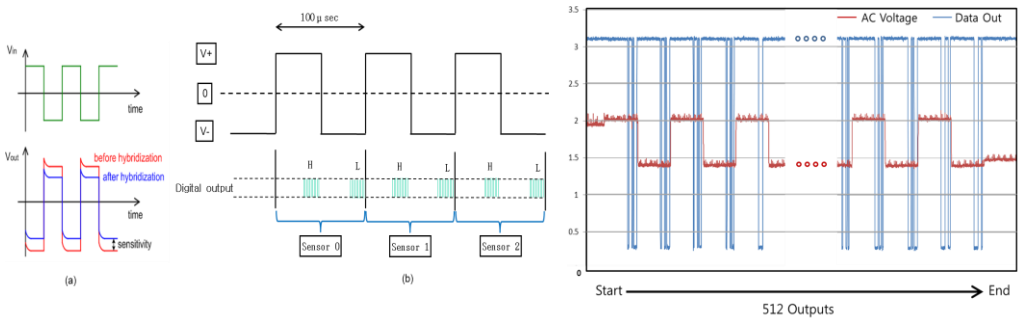


Fig 1. (a) Input/output measurement signals in case of DNA hybridization testing, (b) Timing diagram of CMOS integrated sensor chip and measured sensor signals of sensor array chip.

This work was supported by the IDEC.

[1] K. Woo, J.-M. Woo, J. Ahn, J. Cheon, J. Lim, S. Kim, H. Chun, E. Kim, Y. Park, ACS Nano, 5, 6, (2011).
[2] J.-M. Woo, S. Kim, H. Chun, S. Kim, J. Ahn, Y. Park, Lab on a chip, 13, 3755, (2013).

A 4.0-6.0GHz All-Digital Phase-Locked Loop with a Digitally Controlled Oscillator Using Digitally Controlled Current Source

Sungwoo Kim, Taeho Kim, Sungchun Jang, Sanghyeok Chu, Deog-Kyoon Jeong
Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-747, Korea
E-mail : swkim@isdl.snu.ac.kr

With scaling down to deep-submicron CMOS process, design of an analog charge-pump phase-locked loop has been harder since leakage current of capacitor, large area loop filter capacitor and reduced dynamic range of control voltage. To overcome these problems and to get advantages of portability, programmability and predictability, researchers have studied an all-digital phase-locked loop for decades. This paper describes the design and implementation of an all-digital phase-locked loop(ADPLL) circuit. The proposed ADPLL is composed of time-to-digital converter(TDC), digital loop filter(DLF) and digitally controlled oscillator(DCO). The digitally controlled oscillator is designed for linear and monotonic frequency characteristic using digitally controlled current source. With 65nm standard CMOS process, a prototype ADPLL operates 4.0-6.0GHz.

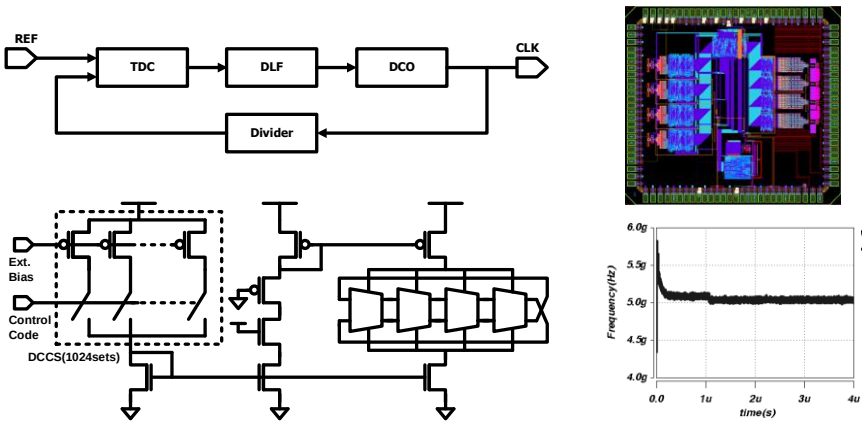


Fig 1. ADPLL Block Diagram, Chip Layout and Simulation Result

Acknowledgement
This work was supported by the IDEC

[1] D.-S. Kim, et al., “A 0.3-1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller,” IEEE Journal of Solid-State Circuits, vol. 45, no. 11, pp. 2300–2311, 2010.
[2] R. B. Staszewski et al., “All-digital PLL and transmitter for mobile phones,” IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2469– 2482, Dec. 2005.

Implementation of Multiple Event Handling Processor

Dabujin Lee, Sehyun Song, Kichul Kim
School of Electrical and Computer Engineering, University of Seoul, Seoul 130-743, Korea
E-mail : dabujin3@naver.com

This paper presents a multiple event handling processor. The processor assists the main processor in SoC to reduce overload of event handling. Typically, if the main processor manages multiple events, it has to handle events one after another. It may take long time to process all events[1].

The main feature of the processor is to process multiple events simultaneously. The processor can reduce processing time by combining multiple events. For example, if three IPs are controlled by the processor, the processor monitors three event signals from IPs. The signals are used to activate event triggering. Suppose the signals are named as A, B, and C. The processor can use an event trigger with complex combination of event signals such as (A>1020)&&(B!=0)&&(C≤0). This makes the processor handle multiple events from IPs at the same time. Another feature of the multiple event handling processor is the high speed data transmission. The transmission is also possible while the processor handles complex combination of events. Fig. 1 shows that multiple IPs are managed by the processor. The IPs which perform similar operations may require overlapped data. If the processor controls data transmission, overlapped data doesn't have to be transmitted repeatedly. The processor analyzes requesting addresses and time from IPs. The IPs use shared data bus and receive read/write control signal from the processor. This reduces the total time which takes all the IPs to receive requested data.

Design for Testability (DFT) scan chain is implemented for checking status registers of the processor. It was fabricated with Hynix 0.35um CMOS technologies. Chip core size is 4000um x 3000um.

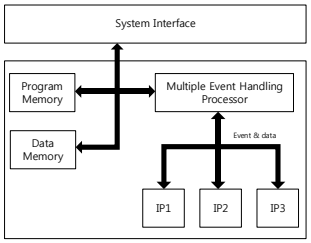


Fig 1. Multiple event handling processor

[1] Hofstatter, M.,A SPARC-compatible general purpose address-event processor with 20-bit l0ns-resolution asynchronous sensor data interface in 0.18μm CMOS, Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium.

Current-Mode SAR ADC for Resistance Variation Analysis Aimed at Adaptive Reference Control in Cross-Point ReRAM

Se-Jin Baik[1], Jong-Min Baek[1], Sang-Yun Kim[1,2], Jae-Koo Park[1], Kee-Won Kwon[1]

[1]*College of Information and Communication Engineering, Sungkyunkwan Univ., Suwon, Korea*

[2]*Memory Division, Samsung Electronics Co., LTD., Hwaseong, Korea*

keewkwon@skku.edu

Resistive Random Access Memory (ReRAM) is the one of the most emerging non-volatile memories, and has wide field of applications in the near future. Because of wide random distribution of cell resistance, we suggested a circuit solution for these device variations: Adaptive Reference Control, on previous work [1]. After scanning reference cells by the sense amplifier, an Analog-to-Digital Converter (ADC) is used to collect the binary data of the conductance of the dummy reference cells distributed over the cell array. However, applying ADC circuit can be a burden for memory system because of power and area. We suggest a current mode SAR (Successive Approximation) ADC circuit instead of Flash ADC, resulting in lower energy consumption and smaller area. Moreover, SAR ADC is compatible for multi-level cell operation because an additional 1 bit is needed for reference generation to cover the wider range of 3 different LRS current. By applying adaptive reference control in multi-level cell ReRAM, It indicates a high yield and speed on read in the future.

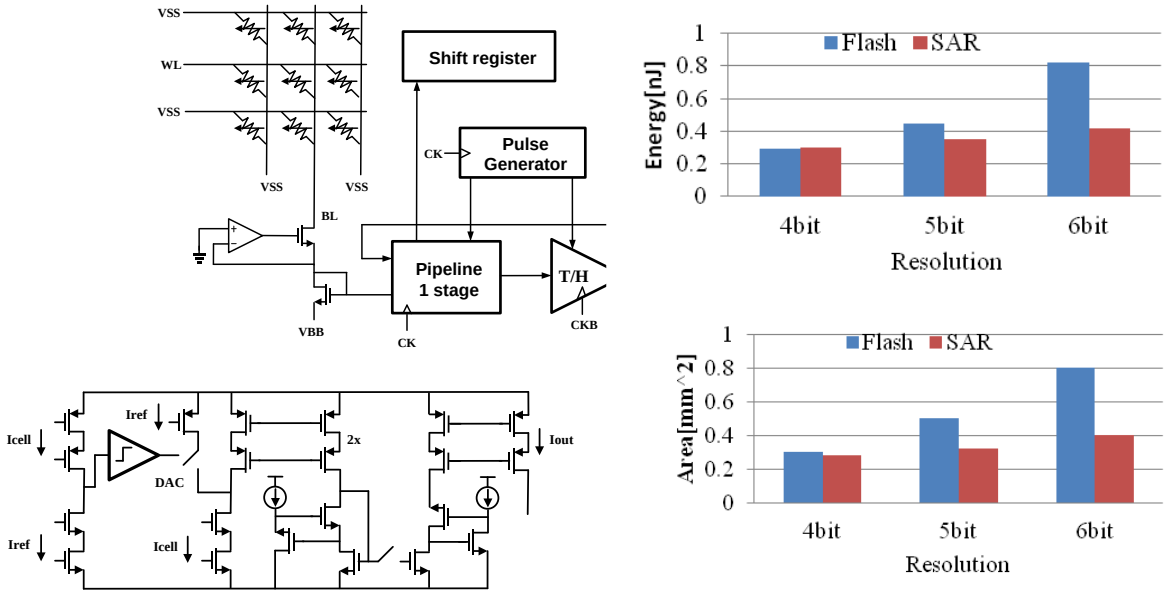


Fig 1. Schematic iof the current mode SAR ADC and power & area comparison with Flash ADC

[1] J.-K. Park, S.-Y. Kim, J.-M. Baek, D.-J. Seo, J.-H. Chun, and K.-W. Kwon, "Analysis of Resistance Variations and Variance-Aware Read Circuit for Cross-Point ReRAM," in *Proc. International Memory Workshop (IMW), 2013, pp. 112-115*

[2] R. Dlugosz, K. Iniewski, "Ultra Low Power Current Mode Algorithmic Analog-to-Digital Converter Implemented in 0.18µm CMOS Technology for Wireless Sensor Network", in *MIXDES 2006, pp. 401-406*

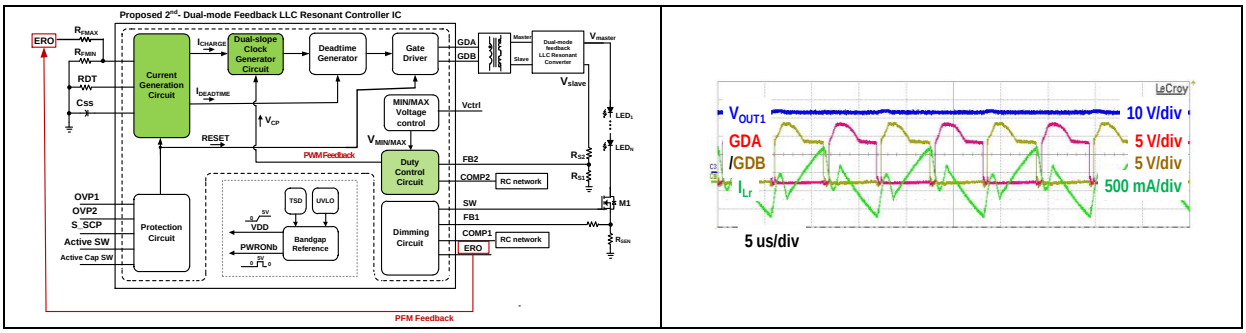
PFM/PWM Dual Mode Feedback LED BLU Driver IC

Hong-Jin Kim, Young-Jun Park, Chang-Jae Yoo, and Kang-Yoon Lee
IC Lab, SungKyunKwan University, Cheeoncheon-dong Jangan-gu, Suwon-si Gyeonggi-do, Korea
E-mail : klee@skku.edu

Recently, light-emitting diodes (LEDs) have become one of the most promising candidates for BLUs and other lighting applications. LLC resonant converter is popularly adapted to consumer or industrial electronics due to their inherent advantages over contending topologies.

Fig. 1 (a) shows the detailed architecture of the proposed controller IC and LED driving circuit. The controller IC consists of a dual-slope sawtooth generator, a dead time generator, a gate driver, a protection circuit, a current generation circuit, a dimming circuit, a duty control circuit and a bandgap reference. The dual-slope clock generator is designed to define an output frequency of gate driver and dead-time depending on the current of dual-slope clock generator. The switching frequency control block is designed to receive the ERO voltage from master stage. The duty control block is designed to receive a feedback voltage of slave stage and to supply VCP that is able to control a duty ratio of gate driver wave.

Fig. 1 (b) shows the proposed LLC resonant control system and the measurement waveforms on steady-state and it can be found that the voltage-second balancing of series inductance current I_{Lr} is achieved for small load.



(a) (b)

Fig 1. The proposed LLC resonant control system and measurement waveforms

[9] Sung-Soo Hong, et al. “A New Cost-Effective Current-Balancing Multi-Channel LED Driver for a Large Screen LCD Backlight Units”, *KIPE Journal of Power Electronics*, Vol. 10, No. 4, pp. 351-356, July. 2010.

[10] Bo Yang and Fred C. Lee, “LLC Resonant Converter for Front End DC/DC Conversion”, in *APEC*, vol.2, pp. 1108-1112, 2002.

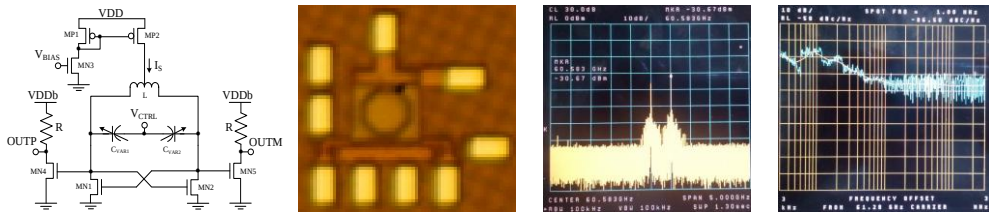
V-band PLL용 60GHz VCO의 설계

이종석, 문용
숭실대학교 전자공학과
E-mail : ljs1385@ssu.ac.kr

밀리미터 웨이브 대역의 고속 데이터 전송에 대한 요구가 높아짐에 따라 높은 주파수의 클락 생성이 필수적이며, PLL 을 주로 사용한다. 전압 제어 발진기 (VCO)는 PLL 에서 가장 중요한 블록이며, 60 ㎓의 VCO 를 PLL 에 사용하면 빠른 락킹 시간과 넓은 락킹 주파수 범위를 얻을 수 있다. 본 논문에서는 V-band PLL 에 적용할 수 있는 60 ㎓ VCO 를 설계했으며 그림 1. (a)에 회로도를 나타냈다. 제안하는 VCO 는 RF 인덕터를 사용한 LC 형 구조이며 2 개의 베렉터는 VCO 의 튜닝범위를 넓혀주기 위해 사용하였다. PMOS 는 전압-전류 특성상 바이어스 회로에는 적합하지만 고주파 동작에 적합하지 않기 때문에 MN1 과 MN2 의 NMOS 를 이용한 교차쌍 구조로 설계하였으며, 이는 부성저항 (-2/gm)을 제공하여 LC tank 에서 발생하는 손실을 줄여준다. V-band 에 적용하기 위해서는 출력전력도 중요한 지표이기 때문에 출력버퍼를 추가했다. 설계한 VCO 는 65 ㎚ CMOS 공정을 사용하여 제작하였고, 칩 제작은 IDEC 의 지원을 받았다. 그림 1. (b)~(d)는 제작한 VCO 의 칩 사진과 측정결과이다. 칩 측정은 프로브스테이션을 사용하여 웨이퍼에서 프로빙하였고, 60.81~62.05 ㎓의 동작범위와 -30.67dBm 의 출력전력, 전원전압 1.2V 에서 14.4 ㎽의 소모전력이 측정됐다. 위상잡음은 중심주파수 61.28 ㎓에서 -86.5dBc/Hz@1MHz 이다. 설계한 VCO 는 V-band 에서의 타 VCO 와 비교하여 낮은 전력소모와 넓음 동작범위를 갖는다[1].

표 1. 기존 연구와의 성능 비교

	Process	Center Freq. [㎓]	FTR [%]	PDC [㎽]
[1]	45㎚ CMOS	70	0.2	45
This work	65㎚ CMOS	61.28	2	14.4



(a) (b) (c) (d)

그림 1. (a)VCO 회로도 (b) 칩사진 (c) 출력 파워 스펙트럼 (d) 위상잡음 측정결과

[1] Katz, A., Degani, O., Shacham-Diamand, Y., Socher, E., "A beyond 60GHz cross-coupled fundamental VCO in 45nm CMOS," IEEE, COMCAS, pp.1-5, Nov. 2009.

Supply Modulator with Compact Size

Seokhyun Yoon, Changhyun Lee, and Changkun Park
School of Electronic Engineering, Soongsil University, Seoul 156-743, Korea
E-mail : shyun85@ssu.ac.kr, airwinds@ssu.ac.kr, pck77@ssu.ac.kr

Envelope tracking (ET) is one of the popular techniques to obtain high efficiency of the mobile transmitters. One of the essential components for the ET systems is a supply modulator. To maximize the overall efficiency of the power amplifier, the bandwidth of the supply modulator is designed to be nearly that of the envelope of the RF signal. Additionally, the efficiency of the supply modulator itself must be improved. In this study, we designed the supply modulator using 0.35-μm BCDMOS technology. The envelope signal detected from the RF signal is used as the input of the supply modulator as shown in Fig. 1. The Class-AB of the supply modulator is composed of voltage follower using rail-to-rail structure. Although the efficiency of the Class-AB is lower than that of the Class-D, Class-AB has high bandwidth compared to the Class-D. Thus, the bandwidth of the supply modulator is determined by the Class-AB. The control block of Class-D is composed of op amp. and hysteresis comparator as shown in Fig. 1. In this work, we designed the power cell of the Class-D with fish-bone type to minimize its layout size. All of the guard-ring of each unit-cell is removed for the compact size. The unit-cell of the power cell has 16 fingers and 8-μm gate width. Fig. 1. shows the voltage and current waveforms of the designed supply modulator. As shown in Fig. 1, the output voltage successfully tracts the input voltage. We use the off-chip inductor at the output of the Class-D amplifier shown in Fig. 1.

Acknowledge – This work was sponsored by ETRI SW-SoC R&BD Center, Human Resource Development Project

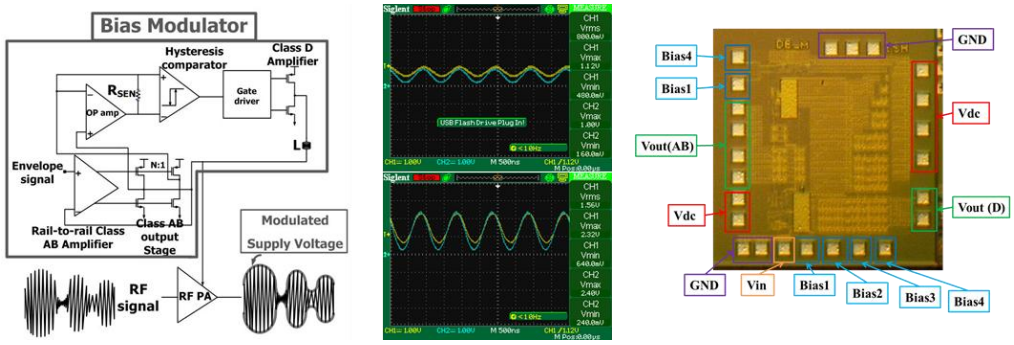


Fig 1. Structure, waveform($1V_{pp}$, $3V_{pp}$@ 1 MHz), layout of the supply modulator data

[1] S. Jang et al, "A Wideband CMOS Supply Modulator Delivering 32dBm Peak Output Power for a Class 3 LTE Envelope Tracking Transmitter", ITC-CSCC 2011, pp.289-292, June 2011.

Improved Layout of LC Tank for Voltage Controlled Oscillator

Milim Lee, and Changkun Park
School of Electronic Engineering, Soongsil University, Seoul 156-743, Korea
E-mail : mlgirlm@ssu.ac.kr, pck77@ssu.ac.kr

In this paper 2.4 GHz CMOS Voltage Controlled Oscillator (VCO) for Industrial Scientific Medical (ISM) band. When designing the VCO, differential pair provides a number of useful properties. However, the use of cross coupled configuration, the resistance and parasitic capacitance occurs. In order to solve this problem in a conventional process layout and other proposed structures. We removed cross coupled structure between the NMOS pair. By proposed structure, the parasitic capacitance of between metal cross-line can be eliminated. Therefore, performance of Voltage Controlled Oscillator will be enhanced.

A CMOS VCO schematic shown in Fig. 1. This is the most widely used is the circuit configuration VCO. When the layout of the circuit cross-structure appears as shown in Fig. 1. We proposed layout of Fig. 1, complement to for disadvantages of this structure.

The designed voltage controlled oscillator is implemented using 0.11-μm RF CMOS process. The size of chip is 1.2 μm x 0.7 μm including the pads.

In this work, the VCO was designed to use a symmetric structure. By removing the cross coupled l structure, parasitic capacitance of between the metal is eliminated, resulting in a frequency down shift can be prevented. In addition, the resistance from the cross coupled structure will be eliminated, so the symmetrical structure is created and the resulting benefits can be provided.

Acknowledge – This work was sponsored by ETRI SW-SoC R&BD Center, Human Resource Development Project

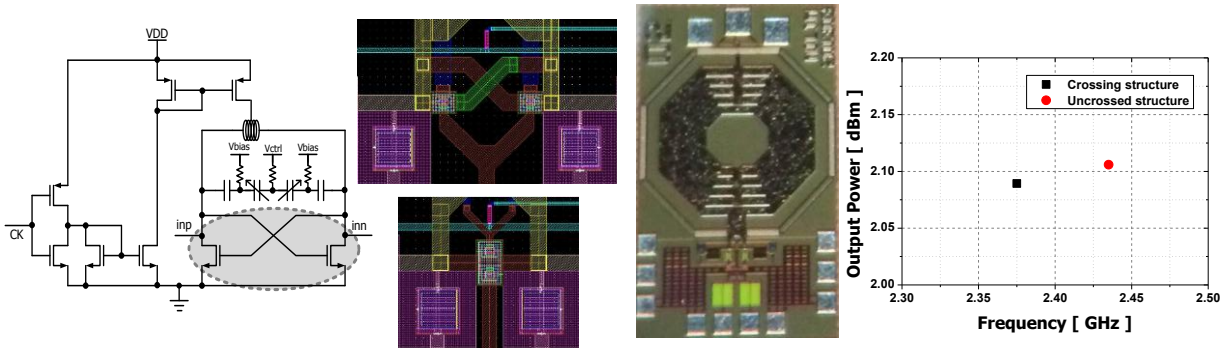


Fig 1. Structure, layout(conventional, proposed), chip photo, simulation

[1] Troedsson, N. ; Sjoland, H., “High performance 1 V 2.4 GHz CMOS VCO”, ASIC, 2002. Proceedings. 2002 IEEE Asia-Pacific Conference on (2002), 185-188.

넓은 입력 범위를 갖는 가변 이득 시간 증폭기

Doohyun Shon and Taewook Kim
Department of Electrical & Electronic Engineering, Yonsei University, Korea
E-mail : doohyun.shon@gmail.com

최근에 시간의 차이를 디지털 값으로 읽어내는 시간-디지털 변환기(TDC, Time to Digital Converter)가 거리 측정 시스템에 핵심 요소로 쓰이고 있다. 본 논문에서는 TDC 의 성능을 향상 시킬 수 있는 넓은 입력범위와 이득이 쉽게 조절 가능한 시간 증폭기를 설계하였다. 시간 증폭기는 두 신호의 시간 차이를 일정한 이득만큼 넓혀진 시간을 내는 시스템이다. 그림 1 은 제안하는 시간증폭기의 블록 다이어그램이다. 기존 SR-latch 가 두 쌍으로 달린 구조의 NAND-gate 에 위 아래로 Header bias 와 Foot bias 를 달아 새로운 구조를 제안하였다. 두 개의 bias 를 통해 전류의 속도를 조절함으로써 시간증폭기의 이득과 입력범위를 조절이 가능하다. Layout 을 완성한 후 cadence spectre 모의실험 도구를 통하여 실험을 하였다. 그림 3 은 시간 증폭기의 칩 사진이다. 패드를 포함한 칩의 크기는 581um*360um 로 매우 작다. 그림 3, 4 는 시간 증폭기의 시뮬레이션 결과로 X 축은 입력시간 차이이고 Y 축은 출력시간 차이이다. Foot Bias 를 통해서 시간 증폭기의 선형적인 입력 범위가 변하는 것을 확인 할 수 있고, Header Bias 를 통해서는 이득이 조절 가능함을 확인할 수 있다. 시간 증폭기의 이득은 2~4.3 으로 조절이 가능하고, 입력범위는 300ps~1200ps 까지 조절 가능하다. 기존에 이득과 입력범위가 입력 범위가 각각 2, 60ps [1], 5, 200ps [2] 로 고정되어 있는 다른 시간증폭기에 비해 성능이 좋고, 두 요소의 가변성은 많은 응용기술에 쉽게 적용될 수 있다.

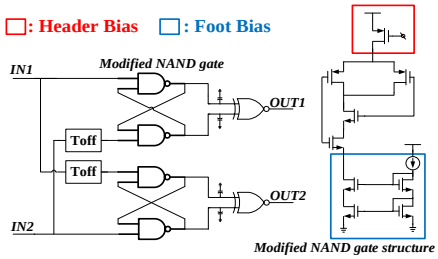


그림 1. 시간증폭기의 블록도

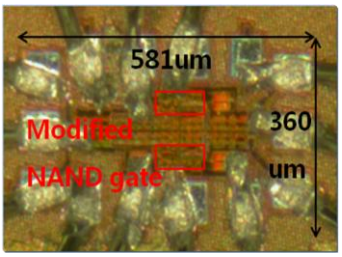


그림 2. Chip Micrograph

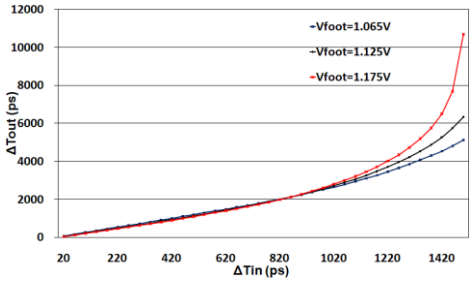


그림 3. Foot Bias 에 따른 선형성 변화

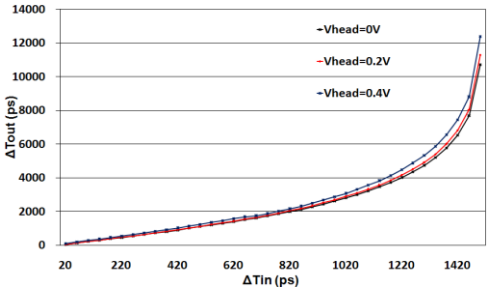


그림 4. Head Bias 에 따른 이득 변화

[1] YoungHun Seo, JunSeok Kim, HongJune Park, and JaeYoon Sim "A 1.25ps Resolution 8b Cyclic TDC in 0.13um CMOS", *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 736–743, Mar. 2012.

[2] Jaejun LEE, Sungho LEE, Yonghoon SONG, and Sangwook NAM, "High Gain and Wide Range Time Amplifier Using Inverter Delay chain in SR Latches", *Proc. IEICE TRANSACTIONS on Electronics Vol.E92-C No.12 pp.1548-1550*

77 GHz 90° , 45° , 22.5° 위상 변위기 설계

이효성, 민병욱
연세대학교 전기전자공학부
E-mail : bmin@yonsei.ac.kr

삼성 65nm CMOS 공정을 이용하여 77 GHz 에서 동작하는 위상 변위기 (Phase shifter)를 설계하였다. High-pass T 구조를 사용하여 90° , 45° , 22.5° 위상 변위 회로를 설계하고, CMOS 스위치를 이용하여 위상 변위가 가능하도록 구현하였다 (Fig. 1). 위상 변위기에서 직렬 스위치(T1)가 켜지고 병렬 스위치(T2)가 꺼지면 위상 변위가 일어나지 않고 (bypass), 직렬 스위치가(T1) 꺼지고 병렬 스위치가(T2) 켜지면 위상 변위가 일어난다[1]. PDK 에서 밀리미터파 대역에서 사용 가능한 MIM capacitor 와 Spiral inductor 모델을 제공하지 않기 때문에 모든 수동 소자들은 Sonnet(2.5D EM Simulator)로 설계하였다. Fig. 2-4 는 측정된 손실과 위상 변화 측정 결과이다.

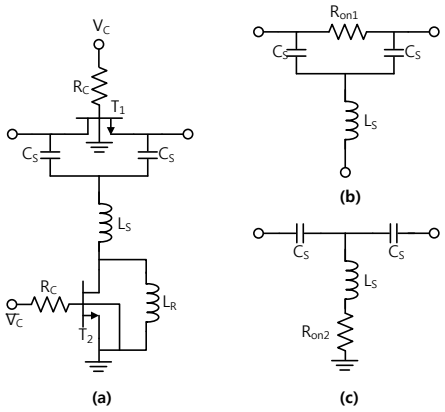


Fig 1. 위상 변위기(a) 및 bypass(b)와 hipass(c) 모델

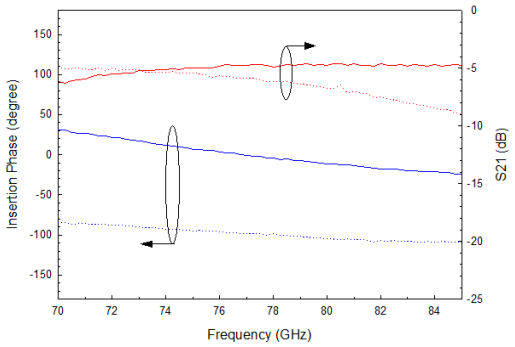


Fig 2. 90° 위상 변위기 측정결과

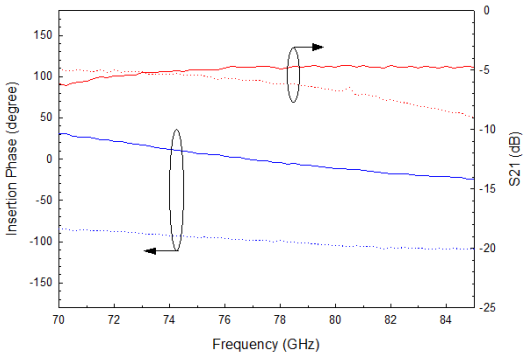


Fig 3. 45° 위상 변위기 측정결과

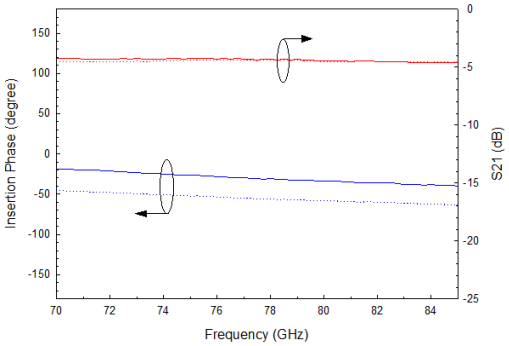


Fig 4. 22.5° 위상 변위기 측정결과

[1] Byung-Wook Min; Rebeiz, G.M., "Single-Ended and Differential Ka-Band BiCMOS Phased Array Front-Ends," *Solid-State Circuits, IEEE Journal of* , vol.43, no.10, pp.2239,2250, Oct. 2008

발룬을 이용한 C-Band 마이크로파 스위치 설계

김경원, 민병욱
연세대학교 전기전자공학과
E-mail : daedoono@yonsei.ac.kr

본 논문에서는 발룬과 SPDT 스위치를 하나의 칩에 집적하여 두 기능을 동시에 할 수 있는C-band 대역의 마이크로파 스위치를 설계하였다. 발룬을 이용하여 Single 신호를 Differential 신호로 변환하고, 변환된 신호는 CMOS 의 스위칭을 통하여 전달 혹은 격리가 되도록 설계하였다. 그림1 (a) 은 발룬을 이용하여 설계된 마이크로파 스위치의 전체 회로도이다. 입력단은 50 Ω Single-ended, 출력단은 100 Ω Differential port이다. 각 출력단은 서로에 대해 센터탭과 같은 역할을 한다. 본 설계에서는 각 출력단에 shunt switch 를 달아서 signal 을 그라운드 시키는 방법으로 각 출력단의 전환이 이루어지게 하였다. CMOS 스위치의 게이트에는 3.5 V 의 동작전압을 가하였고, 산화막 파괴를 막기 위해 20 KΩ 의 저항을 연결하였다. CMOS 스위치의 기생저항과 MIM Capacitor C1은 발룬을 5-6 GHZ에서 정합하는 역할을 한다.

그림 1 (b) 는 설계된 마이크로파 발룬 스위치의 측정 결과이다. 5.5 GHz 에서 3 dB (port 2), 2.4 dB (port 3) 의 삽입손실을, 5-6 GHz 에서 >27.5 dB (port 2), >22 dB (port 3) 의 격리도를 얻을수 있었다. 입출력 반사손실은 5-6 GHz 에서 -15 dB 미만이다.

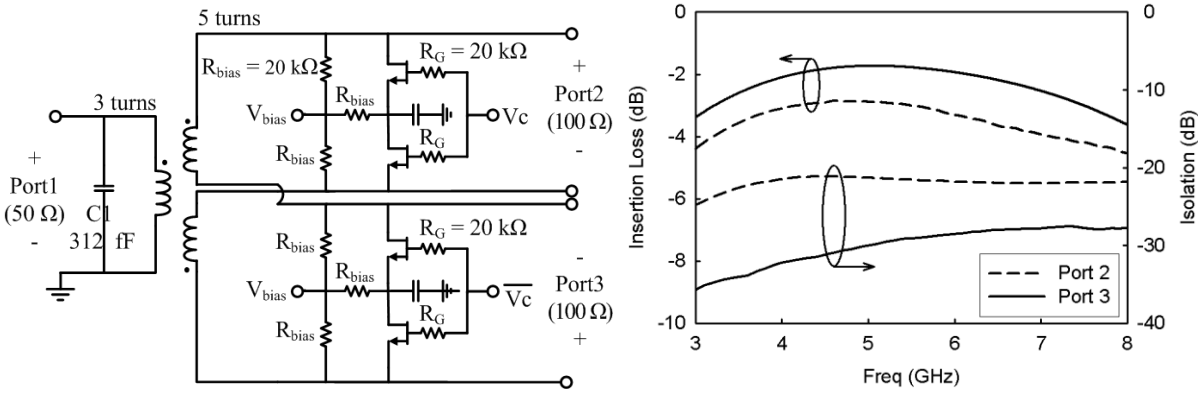


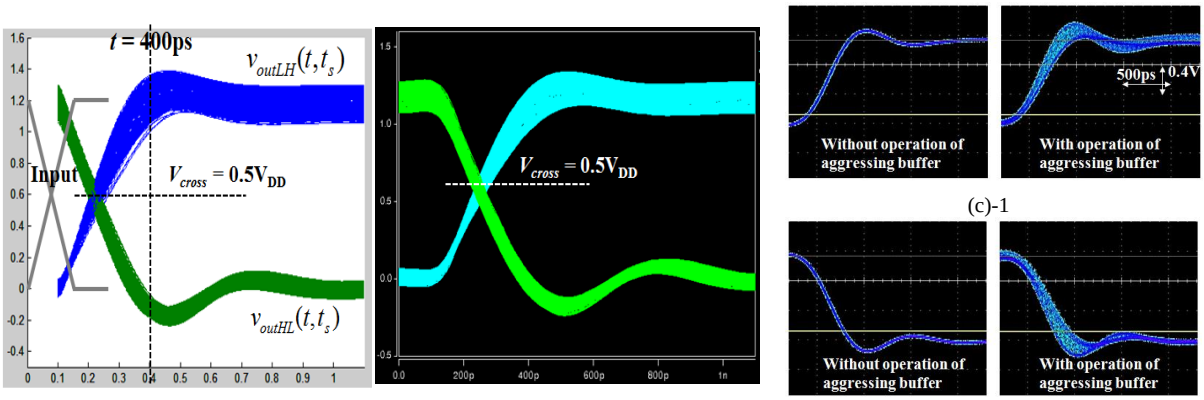
그림 1 (a) C-band 마이크로파 스위치 모식도, (b) 측정결과

[1] Byung-Wook Min, Gabriel M. Rebeis "5-6 GHz SPDT Switchble Balun Using CMOS Transistors," IEEE RFIC Symp. Dig, pp. 321-324, April. 2008 Nano, in press (2013).

Step Response Calculation of a Single-Ended Buffer with Arbitrary Power-Supply Voltage Fluctuations

Eunkyeong Park, Junho Lee, Jingook Kim
School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, Ulsan-gil 50, Ulsan 689-798, Republic of Korea
E-mail : jingook@unist.ac.kr

Design of today's I/O interfaces is becoming increasingly important as the I/O speed increases up to multi-gigabit data rates [1]. One of the significant signal integrity factors is supply voltage fluctuation. The supply voltage fluctuations can cause significant delay changes and amplitude uncertainty in the output voltage of a transmitting or receiving buffer. The expressions for the output waveform of a single-ended inverter buffer with supply voltage fluctuations are derived, including a parasitic inductance in the interconnection to a capacitor load. Arbitrary supply voltage fluctuations can be represented as a Fourier series of frequency, and the output waveform of the buffer can be analytically solved by combining the contributions of all the frequency harmonics. The output transitions of a single-ended buffer can be analytically formulated using the piecewise linear models of MOSFETs. To validate this analytical methodology, a silicon IC with noise-aggresising and victim buffers is designed, fabricated and assembled in a PCB. The overall power distribution network (PDN) of the IC and PCB was modeled from impedance measurements. The results of the step pulse response of the victim buffer with power-supply voltage fluctuations were calculated and validated by comparisons with HSPICE and experimental results as figure.1.



(a) (b) (c)-1 (c)-2

Fig.1 Multiple output transitions Eye diagram from (a)Calculation, (b)HSPICE simulation and (c)-1 Measurement pull up transitions (c)-2 Measurement pull down transitions

[1] J. Fan, X. Ye, J. Kim, B. Archambeault, and A. Orlandi, "Signal integrity design for high-speed digital circuits: progress and directions," *IEEE Transactions on Electromagnetic Compatibility*, vol. 52, no. 2, pp. 392-400, May 2010.

This work was supported by the IDEC.

초소형 센서노드를 위한 MPPT 제어기능을 갖는 삼중입력 에너지 하베스팅 회로 설계

윤은정, 박종태, 유종근
인천대학교 전자공학과
E-mail : unyuj@incheon.ac.kr

에너지 하베스팅은 빛, 진동, 열 등 주변의 버려진 에너지를 전기에너지로 변환하여 사용하는 기술로써 이에 대한 연구는 빛, 진동, 열 등 단일 에너지원을 이용한 연구가 주를 이루고 있다. 에너지 하베스팅을 하기 위한 에너지 변환소자에는 최대 가용 전력점이 있고 이를 출력하기 위해서는 Maximum Power Point Tracking(MPPT)이 필요하다[1-2].

그림 1 은 제안된 삼중입력 에너지 하베스팅 회로의 전체 블록도이다. 각 에너지 하베스팅 회로는 각각 MPPT 제어기능을 갖고 있으며 에너지 변환소자의 개방회로전압과 MPP 전압간의 연관성을 이용하여 간단히 구현하였다. 각각의 Energy MPPT Control 회로에 의해 각 에너지원의 MPP 에서의 전력이 charge pump(CP)로 공급되며 이를 통해 CP 는 센서노드가 동작 가능한 전압(ex: 3V)으로 승압하여 C_{STO} 에 저장된다. 이렇게 빛, 진동 및 열 에너지로부터 수확되어 승압된 에너지는 실시간으로 C_{STO} 에 병합되어 Power Management Unit 에 의해 제어되어 센서노드로 공급된다.

그림 2 는 단일, 이중 그리고 삼중입력의 경우에 에너지 하베스팅 회로의 CP 가 출력한 전압을 비교한 그림이다. 모의실험 결과 승압되기까지 시간이 삼중입력 에너지 하베스팅의 경우가 가장 많은 에너지를 공급하기 때문에 가장 짧았다.

설계된 회로는 각각의 에너지원을 MPPT 제어를 통해 동시에 실시간 병합할 수 있기 때문에 환경 변화에 덜 민감하다는 장점을 갖는다. 설계된 회로는 요구되는 duty rate 가 비교적 낮으며, 빛과 진동 에너지를 동시에 얻기 쉬운 다리와 같은 구조물 모니터링과, 산림 등의 환경모니터링에 적용될 수 있다.

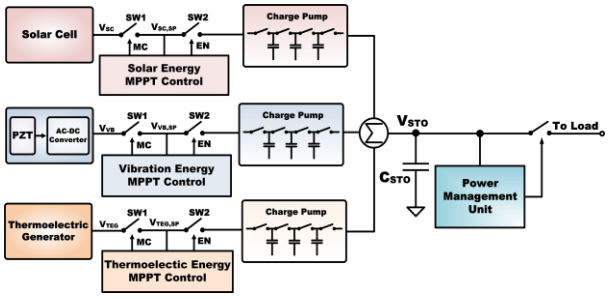


Fig. 1. Triple-input energy harvesting circuit

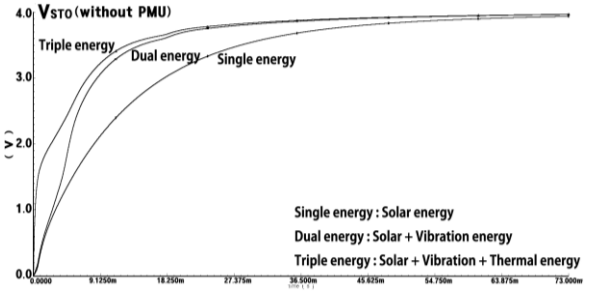


Fig. 2. Comparisons of energy harvesting circuits

[1] D. Dondi, A. Bertacchini, L. Larcher, P. Pavan, D. Brunelli, and L. Benini, "A solar energy harvesting circuit for low power applications," *IEEE ICSET*, pp. 945-949, 2008.
[2] I. Doms, P. Merken, C. Van Hoof, and R. P. Mertens, "Capacitive Power Management Circuit for Micropower Thermoelectric Generators With a 1.4 uA Controller," *IEEE JSSC*, pp. 2824-2833, 2009.

MEMS 가속도센서를 위한 CMOS Readout 회로

윤은정, 박종태, 유종근
인천대학교 전자공학과
E-mail : unyuj@incheon.ac.kr

MEMS 는 마이크로미터 크기의 전자적, 기계적 요소들이 결합된 시스템으로 일반적인 반도체 제조기술을 기반으로 MEMS 공정을 이용한 가속도 센서는 가장 많이 응용되고 있는 부분 중의 하나이다[1]. 이 중 용량형 가속도 센서는 CMOS 회로와 집적화가 가능하고 낮은 전력 소비, 온도 특성 그리고 DC 특성이 좋지만 기생 커패시터의 영향이 크기 때문에 이에 대한 신호의 왜곡 및 제한을 보상할 수 있는 방법이 필요하다[2].

그림 1 은 본 논문에서 제안하는 MEMS 가속도센서를 위한 Readout 회로(ROIC)의 블록도이다. 가속도 센서는 MEMS 공정으로 제작된 용량형 가속도센서로 센서에 가속도가 가해지면 센서의 커패시턴스가 변화하고, 변화된 센서의 커패시턴스는 C-V 변환기에 의해 커패시턴스에 따른 전압으로 변환된다. ∑⊿변조기는 변환된 전압을 디지털 신호로 변환하여 가속도에 따른 듀티 싸이클이 다른 디지털 신호를 출력하도록 한다. 이때 CVC 와 ∑⊿변조기에는 Chopper-Stabilization 와 Correlated-Double-Sampling 기법을 적용하여 저주파 노이즈와 DC 오프셋을 최소화 하였다.

그림 2 는 제작된 ROIC 의 측정파형이다. CVC 의 센서 커패시턴스의 변화가 Δ0pF 일 때 49.5%의 듀티 싸이클을 출력하였고, Δ0.5pF 일 때에는 58.6%, Δ1pF 는 68.2% 그리고 Δ1.5pF 일때는 77.7%의 듀티 싸이클을 출력하였다. 약간의 오차는 있지만 CVC 의 센서 커패시턴스가 0.5pF 씩 증가할 때, 듀티 싸이클은 10% 증가하였다.

본 논문에서 제안된 회로는 MEMS 가속도 센서와 함께 집적화됨으로써 소형화된 하나의 칩으로 제작이 가능하므로 휴대 기기 및 소형기기 등 많은 응용분야에 적용이 가능할 것으로 기대된다.

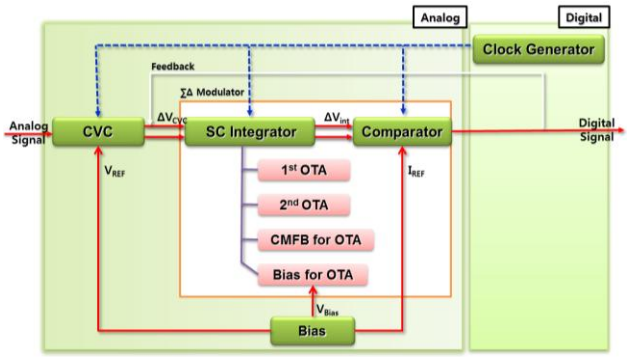


Fig. 1. CMOS ROIC for MEMS Acceleration Sensor

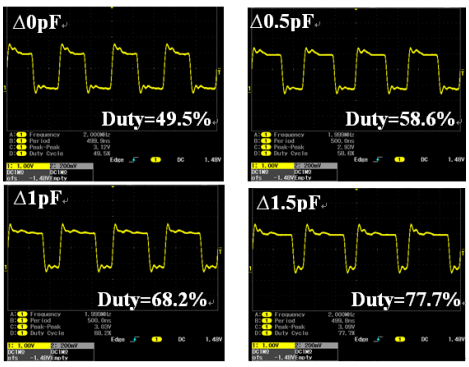


Fig. 2. Measurement Results of the designed chip

[1] 박현식, "휴대전자 기기의 가속도 센서 기술," 정보통신산업진흥원, 2007.
[2] K. Xiaofei, "A fully-differential Chopper-Stabilized Sigma-Delta Interface for Micro Accelerometer," ICMET, pp 726 - 729, 2010.

MPPT 제어 기능을 갖는 열에너지 하베스팅 회로

윤은정, 박종태, 유종근
인천대학교 전자공학과
E-mail : unyuj@incheon.ac.kr

열에너지는 주변에서 발생하는 에너지들 중 하위 에너지로써 에너지 손실 대부분이 열에너지로 나타나고 있다. 이러한 에너지를 전기에너지로 변환하는 에너지 하베스팅 기술을 통해 전기 에너지로 변환한다면 열에너지는 전력공급이 가능한 에너지원으로써 무한한 가치를 가질 것이다. 이러한 열에너지를 하베스팅 하기위해선 열전소자가 필요하고 열전소자에는 최대 전력을 출력하는 MPP(Maximum Power Point)가 존재한다[1].

그림 1 은 본 논문에서 제안하는 MPPT 제어기능을 갖는 열에너지 하베스팅 회로의 블록도이다. 설계된 회로는 열전소자, TEMC 등으로 구성되어 있다. 열전소자(TEG)는 열에너지를 전기에너지로 변환하는 역할을 하며, 열전소자의 MPP 전압은 개방회로전압의 0.5 배 관계에 있다[2]. TEMC 는 열전소자의 개방회로전압과 MPP 에서의 전압간의 비례관계를 이용하여 열전소자의 출력전압이 MPP 근처에서 동작하도록 하는 MPPT 제어 기능을 하며, TEMC 에 의해 생성된 MPPT 기준전압들을 통해 'EN' 신호를 출력하여 열전소자로부터 수확된 에너지를 부하로 공급하는 역할을 한다.

그림 2 는 제작된 칩을 부하저항을 바꾸어가며 V_{Load} 와 EN 신호를 측정한 파형이다. EN 에 따라 부하로 전력공급이 되었고, 부하저항의 크기에 비례하여 듀티 싸이클이 증가하는 것을 확인할 수 있다. 이는 부하저항이 증가하면 부하에서 소모되는 전력이 감소하기 때문에 전력이 감소하는 시간이 길어져 듀티 싸이클이 증가하는 것이다.

본 논문에서는 0.35um CMOS 공정을 이용하여 MPPT 기능을 갖는 열에너지 하베스팅 회로를 설계하였다. 이를 이용하여 보조 발전기로써 다시 공급함으로써 연료 소모를 줄이고 연비를 향상시킬 수 있는 효과를 볼 수 있다.

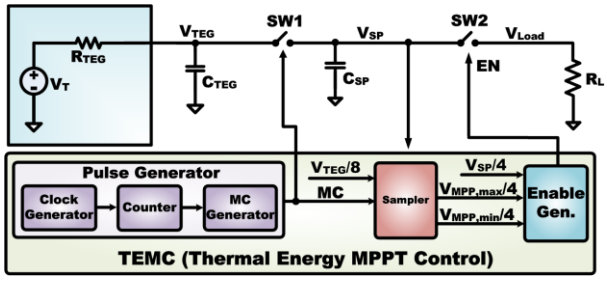


Fig. 1. Thermal Energy Harvesting Circuit

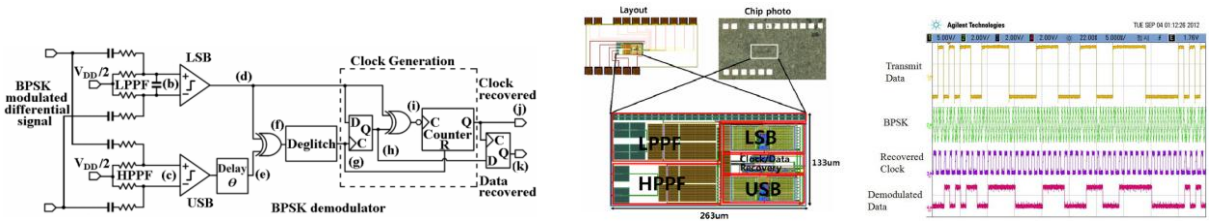
Fig. 2. V_{Load} & EN at different load resistance

[1] I. Doms, P. Merken, C. Van Hoof, R.P. Mertens, "Capacitive Power Management Circuit for Micropower Thermoelectric Generators With a 1.4 μA Controller", IEEE Solid-State Circuits Society, pp 2824-2833, 2009.
[2] Tellurex Thermoelectric Energy Harvester—G1-1.0-127-1.27, Tellurex [Online].

Low power Non-Coherent BPSK recovery circuit for Implantable Biomedical Devices

Tae-Gwon Yun, Benjamin P. Wilkerson, Jin-Ku Kang
Dept. of Electronic Engineering, INHA University
jkang@inha.ac.kr

In a wireless data transceiver system design for implantable biomedical devices, the power consumption of the circuit should be as low as possible. For data modulation, a PSK(Phase Shift Keying) demodulator is usually used in a coherent way. But it usually requires a power hungry phase-locked loop(PLL) block. The proposed non-coherent BPSK demodulating scheme adopts the dual band filtering with additional timing generator to find the symbol. In proposed scheme, the BPSK modulated signal is first processed by marching through the LSB(Lower Side Band) and the USB(Upper Side Band) paths. The outputs from the LSB and USB comparators are used for further processing to find recovered clock. While processing with two filters, the LPPF and the HPPF causes the phase shift on the output. The phase difference between two paths is about 90 degrees with a small variation on a targeted frequency. By processing two outputs from the LSB and USB with additional digital circuits, the data boundaries can be derived with edge pulses. By combining the LSB output with the intermediate data, the carrier signal is generated. Then the clock and the demodulated data could be derived with low power consumption. The proposed circuit has been designed with a 0.18-um technology. The carrier frequency is 2MHz and the data rate is 1Mbps.



(a) (b) (c)

Fig 1.(a) Proposed BPSK demodulator (b) Layout and chip photo (c) Measured waveforms

[1] Y. Hu and M. A. Sawan, " A Fully Integrated Low-Power BPSK Demodulator for Implantable Medical Deivces," *IEEE Tran. Circuits Syst. I, Reg. Papers*, vol. 52., no. 12, pp.2552-2562
[2] C.-S. A. Gong, M,-T. Shiue, K.-W. Yao, and T.-Y. Chen, "Low-power and area-efficient PSK demoulator for wirelessly powered implantable command receivers," *Electron, Lett*., vol. 44, no. 14, pp.841-842, 2008
[3] F. Asgarian and A. M. Sodagar, " A High-Data-Rate Low-Power BPSK Demodulator and Clock Recovery Circuit for Implatnable Biomedical Devices," *IEEE EMBS Conf*., pp. 407-410, 2009.

Design of High Dimming Ratio Power-LED Driver with Preloading inductor current methodology

Woo-Seong Kang, Tae-Jin Jeong, Ji-San Choi, and Gwang-Sub Yoon
Department of Electronic Engineering, Inha University, Incheon, Korea
E-mail : ksyoon@inha.ac.kr

Recently, high-power LEDs are grabbing the attention of many automotive designers by providing numerous advantages [1]. We investigated the preloading inductor current method that it is employed to augment much more simply the transient response of the Power–LED driver. When adjust the brightness of LED by ordering to turn it on or down, depending on the dimming signal with the fixed current form LED. The dimming signal contains information about the current flowing on the LEDs, we can utilized to predict the amount of the current on the inductor. So the inductor current can be preloaded to minimize the rising time of the LED driving current. Based on the dimming signal synchronized, recreate the dimming signal delayed as much as the switching cycle did. It's negotiable to decide the cycle how does it have to be delayed, according to equation (1).

, where η is the power conversion efficiency, Dmax is the maximum duty ratio on the LED driver. Since the inductor current has been already preloaded, the forward current of the LED-string has no difficulty to enter the steady state without ringing. At this moment, the voltages sense from the array of output resistances are saved in the Variable Reference Voltage Generator (VRVG).

Fig 1. The block diagram of the proposed Power-LED driver system

[1] D.Gacio, J.Cardesin, E. L. Corominas, J. M. Alonso, M Dalla-Costa and A. J. Calleja, IEEE (2008)

Design of a 3rd order Delta-Sigma Modulator with a Frequency Detector Circuit

Han-Ul Lee, Su-Hun Yang, Gi-yoon Lee, and Gwang-Sub Yoon
Department of Electronic Engineering, Inha University, Incheon, Korea
E-mail : Oulmandoogmail.com, chunjasuhun@hanmail.net, lky2420@naver.com ksyoon@inha.ac.kr

Today, due to the development of science and technology, interests for human health is increasing rapidly and bio signals such as electroencephalogram(EEG) and electromyogram(EMG) are studied variously [1]. It is more increased to utilize multiple bio signals simultaneously rather than to utilize each bio signal separately. Especially, EEG and EMG signals are mainly used at a time to measure and to analyze bio signals. Meanwhile, developments of the ADC processing bio signals are in progress in many ways. However, ADCs optimized for EEG and EMG signals cannot be used at the same time because of the differences in the frequency band of EEG and EMG signals . According to the trends making the products portable in the medical field, the circuit design techniques for integration and low power are required to process EEG and EMG signals simultaneously.

The input signal goes through the frequency detector and the output signal of the frequency detector controls selection of the integrator of modulator. If the input signal frequency is greater than the reference frequency, (that is, EMG signal) the output signal of the frequency detector selects the high performance operational amplifier within the first integrator. On the other hand, if the input signal frequency is lower than the reference frequency, (that is, EEG signal) the output signal of the frequency detector drives the low performance operational amplifier within the first integrator. The proposed circuit reduces the power consumption by shutting down the operational amplifier which is not used.

The frequency detector circuit enables the first integrator to select either high performance or low performance operational amplifier, depending on the input frequency. This circuit allows the modulator to optimize the dynamic performance to process both EEG and EMG. The simulated performance of the proposed modulator shows SNDR of 98dB and ENOB of 16bit with the supply voltage of 1.8V, at the conversion rate of 256 KHz and input frequency of 1 KHz.

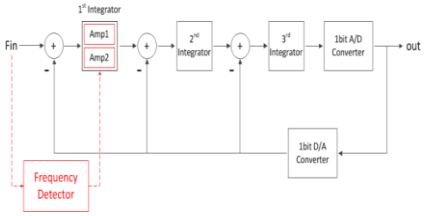


Fig 1. The block diagram of the proposed

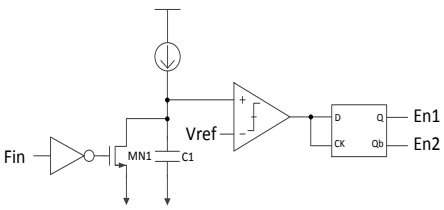


Fig 2. Frequency detecting circuit

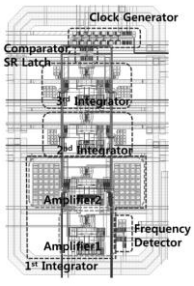


Fig 3. layout

[11] J. [1] Ha-Chul Jung; Jin-Hee Moon; Dong-Hyun Baek; Jae-Hee Lee; Yoon-Young Choi; Joung-Sook Hong; Sang-Hoon Lee; , "CNT/PDMS Composite Flexible Dry Electrodesfor Long-Term ECG Monitoring," Biomedical Engineering, IEEE Transactions on , vol.59, pp.1472-1479, May 2012.

Hardware Implementation of Keypoint Detection Block in SIFT

Byungjun Choi [1] , Sangyoung Lee [2] , Dong Sun Park [3] , Jong Yeol Lee [4]

Department of Electronic Engineering, Chonbuk National University, Jeonju 561-756, Korea [1,2,3,4]

gogocbj@naver.com [1] , lsy564@hanmail.net [2] , dspark@jbnu.ac.kr [3] , jong@jbnu.ac.kr [4]

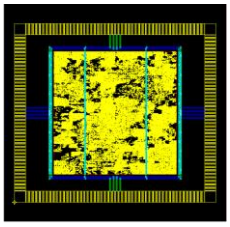
The SIFT(Scale Invariant Feature Transform) is an algorithm which detects not only the invariant keypoints such as image scale and rotation but also illumination change. This algorithm is being utilized in various fields such as object recognition, panoramic screen-making, 3D image restoration and face recognition[1]. However, its operational processing speed is slow in a software environment due to its characteristics of repeating complex operations such as convolution and removal of keypoint. SIFT is mainly composed with three stages : keypoint detection, description and matching. The main purpose of our research is to compare with the processing time of ASIC in a software environment by constructing the keypoint detection into ASIC which has heavy computation time in the process.

17-by-17 tile image is needed to get the keypoint and the center pixel of the image is position of the keypoint. For the large sized image, keypoint is detected by loading images per tile. The detection stages are composed of convolution, DoG(Difference of Gaussian), DoE(Decision of Extrema), and removal of keypoint.

As executed in the 320-by-240 image, The outcome is shown in Fig 1. and Chip information is shown in Fig 2.

(a) (b)

Fig 1. (a) Software Simulation Result Image, (b) VGA Monitor Display Result Image



Total area : 4785445.085403
Operating Frequency : 50Mhz

Fig 2. Chip information

As a result of measuring the average execution time for 17-by-17 image, ASIC is about 28 times faster than PC as shown in Table 1.

Table 1. Operation Time for SIFT Feature Detection.

Unit : μs

	Convolution & DoG	Decision of Extrema	Elimination	Total
PC (fixed point)	188.429	523.004	441.310	1152.743
ASIC (fixed point)	40.530	0.560	0.480	41.570

PC : Intel i5-2450m 2.50GHz, ASIC : 50MHz(0.18 μm)

[1] D. G. Lowe, “Distinctive Image Features from Scale-Invariant keypoints”, International journal of Computer Vision 60(2), 91-110, 2004.

Cognitive Radio 시스템의 NC-OFDM을 위한 저전력 FFT 설계

박서진 정진균

전북대학교 전자공학부

OFDM 시스템에서 FFT(Fast Fourier Transform)는 전력 소모 및 면적 면에서 큰 부분을 차지하는 블록 중 하나이므로 효율적인 FFT의 구현은 OFDM 시스템의 성능향상에 큰 영향을 끼친다. OFDM 송신기에서 주사용자가 사용하고 있는 대역의 subcarrier 에는 데이터를 보내지 않는다. 따라서 사용 대역에 해당하는 FFT 입력은 '0' 으로 할당한다[0]. 본 논문에서는 CR 시스템에 사용되는 FFT의 경우 '0' 입력이 많다는 사실에 근거하여 덧셈 및 곱셈 연산 회로를 제어하여 FFT에서 소모되는 전력을 감소시킬 수 있는 방법을 제안한다. [그림 1]과 같이 FFT의 덧셈, 뺄셈 및 곱셈 연산에 입력신호가 '0' 임을 나타내는 Zero Flag신호를 제어 신호로 작용하여 연산횟수를 감소시킬 수 있다. [표 1]에 Zero flag에 따른 연산의 종류 및 구조를 나타내었다. Case i의 경우 현재의 입력과 이전입력이 '0' 임을 의미 하므로 계산 없이 '0' 을 출력하고 현재의 Zero flag는 '0' 을 유지한다. Case ii와 iii의 경우는 두 입력 중 하나의 입력이 '0' 이므로 덧셈/뺄셈에서는 해당 입력을 bypass하고 곱셈 연산은 수행한다. 마지막으로 Case iv의 경우는 기존의 FFT와 동일하게 연산을 수행한다. 제안된 방법으로 FFT를 구현할 때, 입력 값에 '0' 신호가 들어오게 되면 기존회로와 달리 Zero Detection 스테이지에서 '0' 신호를 검출한다. Zero flag신호는 FFT를 수행하는 나머지 스테이지의 enable신호가 되어 덧셈, 곱셈 연산을 제어하게 된다.

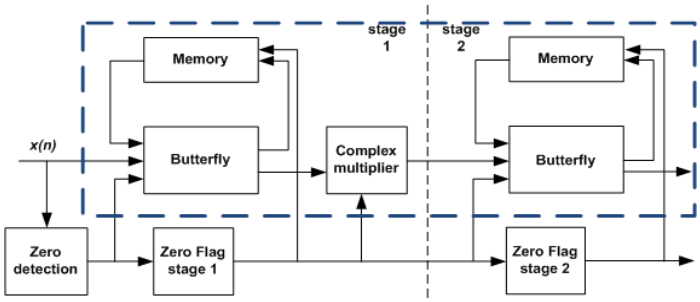


그림1. 제안된 저전력 FFT구조

Case	Zero flag_$i(n)$	Zero flag_$i-1$ $(N/(2i)+n)$	New Zero flag	덧셈/뺄셈 연산	곱셈 연산
i	0	0	0	'0' 출력	'0' 출력
ii	0	1	1	bypass	연산
iii	1	0	1	bypass	연산
iv	1	1	1	연산	연산

표1. Zero Flag의 조합에 따른 연산표

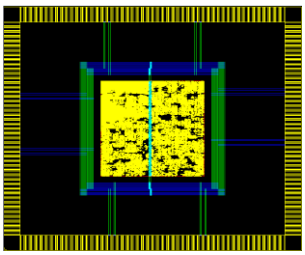


그림2. 최종 layout

[0] In-Gul Jang and Jin-Gyun Chung, "Low-Power FFT Design for NC-OFDM in Cognitive Radio Systems", 2011

[1] S. Haykin, "Cognitive Radio: Brain Empowered Wireless Communications", *IEEE Journal on Selected Areas In Communicarions,* No.2, Vol 23, Feb 2005.

[2] J. Mitola, III, "Cognitive radio for flexible mobile multimedia communications," in *Proc. IEEE Int. Wksp. Mobile Multimedia Commun.*, vol. 1,(San Diego, CA, USA), pp.3-10, Nov. 1999.

Implement of Ring Oscillator for ISM bandwidth

Moonho Lee, Hanggeun Jeong
Chonbuk National University, Korea

The frequency synthesizer consists of PFD(Phase Frequency Detector), charge pump, VCO(Voltage Controlled Oscillator), loop filter, and programmable divider. The tri-state PFD is designed and the two amplifiers are used in the charge pump. The VCO consists of the differential buffer delay stages with symmetric load and replica-feedback biasing. The loop filter is realized by off-chip circuit and the pulse swallow method is used in the divider.

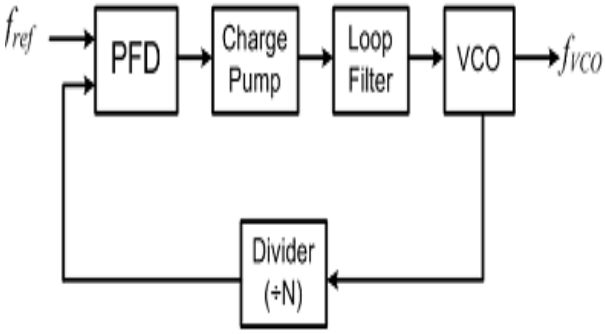


Fig 1. Circuit of PWM boost converter

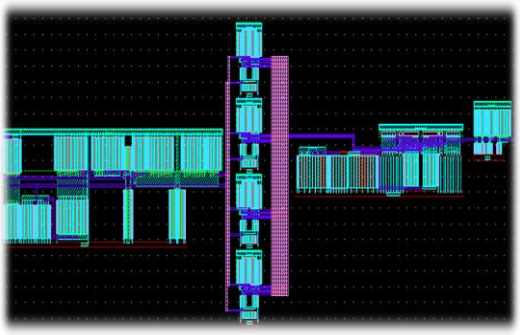


Fig 2. Top Layout

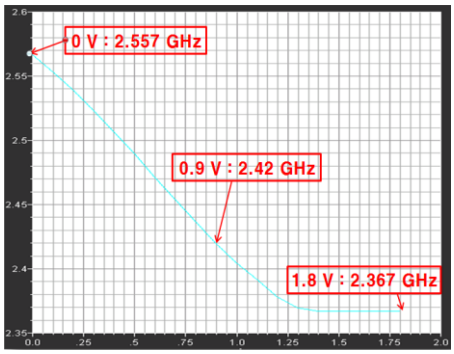


Fig 3. Simulation

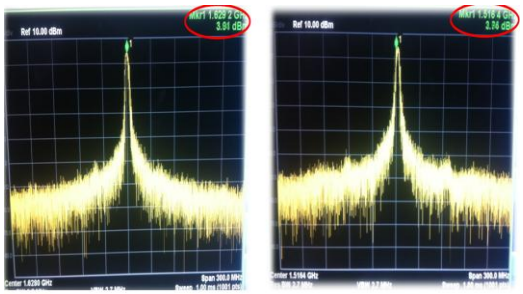


Fig 4. Chip Test

[1] Behzad Razavi 저 김대정, 이강윤, 이종창 역 “아날로그 CMOS 집적회로 설계” : 한빛미디어㈜, 2009.

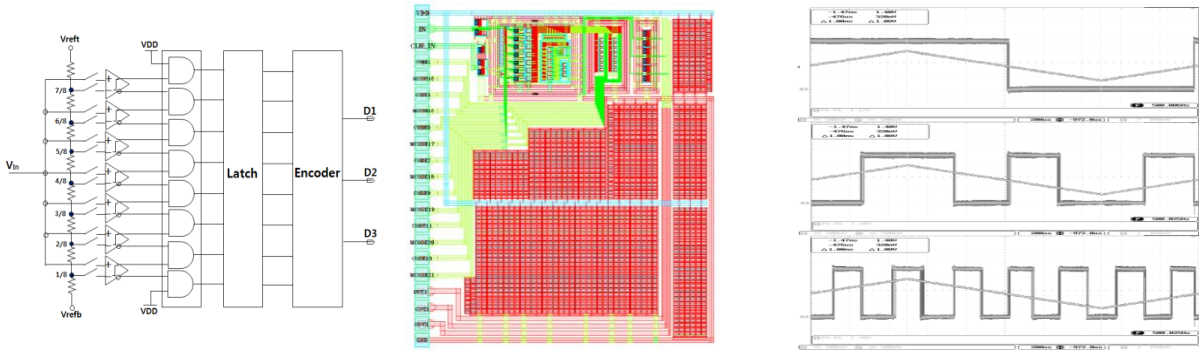
[2] R. E. Phase-locked Loops, Second Ed., New York : McGraw-Hill, 1993.

[3] J. S. Crawford, Frequency Synthesizer Design Handbook, New York : Artech House, 1994.

Implement of 3-Bit Flash A/D Converter in 0.18 um CMOS

Junsik Park, Sanghun Jung, Minji Han, Sungik Cho
Department of Electronic Engineering, Chonbuk National University, Jeonju 561-756, Korea
E-mail : junsik890221@jbnu.ac.kr

High speed and accuracy signal processing system between analog and digital domain are very important because it influences the overall system performance. Analog to Digital Converter (ADC) is one of basic component of this system providing bridge between analog and digital domain system. This paper describes a design of 0.18 μm CMOS 3-Bit Flash ADC for high speed and low voltage applications. Fig. 1 (a) shows a block diagram of conventional Flash ADC. It requires 2^{n-1} comparators and 2^n resistors for "N" bit conversion. Each comparator is working in every clock cycle and produces as "1" when its analog input voltage is higher than the reference voltage applied to it. The outputs of comparators form a thermometer code (TC) which is a combination such as 000…011…111. For digital signal processing, TC is transformed to a binary code through a ROM circuit at final stage. Fig. 1 (b) shows the layout of 3-Bit Flash ADC. The designed structure of 3-Bit Flash ADC has been implemented in a CMOS 0.18μm technology and the simulation is performed by using Cadence Spectre simulator. The supply voltage and the input range are set as 1.6V and 1.0V, respectively. Fig. 1 (c) shows the measurement results of the fabricated chip. Here, the input signal is falling 1.6V to 1.0V and output signal can be obtained paralleled binary code such as 111, 110, 101… 001, 000.



(a) (b) (c)

Fig 1. Proposed Flash ADC (a) Block diagram of Flash ADC (b) Layout (c) Measurement result

[1] M. Subba Reddy, C. Md. Aslam, "Low Power Flash ADC", *International Journal of Computer Applications in Engineering Sciences*, vol. 1, issue 2, pp. 108-111, June 2011
[2] Koen Uyttenhove, Michiel Steyaert, "A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25μm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 1115-1122, July 2003

2bit MDAC for Pipelined ADC in 0.18um CMOS

Seyoung Oh, Hyundeok Kim, Sungik Cho
Chonbuk National University, Korea

본 설계는 Pipeline ADC의 블록 중 MDAC을 설계 하였다. 각 stage는 전 stage의 출력을 샘플링(Sampling)하고, Flash ADC를 사용하여 n비트의 디지털 코드로 양자화 한다.

Flash ADC를 통해 출력된 디지털 코드는 n비트 DAC에 의해 아날로그 신호로 변환되고, 샘플링된 신호와의 차이인 잔류전압을 발생하게 된다. 그리고 잔류전압은 2^n배 만큼 증폭 후 다음 스테이지로 넘어가게 된다.

Pipelined ADC 는 일반적으로 모든 블록들이 연속적인 입력신호에 대해 출력을 생성하여 빠르게 동작하고, 비교기가 적어 면적 및 전력소모도 줄일 수 있는 장점이 있다.

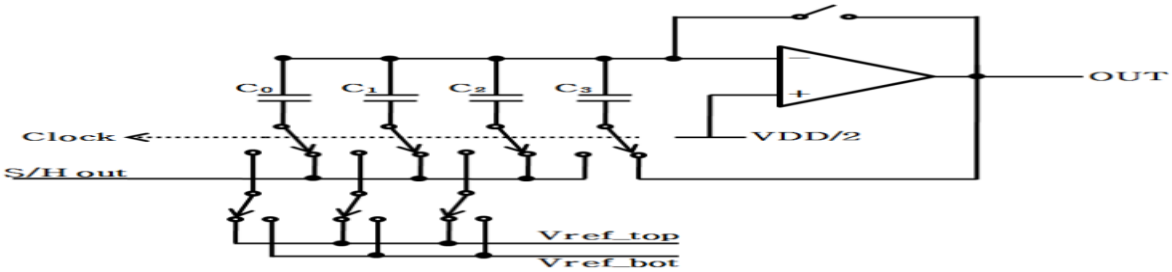


Fig.1 MDAC Block diagram

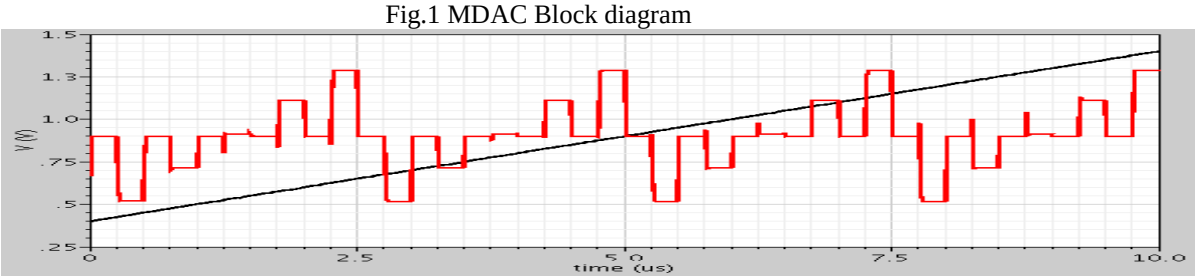


Fig.2 Post simulation Result

이승훈, 김범섭, 송민규, 최종호. “CMOS 아날로그/혼성모드 집적시스템 설계(하)”, 시그마 프레스, 1999

박홍준, “CMOS 아날로그 집적회로 설계(상)(하), 시그마프레스, 1999

Lee Seung-woo, “A Low Power 1.8V 10-Bit 50Msample/s Pipeline Analog to Digital Converter”, August, 2002

CIFB 구조를 갖는 저전력 3차 시그마-델타 변조기

Minwoong Lee, Sanghun jeong, Jaebung Kim, and Seongik Cho
Div. of Electronic & Information Engineering, Chonbuk National University, jeonju 561-756, Korea
E-mail : minwoong@jbnu.ac.kr

SDM(Sigma-Delta Modulator)의 성능은 SNR (Signal to Noise Ratio)로 나타내며 잡음이 작을수록 고성능 SDM을 구현할 수 있다. 잡음을 줄여 SDM의 성능을 높이기 위한 방법들은 많은 전력소모가 필요할 뿐만 아니라 면적 면에서도 비효율적이다. 본 연구는 이러한 단점을 보완 할 수 있는 저전력 고해상도 SDM을 설계한다. SDM의 1차 적분기는 연산증폭기의 전력소모가 작은 저전력 스위치드-커패시터 적분기 회로를 사용하였고[1], 2차 적분기는 지연된 피드백 경로를 추가하여 적분기 1개로 2차 SDM을 구현하였다[2]. 또한 입력에서 지연된 피드포워드 경로를 추가시켜 1차 적분기의 출력스윙을 최소화함으로써 적분기에 사용되는 적분 커패시터의 개수를 줄였다. 따라서 SDM에서 가장 많은 전력이 사용되는 증폭기의 전력소모를 최소화 하였다. 본 연구는 공급전압 1.8V, 입력신호 1Vpp/1KHz, 신호대역폭 20KHz, 샘플링 주파수 2.8224MHz에서 실험하였고, 그 결과 그림. 1과 같이 SNR은 87.1dB이며 ENOB(Effective Number of Bits)는 14-비트 이고 전력소모는 0.2mW이다. 칩은 0.18um CMOS 공정을 이용하여 제작되었고, 레이아웃의 면적은$1mm^2$이다.

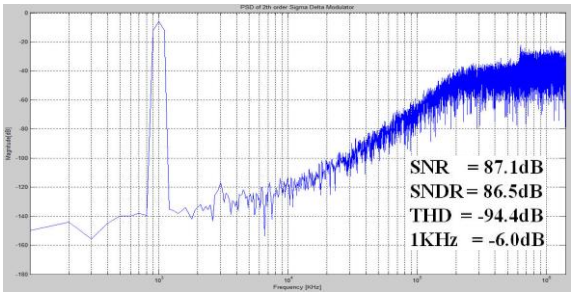


Fig 1. Results of PSD(Power Spectral Density)

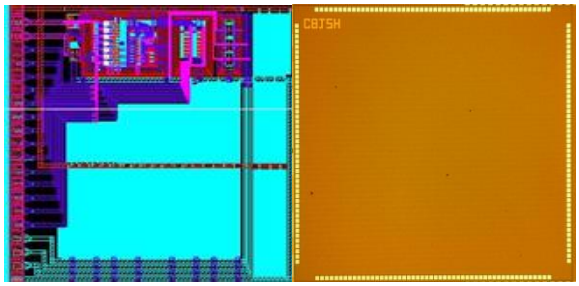


Fig.2 SDM layout and chip

[1] A. Nilchi and D. A. Johns, "Charge-pump based switched-capacitor integrator for modulators," Electron. Lett., vol. 46, no. 6, pp. 400–401, Mar. (2010)

[2] A. Pena-Peres, E. Bonizzoni and F. Maloberti, "A 88-dB DR, 84-dB SNDR Very Low-Power Single Op-Amp Third-Order ∑△ Modulator," IEEE J. Solid-State Circuits, vol.47, no.9, pp.2107-2118, Sep. (2012)

Band Pass Filter with Pseudo-Resistor for Biosensor signal detection

Nam Pyo Hong, Chung-Gun Kim, and Young Wan Choi
School of Electrical and Electronics Engineering, College of Engineering, Chung-Ang University, Seoul 156-756, Korea
E-mail : ychoi@cau.ac.kr

현재 의료의 패러다임이 치료에서 예방과 진단으로 변화하면서 바이오 센서에 대한 관심이 높아지고 있으며, 바이오 센서와 IT 융합기술을 적용하여 의료분야에 적용하기 위한 연구개발이 활발히 진행되고 있다. 바이오 센서는 크게 3 가지로 구분될 수 있다. 환경 호르몬, 암세포 등 특정 물질에 대하여 확인 하거나 감지 할 수 있는 바이오 소자, 생체 감지 물질 (bioreceptor), 신호변환기 (signal transducer)로 구성되어 있다. 이러한 바이오 센서를 구현하는데 있어 소자 이외에도 저전력, 고집적화, 고성능의 특성을 갖는 집적회로 시스템을 구현 해야 한다 [1]. 그림 1 은 바이오 센서 신호 검출을 향상 시키기 위해 band pass filter(BPF)을 설계하였다. 차동 증폭기에 pseudo-resister 와 피드백 커패시터를 이용하여 BPF 의 이득과 컷 오프를 결정할 수 있다. 이를 이용하면 시스템 전체의 노이즈 레벨을 감소 시킬 수 있는 장점을 갖는다. 스위치 (S1, S2)를 on/off 시켜 이득을 변화시킬 수 있다 [2]. 제작된 회로의 칩 사진과 측정 결과 및 시뮬레이션 결과를 비교하였으며 시뮬레이션과 유사한 특성을 갖는다. BPF 의 측정 결과를 보면 S1 과 S2 스위치를 제어하여 midband 이득을 결정할 수 있다. 스위치 하나만 켜졌을 때는 (S1(on), S2(off)) 39.6, 스위치 두개를 다 켰을 때는 (S1(on), S2(on)) 42.5 dB 를 갖는다. 본 논문은 IDEC 의 지원을 받아 설계되었습니다.

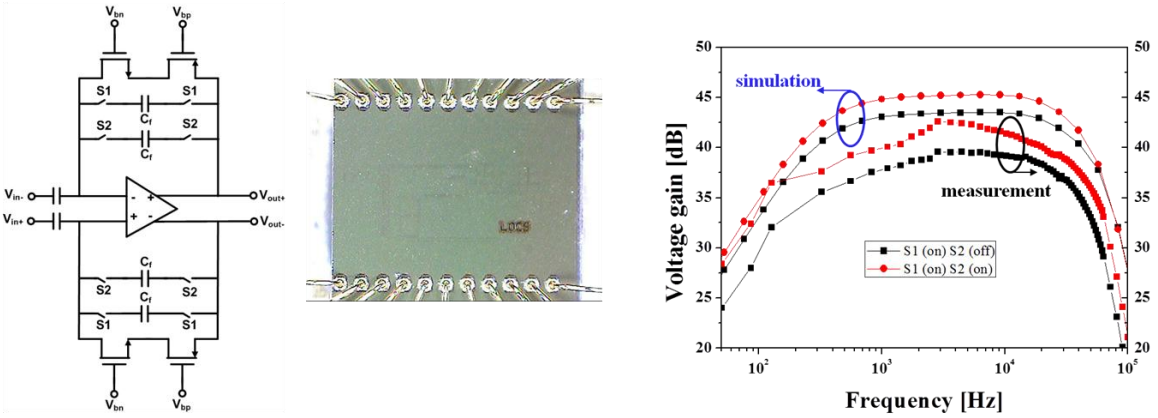


Fig 1. Band Pass Filter schematic and measurement results

[1] G. Ferri, P. De Laurentiis, A. D'Amico, and C. Di Natale, Sensor Actuat A, 92, 263 (2001).
[2] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N.V. Thakor, IEEE T Biomed Circ S, 3, 388 (2009) .

Noise analysis of CMOS pre-amplifier design

In-Il JUNG[1] and Young-Wan Choi*[2]

[1] *Rare Isotope Science Project, Institute for Basic Science, Daejeon, Korea*

[2]*School of Electrical and Electronics Engineering, Chung-Ang University, Seoul 156-756, Republic of Korea*

E-mail : ychoi@cau.ac.kr

We study an improved low noise design method of CMOS charge integrating amplifier for various detection systems. The previous reserch[1] introduced noise models of designing CMOS preamplifier and constant bias current analysis. That is helpful for design CMOS pre-amplifier, however, linearity and gain has also to be considered. Constant current analysis that we mathematically explain and calculate can cause an amplifier design with poor linearity and gain due to low transconductance. We analyze and improve the method of designing low noise circuit of CMOS charge integrating amplifier. Constant current analysis method can cause poor linearity and gain of a preamplifier due to low transconductance, and we confirm this by mathematical proof. Constant overdrive voltage analysis is proposed instead of constant current method. And also we find out that our method considerably lower down the level of thermal noise especially in case of larger size transistor than 1 micro meter. That means more small size transistor can be used as same noise performance.

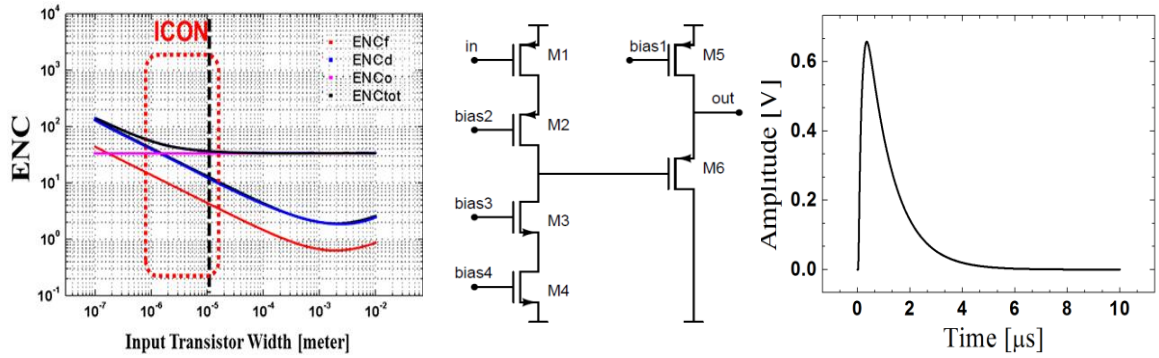


Fig 1. Constant overdrive voltage analysis (Left), the core of the preamplifier design (middle) and output waveform of preamplifier (right)

This work was supported by the IDEC.

[1] I. K.., V-M., S.L. E., J Nucl, Med, vol. 37, pp. 74P, 1996..

[2] R. T., A. R., S. T., et al., J Nucl Med, vol. 37, pp. P75, 1996.

[3] S. P., S. L., C. M., et al., Nucl Med, vol. 36, pp. 718-724, 1995.

A Light Amplitude Modulated Neural Stimulator with Photodiode for Visual Prostheses

Kyomuk Lim, Jindeok Seo, Changho Seok, Hyounho Kim, Seunghyun Im, and Hyoungho Ko*
Department of Electronics, Chungnam National University, Daejeon 305-764, Korea
*E-mail : hhko@cnu.ac.kr

The neural stimulators have been employed to the visual prostheses system based on the functional electrical stimulation (FES). Due to the size limitation of the implantable device, the smaller area of the stimulator IC is highly desired [1]. This paper presents a neural stimulator with photodiode for visual prostheses. The proposed stimulator provides the light amplitude modulated stimulation current using photodiode. In conventional concept of visual prostheses, the image information is captured by external camera, and the converted electronic signal is sent to the implanted chip, therefore, the digital analog converter (DAC) is required in the implanted chip [2-3]. The proposed stimulation scheme with on-chip photodiodes is expected to be fully implantable and to have smaller size than previous external camera system.

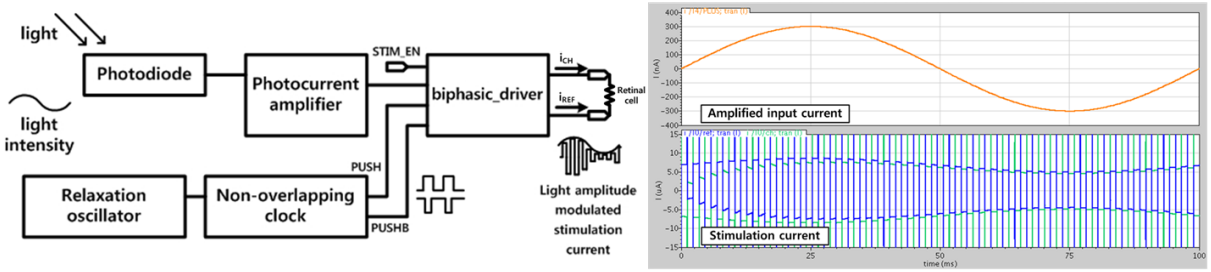


Fig 1. Top level architecture and Light amplitude modulated stimulation current

[1] M. Ortmanns, A. Rocke, M. Gehrke, and H. Tiedtke, “A 232-Channel Epiretinal Stimulator ASIC,” Solid-State Circuits, IEEE Journal of, Vol. 42, No. 12 , pp. 2946-2959, December 2007.
[2] K. Chen, Z. Yang, L. Hoang, J. Weiland, M. Humayun, and W. Liu, “An Integrated 256-Channel Epiretinal Prosthesis,” Solid-State Circuits, IEEE Journal of, Vol. 45, No. 9, pp. 1946-1956, September 2010.
[3] L. Theogarajan, “A Low-Power Fully Implantable 15-Channel Retinal Stimulator Chip,” Solid-State Circuits, IEEE Journal of, Vol. 43, No. 10 , pp. 2322-2337, Nov 2008.

9 bit SAR ADC with Kickback Noise Reduced Comparator

임승현, 서진덕, 임교묵, 석창호, 김현호, 고형호
전자공학과, 차세대전자기판회로학과
*E-mail : hhko@cnu.ac.kr

최근 휴대기기가 발전하면서 집적회로가 저전력으로 동작하고 고성능으로 동작하도록 요구되고 있다. 따라서 신호전달과정의 필수 block 인 ADC 도 이러한 흐름에 맞춰 저전력 고성능으로 동작되어야만 하며 Successive Approximation Register(SAR) 방식의 ADC 는 높은 power efficiency 로 앞서 언급한 조건들을 만족시킬 수 있어 많은 연구가 진행되고 있다.[1][2] 공급전압이 낮아지고 높은 resolution 의 ADC 를 구현하기 위해서는 미세한 전압차이를 구별할 수 있는 comparator 가 중요하다. 특히 ADC 연산과정에서 comparator 의 출력에 의한 kickback noise 는 입력신호를 왜곡시켜 digital 출력 값의 오류를 발생시킨다.[3] 따라서 본 논문에서는 kickback noise 를 감소시킬 수 있는 comparator 를 사용하였다. Fig 1. 에 kickback noise 를 줄인 comparator 를 보였다. 출력 단에서 전압이 크게 swing 하여도 switch KB_cut 이 open 되면서 입력에 대한 영향이 감소되고 또한 preamp 를 2 stage 로 구성하면서 첫 번째 단으로 영향이 직접적으로 미치지 않게 하였다.

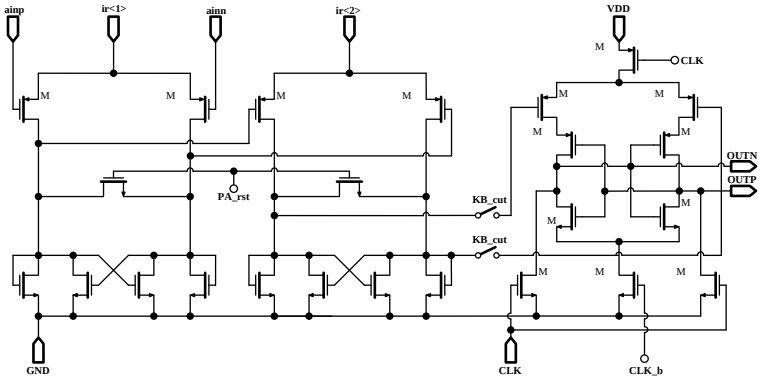


Fig 1. Kickback noise 를 줄인 comparator

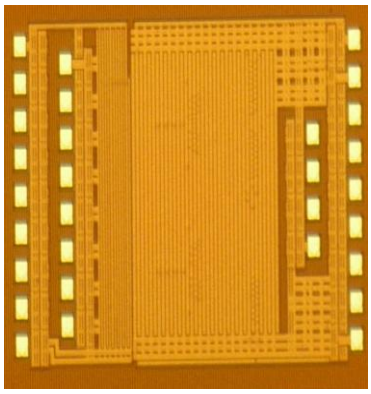


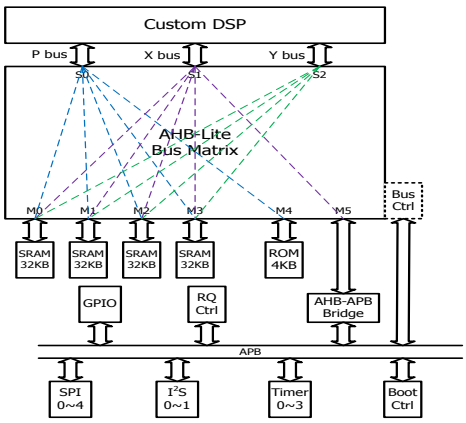
Fig2. 제작된 칩의 사진

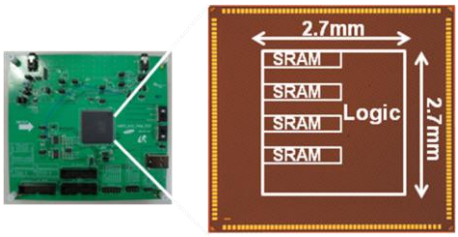
[1] V. Giannini, P. Nuzzo, V. Chironi et al., “An 820μW 9b 40MS/s Noise-Tolerant Dynamic-SARADC in 90nm Digital CMOS”, ISSCC, pp. 238-239, Feb. 2008
[2] J. Sauerbrey, D. Schmitt-Landsiedel, and R. Thewes, “A 0.5-V 1-μW Successive Approximation ADC,” IEEE J. Solid-State Circuits, vol. 38, no. 7, pp. 1261-1265, July. 2003.
[3] A. Baradaranrezaeii, R. Abdollahi, K. Hadidi et al., “A 1GS/s Low-Power Low-Kickback Noise Comparator in CMOS Process”, ECCTD, pp.106-109, Aug. 2011

A Digital Hearing Aid SoC in 65nm CMOS

Wooseok Byun, Hyeji Kim, Yeon-Tae Kim, and Ji-Hoon Kim
Dept. of Electronics Engineering, Chungnam National University, Korea
E-mail : jihoonkim@cnu.ac.kr

Many recent studies show the hearing of people at various ages is getting worse. As the market of the hearing aids expands, there have been many researches about hearing-aid implementation [1]-[3]. The proposed SoC employs the powerful custom DSP (digital signal processor), which has the scalable architecture for high throughput applications, and various peripheral IPs such as I^2S, Timer, and GPIO. All blocks including SRAMs are connected through AMBA. The custom DSP in the proposed SoC has three memory interfaces, which are the masters of the on-chip bus matrix. There are four memory macros of which size is 32KB, respectively, which are used as working memory and program memory. The custom DSP has four 64-bit vector processing units as well as 32-bit scalar processing unit. Three memory interfaces in the custom DSP are 128-bit wide and width of instruction is 64-bit. As denoted in Fig. 1, the total gate count is about 530K (NAND2 Gate Equiv.). The proposed chip has been fabricated using 65nm CMOS process and occupies 7.2mm^2 with 128KB SRAMs as shown in Fig. 1.





Block	Gate Count
Custom DSP	387K
JTAG	19K
On-Chip Interconnect	20K
Peripherals	104K
Total	530K

Fig 1. Proposed SoC Architecture / Fabricated Chip with Die Photo and Gate Count

[1] Q. Peng, H. Corporaal, and M. Lindwer, "A 0.964mW digital hearing aid system," DATE 2011, pp. 1-4
[2] S. Kim, et al., "A Fully Integrated Digital Hearing Aid Chip With Human Factors Considerations," IEEE JSSC, pp. 266-274, Jan. 2008.
[3] A. Pandey, et al., "Low-Delay Signal Processing for Digital Hearing Aids," IEEE TASLP, pp. 699-710, Apr. 2011.

Kogge-Stone 바이패싱 덧셈기 설계

안종훈, 최성림, 남병규
충남대학교 컴퓨터공학과

스마트폰의 급속한 발전에 따라 모바일 시스템의 마이크로프로세서도 빠르게 발전되어왔다. 최근에는 64 비트 모바일 마이크로프로세서가 등장하여 산술논리장치를 위한 64 비트 덧셈기는 필수적인 요소가 되고 있으며[1], 이에 따라 저전력 64 비트 덧셈기에 대한 연구가 활발하게 진행되고 있다[2].

일반적으로 마이크로 프로세서에는 처리속도가 빠른 Kogge-Stone 덧셈기가 많이 사용되고 있으나, 이는 높은 전력소모에 따른 문제를 가진다. 본 논문에서는 이를 해결하기 위해 바이패싱 (bypassing)구조를 적용하고 있는데, 바이패싱 구조는 특정입력 패턴에 대하여 입력 값을 출력으로 직접 전달하여 스위칭 전류를 차단하는 방식이다. 이 기법은 일반적으로 CSA (Carry Save Adder) 에 적용되어 왔으나[3] 본 논문에서는 이를 CPA (Carry Propagation Adder)에 적용한 Kogge-Stone 바이패싱 덧셈기를 설계하였다. 그림 1 에 Kogge-Stone 바이패싱을 위해 새롭게 제안된 캐리 생성 셀 (generation cell)의 구조와 이를 적용한 Kogge-Stone 바이패싱 덧셈기의 성능을 나타내었다.

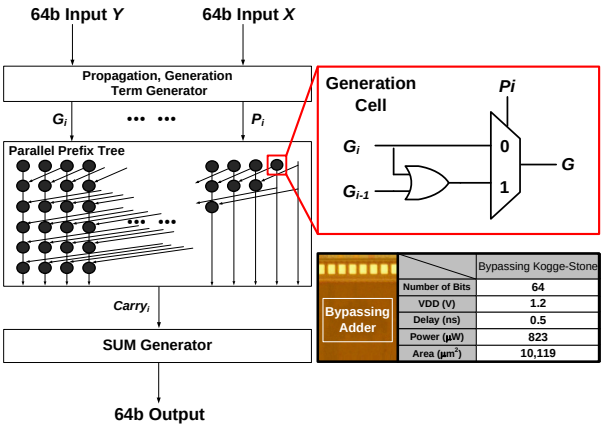


그림 1. Kogge-Stone 바이패싱 덧셈기 구조와 성능 테이블

[1] John Goodacre, “Technology Preview: The ARMv8 Architecture,” *ARM Ltd*, Nov. 2011. Available: http://www.arm.com/files/downloads/ARMv8_white_paper_v5.pdf

[2] K.Nehru et al., “Design of 64-Bit Low Power Parallel Prefix VLSI Adder for High Speed Arithmetic Circuits,” *IEEE Int. conf. Communications and Applications*, Feb. 2012.

[3] C. C. Wang et al., "Low-Power Multiplier Design using a Bypassing Technique," *Journal of Signal Processing Systems*, vol. 57, no. 3, pp. 331-338, Dec. 2009.

A capacitance multiplier using the current conveyors

Dae-Hwan Lee, Min-Su Kim, and Yeong-Seuk Kim*
Dept. of Semiconductor Engineering, Chungbuk National University, Cheongju 361-763, Korea
E-mail : kimys@cbu.ac.kr

The integration of large capacitance over 100 pF is difficult in CMOS technologies because of significant area consumption. A possible solution is the use of capacitance multipliers, which performs the multiplication of small capacitance values. We propose capacitance multiplier using the second current conveyors (CCIIs). Basically, the second current conveyor (CCII) is a three terminal device labeled with X, Y and Z. The resistance at Y terminal is ideally infinite, thus no current flows through Y. The voltage at X terminal is a replica of the applied voltage to Y terminal. The current at X node is equal to the one at Z node. The positive type (CCII+) and negative type (CCII-) conveyors depend on the flowing current direction at Z node [1-2].

Fig. 1 shows the proposed capacitance multiplier using the positive and negative CCIIs. For capacitance multiplier, the input equivalent capacitance C_{Eq} can be multiplied by the ratio C_2 and C_1. Hence, the multiplied capacitance C_{Eq}, which is C_2/C_1 times greater than the reference capacitance C_S, is obtained. The CCII operates in class AB mode with a rail to rail voltage swing [3]. The equivalent capacitance is the multiplied capacitance of C_S by the ratio C_2 and C_1. The capacitor multiplier was fabricated using Magnachip 0.18-μm CMOS process.

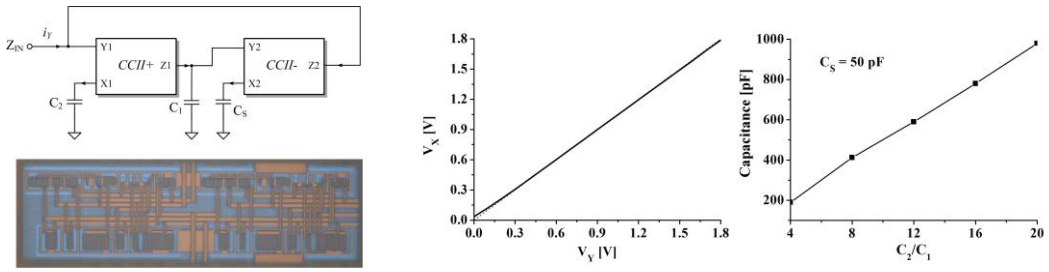


Fig. 1 Capacitor multipler using CCIIs and electrical characteristics.

[1] G. Di Cataldo, G. Ferri, S. Pennisi, in Proc. ISCAS, pp. 343-346 (1998)
[2] G. Ferri, N. C. Gerrini, Low-vlotage low-power CMOS current conveyors, New York: Kluwer, 2003.
[3] Hassan O. Elwan and Ahmed M. Soliman, IEEE Trans. Circuits Syst. I, 44, 9, pp.828-835 (1997)

HV EDMOS with LNDC (laterally Non-uniform Doped Channel)

Min-Hyuk Sung*, Min-Su Kim*, Ki-Ju Baek*, Yeong-Seuk Kim* and Kee-Yeol Na**
*Department of Semiconductor Engineering, Chungbuk National University, Cheong-ju, Korea
**Department of Semiconductor Electronics, Chungbuk Provincial College, Ok-Cheon, Korea
E-mail : keeyeol@cpu.ac.kr

An n-channel high-voltage extended drain metal-oxide-semiconductor (EDMOS) device with lateral non-uniform doped channel (LNDC) is presented in this paper. Channel doping of the proposed LNDC EDMOS is modulated laterally by both p-well and p-substrate. The laterally modulated doping profile can reduce magnitude of electric field at drain junction as well as enhance g_m. The proposed device fabricated using the 0.18 μm standard low-voltage CMOS process without any process modification. The experimental measurements showed the improved I-V characteristics of the proposed LNDC EDMOS: higher g_m, larger I_{DS}, lower g_{ds} and improved BV behavior.

Acknowledgement: This work was supported by the IDEC.

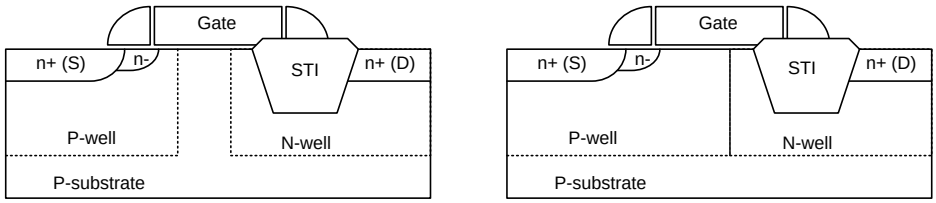


Fig 1. Cross-section of the EDMOS devices: (a) Proposed, (b) Conventional.

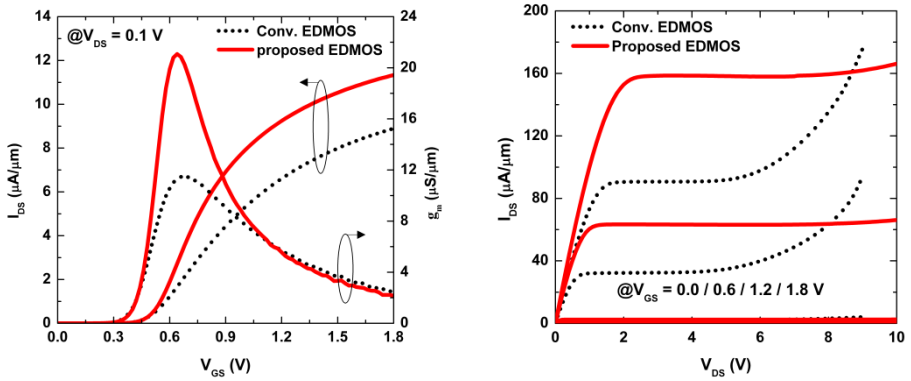


Fig 2. Measured I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics

[1] C. Bulucea et al., IEEE T-ED, 57(10), p.2363, 2010.
[2] K.-Y. Na et al., IEEE T-ED, 60(10), p.3515, 2013.
[3] Han et al., IEEE T-SM, 26(2), p.248, 2013.

프로세서 침입탐지를 위한 아날로그 센서 회로 설계

고강호, 신상진, 김석만, 조경록
충북대학교 정보통신공학과
E-mail : {khko, sjshin, smkim}@hbt.cbnu.ac.kr, krcho@cbnu.ac.kr

본 논문에서는 반도체 칩에 시도되는 불법 복제와 무단 사용을 방지하기 위한 침입탐지 기능 회로들을 구현하고 제작된 칩을 검증한다[1]. 칩을 불법 복제하기 위한 방법 중 글리치 공격(glitch attack)은 칩에 인가되는 신호를 빠르게 변화시켜 칩의 정상동작에 영향을 주어 그 자료를 토대로 분석하는 방식이다[2]. 이러한 공격을 탐지하기 위해 Current mirror 회로 기반의 과전류 검출회로를 통하여 전류 감시대상 회로(CUT, circuit under test)에 흐르는 전류 I_{DD}를 감시하는 회로를 제안. 또한, 반도체 칩의 오동작을 유도하기 위한 고의적 목적으로 직접적인 열을 가해 칩의 온도를 상승 시킬 수도 있다. 이 때는 Band gap reference 회로의 출력 전류가 온도 변화에 비례하게 변하는 특성만을 이용하여 온도 변화를 감지할 수 있다. 이로써 외부로부터의 공격을 탐지 할 수 있다.

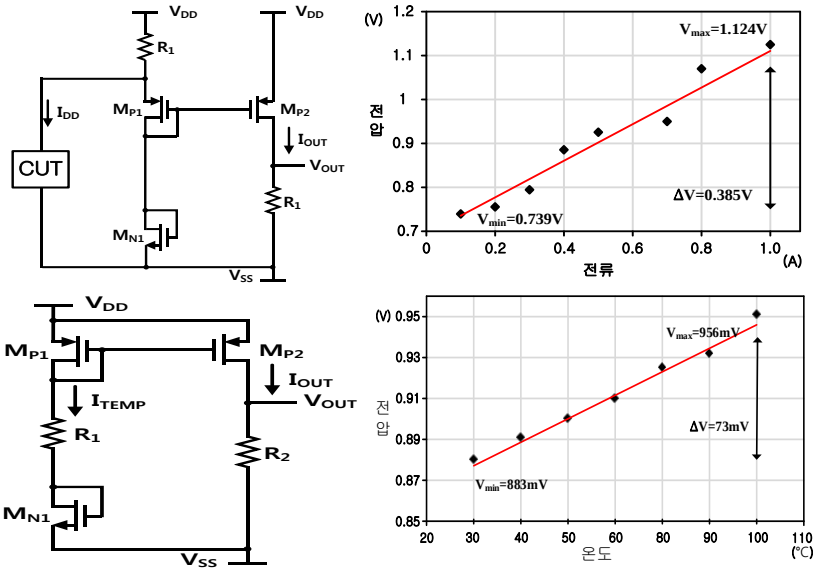


그림 1. 제안하는 탐지 회로와 칩 측정 결과

[1] G.E. Suh and S. Devadas, “Physical Unclonable Functions for Device Authentication and Secret Key Generation,” IEEE Design Automation Conference, pp.9-14, Jun. 2007.

[2] A.G. Yanci, S. Pickles, and T. Arslan, “Detecting Voltage Glitch Attacks on Secure Devices,” BLISS, pp.75-80, Aug. 2008.

Highly efficient supply modulator for Envelope Tracking RF Power Amplifier (ET RF PA)

Jimin Kwon, Jungjoon Kim, and Bumman Kim
Department of Electrical Engineering, POSTECH, Pohang 790-784, Korea
E-mail : nalge@postech.ac.kr

Recently, Envelope Tracking RF Power Amplifier (ET RF PA) is considered as a next-generation PA approach because of its structural potentiality of high efficiency and broad-bandwidth operation. The key operation is that the drain bias of PA device moves along with the input voltage amplitude, which improves the drain efficiency of RF PA because when the input power is small and the drain bias is relatively high, it generates DC power dissipation which is unnecessary to amplify the small input signal. Among many issues, one of the most important parts in ET PA design is to design highly efficient supply modulator which supplies properly modulated power to PA. To achieve high efficiency in envelope tracking power amplifier, highly efficient supply modulator design must precede it. Thus, highly efficient supply modulator circuit is designed by reducing power loss in linear amplifier. It achieved 80% efficiency in simulation. This work was supported by the IDEC.

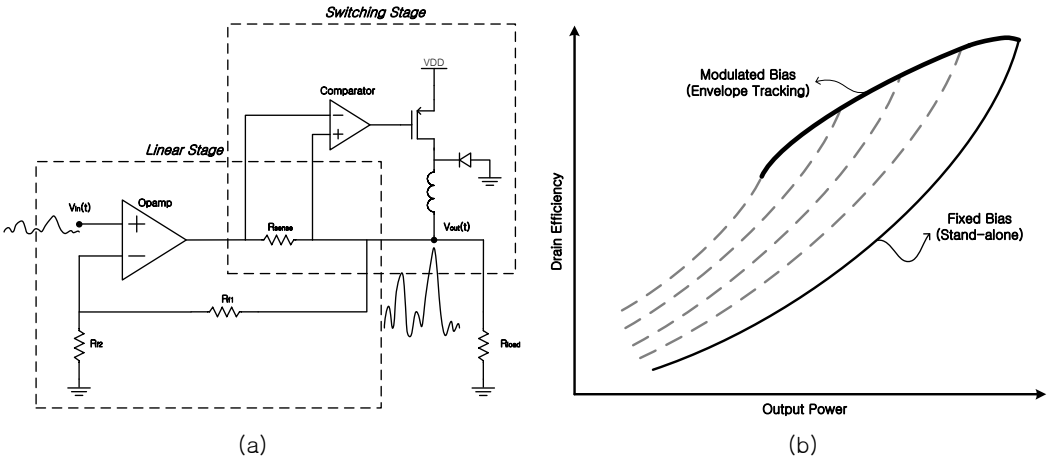


Fig 1. (a) Supply Modulator for ET (b) Drain Efficiency Trajectory in ET

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Highly efficient quadrature transmitter using RF Digital-to-Analog Converter (RF DAC)

Hadong Jin, Dongsu Kim, and Bumman Kim
Department of Electrical Engineering, POSTECH
San 31, Hyoja-dong, Nam-gu, Pohang, Gyeungbuk, 790-784, Republic of Korea
E-mail : hdjin@postech.ac.kr

CURRENT mobile handsets for 3G and 4G support many communication standards and many frequency bands. For this multi-standard and multi-band radio architecture, a digital intensive RF transmitter design, instead of an analog circuit based design, is necessary because the transmitter has many advantages such as high controllability, small silicon area and low cost, and low power consumption. Previous RF DACs used a Gilbert cell mixer for frequency up-conversion. We replaced the complex Gilbert cell mixer with simple digital gates (Fig 1.). This alteration saved area because a Gilbert cell mixer is large. We set 8-bit input codes to get the advantages of two code structures. The Most Significant Bit (MSB) and the next 6 bits are represented using Thermo codes, and the Least Significant Bit (LSB) is represented using Binary code. We measured implemented RFDAC using continuous wave (CW) and Long Term Evolution (LTE) signals with 800-MHz carrier frequency. The pre-processed digital I and Q signals were generated by a FPGA board and their sampling rate was 50 MHz. This work was supported by the IDEC.

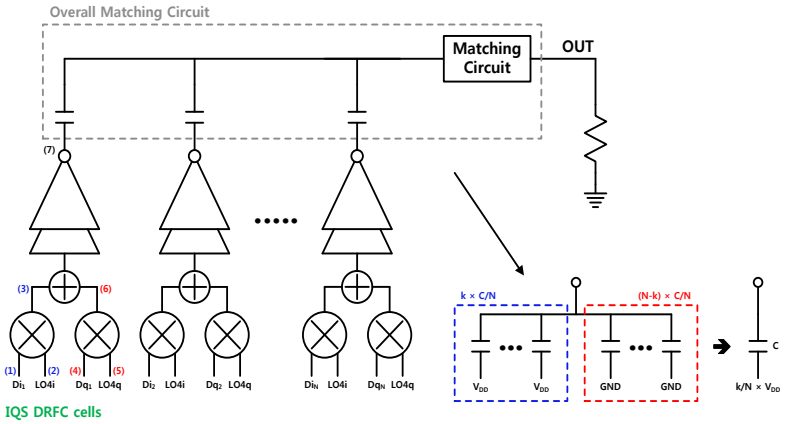


Fig 1. Proposed circuit diagram

[1] S.-M.Yoo, J. S. Walling, E. C. Woo,and D. J. Allstot, "A switched-capacitor power amplifier for EER/polar transmitters," *ISSCC Dig. Tech. Papers*, pp. 428-429, Feb. 2011.
[2] Dongsu Kim, Hadong Jin, Sangsu Jin, and Bumman Kim, "Highly Efficient and Wideband Digital Quadrature Transmitter," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Seattle, WA, USA, Jun. 3-5, 2013.

A 0.4 V Driving Multi-Touch Capacitive Sensor with the Driving Signal Frequency set to (n+0.5) Times the Inverse of the LCD VCOM Noise Period

Jae-seung Lee, Dong-Hee Yeo, Jae-Yoon Sim, Byung-Sub Kim, and Hong June Park

Pohang University of Science and Technology (POSTECH), 77 Cheongam-Ro, Nam-Gu, Pohang, Gyungbuk, 790-784

E-mail : {reput, hjpark}@postech.edu

A mutual-capacitance measuring touch sensor placed on a LCD panel is widely used smart devices. The LCD panel has a VCOM plane or grid, which has capacitively-coupled noise from the gate driver pulse and the source driver image signals. To reduce the effect of this noise, which is called VCOM noise, on the mutual-capacitance measuring TSP output, a large-swing voltage is used for the TSP driving signal (VSTM). The peak-to-peak swing of the TSP driving signal is as high as 18 V[1]. In [2], the peak-to-peak TSP driving voltage is reduced to 5 V by performing the touch sensing operation during the VBLANK period only, which requires a non-standard LCD with the VBLANK time being 25% of a display frame time.

In this work, the peak-to-peak TSP driving signal (VSTM) is reduced down to 0.4 V with a good sensing ability.

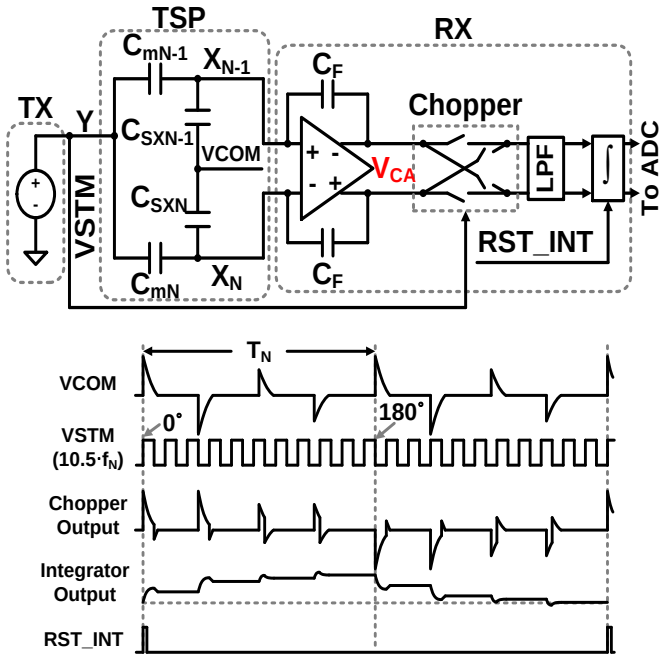


Fig. 1. Proposed front-end (a) circuit (b) timing diagram

[1] C. H. Krah, “Automatic Frequency Calibration,” US2008/ 0157882, Jul. 2008.

[2] S. P. Hotelling, et. al., “Single-Chip Touch Controller with Integrated Driver System,” US2009/0009483, Jan. 2009.

1축 진동형 MEMS 자이로의 구동회로 제작

[1] 김민서, [3] 임을수, [2] 권혁진, [3] 황인철, [2] 임근배
[1] 융합생명공학부, [2] 기계공학과, 포항공과대학교, 포항 790-784, [3] 전기전자공학과, 강원대학교, 춘천 200-701, 대한민국
E-mail : kminseo315@postech.ac.kr

MEMS 기술을 이용한 마이크로 자이로스코프는 자동차, 휴대폰 등 광범위한 영역의 산업에 이용되고 있다. 마이크로 자이로의 대부분은 코리올리 효과에 기반한 진동형자이로이다. 검증질량을 변위로 진동시킬 때 특정한 축 방향으로 회전이 가해지면 각속도의 크기에 비례하여 발생되는 부차적인 진동을 감지하여 각속도를 측정한다. 본 연구진은 MEMS 1 축 진동형 자이로의 구동을 위한 회로를 설계하였고 시뮬레이션을 바탕으로 CMOS 공정을 통해 칩으로 제작하였다. 자이로를 구동하기 위한 자체 발진회로는 정전용량의 변화를 전하 증폭기를 통해 측정하여 출력되는 신호를 phase shifter 와 limiter 를 이용하여 구동신호로 만들고 이 신호가 구동부에 입력되도록 만들어졌다. 자이로의 측정축에서 얻는 신호는 자이로의 고유 진동수를 가지며 수 nA 크기의 매우 작은 신호이므로 높은 DC gain 을 갖는 이단 증폭기와 rail-to-rail 방식의 증폭기를 설계하여 신호를 증폭하였다.

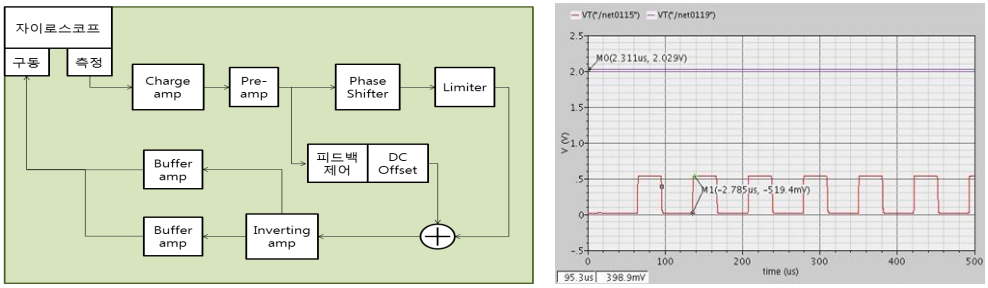


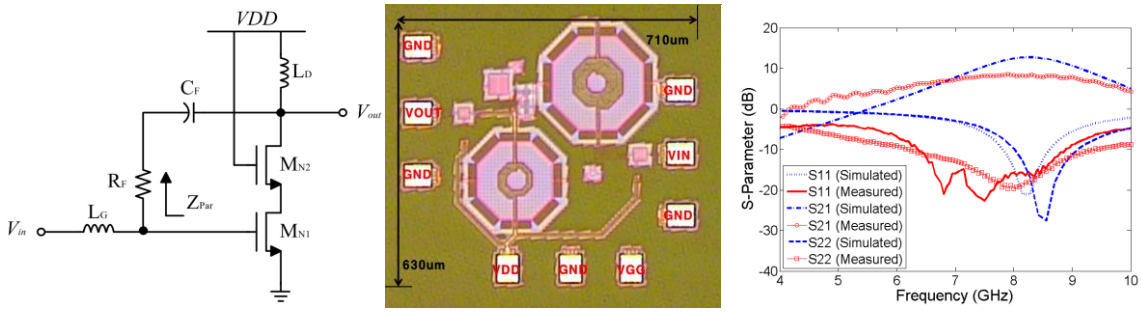
그림 1. 자체 발진 회로 구성도와 최종 출력 구동신호의 시뮬레이션 결과

[1] C.Acar, Robust Micromachined Vibratory Gyroscopes, Ph.D.theis, Univ. of California, Irvine(2004).
[2] Robert F. Coughlin, Operational amplifiers and linear integrated circuits, 6th ed, Prientice Hall
[3] 석세영,성중우,이상우,김청월,임근배, 자이로스코프의 구동변위를 일정하게 제어하는 피드백 자체 발진 회로, 2011 한국군사과학기술학회 종합 학술대회, 2011, pp.180

6.2 – 9.7 GHz LNA Using Series RLC Input Matching and Resistive Feedback

Ji An Park, Choon Sik Cho
School of Electronics, Telecommunication and Computer Engineering, Korea Aerospace University, Goyang, Korea
E-mail : violet8866@kau.ac.kr

LNA design using resistive feedback with shunt and series RLC input matching for wide bandwidth and good linearity with reasonable gain is proposed. Fig. 1 (a) shows schematic of the proposed LNA where cascode configuration is exploited and gate inductor is employed. Fig. 1 (b) shows photograph of the proposed LNA circuit. Fig. 1 (c) shows post-layout simulation and measurement results of S-parameters, where bandwidth of S21 is 3.5 GHz with noise figure of 5.1 dB at 8 GHz. Input matching citcuit of proposed circuit in Fig. 1 is analyzed and simplified with Q factor of equivalent parallel RLC circuit. With this analysis input matching can be calculated with L_G and L_D and compared with Rin(50Ω). By removing degenerate inductor circuit is designed with smaller chip size and much selectable gate and drain inductor. The fabricated proposed LNA circuit chip size including pads takes 710 ㎛ x 630 ㎛ for the fully integrated LNA.



(a) (b) (c)

Fig 1. (a) : The Proposed LNA architecture, (b) : Chip photo of the proposed LNA, (c) : Measured and simulated S-parameters.

[1] H. Jhang and S.S. Edgar, “Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial,” IEEE Trans. Circuits and Systems, vol.58, no. 1, pp. 22-36, Jan. 2011.

10-bit, 40 MS/s, 30 mW Pipelined ADC in 0.18 um CMOS Technology

Cheolmin Ahn, Youngsik Kim
Department of Information and Technology, Handong Global University, Pohang 791-708, Korea
E-mail : adsums@hgu.edu

The increasing demands for portable video applications and wireless communications have made the design of high-speed analog-to-digital converters (ADCs) under limited power dissipation a very hot research topic in recent years. For these applications, because of the increase in the transferred data volume and resolution of video data, there have been demands for higher sampling rates in the ADCs that convert analog signals to digital signals. Also, system-on-a-chips (SOCs) that contain analog circuits and digital signal processing circuits in a single chip are required to achieve higher performance and lower costs. ADCs occupy the principal part of analog circuits in SoCs; therefore, reducing the ADC power consumption helps reduce the power consumption of an entire SoC[1-3]. The architecture of the proposed 10-bit ADC is based on a pipelined architecture. The speed and power consumption of 10-bit ADCs have been improved by using the pipelined architecture. To obtain a high bandwidth and high DC gain with a low supply voltage, a folded-cascode amplifier with a gain-boost technique was used. This chip has been fabricated with a 0.18 um CMOS technology. The effective chip area is 1.051 mm x 0.630 mm and it consumes 16 mA at 1.8 V power supply with 40 MHz clock.

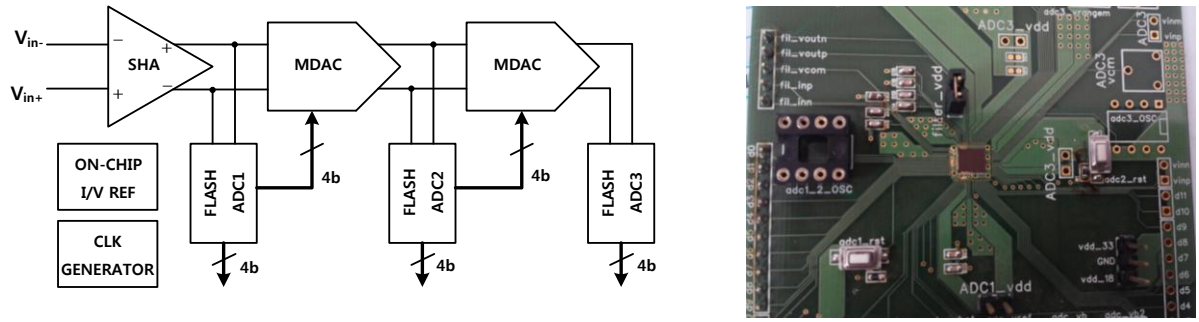


Fig 1. Block diagram of 10-bit pipelined ADC and the layout of the test PCB

[1] R. Wang, K. Martin, D. Johns, and G. Burra; A 3.3mW 12 MS/s Pipelined ADC in 90 nm Digital CMOS. ISSCC Digest of Technical Papers, 2005, p.278-279
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[3] D. Miyazaki, S. Kawahito, and M. Furuto: A 10-b 30-MS/s Low-power Pipelined CMOS A/D Converter Using a Pseudodifferential Architecture. IEEE J. Solid-State Circuits, 38, 2, p.369-373(2003).

Design and Implement of 8-bit Segmented Type DAC in 0.35 um Technology

Cheolmin Ahn, Youngsik Kim
Department of Information and Technology, Handong Global University, Pohang 791-708, Korea
E-mail : adsums@hgu.edu

The interface between the field of wireless communications and the mixed signal area becoming one of the most challenging blocks to design in the telecommunication devices of today [1]. In different applications, DAC (Digital-to-Analog Converter) requires different performances, and for the communication application, DAC should have good linearity performance [2]. The segmented type DAC which mix various type DACs appropriately is commonly used to implement high speed and high resolution DAC. Binary weight array type DAC is a critical problem when switch turn around, and it brings a DNL error and have a glitch problem. In contrast, thermometer code type DAC is strong in monotone increasing, glitch problem [3]. In this paper, MSB part is implemented with thermometer code type DAC which is strong in monotone increasing, and glitch, and LSB part is implemented with R-2R ladder array DAC. This chip has been fabricated with a 0.35 um CMOS Technology. The effective chip area is 1.1 mm x 0.52 mm and it consumes 3.5 mA at 3.3 V power supply with 20 MHz clock. The INL is -3.66, +3.51 LSB and DNL is -0.74, 0.68 LSB.

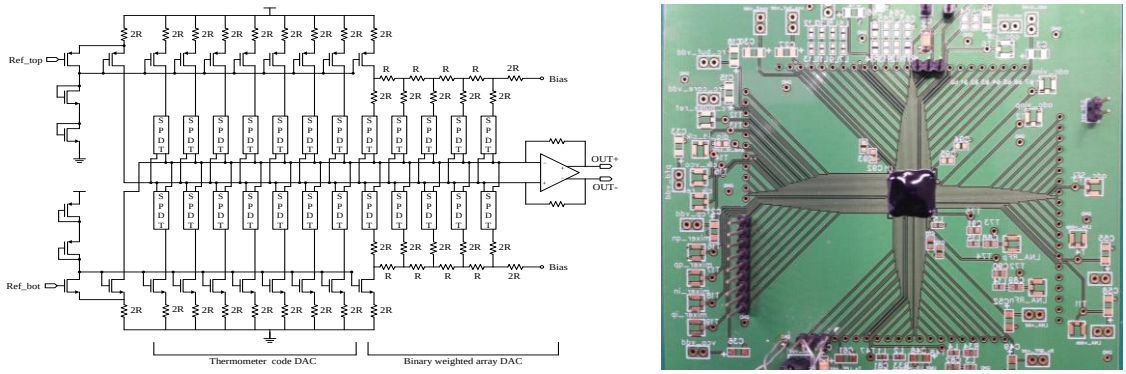

Fig 1. 8-bit segmented type DAC and the PCB layout for test DAC

[1] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.
[2] ZHU Zhang-ming, YANG Yin-tang, CHANG Chang-chun.Design of a 5V, 14-bit high speed digital-to-analog converter for telecommunication applications [J]. JOURNAL OF XIDIAN UNIVERSITY2004,31 (3):pp.352.356.
[3] Raja, G.; Bhaumik, B., "16-bit segmented type current steering DAC for video applications," VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on , vol., no., pp.6 pp.,, 3-7 Jan. 2006

An Envelope Tracking Modulator for the Mobile Power Amplifiers

Minchul Kim and Junghyun Kim
Department of the Electronics and System Engineering, Hanyang University
E-mail : mck@hanyang.ac.kr

In the mobile phone, the power amplifier is the one of the most power consumption device. This lead to the many research about the efficiency enhancement in power amplifier. In recent research, the envelope tracking technic [1] has not only received attention but also the high efficient supply modulator [2]. This envelope tracking modulator is composed of the two parts in Fig.1 (a). First, the linear stage which consists of a negative feedback op amp and a class AB buffer is the voltage source for the amplifying the input envelope. Second, the switching stage which consists of the DC-DC converter, control block and etc is the current source for the increasing the efficiency of the envelope tracking modulator. The result of the modulator in Fig. 3 (c) showed the waveform of the input envelope signal and amplified output signal. The gain of the modulator can be found by the transfer function in Fig. 1 (d). This work was supported by the IDEC.

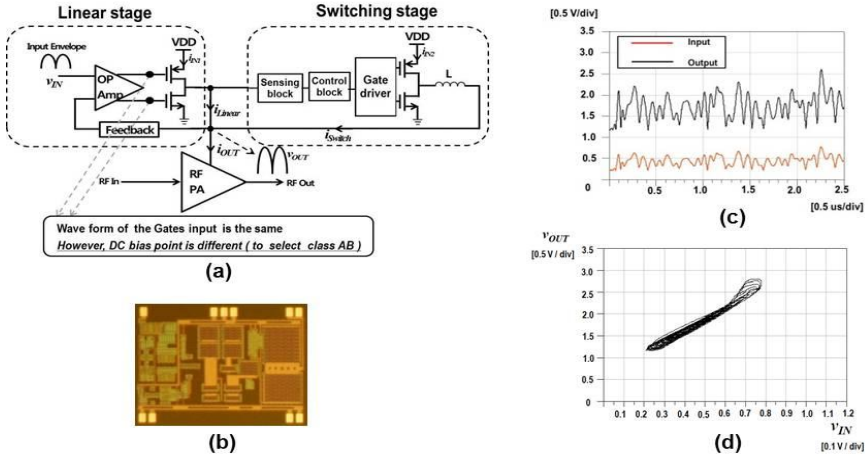

Fig 1. (a) Block diagram of the envelope tracking modulator, (b) Photograph of the fabricated MMIC, (c) waveform of the input and output, (d) transfer function.

[1] D. Kim , D. Kang , J. Kim , Y. Cho and B. Kim "Wideband envelope tracking power amplifier for LTE application", IEEE Radio Freq. Integr. Circuits Symp., pp.275 -278 2012.
[2] J.Choi, D.Kim, D. Kang and B. Kim, “A polar transmitter with CMOS programmable hysteretic-controlled hybrid switching supply modulator for multistandard applications”, IEEE Trans. Microw. Theory Tech., vol. 57. no. 7. pp 1675–1686, July 2009.

PFM-PWM Dual-mode Circuit using CMOS OTAs

Min-Hye Kang, Fan Zhang, and Hee-Jun Kim
Department of Electronic Systems Engineering, Hanyang University, Ansan, Korea
E-mail : hjkim@hanyang.ac.kr

Even though the well-known control techniques, PWM and PFM, have been widely used in many fields such as power conversion systems, these techniques are suffered from their limited load ranges causing a switching loss and an efficiency problem [1]. To solve the problems, we present a PFM-PWM control method using OTAs which have an attractive property of good integration for ICs form [2]. Fig 1 shows a circuit diagram of the proposed circuit and its result of frequency and duty characteristic simulated with HSPICE in a M/H 0.35μm 3.3V CMOS process. The circuit consists of two OTA-R positive-feedback Schmitt triggers. By comparing a sensing current, I_{SEN} with a reference current, I_{REF}, either PFM- or PWM-mode is determined. The frequency of PWM signal is determined by the first-stage Schmitt trigger composed of the OTA1 and OTA2, while the on-time of PFM signal is controlled by the second-stage Schmitt trigger composed of OTA3 and OTA4.

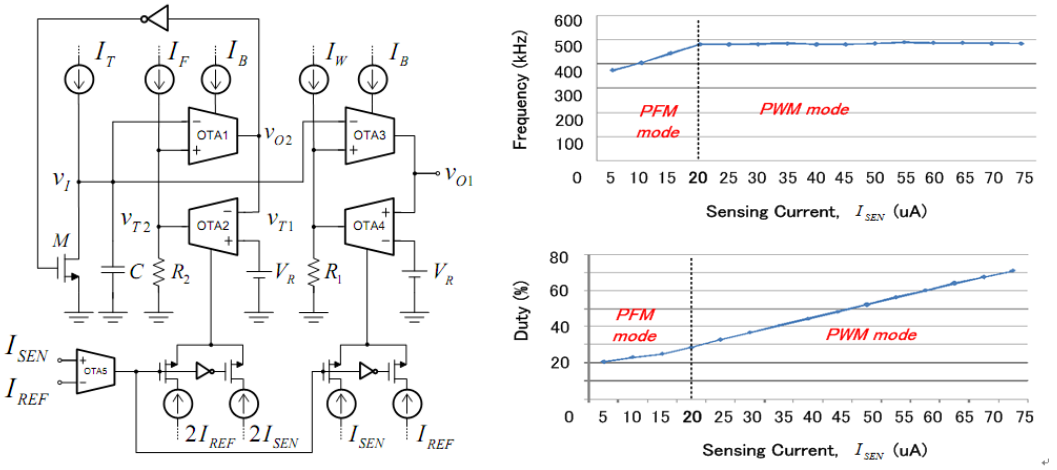

Fig 1. The proposed circuit and its frequency and duty characteristic graph

[1] Y.-S. Kim, B.-M. No, J.-S. Min, S. Al-Sarawi, and D. Abbott, "On-chip current sensing circuit for current-limited minimum off-time PFM boost converter," *SoC Design Conference (ISOCC), 2009 International*, vol., no., pp.544-547, 22-24 Nov. 2009

[2] H. Kim, H.-J. Kim, and W.-S. Chung, "Pulsewidth Modulation Circuits Using CMOS OTAs," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol.54, no.9, pp.1869-1878, Sept. 2007

Wide gain Range Variable Gain Amplifier

Chang-Woo Lim and Tae-Yeoul Yun
Department of Electrical Engineering and Computer Science, Hanyang University, Seoul, Korea
E-mail : Changs87@hanyang.ac.kr

Variable gain amplifiers (VGAs) are used to maximize the dynamic range of overall systems in many applications. The VGA is normally employed in a feedback loop to implement an automatic gain control (AGC) amplifier. The AGC amplifier is a circuit that automatically controls its gain in response to the amplitude of the input signal, leading to a constant-amplitude output.

As an all-CMOS implementation, there are two approaches to realize VGAs depending on the control signal is digital or analog. In digitally controlled VGAs require a large number of control bits to reduce the jumps. Thus, for applications that require smooth gain transitions, the VGAs controlled by analog signal are preferred. This paper designed an analog VGA topology that can provide a very wide gain variation. The block diagram of entire system is shown in Fig. 2. And dashed box indicate VGA that designed in this work. The VGA consist of control circuit block and amplifier block. Control circuit block control current of amplifier block and gain. The amplifier consists of an input source-coupled pair and diode-connected loads. The designed amplifier block have 3stage for large variable gain, and include the common-mode feedback circuit. The designed VGA is fabricated 110nm CMOS technology and occupied 1.26mm^2 including pads. Fig.3 shows the microphotograph of VGA. As shown in Table 1, the designed VGA has overall gain variation of 69.3 dB. And the VGA dissipated an average 40mA from a 1.5-V supply.

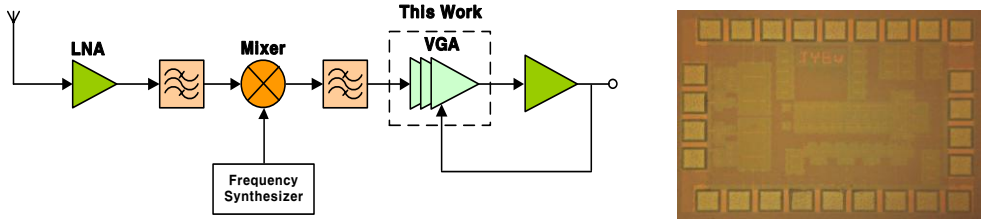

Fig 1. System block diagram (left), Microphotograph of designed VGA (right)

TABLE I. PERFORMANCE SUMMARY

Process	Power consumption	Gain Range	Area
110nm CMOS	61mW	69.3dB	1.4*0.9 mm^2

REFERENCE

Q.-H. Duong; Quan Le, C.-W. Kim, S.-G Lee "A 95-dB linear Low-Power Variable Gain Amplifier" IEEE Trans. Circuits Syst. Ⅰ Regular papers, Vol. 53, No. 8, Aug. 2008.

W. M. Christopher, "A variable gain CMOS amplifier with exponential gain control," in *Dig. Tech. Papers IEEE Symp. VLSI Circuits*, 2000, pp. 146–149.

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A High-Image-Quality Data Driver IC for Flat Panel Displays

Jong-Seok Kim and Byong-Deok Choi
Department of Electronic Engineering, Hanyang University, Seoul 144-791, Korea
E-mail : bdchoi@hanyang.ac.kr

The uniformity of the data driver for flat panel display cannot be overemphasized since it determines the display quality. The random offset voltage at the buffer amplifiers in the data driver degrades the uniformity of data driver. To reduce the offset voltage, autozeroing [1] and offset averaging [2], [3] can be used, but these methods increase the circuit area since they requries additional devices and signals. To resolve these problems, we propose a high uniformity data driver IC using a digital calibration method without channel area increase. Fig. 1 shows the proposed data driver. In the offset measurement phase, ADC measures the offset of buffer amplifier and stores the measured offset data in memory. In the calibration and driving phase, the calibration logic can provide offset-calibrated data by subtracting the offset voltage from original RGB data. With this operation, the proposed data driver can achieve high uniformity. The proposed data driver was fabricated in 0.35 μm CMOS process. The proposed data driver IC is basically based on the traditional data driver structure, but a 10-bit resolution, 6-bit window range SAR-ADC is implemented to measure the offset voltage. The calibration logic and offset memory is not included in this IC since it can be located in timing-controller and external EEPROM which are already used for display systems. The measured offset voltage with the proposed method is drastically reduced from over 20 mV to under 5 mV which means the error is under 0.5 LSB of DAC. Therefore, we can conclude that the proposed data driver can provide very high uniformity.

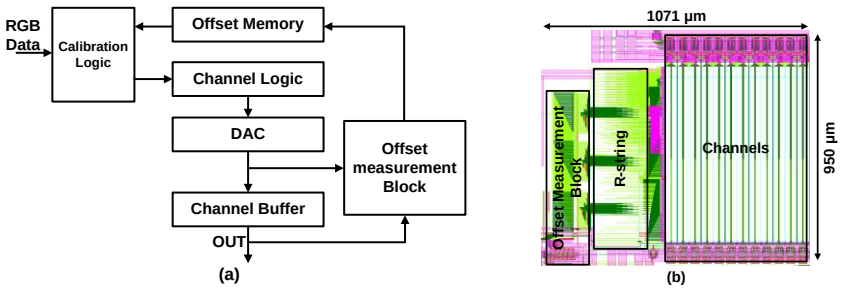

Fig. 1. Proposed data driver with offset calibration method (a) block diagram and (b) layout

[1] C. C. Enz et al., Proc. of the IEEE, 84, 584, (1996)
[2] J. H. Kim et al., IEEE Trans. on Consumer Electronics, 51, 1042, (2005)
[3] C.-H. Tsai et al., IET Circuits, Devices & Systems, 4, 539, (2010)

A CMOS Temperature Sensor Using Multi-Core Structure

Tai-Soon Park, and Sang-Gyu Park
Department of Electronics Computer Engineering, Hanyang University, Seoul, Korea
E-mail : bbamari_ts@naver.com

A multi-core temperature sensor is proposed with ±0.3 ℃ maximum inaccuracy over the range of 0 ℃ to 120 ℃. The multi-core temperature sensor uses a constant-gm structure using MOSFETs operating in intermediate-inversion region. Multi-core temperature sensor could be achieved due to relatively small size of MOSFETs[1-4]. Each temperature sensor core occupies 14 μm · 11 μm in area and consumes 10 μW of power.

Proposed temperature sensor can be used to compensate the temperature variations of various CMOS circuits such as DSP, display driver IC, and CPU.

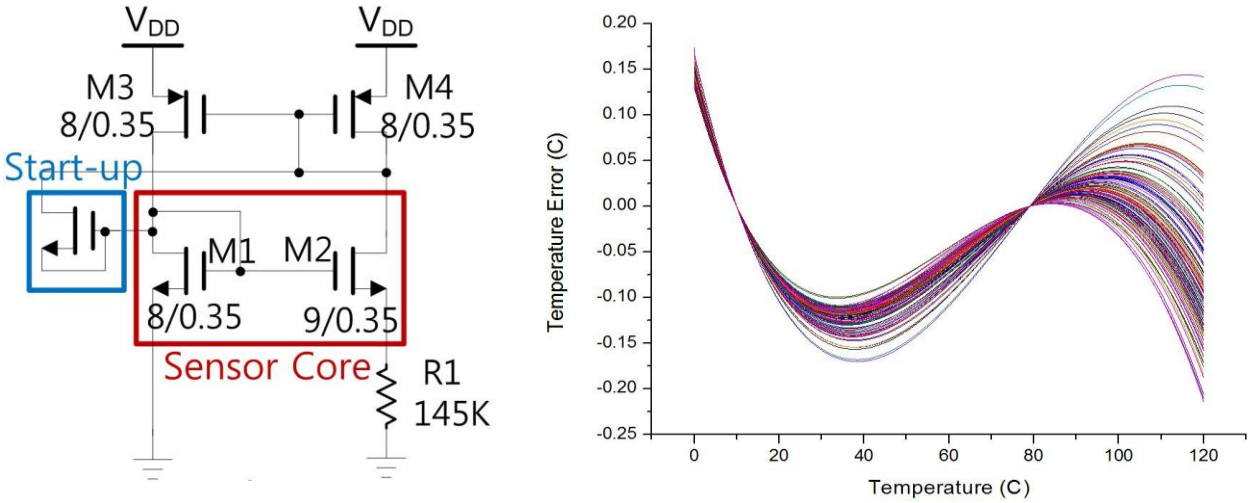

Fig 1. Schematic of the proposed temperature sensor and Sensor error by Monte-carlo simulation

Acknowledgement

This work was supported by the IDEC.

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[3] G. C. M. Meijer, G. Wang, and F. Fruett, "Temperature sensors and voltage references implemented in CMOS technology," IEEE Sensors J., vol. 1, no.3, pp. 225-234, Oct. 2001.

[4] A. Bakker and J. H. Huijing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 933-937, Jul. 1998.

High-Linearity Variable-Gain Drive Amplifier

Jun-Young Park and Tae-Yeoul Yun
Department of Electrical Engineering and Computer Science, Hanyang University, Seoul, Korea
E-mail : jypark7@hanyang.ac.kr

In recent years, a lot of power amplifier (PA) is used in wireless system, which causes expensive component in a radio frequency (RF) transmitter because of a bulky off-chip. In order to reduce the burden of the PA, a drive amplifier (DA) is required to supply a sufficient power gain to the PA, also it needs a variable gain. In addition, the DA should be high-linearity performance because of the high output power and the digital modulation scheme [1]. Therefore proposed DA is designed for high linearity and variable gain. There are many linearization methods such as feedback, feed-forward, harmonic termination, and optimal biasing, which decrease a third-order derivative coefficient of a large-signal transfer function [1-3]. The feedback technique is regarded as the most effective technique among those ones with respect to stability of amplifier about a temperature and a process variation, particularly in negative feedback. Therefore a negative feedback method using IM3 cancellation technique is adopted at the DA. The variable impedance at the DA load using triode region MOSFET such as resistor in parallel can control gain. If a gain is controlled by added or subtracted current, it causes mismatched IM3 cancellation. Therefore it is better to adopt variable load impedance at a required high linearity amplifier.

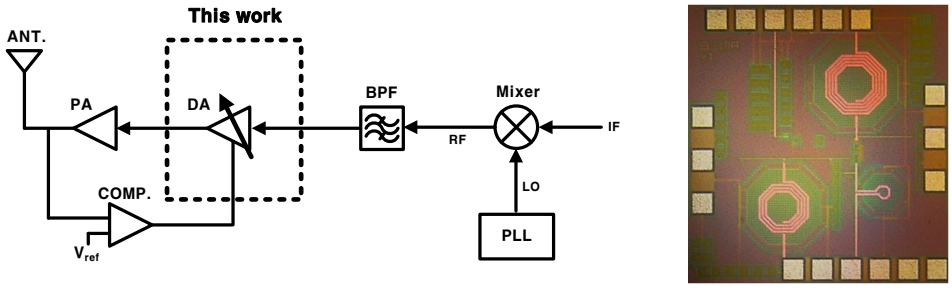

Fig 1. The Block Diagram of Direct Conversion Tx (left), Microphotograph of the Chip (right)

TABLE I. PERFORMANCE SUMMARY

	Tech.	Gain [dB]	BW [GHz]	OP1dB [dBm]	OIP3 [dBm]	Area [mm^2]	PD [mW]
This work	0.11 μm CMOS	4.65 ~ 12.19	2.1 ~ 2.7	> 5.7	> 14.3	1.15	12.2

[3] Do-Gyun Kim, Nam Pyo Hong, Young-Wan Choi, "A Novel Linearization Method of CMOS Drive Amplifier Using IMD Canceller," *Microwave and Wireless Components Letters, IEEE*, vol.19, no.10, pp.671-673, Oct. 2009.

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Capacitive Touch Screen Panel Readout Circuit against Display Noise

Duhyun Jeon, Hyun-Woo Kim, and Byong-Deok Choi
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : bdchoi@hanyang.ac.kr

Recently, the distance between a touch screen panel (TSP) and a LCD panel is becomming closer for compact devices. This trend increases the effect of a display noise on the touch performance, which is coupled from LCD common-electrode to TSP RX lines when data or gate line voltage changes. To make the TSP robust against this noise, there are several approaches are proposed such as synchronization of readout circuit with display driver IC [1] and subtracting the similar noise current from the adjacent reference line [2]. The designed readout circuit for touch screen panel consists of sensing block, ADC, excitation driver and timing controller as shown in Fig. 1(a). In the sensing block, a charge amplifier converts the RX line-induced-charge from TX to a voltage. After then a touch event can be detected depending on charges amplified to the output node. The timing controller is responsible for synchronization between sensing block, excitation driver control signal with VSYNC and HSYNC signals from the display driver IC. This synchronization is done such that detection of a touch event is performed to avoid a display noise. Sensing block measurement result is shown in Fig. 1(b).

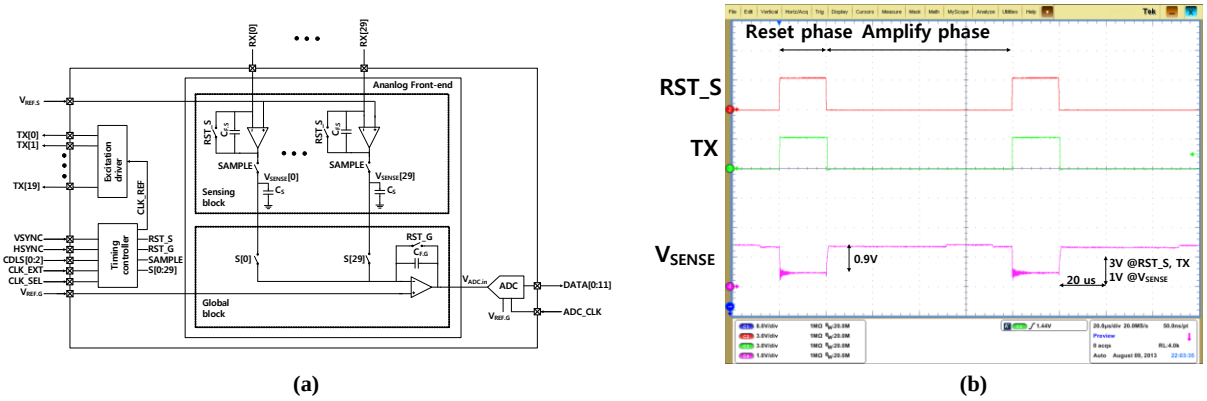

Fig 1. (a) Block diagram of designed chip (b) Sensing block measurement result

[1] I.-S. Yang, O.-K. Kwon, IEEE Trans. On Consumer Electronics, 57, 3, 1027-1032 (2011).
[2] K.-D. Kim, S.-H. Byun, Y.-K. Choi, J.-H. Baek, H.-H. Cho, J.-K. Park, H.-Y. Ahn, C.-J. Lee, M.-S. Cho, J.-H. Lee, S.-W. Kim, H.-D. Kwon, Y.-Y. Choi, H. Na, J. Park, Y.-J. Shin, K. Jang, G. Hwang, M. Lee, ISSCC, 116-117 (2012)

10-bit Two-Step Single Slope ADC for A Low-Power CMOS Image Sensor

Duhyun Jeon, Don-gu Lee, and Byong-Deok Choi
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : bdchoi@hanyang.ac.kr

A single slope ADC (SSADC) is widely used for CMOS image sensor because of simple implementation and low area. However, a SSADC requires 2^N clocks for N-bit resolution. To overcome this speed limiation, a two-step single slop ADC was proposed with L-bit coarse operation and M-bit fine operation, and N = L+M [1]. Although it reduces the converstion time, it increases power consumption and area because multiple ramp generators are required for fine conversion. These issues can be alleviated by only using a single ramp generator for both coarse and fine operations [2]. In this chip design, a two-step SSADC is designed with single ramp generator. The designed ADC operation is shown in Fig. 1. The timing diagram shows only 2-bit MSB and 2-bit LSB operations for simple description. In coarse conversion, MSB is decided from full-scale V_{Ramp} and V_{IN} comparison. When V_{Ramp} is higher than V_{IN}, control logic samples the voltage difference (V_C) between V_{IN} and V_{Ramp} to holding capacitor (C_H). In fine conversion, this residue is added to reference voltage (V_{REF}) and compared with the fine ramp signal in the range of one MSB. Due to using only residue value in the fine conversion, a single ramp signal can be applied to all column ADC. Because multiple ramp signals are not required for fine conversion, the power consumption can be reduced compared with the case of multiple ramp signals.

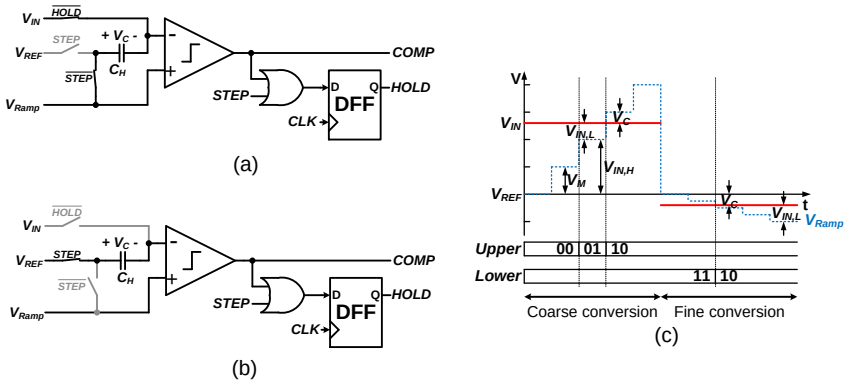

Fig 1. Two-step SSADC operation (a) coarse conversion (b) fine conversion (c) timing diagram

[1] M. F. Snoeij, A. J. P. Theuwissen, K. A. A. Makinwa, J. H. Huijsing, JSSC, 42, 12, 2968-2977 (2007)
[2] S. Lim, J. Lee, D. Kim, G. Han, Trans- on Electron Device, 56, 3, 393-398 (2009)

Energy/Power efficient Multimedia Processor for Low-Level Image Processing with DVFS and Dynamic gating

Jun-Seok Park, Hyo-Eun Kim, Sang-Hye Chung, Jaehyeong Sim,
Wongyu Shin, Dongil Lee, Jeongmin Yang, and Lee-Sup Kim
Department of Electrical Engineering, KAIST, Daejon, Korea
E-mail : jspark@mvlsi.kaist.ac.kr

Today's handheld devices integrate homogeneous parallel stream processors for media acceleration to satisfy the computational needs [1]. On the other hands, multi/many-core platform becomes the largest power and energy consumer in the overall processors because of the computing power in real operation. So, a dedicated power management technique is required to supporting dynamic voltage frequency scaling (DVFS) or power gating in chips for enhancing power/energy efficiency. Operations in multimedia applications such as image processing or computer vision include high data/task-level parallelism, so multiple single-instruction-multiple-data (SIMD) cores with a bunch of processing elements (PEs) are necessary. Flexible core architecture is proposed to support image processing as shown in Fig. 1. It integrates homogeneous SIMD cores for coarse-grained MIMD configuration and each 8-wide SIMD core are implemented based on 16-bit fixed point data-paths. To enhance energy efficiency, DVFS and dynamic power/clock gating are implemented. The clock frequency is adjusted by integrated wide-range programmable PLLs based on [2]. The proposed hardware fabricated on 65nm CMOS technology. Since overall system achieves 28.8 GOPS, it can support real-time low-level image processing in Full-HD resolution.

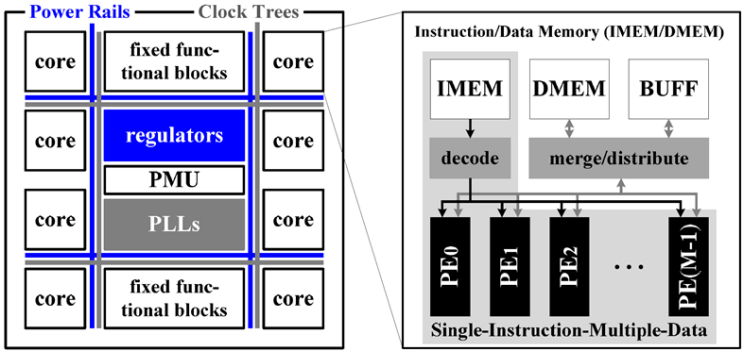

Fig 1. Proposed vision hardware

[1] H.-E. Kim, J.-S. Park, J.-S. Yoon, S.-H. Kim, L.-S. Kim, IEEE JSSC, (2013).
[2] J. G. Maneatis, IEEE JSSC, (1996).

An Inductorless Wideband LNA in 0.18-μm CMOS Technology

Yang Hun Lee, Sun Yool Kang, and Chul Soon Park
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : yangpur@kaist.ac.kr

Recently, radios for multi-purpose applications are emerging market, eventually trying for cognitive radio solutions. Each application receiver has ideneitcal frequency bad. To satisfy these applications, it its necessary to integrate different wireless receivers composed on chip.

In this paper, we desiged a wideband LNA on a 0.18-μm CMOS process. A conventional wideband LNA have several drawbacks, such as high power consumption, and large chip area due to an inductor. The designed wideband LNA is inductorless architecture that market small size and low cost design. The designed LNA chip area is 0.18 × 0.18 mm^2, including all pads. The designed LNA has 21.8 dB voltage gain and 2.1 dB noise figure at 2.4 GHz.

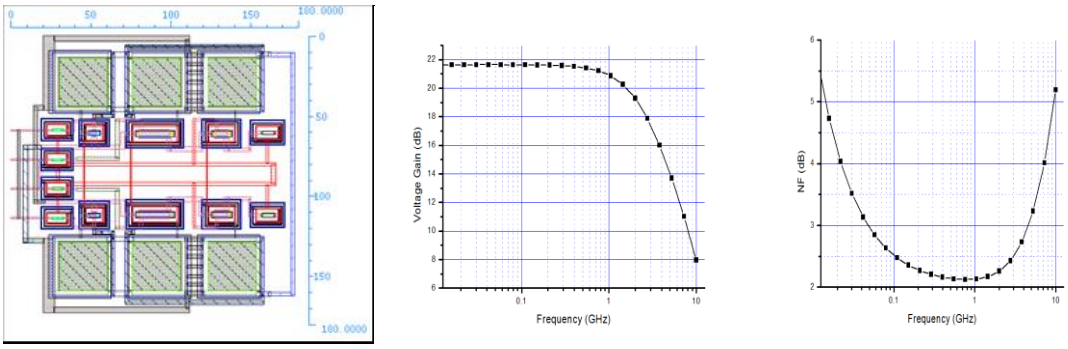

Fig 1. Layout, voltage gain and noise figure of the designed LNA

BER optimum adaptive reference calibration ADC

Sejun Jeon, Hyeon-Min Bae
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, 305-701 Republic of Korea
E-mail : jsjwin@kaist.ac.kr

The increasing demand for bandwidth requires power-efficient and high-speed communication systems. Excessive skin and dielectric loss in a multi-Gb/s wireline channel necessitates a complex equalizer for the compensation of severe intersymbol interference (ISI). Analog domain equalizers has been widely incorporated in wireline receivers for the compensation of moderate ISI of the channel owing to its power-and-area efficiency. However, the sensitivity to process, voltage and temperature (PVT) variations and the limited dynamic rage prevent their use in complex equalizers. Wheares, the digital domain equzliaers are robust to PVT variations and enable complex signal processing for the enhanced BER performance [1]. However, excessive power consumption and the design complexity of an ADC are the main obstacles for their wide-spread use in commercial applications despite recent advances in CMOS technologies. We implemented low-resolution ADC based receiver to acieve BER performance improvement under given hardware complexity using ADC reference level calibration algorithm [2]. Fig. 1 shows the BER-SNR curves for various ADC resolutions, and 2.5bit BER-optimum ADC achived more than 4dB performance improvement over conventilnal 2.5bit ADC.

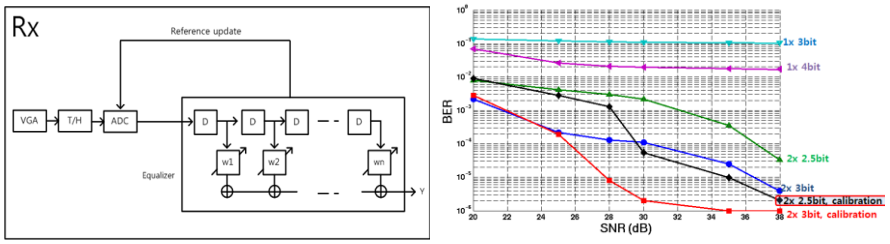

Fig 1. System block diagram and BER-SNR curves for low resolution ADC based receivers

[1] J. Cao, B. Zhang, U. Singh, D. Cui, A. Vasani, A. Garg, W. Zhang, N. Kocaman, D. Pi, B. Raghavan, H. Pan, I. Fujimori, and A. Momtaz,“A 500 mW ADC-Based CMOS AFE With Digital Calibration for 10Gb/s Serial Links Over KR-Backplane and Multimode Fiber,” IEEE J.Solid-State Circuits, vol. 45, no. 6, pp. 1172-1185, Jun. 2010.
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A Low-Power Parallel Multiplier based on Optimized Bypassing Architecture

Sunjoo Hong, Hyunki Kim, and Hoi-Jun Yoo
Department of Electrical Engineering, KAIST, Daejeon, Korea
E-mail : hongsj93@kaist.ac.kr

Recently, low power Digital Signal Processing (DSP) technology is widely used in battery-powered mobile devices. Especially, the multiplier is the critical arithmetic operation unit, and many previous works tried to reduce the switching activity of the multiplier. Among them, the bypassing scheme disables the operations in some rows or columns to save the switching power consumption [1]. In [2], the 2-dimensional bypassing multiplier is proposed, but the additional logics take large circuit overhead. In this paper, a low power parallel multiplier based on optimized bypassing architecture is proposed. The proposed optimized bypassing architecture has two kinds of adder cells. One is the two-dimensional bypassing adder (TDBA) which performs both row and column bypassing scheme simultaneously, and the other is the modified row-bypassing adder (MRBA) for the proposed row-bypassing scheme. When 8×8 parallel multiplier adopts the proposed optimized bypassing architecture, the power consumption of proposed multiplier is reduced by 15.7 % and 48.8%, compared to row-bypassing multiplier [1] and 2-dimensional bypassing multiplier [2], respectively.

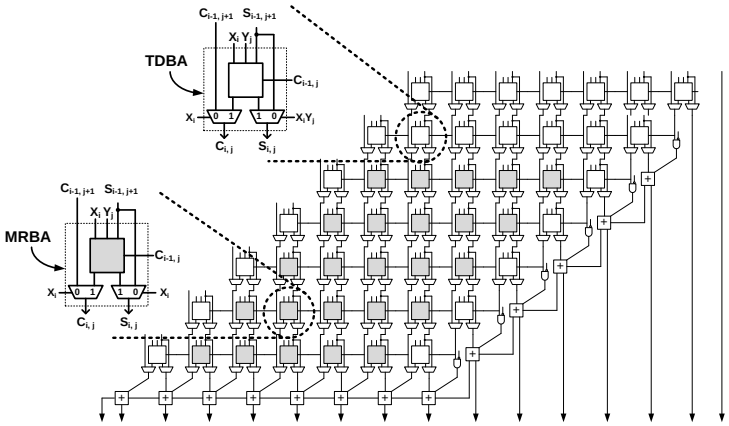

Fig 1. Optimized bypassing architecture for parallel multiplier

* This work was supported by the IDEC.

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A Dynamic Electrode Impedance Matched Acupuncture-Type Diagnosis System

Kiseok Song, Taehwan Roh, Minseo Kim, and Hoi-Jun Yoo
Division of Electrical Engineering, School of EE, KAIST, Daejeon, 305-701, Korea
E-mail: sks8795@eeinfo.kaist.ac.kr, kiseok.song87@gmail.com

A dynamic electrode impedance matched acupuncture-type diagnosis system is proposed for an active electro-acupuncture (EA) treatment with the concurrent feedback of physiological signals. The 4-channel ExG sensor front-end and the independent component analysis (ICA) processor, is used for the acquisition of pure ECG, EEG, and EMG signal when the EA stimulation is simultaneously applied to the human body. The EA stimulator front-end adopts both the large time constant (LTC) S/H current matching technique [1] and the offset current regulation [2] for the accurate charge balancing. As a result, it can achieve less than 10 nA DC offset current. There are 25 concentric circular electrodes in the bottom of the proposed system. The dynamic electrode impedance matching circuit monitors the stimulation voltage swing and optimizes the area of the stimulation electrodes and the sensing electrodes for the high CMRR. The proposed diagnosis IC of 25mm^2 is fabricated in 0.13 μm RF CMOS technology, and dissipates only 3.6 mW from 1.2 V.

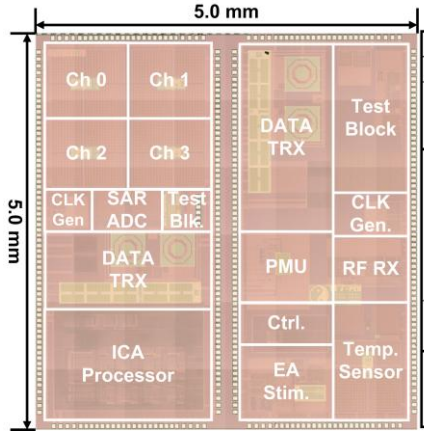

TABLE I. CHIP SUMMARY

Process	0.13μm RF CMOS	
Die Size	5.0 × 5.0mm² (including pads)	
Power Consumption	Coin Battery	1.2V, 6.2mAh (I_{MAX}=18mA)
	Max. 3.6mW (I_{STIM}=520μA)	
Multi-Modal Sensor Front-End	ECG, EMG, EEG	
	Sampling Rate	2kHz
	Gain	54/60/74/80 dB
	Bandwidth	0.3Hz~1kHz
	Input Noise	0.3Hz~1kHz
	CMRR	> 85dB
ICA	# of Channel	4
	Method	Fast ICA
EA Stimulator Front-End	Amplitude	40~520μA
	Frequency	1~500Hz
	DC Offset	< 10nA

Fig 1. Chip micrograph and its performance summary.

Acknowlegment: This work was supported by the IDEC.

[1] K. Song, and et al., "A Sub-10nA DC-Balanced Adaptive Stimulator IC with Multimodal Sensor for Compact Electro-Acupuncture System," *IEEE ISSCC Digest of Technical Papers*, pp. 296-297, Feb. 2012.

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Adaptive Output-Voltage Boost Converter for Compact Electro-Acupuncture System

Hyungwoo Lee, Yongsu Lee, and Hoi-Jun Yoo
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST)
E-mail : hwlee@eeinfo.kaist.ac.kr

Electro-acupuncture [1] is a combination of acupuncture and electric stimulation. In general treatment, the maximum stimulation current should be up to 1mA. Moreover, the contact impedance of needles is modeled as the series of 150 ohm-resistor and 17 nanofarad-capacitor. As a result, the boost converter is required to provide high voltage supply, more than 3V, to the current driver for staring the high contact impedance with high efficiency.

Fig.1 shows the architecture of the proposed adaptive output-voltage boost converter. It consists of two main blocks. One is Adaptive Boosting Core (ABC) and the other is Stimulation Current Sensing and Feedback. Fig.2 shows the efficiency of the boost converter versus the stimulation current, loaded to the converter. As a result, it is possible to maintain the efficiency about 70% for the stimulation current range from 40μA to 1mA. This work was supported by the IDEC.

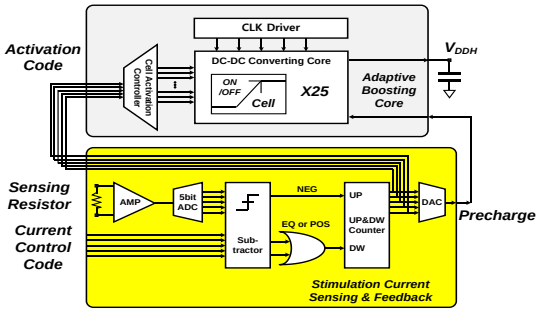

Fig 1. Overall Architecture of the proposed adaptive output-voltage boost converter

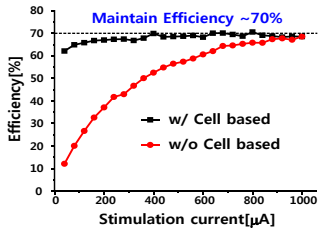

Fig 2. Conversion efficiency with the stimulation current

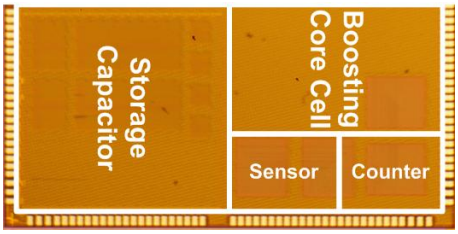

Fig 3. Chip photograph

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A 34.1fps Scale-space Processor with Two-dimensional Cache for Real-time Object Recognition

Youchang Kim, Junyoung Park, Gyeonghoon Kim, Jin-Mook Lee, and Hoi-Jun Yoo
Department of Electrical Engineering, KAIST, Daejeon, Korea
E-mail : youchang.kim@kaist.ac.kr

A scale-space processor with two-dimensional cache is proposed to achieve real-time object recognition in HD 720p images. Scale-space is the most commonly used concept to achieve scale-invariant property in object recognition, however its high computational cost makes it hard to implement a real-time object recognition processor. We employ hierarchical convolution accelerator (HCA) which computes multiple pixels in a single cycle with various kernel sizes. In addition, two-dimensional cache (2D Cache) supports accessing column-wise consecutive data from any image window. A pre-fetch controller for the proposed 2D Cache improves the hit rate by exploiting the sequential access pattern of convolution tasks. As a result, the scale-space processor achieves 34.1fps on a HD 720p image while consuming peak power of 84.5mW.
*This work was supported by the IDEC.

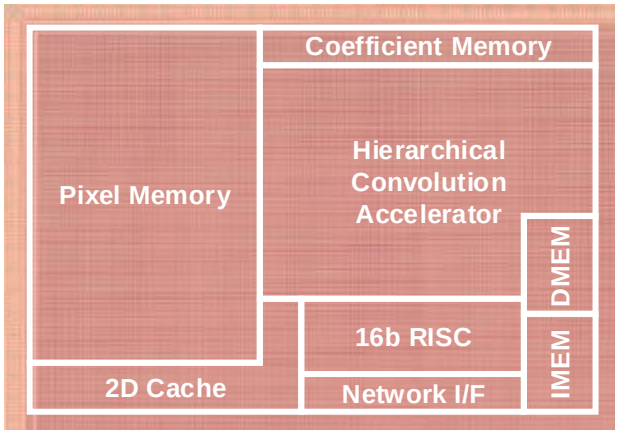


Figure 1. Chip Photograph

[1] David G. Lowe, “Distinctive image features from scale-invariant keypoints,” International Journal of Computer Vision, vol. 60, no.2, pp. 91-110, 2004.
[2] Tony Lindeberg, “Scale-space theory: A basic tools for analysing structures at different scales,” Journal of Applied Statistics, vol. 21, no. 2, pp. 225-270, 1994.
[3] Alan Jay Smith, “Cache memories,” ACM Computing Surveys, vol. 14, no. 3, pp. 473-530, 1982.

A 37.5 μW Body Channel Communication Wake-up Receiver with Injection-locking Ring Oscillator for Wireless Body Area Network

Hyunwoo Cho, Joonsung Bae, Jaeeun Jang, and Hoi-Jun Yoo
Department of EE, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea
E-mail : hwcho@kaist.ac.kr

In the body channel communication which is the most energy efficient wireless communication method [1], the usage of the wake-up receiver can be a possible solution for the efficient duty-cycled communication. The wake-up receiver continuously monitors the channel for requests and activates the transceiver while consuming little amount of power compared with main receiver. In this paper, the BCC wake-up receiver for efficient duty cycled communication is proposed. The proposed wake-up receiver uses the injection-locking ring oscillator (ILRO) to amplify the input signal and PLL based demodulator is adopted to directly demodulate the FSK modulated signal [2].

The overall architecture of the proposed wake-up receiver is shown in Fig. 1. The input signal is frequency modulated to compatible with main receiver [2]. Since the body channel has band pass characteristics between 30MHz to 120MHz, we select the frequency of 40MHz and 50MHz for data 0 and data 1. The ring oscillator amplifies the input signal to the full swing rectangular signal with negligible power consumption due to the injection-locking phenomenon. The fully amplified frequency modulated input signal is demodulated to the digital signal by using the PLL-based demodulator. The fabricated chip process is 130nm and supply voltage is 0.7V for low power consumption and chip area is 1.6mm^2. The total power consumption is 37.5μW with -62.7dBm sensitivity which is the lowest power consumption in the world.

This work was supported by the IDEC

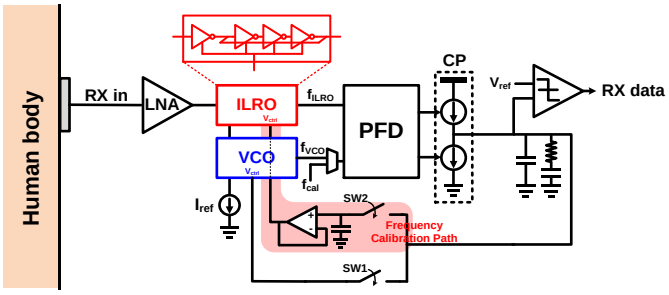


Fig 1. Overall architecture of the proposed wake-up receiver

[1] N. Cho, L. Yan, J. Bae, and H. –J. Yoo, IEEE ISSCC, in press (2008).
[2] H. Cho, J. Bae, and H. –J. Yoo, IEEE T-CAS I. in press (2013)

High-speed Support Vector Machine Processor

Junyoung Park, Kyeongryeol Bong, and Hoi-Jun Yoo
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : junyoung.park@kaist.ac.kr

Support Vector Machine (SVM) has been widely used as a decision making algorithm in many intelligent applications. The reason why many applications adopt SVM is well described in [1]. The main obstacles to the hardware implementation of SVM is the processing speed. The operations of SVM contains some non-linear kernel computations such as polynomial, gaussian radial basis function, or sigmoidal hyperbolic separating function. Nowadays high-performance desktop microprocessors have built-in floating point hardware, but it is not suitable in the embedded system. In this work, we present an automated non-linear kernel operation processing elements with fixed-point calculation approximation. It provides sufficient accuracy for most pattern recognition applications such as object recognition, bio-signal recognition. The top architecture of the proposed SVM processor is shown in Fig. 1. It consists of 3-stage programmable controller with 2-kBytes instruction memory and separated 4kByte data memory. For special instructions for SVM kernel operations, it adopted 20 processing elements for Kernel computation. It provides the results from the fixed-point LUT(look-up-table) based memory. In the SVM algorithm, one of the kernel parameter is constant during the evaluation so the Kernel memory is pre-fetched before loading the query vector. The proposed processor is implemented using 65nm CMOS technology. The fabricated processor operates under 200 MHz clock frequency. The proposed SVM architecture is integrated together with an object recognition processor for its pattern recognition evaluation.

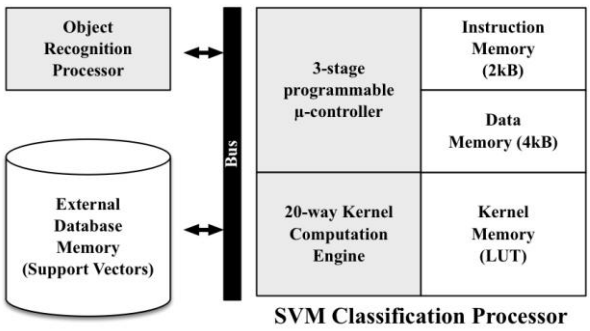


Fig 1. Top architecture of the proposed processor

This work was supported by the IDEC.

[1] C.J.C. Burges, A tutorial on support vector machines for pattern recognition, Data Mining and Knowledge Discovery, Vol. 2, pp.121-167, 1998.

Retinex Image Enhancement Processor for Robust Illumination Adaptation

Junyoung Park, Sung-Pill Choi, and Hoi-Jun Yoo
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : junyoung.park@kaist.ac.kr

The conventional video recording devices perform poorly in the cases of rapid changes of light intensity due to the limited dynamic range of their image sensors. In the case of autonomous vehicles or mobile intelligent robots, the vision systems are continuously exposed to dynamic lighting condition changing, for example, when passing through tunnels, facing specular reflections. In conventional method, wide dynamic range CCD or CIS have been implemented to resolve these problems. In the contrary, human being can easily see individual objects both in the sunlight and shadowed area, since the eye locally adapts while scanning the different regions of the scene [1]. So the computational model of human retina, a.k.a. Retinex, has been adopted for our hardware system. The proposed processor consists of two hardware elements: one is Recursive Gaussian Engine (RGE) and another is the Reflectance Calculation Engine (RCE). It is shown in Fig. 1. RGE performs Gaussian filtering in the recursive method for low hardware overhead. In a conventional method, the radius of the Gaussian filter window is usually determined by 3 times of the scale parameter (σ) of the filter in most cases. Considering the fact that Retinex algorithm requires several different types of scale value, different size of windows are required. The undetermined window size should be avoided in the pipelined operation because the execution time is unexpected. The proposed processor is implemented using 0.11μm CMOS technology through IDEC MPW. The operating frequency of the processor is 100 MHz at 1.2V. The proposed system is capable of performing the QVGA-sized image enhancement in 30fps real-time.

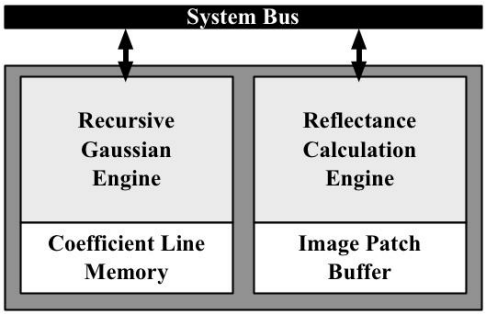


Fig 1. Top architecture of the proposed processor

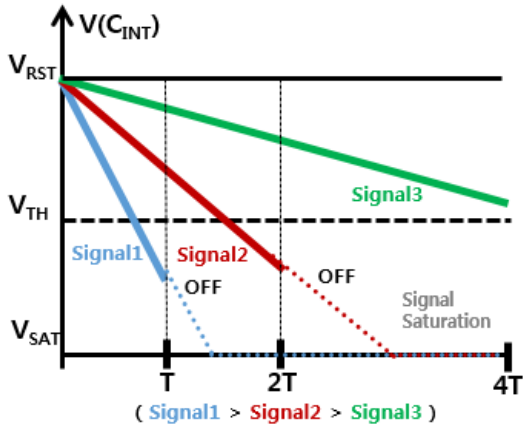
This work was supported by the IDEC.

[1] Z. Rahman, et al., A Comparison of the Multiscale Retinex With Other Image Enhancement Techniques, IS&T's 50th Annual Conference: A Celebration of All Imaging, 1997.

A Low-Power Integrator Circuit Design for Infrared Sensor

Yeong Seon Kim, Hee Chul Lee
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Korea
E-mail : kimgo12@kaist.ac.kr

An infrared(IR) image sensor module is a system that detects an image signal by the IR wave. In this paper, a low-power integrator circuit diesign for the IR image sensor module was proposed. The integrator is the circuit that integrates a current signal in the capacitor during the integration time (4T). In case of large- signal (signal1 and signal2), the signal is saturated in the integration time. The saturated signal do not need to be integrated. Therefore, it is possible to turn off the integrator and save the power consumption of the integrator. To find the signal1, a comparator compares V(CINT) with VTH at T(sec). If V(CINT) is lower than VTH, a logic circuit turns off the integrator. To find the signal2, the comparator compares V(CINT) with VTH at 2T(sec). If V(CINT) is lower than VTH, the logic circuit turn off the integrator. The power consumption of the integrator which is turned off at T=35usec or 2T=70usec is lower than the power consumption of the conventional integrator which integrates the current signal during 4T=140usec. The operation of the proposed integrator and the power consumption of the proposed integrator were verified by the simulation.



Simulation Result		
	Integrator operation time [sec]	Power Consumption during 140usec [uW]
Signal1	35u	53.23 ~ 61.98
Signal2	70u	119.7 ~ 123.9
Signal3	140u	246.9 ~ 253.3

Fig 1. Time diagram of Proposed Integrator and its Power consumption result

[1] D.H. Woo, C.H. Hwang, Y.S. Lee and H.C. Lee – Time based pixel-level ADC with wide dynamic range for 2-D LWIR applications on Electronic Letters, 2005, volume 41, Issue 14.
[2] M. Keating, Low power Methodology Manual, Springer, 2007.

Self-bias controlled ROIC for Uncooled Infrared sensors

Y. M. Jo, D. H. Woo and H. C. Lee
Department of Electrical Engineering, KAIST, Daejeon 305-701, Republic of Korea
E-mail : ymjo@kaist.ac.kr

Recently, low power, low price and small microbolometer are required. One of limiting factor is thermo-electric cooler (TEC). It makes microbolometer which is sensitive to temperature have stable temperature. And the TEC require 0.5 to 2W of power and 3 to 10cm^3 of a additional volume.[1] So, the ROIC need to get rid of the TEC. But, it makes DC output level and dynamic range change. We designed self-bias controlled ROIC for solving the problems without the help of digital system.

We propose a self-bias controlled circuit in which bias voltage is no longer constant and changes according to the temperature values. Fig. 1 shows the self-bias controlled unit cell circuit. And eq. (1) is output voltage of the proposed circuit. In eq. (1), b_D and b are very similar value. So, Vout is almost constant value with operating temperature. It means that dynamic range and DC output level are insensitive to temperature.

$$V_{out} = \left(\frac{I_{bias} \cdot R_{Do} \cdot T^{-3/2} \cdot e^{b_D/kT}}{R_o \cdot T^{-3/2} \cdot e^{b/kT}} \cdot T_{\text{int}}\right) / C_{\text{int}} \approx \frac{I_{bias} \cdot R_{Do} \cdot T_{\text{int}}}{R_o \cdot C_{\text{int}}} \quad (1)$$

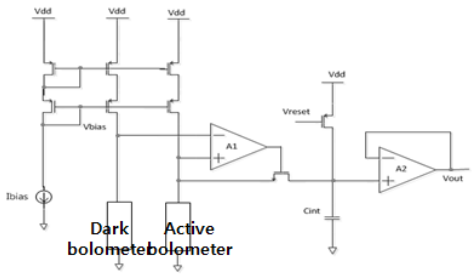


Fig 1. Proposed self-bias controlled ROIC

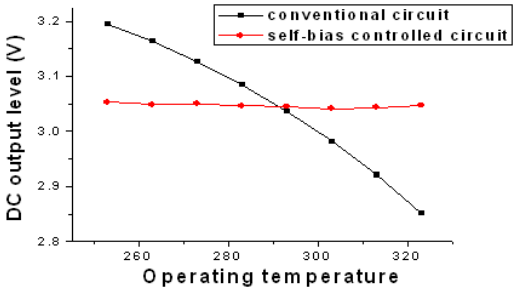


Fig 3. DC output level of proposed circuit (measurement)

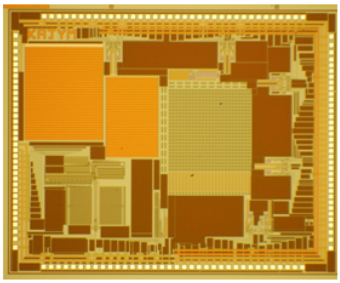


Fig 2. Fabricated chip (IDEC MPW H/M 0.35um process)

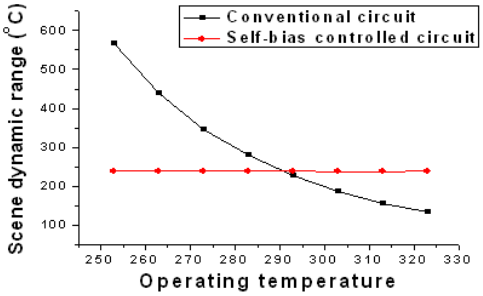


Fig 4. Expected scene dynamic range (calculated)

[1] William J. Parrish, James T. Woolaway, "Improvements in uncooled systems using bias equalization," Proc. SPIE, (1999)

[2] P.K. Chan et al., "Designing CMOS folded-cascode operational amplifier with flicker noise minimization," Microelectronics Journal 32, (2001)

Emulated zero-inductor current sensor for buck-type DC-DC converter

Sung-Wan Hong
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : hsw_0930@kaist.ac.kr

In the synchronous type converter, zero inductor current sense is required to increase power efficiency in the light load condition. To sense zero inductor current, the current flown through the PMOS power switch (M_p) is usually sensed by sensing voltage difference between both sides of M_p, however, this is not easy because the voltage difference is quite small. This problem can be solved by using emulated zero inductor current sensor shown in Fig. 1. In this circuit, rising and falling slope of inductor current are emulated in form of voltage as shown in this figure, similar to [1]. When M_p is turned on with clock of Φ_p, emulated voltage (v_{AC_i}) for zero-inductor current sensor is reset to the reference voltage during quite short time. After that, the v_{AC_i} increases with the rising slope shown in this figure until power NMOS switch (M_n) is turned on with clock of Φ_n. In this time, v_{AC_i} decreases with the falling slope shown in this figure. If the v_{AC_i} decreases below than the reference voltage, the M_n is turned off because this mean that inductor current becomes zero. If not, the M_p and M_n are switched regardless of this circuit. Measured waveform is shown in Fig. 2. As shown in these waveforms, the DC-DC converter properly operates in discontinuous conduction mode (DCM) due to the proposed the zero-inductor current sensor. This work was supported by the IDEC.

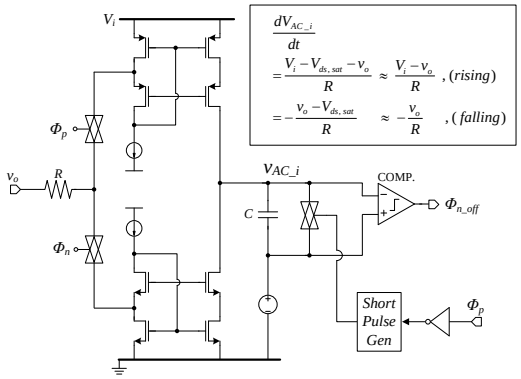


Fig. 1 Schematic of zero-inductor current sensor

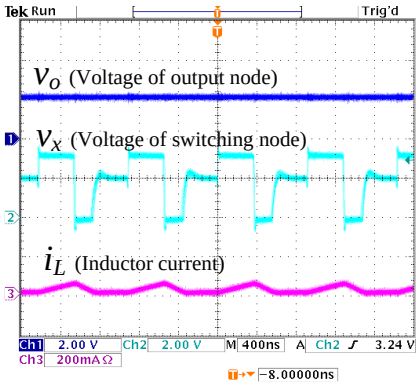


Fig. 2 Measured waveforms when I_o is 15 mA

[1] L. H. Phuc, et. al., "Integrated zero-inductor-current detection circuit for step-up DC-DC Converters", Electron. Lett., vol. 42, no. 16, pp, 943-944, Aug. 2006
[2] Erickson, R. W., and Maksimovic, D. : 'Fundamentals of power electronics' (Kluwer Academic, 2001, 2nd edn.), Chaps 11 and 12

CMOS Band-gap Reference with High PSRR and Low TC

Seki Kim, Gyu-Hyeong Cho
Electronic Engineer, Korean Advanced Institute of Science and Technology, Daejeon 305-701, Korea
E-mail : seki_kim@kaist.ac.kr

기준전압회로(Bandgap Reference)는 아날로그 또는 Mixed-Signal 회로의 필수적인 요소로써 이 회로가 정상동작 하지 않을시에는 해당 회로가 올바르게 동작할 수 없기 때문에 가장 기본적이면서 중요한 부분이다. 기준전압회로는 Supply 전압의 움직임과온도의 변화에 둔감해야 한다. 즉, 높은 PSRR 과 낮은 TC 특성이 필요하다. [1],[2],[3]

본 논문에서는 낮은 TC 특성을 낼 수 있는 보상회로와, 대부분의 회로에 간단하게 추가하여 높은 PSRR 을 얻을 수 있는 Pre-regulator 를 이용하여 구현한 Bandgap Reference 회로를 제안한다.

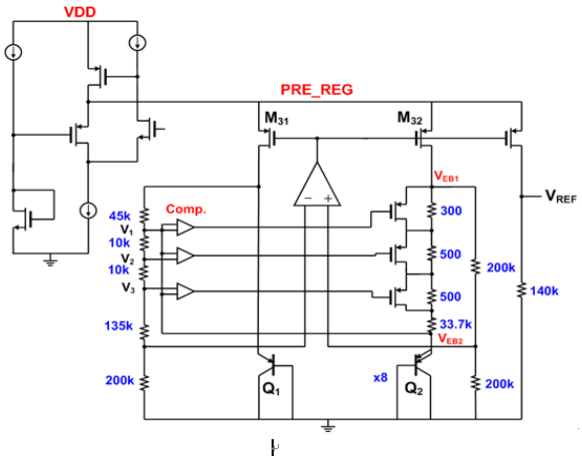


그림 1. 제안된 최종 Band-gap Reference 의 구조

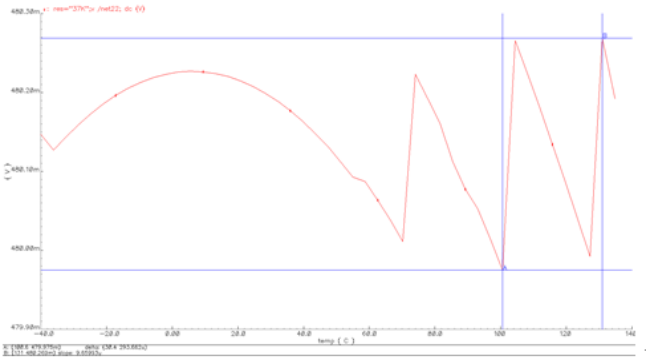


그림 2. 제안하는 BGR Voltage Curvature

[1] Adriana Becker-Gomez, "A Low-Suplly-Voltage CMOS Sub-Bandgap Reference," in *IEEE Transaction on Circuit and Systems-II(TCASII)*, 2008, pp. 609-613
[2] Guang Ge, "A Single-Trim CMOS Bandgap Reference with a 3-sigma Inaccuracy of ±0.15% from -40℃ to 125℃," in *IEEE Inl. Solid State Circuit Conference(ISSCC)*, 2010, pp. 78-79
[3] Raymond T. Perry, "A 1.4V Supply CMOS Fractional Bandgap Reference." In *IEEE J. Solid-State Circuit*, 2007, pp. 2180-2186

적혈구 응집능 측정 Read-Out IC 설계

최석환, 조규형
한국과학기술원 전기 및 전자공학과
E-mail : skhwany@kaist.ac.kr

혈관 속의 혈액의 속도가 높고 낮음에 따라 혈구가 퍼지고 응집되는 경향이 있다. 이를 적혈구 응집능(Aggregability)이라 하여 심혈관 질환과 관련이 있는 인자로 다루어 지고 있다[1-3]. 기존의 측정방법은 주로 광학적인 방법으로서 혈액에 빛을 투과하여 투과된 빛의 양으로 응집능을 판단하기도 한다. 광학방식은 적은 시료량, 일회용 마이크로채널의 사용 등으로 편리하다는 장점이 있지만, 장비의 크기와 복잡성, 긴 측정시간의 단점이 있다. 본 논문에서는 소량의 혈액으로 측정과정의 복잡성을 최소화 하여 소형 진단기기로의 실현가능성이 있는 응집 측정 시스템을 제안하고 있다. 본 시스템은 Fig. 1 와 같이 채널 과 측정 회로로 구성되어 있다. 채널은 손가락에서 채취한 한 방울(5~6ul) 정도의 전혈(Whole Blood)이 필요하고, 부착된 전극을 통해 측정 회로와 연결된다. 채널 바닥에 존재하는 금속바늘은 채널 아래의 회전하는 자석과 함께 회전하므로 혈구를 분산 혹은 응집시키게 된다. 측정회로는 시험적으로 discrete 소자들로 구성된 회로를 바탕으로 ROIC 를 설계하게 되었다. 여기서 나오는 최종적인 출력은 응집지수 계산에 쓰이는 값이 된다. Fig. 2 는 설계된 ROIC 를 주요 기능을 중심으로 그린 블록도이다.

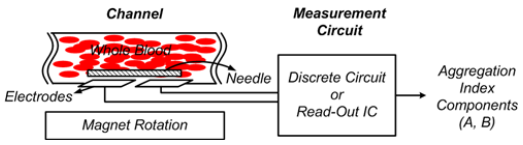


Fig 1. Total Measurement System

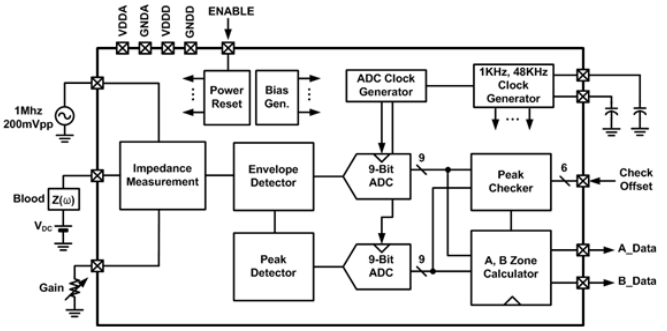


Fig 2. Block Diagram of the ROIC

References

[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, Nat. Nanotechnol. 6, 147 (2011).

[2] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee, ACS Nano, in press (2013).

* This work was supported by the IDEC.

5 Level Audio Power Amplifier for reducing the switching noise and EMI effect

Young-Sub Yuk, Hui-Dong Gwon, Sung-Won Choi, and Gyu-Hyeong Cho
Department of Electrical Engineering, KAIST, Korea
E-mail :bvtop@kaist.ac.kr, wings@kaist.ac.kr, and swon0927@kaist.ac.kr

This paper presents the measurement results of the fabricated chip for the [1] with Dongbu 0.35um CMOS process. Fig.1 shows the proposed audio power amplifier. The output of this amplifier has 3 levels that consist of Vdd/2, ground and –Vdd/2 when the output power is relatively small. However, when the output power is large, to reduce the switching noise and EMI effect, the output of the proposed amplifier has 5 levels that consists of Vdd, Vdd/2, ground, -Vdd/2 and -Vdd. This audio amplifier has fully differential structure for using filter-less structure. The fully differential error amp in Fig 1 integrates the error signals at the error cap. Then these error signals are converted to conventional PWM signal when the output has 3 levels. On the other hands, when the output has 5 levels, the DC shifter changes the DC component of the error signal to generate the modified PWM signal for controlling the output switches. The PWM transformer in the Fig 1 is for distributing this modified PWM signal to the output switch groups correctly. Fig 2 shows the measurement waveform for the proposed audio power amplifier. When the output power is relatively small, the output has 3 levels. On the contrary, when the output power is large, the output has 5 levels. As can be seen in the Fig 2, the output current has clean sinusoidal shape.

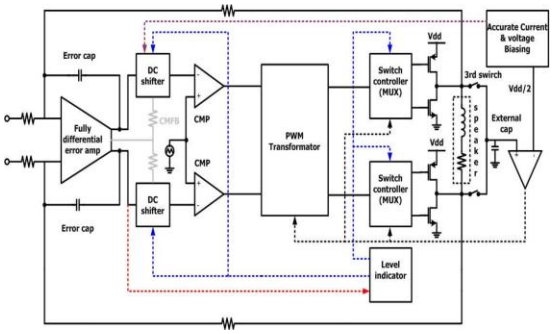
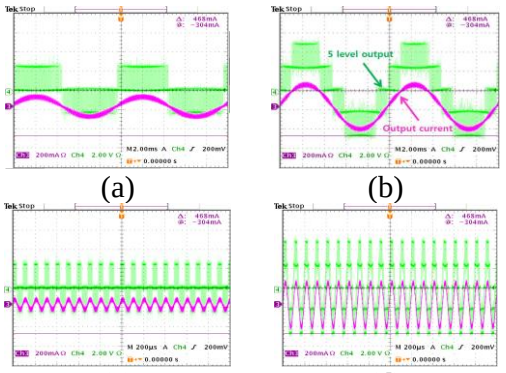
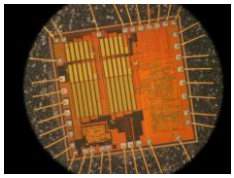


Fig 1. A proposed 5 level audio amplifier



(a) (b) (c) (d)

Fig 2. 3level output and current at 100Hz (a), 5 level at 100Hz, 3 level at 10KHz (c) and 5 level at 10KHz



Process	0.35um
Supply	5V
Efficiency (peak)	92.5% (simulation)
THD	0.16%
Area	6.25 mm²

Young-Sub Yuk, 5 Level Filter-free Ckass D Audio Power Amplifier for Portable Applications. Master's Thesis, KAIST, 2008

Bae-Kun Choi, High frequency Switching Audio Amplifier for Portable Application using 0.35um CMOS technology, KAIST, Ph.D Thesis, 2006

J.Y. Ryoo, 1W Analog/Switching Mixed-mode Audio Amplifier with on-chip power MOSFET using 0.35um CMOS process, KAIST, Ph.D Thesis, 2004

40V 16 channels PWM LED current driver for display applications

Park, Changbyung

Dept. of Electrical Engineering, KAIST, Daejeon 305-701, Korea

E-mail : pcb@kaist.ac.kr

Most of the mobile devices which adopt liquid crystal display (LCD) are equipped with light emitting diode (LED) back light unit (BLU) due to its compactness and lower power consumption than cold cathode fluorescent lamp BLU. Recently not only mobile devices but also household appliances use LED backlit LCDs. Mobile devices usually control the brightness of the BLU depending on ambient illuminance to manage power consumption. Since the color temperature of LED varies with respect to the flowing current and the color temperature variation over brightness change is undesirable in display application, Pulse Width Modulation (PWM) control is used to vary the brightness of the screen. Brightness of the BLU is controlled by the on-time of LED within constant period and the LED current driver generates PWM output current for the dimming of the LED string synchronous with external control signal. In this case, the operable drain voltage and reference current should be designed as low as possible because of low power consumption and thermal issue and the current switching transient time should be fast for accurate PWM dimming resolution. In this paper, 16 channel 100 mA/channel LED current driver with fast current rising time is proposed.

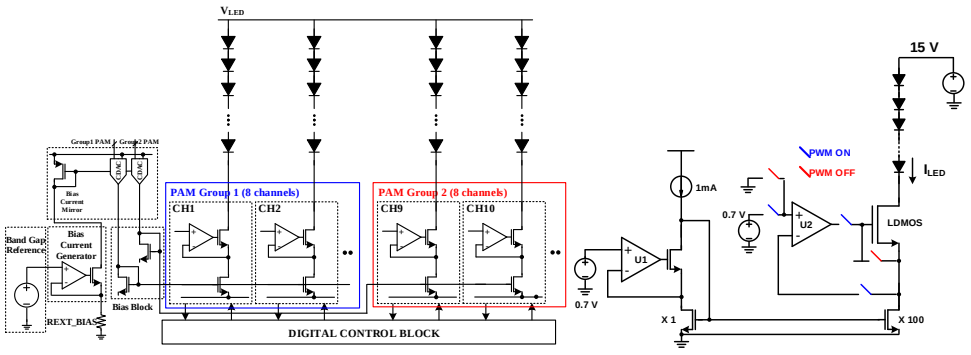


Fig 1. Overall structure of the proposed PWM LED current driver.

Seok-in Hong, *et. al*. “A double-loop control LED backlight driver IC for medium-sized LCDs”, ISSCC, pp116 – 117, Feb 2010.

Freescale, “MC34854 Datasheet”

Maxim, “MAX17061 Datasheet”

On Chip PID Compensation

Sunwoo Lee, Gyu-Hyeong Cho
Electronic Engineer, Korean Advanced Institute of Science and Technology, Daejeon 305-701, Korea
E-mail : leesungwoo@kaist.ac.kr

전력변환기의 소형화는 저전력 모바일 어플리케이션에서 가격 경쟁력과 공간이용의 유연성을 위해 필수적이다. Off Chip 수동요소들의 전체 크기는 칩 크기에 비해 매우 크기 때문에 Off Chip 수동요소들의 수의 감소는 공간을 보다 효율적으로 활용하고 변환기의 비용을 절감하는 데에 효과적인 방법이다. [1] [2]

본 논문에서는 크기를 줄이는데 효과적인 PID 보상 방법을 제안하고 있다. 이것은 PI 보상 요소들 뿐만 아니라 PD 보상 요소들의 크기를 크게 줄일 수 있다.

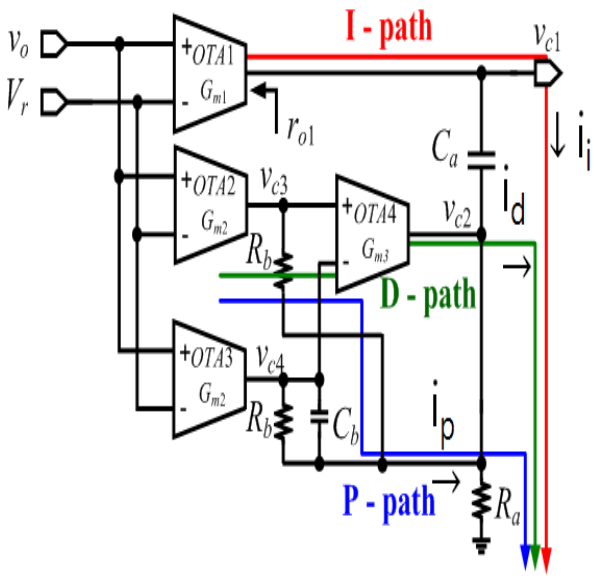


Fig 1. The Proposed PID

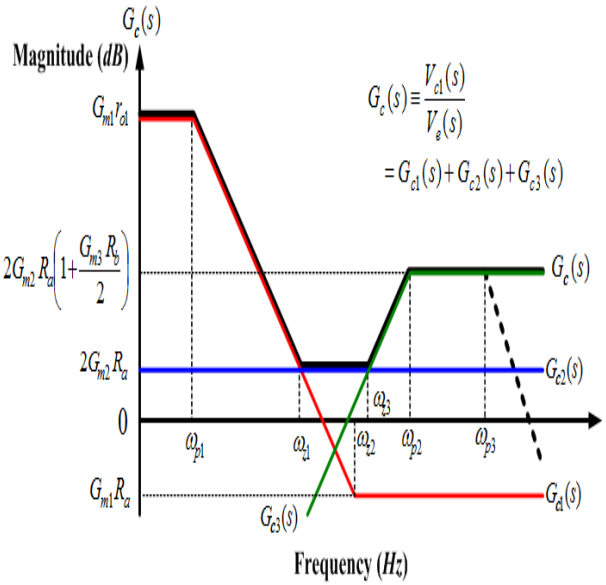


Fig 2.The Bode Plots of the proposed PID

[1] K.-H.Chen, H.-W.Huang, and S. –Y.Kuo, “Fast-transient dc-dc converter with on-chip compensated errop amplifier”,IEEE Trans. Circuit Sys. Exp. Briefs, vol.54, no.12,pp.1150-1154,Sec2007 (2007)

[2] S.W.Wang, W.J.Woo, G.H.Cho, and G.H.Cho, “Emulated multi-path PID compensator for buck converters with large step-down ratio,”in Proc. IEEE Eur. Solid-State Circuits Conf.(ESSCIRC), 2012,pp.446-449 (2012)

Digitally Aided Analog Multiplier Based on a Resistor-String Digital to Analog Converter

Seungchul Jung and Gyu-Hyeong Cho
KAIST, Daejeon, South Korea
E-mail : jung@seungchul.com

In order to identify power information in an AC–DC or a DC–DC converter controlled by regulated power, a multiplier is necessary, as the power information is estimated by the value of the voltage multiplied by that of the current. Many analog multipliers have been studied; however, they are not free from process variations [1, 2]. In this paper, a digitally aided analog multiplier is proposed. Based on digital operation, this analog multiplier is robust from process variations. The proposed multiplier is based on a resistor-string digital-to-analog converter (R-DAC) [3]. The supply voltage of the resistor string (R-String) is usually a constant voltage, V_{DD}, and the pass transistor logic (PTL) selects one point in the R-String according to the digital input. In other words, the output voltage of the R-DAC V_{dac} is proportional to the supply voltage of the R-String. In order to use an R-DAC as a multiplier, the idea is that one input V_a is sampled and saved as a counter value in advance. Then, using the fixed preset value, the supply voltage of the R-String is changed from V_{DD} to another input voltage, designated as V_b. As a result, V_{dac} becomes V_a times V_b divided by V_{DD}.

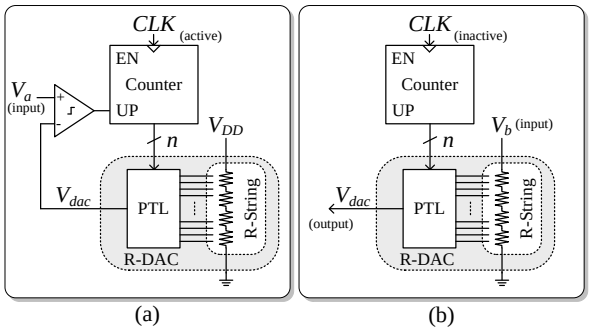


Fig 1. The operation of the multiplier: (a) *Sample Phase*, (b) *Output Phase*

[1] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits. John Wiley & Sons, Inc., 2001, Chap. 10.
[2] D. A. Johns and K. Martin, Analog Integrated Circuit Design. John Wiley & Sons, Inc., 1997, Chap. 8.
[3] D. A. Johns and K. Martin, Analog Integrated Circuit Design. John Wiley & Sons, Inc., 1997, Chap. 12.

A Novel Current Balancing Technique for the Four-Phase Buck

Jun-Han Choi, and Gyu-Hyeong Cho
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : junhan.choi@kaist.ac.kr

벅 컨버터의 경우 리플을 줄이기 위해서 스위칭 주파수를 높여야 하는 반면, 멀티페이즈 벅 컨버터는 리플 전압을 줄이기 위해 페이즈의 개수를 늘리게 된다. 초기에 2-페이즈 벅 컨버터[1]가 연구의 주를 이루었으나, 요구되는 성능이 증가해 감에 따라, 3개이상의 페이즈를 요구하는 컨버터의[2] 연구가 활발해지고 있다. 이와 함께, 페이즈가 증가함에 따라 전류 밸렁싱 테크닉이 중요해지고 있다. 각 페이즈에서 드라이빙하는 전류의 크기는 인덕터 값과 스위칭 듀티 등의 영향을 받게 된다. 이때, 각 페이즈 간 인덕터 미스매치와 스위칭 듀티 미스매치는 전류의 차이를 극적으로 증가시키는 요인이 된다. 본 논문에서는 Figure 5에 보이는 것과 같이 4-페이즈 벅컨버터를 구현하였다. 실효 스위칭 주파수를 높이기 위해 4-페이즈가 적용이 되었으며, 실제 각 페이즈의 스위칭 주파수는 20MHz로 설정이 되었다. Figure 6 에 보이는 바와 같이 전류 밸런싱 회로가 설계되었다. 4개의 페이즈의 평균값을 기준으로 각 페이즈의 전류가 수렴하도록 하여 밸런싱을 맞추었다. 이때, 전류 센스와 평균 전류 센스는 저항과 캐패시터를 사용하여 만들었다. Figure 7 에 보이는 바와 같이 4개의 페이즈가 구현이 되었으며, 전류 밸런싱을 위한 RC 블록 및 컨트롤 블록이 설계되었다.

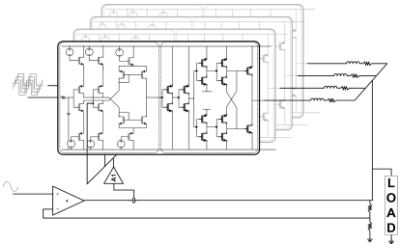


Figure 5. The Conceptual Design of the Multi-Phase Buck

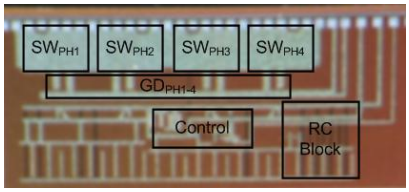


Figure 7. IC Micrographs of the 4-Phase Buck

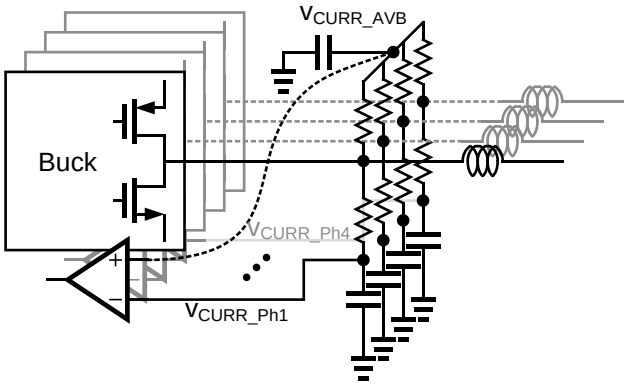


Figure 6. Proposed Current Balancing Technique

[1] Wu, P.Y., et al, "A Two-Phase Switching Hybrid Supply Modulator for RF Power Amplifiers With 9% Efficiency Improvement," Solid-State Circuits, IEEE Journal of , vol.45, no.12, pp.2543,2556, Dec. 2010.

[2] Pengfei Li, et al, "A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters," Solid-State Circuits, IEEE Journal of , vol.44, no.11, pp.3131,3145, Nov. 2009.

A Layout Technique for the Highly-Matched Current Bias Cell

Jun-Han Choi, and Gyu-Hyeong Cho
Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea
E-mail : junhan.choi@kaist.ac.kr

아날로그 회로설계에 있어, 레이아웃 기법의 중요성은 여러 가지 책들[1]에서 강조가 되는 사항 중에 하나이다. 대부분의 IC에는 전류 바이어스 셀이 필요한데, 이러한 바이어스 셀은 많은 경우 매칭이 중요한 경우가 많다. 특히 상대적으로 거리가 떨어져 있는 두 개 이상의 증폭기를 매칭시키기 위해서는 전류 바이어스 셀을 고도로 매칭시키는 것이 중요한 문제가 된다. 본 논문에서는 N개 이상의 바이어서 전류가 필요한 IC에서 고도의 매칭을 유지하며, 체계적인 레이아웃 기법을 소개한다. Figure 5에 보이는 것과 같이 전류 바이어스 셀을 구성할 수 있다. 고도의 매칭을 위해서는 각 캐스코드 셀들은 같은 사이즈를 가져야만 한다. 또한 단일 IC에 많은 기능들을 집적화 하면서 바이어스 셀의 크기가 커지는 경향이 있다. 이는 캐스코드 셀 사이에 미스매치를 유발하게 된다. Figure 10.(a)는 에 보이는 바와 같이 cascode 셀은 (b)와 같이 두 개로 나누어 구성하는 것이 좋다. 두 개의 Half 셀은 추후 Inter-Digitized 되어 고도의 매칭을 유지하는 기본 구조가 된다. Figure 10.(c)에 보이는 것이 기본 캐스코드 셀을 간략하게 레이아웃 한 그림이다. 이러한 캐스코드 셀 N+1개를 이용하여 거대한 바이어스 셀을 만들 수 있으며, 이를 이용할 경우 레이아웃에 투자된 시간대비 훌륭한 매칭을 유도하는 것이 가능하다. Figure 9에 보이는 바와 같이 전류 sourcing을 위한 PMOS 바이어스 셀과 전류 sinking을 위한 NMOS 바이어스 셀을 레이아웃 하였다. 실제 IC에 들어간 위 블록의 크기는 0.045mm^{2}으로써, 일반적인 전류 바이어스 셀보다 크기가 커지지만, 매칭 성능은 월등히 향상되었다.

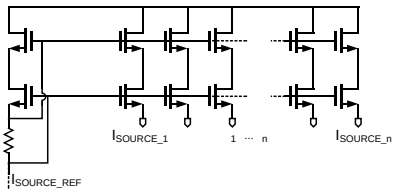


Figure 8. A Basic Current Bias Cell Circuits using Cascode

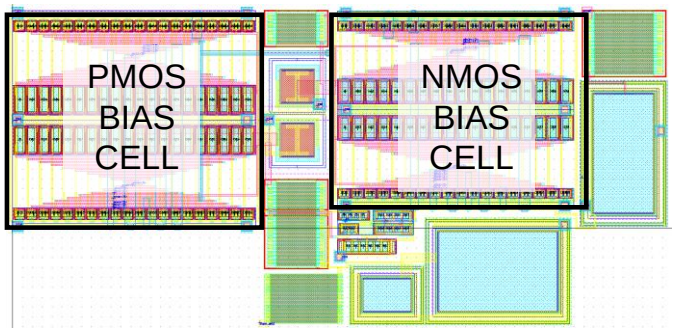


Figure 9. IC Layout for Micrographs of the 4-Phase Buck

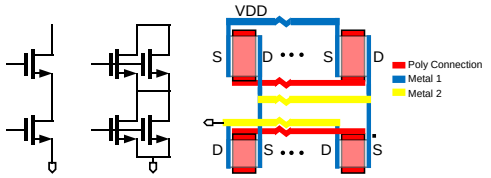


Figure 10. Detailed Layout Implementation

[1] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley&Sons, Inc., 2001.

Streaming ISO18000-6 Type C RFID Tag Design

Joon Goo Lee, Seon Wook Kim, Jae-Sung Rieh, Jongsun Park, and Chulwoo Kim
School of Electrical and Computer Engineering, Korea University, Seoul 136-701, Korea
E-mail : seon@korea.ac.kr

Faster wireless communication with lower power consumption and cost is desirable for most embedded communication systems. We extended the ISO18000-6 Type C [1] that is one of major UHF band RFID protocols, and prototyped the extension [2] with 0.11um technology. Our prototyped system supports up to x5 higher data rate than the original one while supporting the original RFID protocol. The modified protocol supports four new commands and one corresponding response format for efficient large data transmission by considering communication quality and resizing packets dynamically. For this purpose, we added a large-scale memory controller that interfaces with MLC type GByte off-chip flash memory, and modified a response generator. Our RF front-end consists of a 12-stage VM (voltage multiplier), a low drop-out regulator for digital V_{DD}, a ring oscillator to provide 10MHz clock, an envelope detector as a demodulator, a Schmitt trigger for load modulation, and power-on-reset for global reset. Layout and test board are shown in Fig 1. RF block is 680um by 950um and an area of the synthesized digital logic was reported as 72,800um^2. We used the Synopsys PrimeTime to estimate digital power consumption with maximum data rate condition (800kbps for forward and 3.2Mbps for backward). Estimated total power was 69.8 microwatts (V_{DD}=1.2V) and 56.9 microwatts (V_{DD}=1.08V). Our baseband modem operates as we expected. The result of the Friis equation with reasonable assumptions for mobile use, memory power consumption [3], and tag performance show that an operational distance is 5 cm.

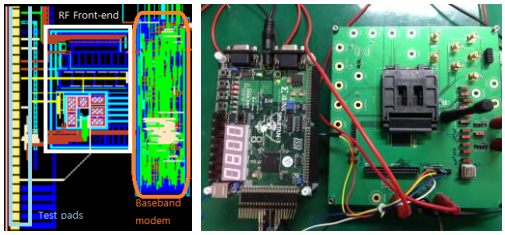


Fig 1. Post layout result of our design and PCB for IC test.

[1] ISO/IEC 18000-6 standard document. (2010).
[2] S. Hwang, Y. Han, S. Kim, J. Park, J.-O. Kim, and Y. Min, ETRI Journal, 33(3):382-392, (2011).
[3] V. Mohan, T. Bunker, L. Grupp, S. Gurumurthi, M.R. Stan, and S. Swanson, TCAD, 32(7):1031-1044 (2013).

저 복잡도를 가지는 2Gbps급 IEEE 802.11ac용 LDPC 인코더의 FPGA 구현

박효빈, 김나래, 이성주*
세종대학교 정보통신공학과
E-mail : hb8971@itsoc.sejong.ac.kr, narae@itsoc.sejong.ac.kr, seongjoo@itsoc.sejong.ac.kr

저밀도 패리티 검사 코드(LDPC)는 오류 정정 코드(ECC) 기술의 하나로 IEEE 802.11ac 와 같이 초고속 데이터 통신에 적용되고 있다. 본 논문에서는 2Gbps 급 IEEE 802.11ac 무선랜 시스템에 적용 가능한 효율적인 LDPC 부호화기의 구조를 제안하고 FPGA 칩셋을 사용하여 시스템을 검증한다. 제안하는 LDPC 부호화기의 구조는 높은 데이터 전송률을 지원하기 위하여 행렬 곱셈 연산 시 행 방향 연산 및 부분 병렬처리 연산을 사용하고[1], IEEE 802.11ac WLAN 시스템의 다양한 부분 행렬 크기(27x27, 54x54, 81x81)로 인하여 생기는 높은 복잡도를 해결하기 위해 Barrel shifter[2]의 공유 구조를 사용하여 기존 복수의 Barrel shifter 구조 대비 F/F 의 수를 약 40% 줄였다. 본 논문에서는 시스템의 검증을 위하여 1 프레임의 이미지 스트림을 입력으로 받아들여 부호화 과정을 거친 후 AWGN 채널 환경을 통과하고 복호화 과정을 거친 출력 이미지 스트림과 부호화 과정을 거치지 않고 AWGN 채널 환경만을 통과한 출력 이미지 스트림을 비교하여 LDPC 부호화기의 성능을 검증한다.

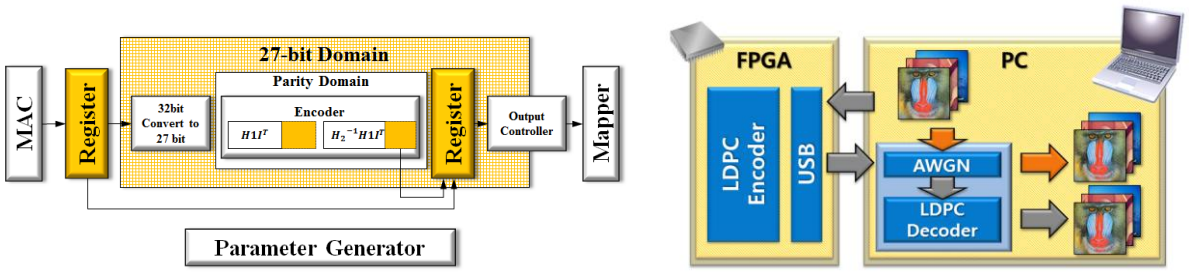


그림 1. LDPC 부호화기의 구조 및 시스템 검증 환경

[1] 정용민, 정윤호, 김재석, “구조적 LDPC 부호의 저복잡도 및 고속 부호화기 설계,” 대한전자공학회 논문지 제 46 권 SD 편 제 10 호, pp. 61-69, Oct. 2009.
[2] A. Mahdi, N. Kanistras, and V. Paliouras, ”An encoding scheme and encoder architecture for rate-compatible QC-LDPC codes,” IEEE Workshop on Signal Processing Systems (SiPS), pp. 328-333, Oct. 2011.

Design of a Fractional-N Frequency Synthesizer for Near Field Communication

Hyuk Ryu, Keum-Won Ha, Joonhong Park, and Donghyun Baek
School of Electrical Engineering, Chung-Ang University, Seoul 156-756, Korea
E-mail : ryuhyuk@naver.com

This paper proposes a 1735.68 MHz fully integrated fractional-N frequency synthesizer for a 13.56 MHz NFC transceiver [1]. The proposed frequency synthesizer is composed of phase locked loop circuits [2] and a proposed high speed logic divider for NFC carrier frequency. To save the power consumption, the high speed logic divider is designed only combination of logic blocks which are high speed D flip-flops and primitive standard cells. The proposed frequency synthesizer is implemented using 0.13 um CMOS technology. The active area occupies 0.23 mm^2 with integrated loop filter. The implemented frequency synthesizer has successful and expected experimental results which can generate 27.12 MHz carrier frequency with 6.92 mA current consumption.

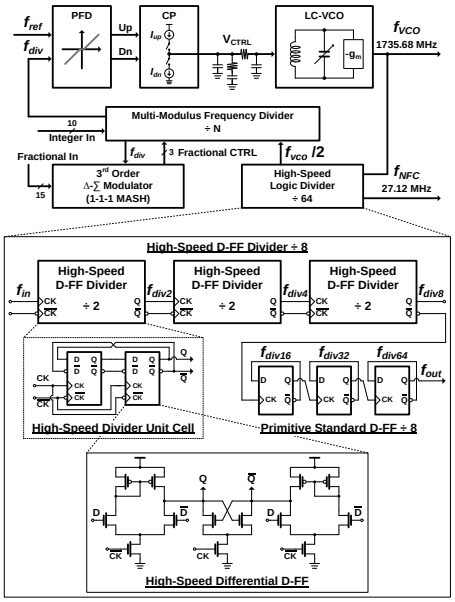


Fig 1. Overall Structure

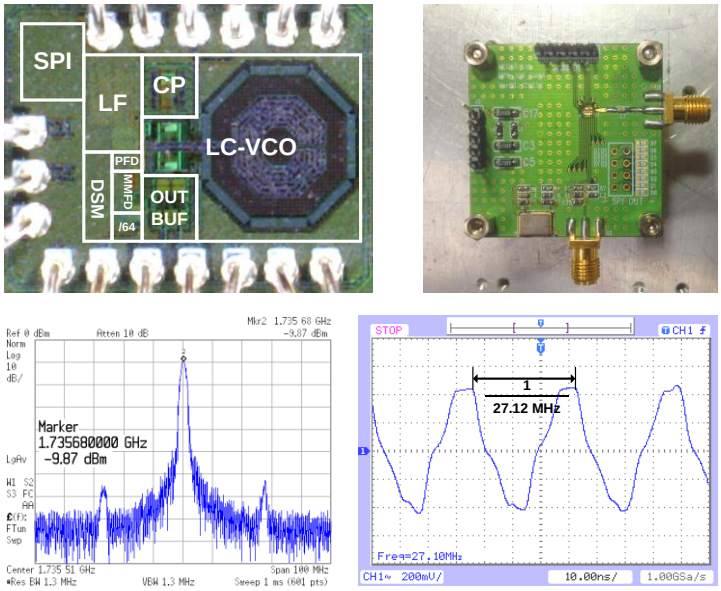


Fig 2. Implemented die photograph and experimental results

This work was supported by the IDEC.

[1] ECMA-340 2nd Edition: Near Field Communication Interface and Protocol (NFCIP-1) (2004).
[2] J. Lee et al., “Charge pump with perfect current matching characteristics in phase-locked loops”, Electronics Letter, vol.36, no.23, pp.1907-1908 (2000).

용량형 입력 임피던스 증가 루프를 적용한 생체 신호 측정 회로

석창호 [1], 임교묵 [2], 서진덕 [1], 김현호 [1], 임승현 [1], 고형호 [1,2*]
[1] *전자공학과*, [2] *차세대전자기판회로학과, 충남대학교*
[*]E-mail: hhko@cnu.ac.kr

생체 신호 측정 기술의 발달로 바이오-메디컬 응용분야에 다양한 진보를 가져왔고, 특히 최근에는 유비쿼터스 헬스 케어 등 모바일 환경에서의 생체 신호 측정의 중요성이 대두되고 있다. 그리고 뇌파 모니터링을 통하여 새로운 유저 인터페이스인 BMI (Brain-Machine Interface)를 구현하여, 생각만으로 기계를 제어할 수 있는 개념들이 등장하고 있다. 뇌파 신호의 특성으로 인해 EEG (Electroencephalogram) 센서는 높은 증폭과 입력 임피던스를 요구한다. 특히 모바일 환경에서 생체 신호 획득을 위해서는 별다른 의료적 처리가 불필요한 건식 전극의 사용된다. 기존의 기술은 건식 전극 등 높은 출력 임피던스를 갖는 신호를 계측하는데 한계가 있다. 이러한 건식 전극의 높은 출력 임피던스를 극복하기 위하여 입력 임피던스 증가 루프가 개발 되었다. 이 기술은 계측 증폭기의 출력을 증폭기의 입력으로 양의 피드백 (positive feedback) 하여 임피던스 증가 루프를 구현하였다 [1, 2].

본 논문에서는 새로운 방식의 용량형 입력 임피던스 증가 루프를 제안한다. 기존의 방식은 추가 증폭기가 필요하여, 회로의 면적 및 전류 소모를 증가시켰다. 본 논문에서는 추가 증폭기 없이 임피던스 증가 루프를 구현하여, 면적 및 전력 소모를 개선하였다. 측정 결과, input referred noise 는 초퍼 안정화 회로를 enable 시 1.49 μVrms 로 측정되었다. 임피던스 증가 루프의 캐패시터에 따라 입력 임피던스가 증가한 결과를 그림 1에 보였다. 증가 루프가 적용되지 않았을 때 입력 임피던스는 644 MΩ이며, 적용되었을 때 입력 임피던스는 3.5 GΩ으로 확인 할 수 있다.

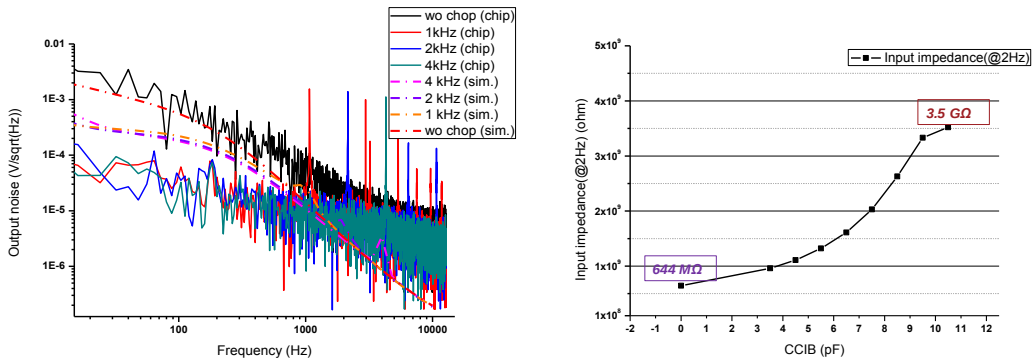


그림 1. (좌) 출력 노이즈 측정 결과 (우) Impedance boosting loop 의 capacitor 에 따른 IA 증폭기의 Input impedance

T. Y. Wang, M. R. Lai, C. M. Twigg, S. T. Peng, "A Fully Reconfigurable Low-Noise Biopotential Sensing Amplifier With 1.96 Noise Efficiency Factor," *IEEE Tran. Biomed. Circuits Syst.*, 2013.

J. Xu, R. F. Yazicioglu, B. Grundlehner, P. Harpe, K. A. A. Makinwa, C. V. Hoof, "A 160 μW 8-Channel Active Electrode System for EEG Monitoring," *IEEE Tran. Biomed. Circuits Syst.*, vol. 5, no. 6, Dec. 2011.

트위스티드 연결구조를 이용한 small 스윙 도미노 회로

안상윤, 김석만, 조경록
충북대학교 정보통신공학
E-mail : {syahn, smkim}@hbt.cbnu.ac.kr, krcho@cbnu.ac.kr

본 논문에서는 도미노로직에서 PMOS, NMOS 입력의 cross 커넥션 방식을 이용하여 신호의 크기를 감소시켜 소비전력을 줄이는 small swing 기술을 제안한다[1-3]. 그림 1 은 본 논문에서 제안하는 피드백 방식의 저전압 스윙 회로와 시뮬레이션 결과를 나타낸다. clk=0 인 예비충전 단계에는 PMOS 가 on 상태가 되어 out 노드의 전압이 증가하고 out 노드의 전압은 PMOS 의 게이트에 피드백 되어 입력된다. out 노드의 전압이 증가하면 PMOS 가 off 상태가 되어 더 이상 out 노드의 전압은 증가하지 않고 out 노드의 전압은 VDD 보다 낮은 전압값을 유지한다. 또한 clk =1 인 로직결정 단계에서는 NMOS 가 on 상태가 되며 NMOS 네트워크의 입력에 의해 로직이 1 로 결정되면 out 노드의 전압은 낮아진다. out 노드의 전압은 NMOS 의 게이트에 피드백 되어 입력되며 out 노드의 전압이 낮아져 NMOS 의 상태를 off 로 만들면 out 노드의 전압은 더 이상 감소하지 않고 0V 보다 높은 전압으로 유지된다. NMOS 네트워크의 입력에 의해 로직이 0 으로 결정되면 out 은 기존 전압값으로 유지된다. 제안된 회로는 0.18μm CMOS 공정을 사용하여 제안한 회로의 출력전압은 최소 0.7VDD 의 스윙폭을 갖는다. 제안된 회로의 출력스윙은 공급전압의 40%스윙으로 일반적인 풀스윙 도미노 로직에 비해 전력소비가 63%로 감소했다.

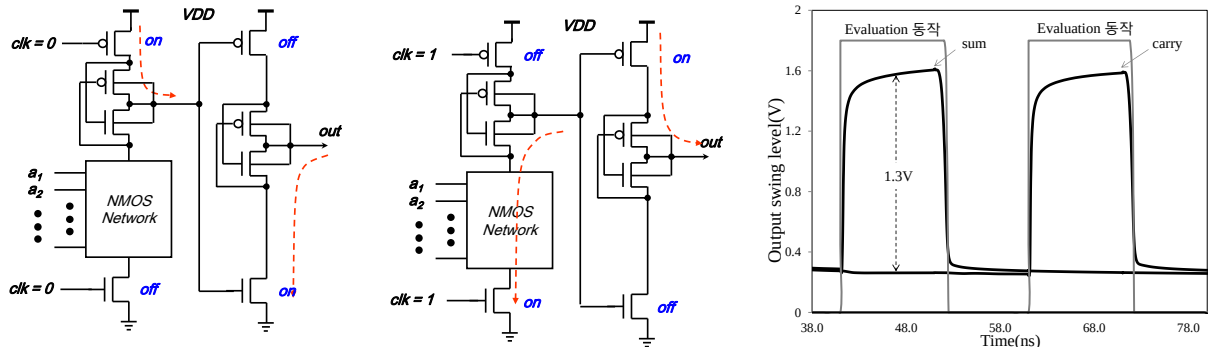


그림 1. 제안하는 저전압 스윙 회로 및 시뮬레이션 결과

[1]강장희, 김정범, "Low-Swing 기술을 이용한 저 전력 CVSL 전가산기 설계," 전자공학회논문지 SD 편, 제 42 권, 제 2 호, pp41-48, 2005.
[2]S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design (3rd. edition)," mcgraw Hill, 2003.
[3]Zhiyu Liu and Volkan Kursun, "Robust Dynamic Node Low Voltage Swing Domino Logic with Multiple Threshold Voltages", International Symposium on ISQED, 2006. pp.30-36.

M2M authentication module based on PUFs

Piljoo Choi and Dong Kyue Kim
Department of Electronics Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : DQKIM@hanyang.ac.kr

Machine-To-Machine (M2M) [1] is the technology which makes decision and controls itself after collecting and processing necessary information by embedded systems or computers with sensors or communication devices. Human control is minimized, and machines do dangerous or time-consuming jobs instead of human. Recently, due to wide spread of various internet ecosystems and market saturation of established communication markets, the M2M industry is emerging as a promising business for the next generation. The stable growth of the M2M industry is based on safe network environments, which needs a mutual authentication mechanism. Hence, we propose M2M authentication mechanism based on Physical Unclonable Functions (PUFs) [2]. For M2M authentication mechanism, we designed an M2M authentication hardware module based on PUFs.

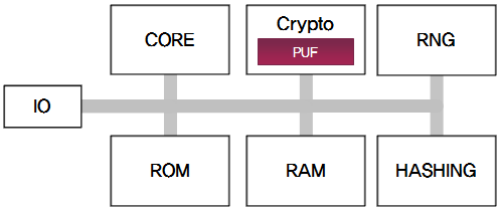


Fig 1. Structure of M2M authentication module

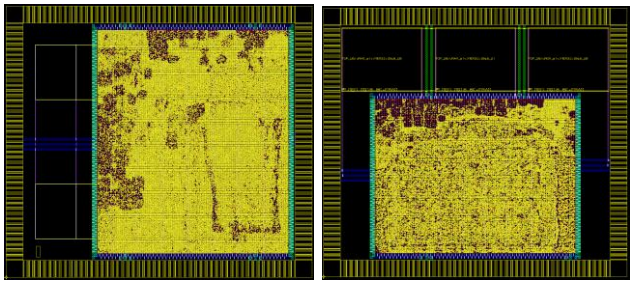


Figure 11. Layouts of implemented modules

[1] ETSI TS 102 689 v1.1.1, Machine-to-Machine Communications (M2M); M2M Service Requirements, 2010.
[2] Ravikanth Pappu, Ben Recht, Jason Taylor, and Neil Gershenfeld, "Physical One-Way Functions", Science, Vol 297, no. 5589, pp. 2-26-2030, 2002.

Offline User Authentication Method of Smart Card using PUF

Jae Seong Lee and Dong Kyue Kim
Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jslee@esslab.hanyang.ac.kr

Smartcard is the IC card in the narrow sense. It includes CPU performs operations by itself and stores information. It can provide more various applications including security applications than magnetic card. Therefore, it has replaced magnetic cards. In this paper, we propose an offline user authentication for smartcards with combining two authentication methods.

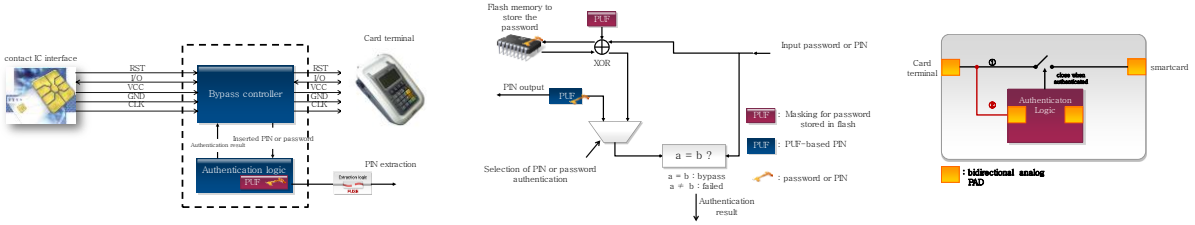


Fig 1. Applied system and authentication logic

This authentication circuits has two selective authentication mechanisms: PIN and password. Fig. 1 shows the authentication circuits with two authentication methods. It consists of two PUF circuits, flash memory, some combinational logics (value comparator and selector of authentication methods). PIN authentication decides the success of that using coincidence between a PUF PIN and an inserted PIN. On the other hand, password authentication uses coincidence of two encrypted passwords with a PUF key: stored one in a flash memory and inserted one.

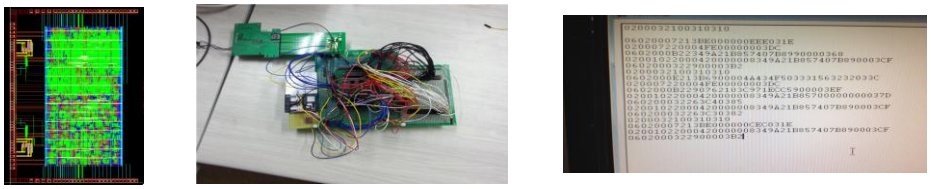


Fig 2. Applied system and authentication logic

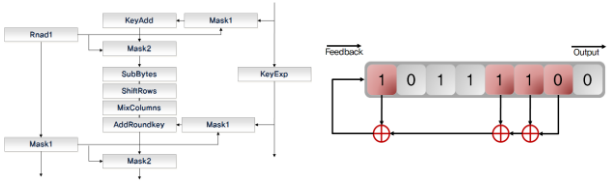
We embodied this authentication circuit as the chip using 0.11um process as fig. 2-(a). We verifies the result as fig. 2-(c), which shows that the terminal can interact with IC card after it was authenticated by the authentication circuit chip using test board as fig. 2-(b). The bypass controller includes a switch connecting between the terminal and the smartcard according to success or failure of authentication.

[1] Ravikanth Pappu, Ben Recht, Jason Taylor, and Neil Gershenfeld "Physical One-Way Functions", Science, Vol 297, no. 5589, pp. 2-26-2030, 2002.

AES hardware module with masking against side channel attacks

Jae Seong Lee and Dong Kyue Kim
Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jslee@esslab.hanyang.ac.kr

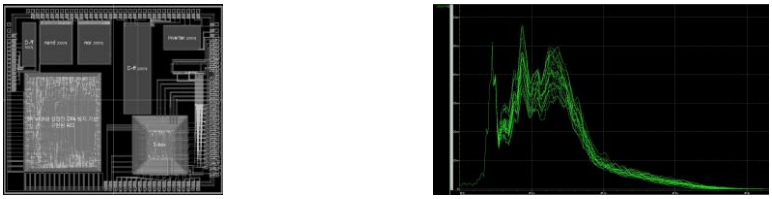
Practical security hardware modules also generate side channel information such as power consumptions and electro-magnetic waves. This side channel information depends on arithmetic operations using plaintexts and the cipher key, so attackers can guess the cipher key using this information. This attack is called side channel attack. It is one of representative hardware attacks, which are commonly used. Due to this necessarity to implement a hardware with countermeasures against side channel attacks, we design an AES hardware module, which is the most used security algorithm, with masking methods against side channel attacks, and embody it as the hardware chip using 0.35um process.



(a)Architecture (b)LFSR

Fig 1. Whole architecture of AES hardware module

Fig. 1 shows the whole architecture of AES hardware module with masking methods. An intermediate value, V, is hidden by m, generated by an embedded random number generator, Linear Feed-back Shift Register (LFSR).



(a)Chip layout (b)Power consumption of AES with masking methods

Fig 2. The result of implementation

Fig. 2 shows the layout and power consumption for the AES security hardware system with masking methods using a 0.35um CMOS process. The waveforms of power consumptions have the different waveforms despite the same inputs.

[1] FIPS PUB 197, National Institute of Standards and Technology, Advanced Encryption Standard, 2001.

SI/PI Co-simulation including Voltage Regulating Circuitry for High-performance Multi-chip Packages

JuHwan Lim, JongJoo Lee, SoYoung Jung, and JoonHee Lee
Memory Division, Samsung Electronics, Korea
E-mail : juhwan.lim@samsung.com

As new NAND specification such as toggle 2.0 has been standardized and developed for high-speed and high-performance flash solution products, I/O supply voltage has been reduced from 3.3V to 1.8V because of the adoption of high-speed stub series terminated logic(SSTL) I/O. Accordingly, because of issues of the backward compatibility with previous specifications and the power budget, voltage regulator, which was implemented in the controller chip mounted together in a package, should supply the power to SSTL I/O. The output of voltage regulator was assumed by ideal voltage source in the conventional signal and power integrities(SI/PI) co-simulation [1]. In this work, we propose the advanced SI/PI co-simulation methodology including voltage regulator circuitry for high-perfomance multi-chip packages. Fig. 1 shows the improvement examples of the NAND interface PCB design operating DDR 400Mbps. Fig. 1(a) shows the eye result by convential simulation and no big issue except somewhat larger jitter. On the other hand, Fig. 2(b) shows the eye result by simulation including votage regulator circuitry and very poor eye opening for the same PCB model as Fig 1(a). It is because the wrong-designed power delivery network(PDN) in the PCB causes a very large voltage drop while I/Os are simultaneously switching, and as the result, very large jitter was induced. Fig. 1(c) shows the good eye result of the revised PCB. In conclusion, we enable the exact prediction from the advanced SI/PI co-simulation including voltage regulator circuitry, and can detect and improve the weak point in PCB PDN design.

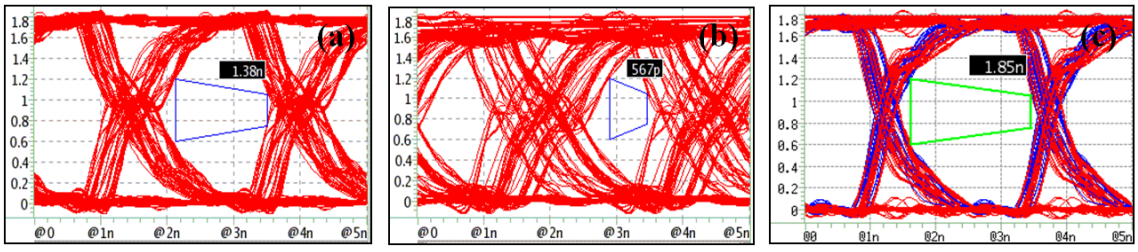


Fig. 1. (a) Conventional and (b) advanced simulation result for initial design, (c) final result

[1] Jongjoo Lee et al, 53rd Electronic Components and Technology Conference, pp1440-1444 (2003).

전류 보조 접합 방법에 의한 Cu-Cu 직접 접합 방법

마성우[1], 신찬호[1], 안기원[2], 이정환[3], 김기범[3], 서민석[3], 변광유[3], 김영호[1,2,*]
[1]한양대학교 나노반도체공학과 [2]한양대학교 신소재공학부 [3]SK 하이닉스 반도체
*E-mail: kimyh@hanyang.ac.kr

칩과 칩을 연결하기 위하여 Cu 와 Cu 를 직접 접합하는 방법은 얇은 솔더 층을 이용한 기존의 방법에 비해 여러 가지 장점들이 있다 [1]. 그러나 Cu 와 Cu 의 직접 접합 방법으로 충분한 접합력을 얻기 위해서는 고온, 고압, 장시간의 접합 조건이 필요하다는 단점이 있다 [2]. 본 연구에서는 Cu/Cu 계면에서의 고상확산을 증가시켜 접합력을 증가시키고 접합 온도와 시간을 단축하기 위해 전류 보조 접합 방법(current assisted boding technology)을 제안하였다. 20 ㎛ x 20 ㎛ 크기의 Cu 범프를 Si wafer 위에 형성하여 flip chip 접합 방법으로 daisy chain 구조를 형성하였으며, 접합하는 동안 일정한 전류를 흘려주었다. 전기적 특성을 평가하기 위하여 접촉 저항을 4-point probe 방법으로 측정하였고, 기계적 특성을 평가하기 위하여 전단강도를 측정하였다. 실험 결과 접합 시 전류를 흘려준 경우가 접촉저항이 낮고, 전단강도는 큰 것을 확인하였다. 열충격 시험(-55℃/+125℃)을 1000 cycles 까지 수행한 결과, 접합 시 전류를 흘려준 경우가 더 좋은 신뢰성을 나타내어 전류를 이용한 접합방법이 효과가 있음을 확인하였다.

본 연구는 SK 하이닉스 반도체의 지원을 받아 수행되었습니다.

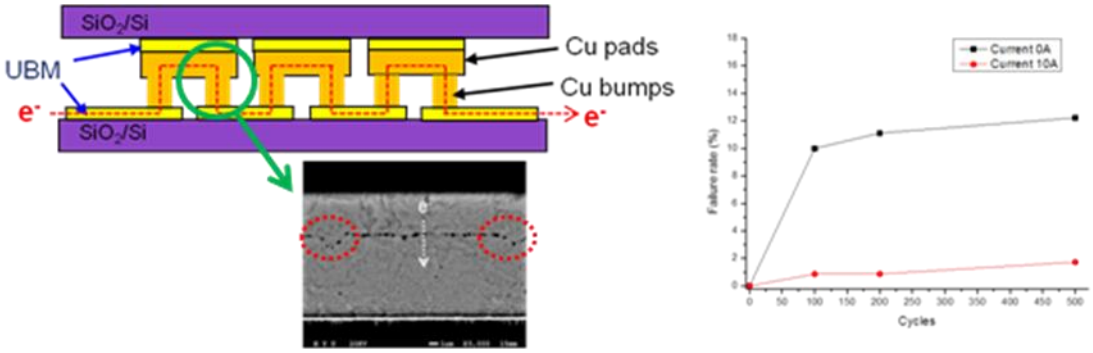


Fig 1. 접합 공정의 개요 및 열충격시험 결과

[1] Rachid Taibi, Léa Di Cioccio, Cedrick Chappaz, et. al., Proceeding of Electronic Componests and Technology Conference, pp. 219-225 (2010).
[2] J. Lannon Jr., C. Gregory, M. Lueck, A. Huffman, and D. Temple, Proceeding of Electronic Componests and Technology Conference, pp. 355-359 (2009).

Parametric Study for Optimum Ag wire Bondability

Kwang-Soo Kim, Jae-Seung Seok, Kyung-Man Kim, Sung-Wook Hwang, Hai-Ick Kim, Joon-Young Oh and Joon-Hee Lee

Solution Development Team, Flash Development, Samsung Electronics Co., Ltd., Korea

E-mail : ks4617.kim@samsung.com

Recently, there is a growing intrest in alternative wiring material to Au because of dramatic increase of Au cost [1,2]. Cu is the most 'cost competitive' solution among alternatives, but has limitation in the reliability ensurance point of view because its hardness is too high to ensure pad reliability. On the other hand, Ag has excellent electrical characteristics, and its reliability and hardness is similar to those of Au[2], but bondability should be solved befere being considered as alternative. In this study, improvement of bondability of Ag is studied. 4 Critical bonding formations, such as 'small chip bonding', 'fine pad pitch bonding', 'chip to chip bonding of cascade stack' and 'RDL (Redistributed Layer) bonding' were optimized. The result shows that non IMC (Intermetallic Compound) formation problems in 'small chip bonding' and short fail problems in 'fine pad pitch bonding' are solved. Also factors which affect the intermetallic quality in the joint area of 'chip to chip bonding' was figured out and same quality as Au was obtained from the evaluation of Forward and Reverse bonding method on RDL. The bonding quality was proved from environmental reliability test such as Pre-cond L2, T/C, uHAST, HTS, LTS, THB and HTDR.

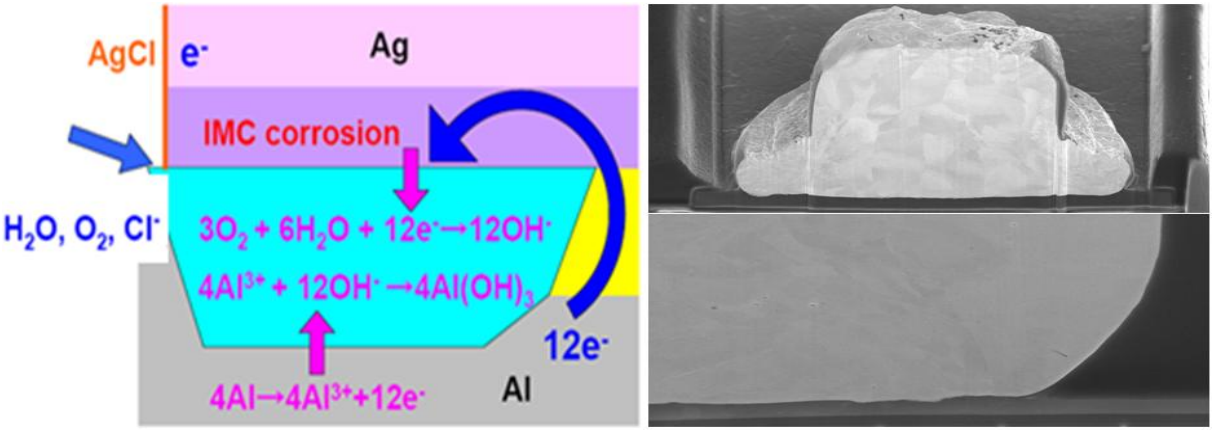


Fig 1. Galvanic corrosion and FIB in Ag-Al system

[1] Liao Jun Kai, Liang Yi Hung, Li Wei Wu, Men Yeh Chiang, Don Son Jiang, C.M. Huang and Yu Po Wang, Electronic Components and Technology Conference, p.1163(2012).

[2] Kyung-An Yoo, Chul-Uhm, Tae-Jin Kwon, Jong-Soo Cho, Jeong-Tak Moon, Electronics Packaging Technology Conference, p.851(2009)

40 um pitch micro bump의 interconnection 평가

Seunghyun Lee, Seongkwon Chin, Sukwoo Jeon and Namseog Kim
SK hynix Inc., *2091 Gyeongchung-daero Bubal-eub Icheon-si Gyeonggi-do, Korea*
E-mail : seunghyun2.lee@sk.com

본 연구에서는 2.5/3D Package 에서 널리 사용되고 있는 micro bump 의 관한 내용으로, 미세 pitch 개발에 따른 interconnection 평가 및 UBM shape 에 따른 solder 흘러내림 평가를 진행 하였다. Micro bump 는 40 um pitch 에 20 um diameter 로 제작 되었으며, UBM 은 Ni 3um, solder (Sn-2.1Ag)14 um 로 제작 하였다. Micro bump 의 interconnection 은 SEM, TEM 으로 관찰하였으며, Bump 표면은 Auger 장비를 이용하여 분석 하였다. Micro bump 의 interconnection 은 bump 표면의 wrinkle 및 solder volume 에 따른 큰 영향은 없었으며, flux 에 잔존하는 C layer 에 따라 큰 영향을 받았다. solder 흘러내림의 경우는 UBM 의 shape 에 따라 큰 영향을 받는걸 확인 하였다.

Modeling and Analysis of EUV Mask Defects for Resist Pattern

Sang-Kon Kim[2]
Department of Applied Physics, Hanyang University, Aansan 151-747, Korea
E-mail : sangkona@hanyang.ac.kr

For the approach of extreme ultraviolet (EUV) lithography to its realization, defects of multilayer mask and line-and-space resist patterns bear challenges. Multilayer defects are partially invisible to traditional mask inspection tools and they cannot be completely characterized with existing metrology tools. Current EUV defect level is too high to accept for device volume production []. In this paper, defects of multilayer mask and line-and-space resist patterns are modeled and simulated by using an efficient rigorous modeling and the stochastic effects. EUV defect control of multilayer mask and line-and-space resist patterns is investigated from the viewpoint of simulation results. This study will be helpful in understanding EUV defect and will also give insight into the EUV defect control for device volume production.

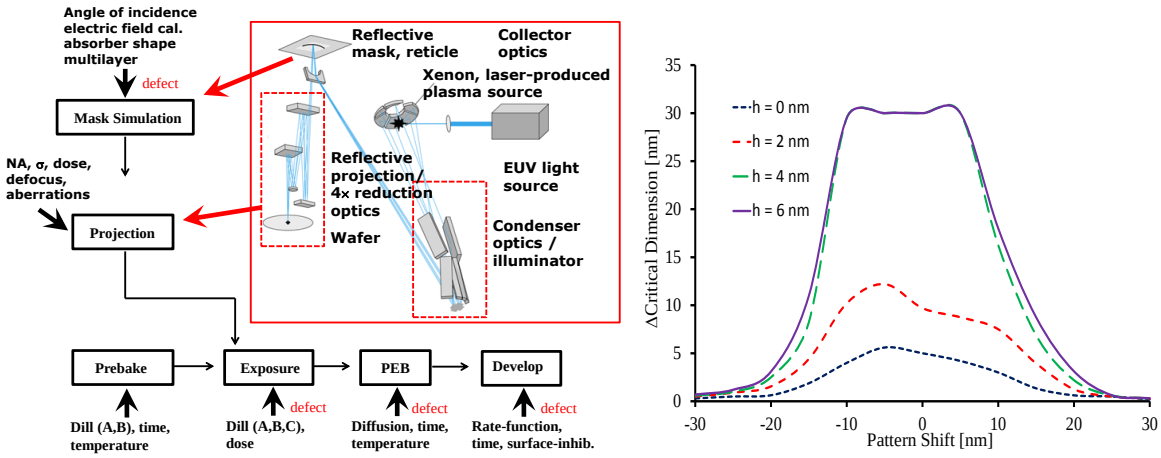


Fig 1. Schematic structure flow of EUV mask defects and maximum CD difference with top height *h* of defects.

[1] P. Liu, X. Xie, W. Liu, K. Gronlund, SPIE Vol. 8679, 86790W (2013).
[2] T. Kozawa, J. J. Santillan, and T. Itanib, SPIE Vol. 8679, 867913 (2013).

[2]Tel: +82-(0)10-4100-6697; Fax: +82-(0)2-6499-3397; E-mail: sangkona@hanyang.ac.kr, sangkona@hotmail.com; Web: www.sangkon.info

EUV 마스크 검사용 Coherent EUV 광원 개발

김용수 [1,2], 안준모 [1], 성하민 [3], 조운조 [1], 박민철 [1], 김점술 [3], 김재헌 [1], 우덕하 [1], 이석 [1], 이주한 [2], 김용태 [1], 전영민 [1]
[1] 한국과학기술연구원 센서시스템연구센터, [2] 서울시립대학교 전자전기컴퓨터공학과, [3] 레이저 스펙트라
E-mail : ymjhon@kist.re.kr

ArF 노광기술의 한계를 극복할 차세대 노광기술로 EUV(Extreme UV, 극자외선) 노광기술이 주요 반도체업체에서 시험생산단계에 이르는 등 이에 대한 연구개발이 전세계적으로 빠르게 진행되고 있다[1]. 본 연구에서는 HHG(High-Harmonic Generation, 고차조화파 발생)[2, 3]을 이용하여 Coherent EUV 광원을 개발하였고, 그 출력특성을 측정하였다. EUV 발생용 HHG 을 위한 펌핑용 레이저 광원으로는 중심파장 796 nm, 펄스폭 35 fs, 펄스 반복률 1 kHz, 펄스당 에너지 5 mJ 의 Mode-Locked Ti:Sapphire 레이저를 사용하였으며, EUV 발생 매질로 Ne 가스를 사용하였다. 출력 스펙트럼은 47 차부터 67 차까지의 홀수 차수에 해당하는 HHG 광이 측정되었으며, 59 차(13.5 nm)에서 세기가 가장 크도록 발진조건을 최적화하였다. 또한 가스셀의 위치와 Ne 가스의 압력 변화에 따라 EUV 광의 출력을 측정하여, EUV 광의 SNR 이 최대가 되도록 최적화 실험을 수행하였다.

본 연구는 지식경제부 및 한국산업기술평가관리원의 산업원천기술개발사업(정보통신) [10039226, EUV 마스크 actinic 검사장비 및 멀티전자빔 웨이퍼 검사기술개발]의 일환으로 수행하였음.

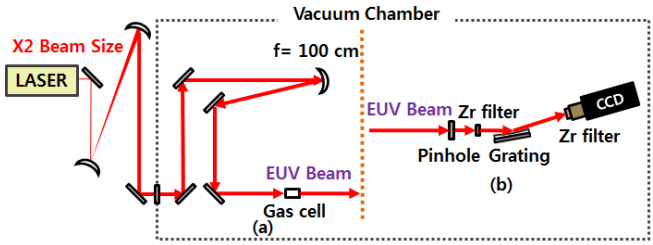


그림 1.

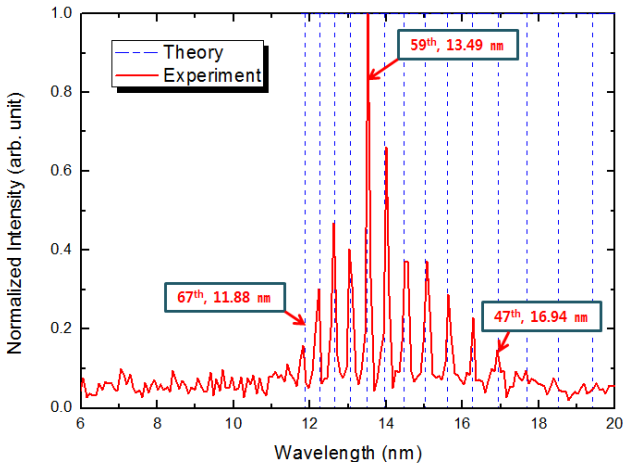


그림 2.

그림 1. 실험 장치도; (a) EUV 광원 장치도 (b) EUV 분광기 장치도, **그림 2.** 분광기로 측정된 EUV 광의 스펙트럼

[1] B. Wu and A. Kumar, J. Vac. Sci. Technol. B 25, 1743-1761 (2007).
[2] P. B. Corkum, Phys. Rev. Lett. 71, 1994-1997 (1993).
[3] E. Constant, D. Garzella, P. Breger, E. Mevel, C. Dorrer, C. Le Blanc, F. Salin, and P. Agostini, Phys. Rev. Lett. 82, 1668-1671 (1999).

Fabrication of Nano-size Cross Array Patterns by Nano Imprint Lithography

Dohyung Kim, Youngin Gil, Changhwan Choi*
[a] Division of Materials Science & Engineering, Hanyang University, 133-791, Seoul, Korea
E-mail*: cchoi@hanyang.ac.kr

비노광 방식의 나노임프린팅 리소그래피 (Nano-Imprint Lithography, NIL) 기술은 기존의 노광 방식인 포토리소그래피 대비 나노스케일의 다양한 패턴 및 구조를 형성하는데 있어 유망한 기술 중 하나이다 [1]. 본 실험은 Liquid Bridge 효과 [2]기반 열 임프린팅 방법을 이용하여 나노스케일의 금속층을 전사(transfer)하였고, 이러한 금속층을 동일한 방법으로 적층하여 Cross-array 구조로 제작해 보았다. 실험에 사용된 금속층은 Thermal evaporator 로 증착된 Al 을 이용하여, 낮은 표면에너지를 갖는 복제 폴리머(PUA)몰드 위에 증착을 실시하였다. 이때, Thichloro-silane 계열의 자기 조립 단분자층(SAMs)이 폴리머 몰드에 형성되어 낮은 표면에너지를 갖게 되면, 양각부위의 잔여 금속층은 DI water 와 Etahnol 을 이용한 Wet cleaning 방법으로 손쉽게 제거가 가능하다. 잔여층이 제거된 폴리머 몰드는 열 임프린팅 공정을 통해 음각 내부의 금속층을 전사하게 되는데, 이때, 공정압력과 온도의 조절을 통해 단층의 금속층을 구현하는 것뿐만 아니라, 공정압력을 조절하여 패턴의 손상 없는 적층형 금속층 구조를 형성할 수 있었다. 적절한 공정압력(10 atm)이 가해질 경우, 원하는 위치에 정확히 패턴을 전사할 수 있었으며, 이러한 압력하에 Liquid Bridge 역할에 사용되는 용매인 Ethanol 을 제거하기 위해 공정온도(80~100℃)에서 휘발시킨다. 위와 같은 동일한 방법으로 공정압력(5~8bar)을 낮춰 두 번째 금속선을 구현할 경우, 적층형 Cross-array 구조를 구현할 수 있었다. 본 연구는 나노스케일 금속 패턴이 요구되는 반도체 분야와 3D 적층 공정이 요구되는 뉴로모픽 소자 형성에 유용한 기법이 될 것으로 사료된다.

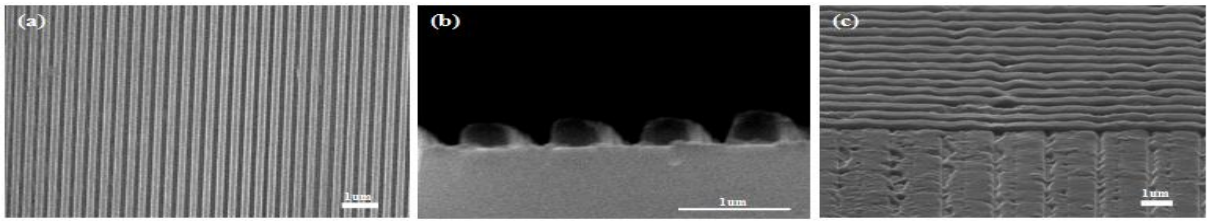


Fig 1. Fabrication of single metal layer (a), (b) and cross-array structure (c)

[1] Guo, L. J. Nanoimprint lithography Adv. Mater. 19, 495–513 (2007)
[2] K Oh, BH Lee, JK Hwang, H Lee, S Im, MM Sung. Small 5, 558–561 (2009)
본 연구는 한국연구재단을 통해 미래창조과학부의 미래유망 융합기술 파이오니어사업으로부터 지원받아 수행되었습니다 (2012-0009460).

Passivation layer effects on oxide semiconductor thin films during thermal annealing

Chi-Sun Hwang, Sang-Hee Ko Park, Sung-Heang Cho, Min Ki Ryu, Himchan Oh, Jong-Heon Yang
Su Jae Lee, Chunwon Byun, Jonghyurk Park, Jae-Eun Pi, Eunsuk Park, Ohsang Kwon, Hee-Ok Kim,
and Jong Woo Kim
Oxide TFT Research Section, ETRI, Daejeon 161, Korea
E-mail : hwang-cs@etri.re.kr

Recently, oxide TFTs have been received great attention for the application to high quality TFT-LCD and large area OLED panel. It is well known that the electrical and optical properties of oxide semiconductors is changed significantly by thermal annealing process[1]. Moreover, environment of the oxide semiconductors during thermal annealing process affects the change of electrical properties[2]. In general, oxide semiconductor layer is covered by passivation layer in the device structure of TFTs. The typical passivation layers used for oxide TFTs are PECVD SiOx or SiNx layer. Another candidate for the passivation layer is ALD AlOx layer, which is well known as excellent encapsulation layer. The evolution of electrical properties of oxide semiconductor layer and oxide TFTs was investigated during thermal annealing processes under various passivation layers. The experimental results and the possible origin will be discussed.

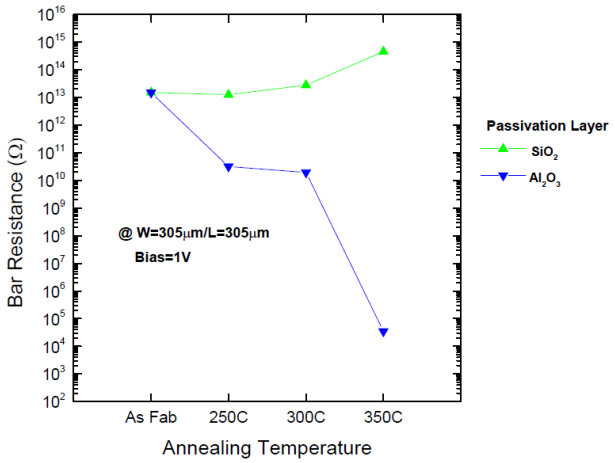


Fig 1. The change of resistance of IGZO layer during successive thermal annealing

[1] Toshio Kamiya, Kenji Nomura, and Hideo Hosono, Phys. Status Solidi A, **206**, 860 (2009)
[2] Jae Kyeong Jeong, et. al.,SID'08 proceeding, 1 (2008).

Double-layered vertically integrated amorphous-$In_2Ga_2ZnO_7$ thin-film transistor

Sang Ho Rha[1#], Un Ki Kim[2#], Jisim Jung[2], Eun Suk Hwang[2], Jung-Hae Choi[3], and Cheol Seong Hwang[2*]

[1]*Department of Nano Science and Technology, Graduate School of Convergence Science and Technology, Seoul National University, 864-1 Yiui-Dong, Yeongtong-Gu, Suwon, Kyonggi-Do 443-270, Korea*

[2]*WCU Hybrid Materials Program, Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea*

[3]*Electronic Materials Research Center, Korea Institute of Science and Technology, Seoul 136-791, Korea*

E-mail : kimmaly1@snu.ac.kr

In this study, two serially connected and vertically integrated a-IGZO TFTs were fabricated using a gate-first fabrication process with two types of gate insulators (PECVD SiO_2 and thermally-grown SiO_2). The t- and b-TFTs show well-behaved transfer characteristics, with an I_{on}/I_{off} ratio (~ 10^8) and an SS value of 0.6 V/dec., which are much improved device parameters compared with the previously reported single-layer V-TFT, for which the gate-last fabrication process was adopted. This is due to the favorable distribution of the electric field by the V_d and V_g of the TFTs, where the influence of V_d on the channel can be minimized compared with that from V_g. The two serially connected TFTs behave well and rather independently of each other, suggesting the possibility of adopting the present structure in vertically integrated memories using a-IGZO channels. The effects of possible interactions of the two serially connected TFTs on their transfer characteristics are also well understood from the positive charge trapping within the PECVD SiO_2 gate dielectric or its interface with a-IGZO layer during the voltage sweep into the highly negative gate voltage region, while the trapped charges detrapped during the subsequent voltage sweep into the positive gate voltage region. This could be understood only from such serially connected V-TFT structure, which provided a better understanding on the underlying physics of a-IGZO based TFTs. Thermally-grown SiO_2 did not induce such deleterious charge trapping behavior revealing the importance of high-quality of gate insulator even for the IGZO-TFTs.

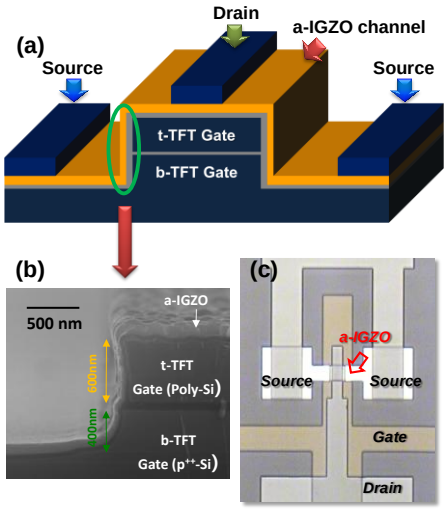


Figure 12. Schematic diagrams showing the fabrication process; (a) schematic diagram and (b) cross-section SEM image of the completed T-V-TFT. (c) Top-view optical microscope image showing the layout of test circuit.

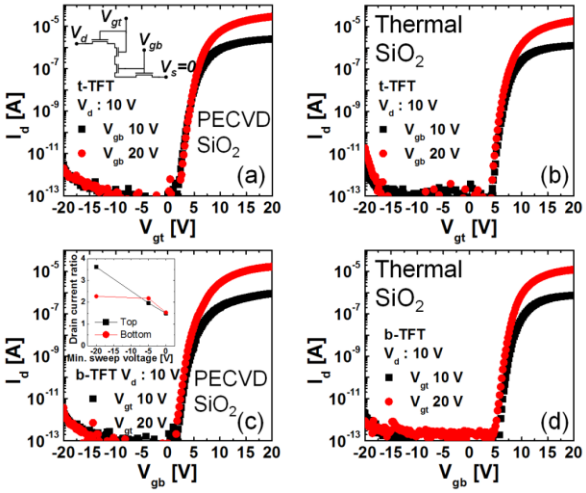


Figure 13. (a) shows I_d – V_g curves of for sample P when V_{gt} varies at the V_{gb} of 10 V or 20 V for V_d of 10 V, and (c) shows I_d – V_g curves of for sample P when V_{gb} varies at the V_{gt} of 10 V or 20 V for V_d of 10 V. (b) and (d) show the corresponding curves for sample T.

Nonvolatile memory operations of In-Ga-Zn-O TFTs using conductivity-modified ZnO charge-trap layers prepared by atomic-layer deposition

Jun-Yong Bak[1], Min-Ki Ryu[2], Sang-Hee Ko Park[2], Chi-Sun Hwang[2] and Sung-Min Yoon[1,*]

[1]*Dep. of Advanced Materials Engineering for Information and Electronics, Kyung Hee University.*

[2]*Oxide TFT Research Team, Electronics and Telecommunications Research Institute (ETRI)*

E-mail: sungmin@khu.ac.kr

Charge-trap-based nonvolatile memories (CTMs) have been researched owing to their higher chip density, CMOS process compatibility, and multi-bit operations in the field of Si electronics. In recent days, oxide-semiconductor-based CTMs have also attracted much attentions from their transparency in a visible range, low-temperature process compatibility, and 3-dimensional integration capability [1]. From these viewpoints, the oxide CTM device can be a promising candidate for the next-generation highly-functional transparent and flexible memory applications. However, according to the previous works, there remain some technical issues such as long program speed, high operation voltage, and short retention time, which can be enhanced by optimizing the gate-stack of memory transistor design including the employed materials and their thickness values. Especially, the electric properties of charge-trap (CT) layers are very important to guarantee the efficiency of charge trapping/detrapping, and hence the conductivity control of oxide CT layer from insulating to conducting is expected to have great influence on the memory behaviors. In this work, we proposed the oxide CTM thin-film transistors (TFTs) using atomic-layer deposited (ALD) ZnO CT layers for improving the nonvolatile memory characteristics and investigated the effects of electric conductivities of employed ZnO CT layers.

The top-gate bottom-contact CTM TFTs were fabricated on the glass substrate, as shown in Fig. 1(a). A 150-nm ITO was patterned into source/drain regions. An In-Ga-Zn-O (IGZO, 20 nm) film was prepared as an active channel layer. Then, 5-nm Al_2O_3 tunneling layer and 50-nm ZnO CT layer were successively deposited by ALD. Here, the electric conductivity of ZnO was effectively modulated by controlling the deposition temperatures to 100, 150, and 200 ^oC. After the one-step patterning of triple layers, the 100-nm Al_2O_3 was formed by ALD as a blocking layer. The gate electrode was formed by the thermal evaporation of Al. Finally, the fabricated devices were annealed at 200 ^oC in a vacuum for 2 h. Fig. 1(b) shows the transfer characteristics of the fabricated IGZO CTM TFTs using ZnO CT layer prepared at 100 ^oC, in which the width of memory window and memory on/off ratio were obtained to be 17.1 V and 8-orders-of-magnitude, respectively. The memory on/off ratio more than 4-orders-of-magnitude was retained even after the lapse of 10^4 s. It was also confirmed that appropriately controlled carrier concentration of the ZnO CT layer could lead to very stable and reliable memory behaviors including higher program speed, larger number of cyclic operations, and longer retention time. Detailed device properties of IGZO CTM TFTs employing the conductivity-modified ZnO CT layer will be discussed.

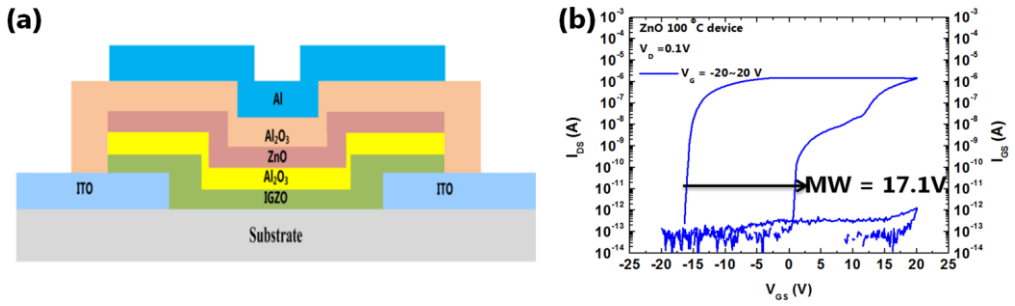


Fig. 1. (a) Schematic cross-sectional view and (b) transfer characteristics of the fabricated CTM TFTs.

[1] H. Yin et al., Appl. Phys. Lett. 93, 172109 (2008).

Extraction of Interface Trap Density at Gate Dielectric and Organic Semiconductor from Photo-conductivity of Organic Thin Film Transistors

Seung-Hyeon Jeong and Chung-Kun Song*
Department of Electronics Engineering, Dong-A University, Busan 604-714, Korea
*E-mail : cksong@dau.ac.kr

최근 유기박막트랜지스터의 성능은 플렉서블 디스플레이와 같은 플렉서블 전자소자에 사용할 수 있을 정도로 향상되었다 [1]. 하지만, 성능에 많은 영향을 미치는 계면트랩에 대한 연구는 많이 미흡하다. 본 논문에서는 온도와 광에 의한 전도도의 변화로부터 게이트 유전체인 PVP 와 유기반도체인 펜타센 계면의 트랩 밀도를 전 에너지 대역에 걸쳐 추출하였다 [2-3]. 또한 산소 환경 또는 산소/수분 환경에 노출 시킨 뒤 계면트랩밀도의 변화를 관찰하였다. 산소에 의한 영향은 이동도의 감소, 문턱전압의 이동, 부문턱전압의 기울기 증가에 영향을 미치고, 수분은 문턱전압의 이동에 영향을 미치는 것으로 나타났으며, 이러한 영향을 주는 계면트랩에 대하여 분석하였다. 본 연구로 인해 유기박막트랜지스터의 주된 열화 원인을 찾았고, 이는 유기물을 이용한 전자소자의 성능 향상에 기여할 것으로 판단된다.

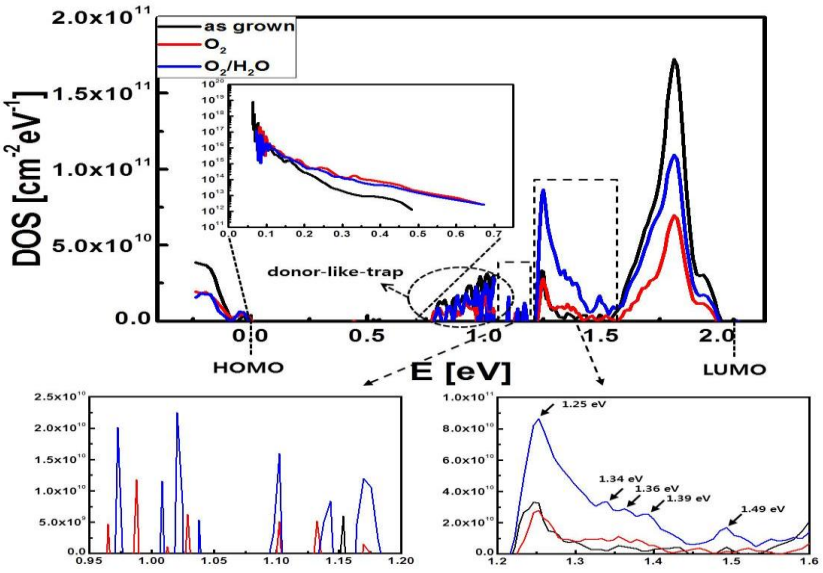


Fig 1. Interface Trap DOS profile at PVP/pentacene interface of OTFTs

[1] G. H. Gelinck, et. al., Nat. Mater. 3, 106 (2004)
[2] W. L. Kalb, K. Mattenberger and B. Batlogg, Phys. Rev. B 78, 035334 (2008)
[3] K. Lee, et.al., Adv. Mater. 22, 3260 (2010)

Fast Recovery Diode Embedded Normally-off AlGaN/GaN MOSHFET

박봉렬, 이정연, 이재길, 한상우, 차호영
홍익대학교
E-mail : hcha@hongik.ac.kr

AlGaN/GaN 기반 스위칭 트랜지스터는 물질 고유의 우수한 특성으로 인하여 차세대 전력반도체로 주목을 받고 있다. [1-2] AlGaN/GaN 스위칭 트랜지스터가 인버터 구동에 사용될 때 각각의 단일 트랜지스터는 스위칭 동작 시 off-state loss 를 줄이기 위하여 트랜지스터 외부의 fast recovery 다이오드 연결이 필수이다. 하지만 외부로 연결된 다이오드는 도선의 길이로 인한 기생 인덕턴스 성분으로 스위칭 손실이 발생할 뿐만 아니라 전체 트랜지스터 면적도 상당히 커지게 된다. 이러한 단점을 극복하고자 본 연구에서는 normally-off 트랜지스터와 fast recovery 다이오드 단일 칩 집적화를 이루었다. 제작된 소자의 특성으로 트랜지스터 문턱전압 2.8 V, 다이오드 턴온 전압 1.2 V, 애노드-드레인 간격 8 μm 에서 최대 항복전압 849 V 를 나타내었다. 또한 게이트 전압 16 V 에서 온저항 2.66 mΩcm^2 의 우수한 특성을 달성하였다.

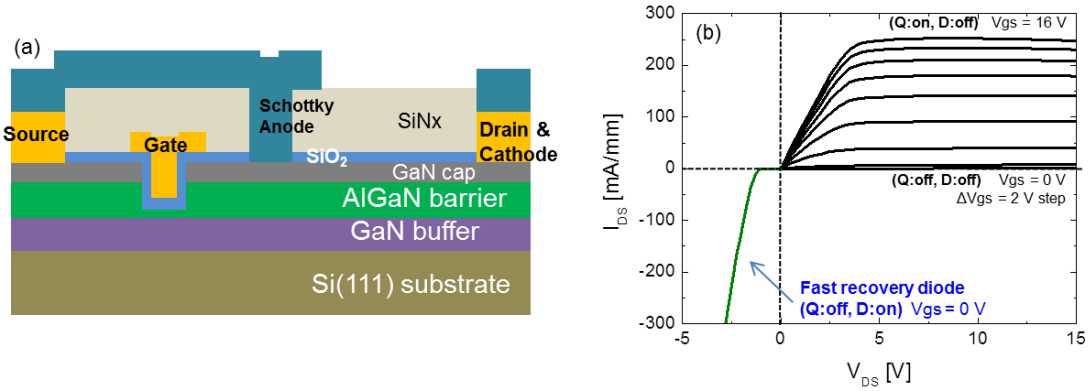


Fig 1. 제작된 소자의 단면도 (a), 전류-전압 특성 (b).

Acknowledgements

This work was supported by National Research Foundation of Korea (NRF) grant (No. 2012042153) and Nano Material Technology Development Program (No. 2012035274) through the NRF funded by the Ministry of Education, Science and Technology.

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[3] Ambacher O *et al* 1999 *J. Appl. Phys.* **85** 3222- 33

Home appliance 용 전력소자의 스위칭 항복 전압 향상을 위한 p-GaN gate HFET 의 gate 특성 연구

송미선, 김웅선, 신종훈, 장태훈
LG 전자 System IC 연구소 IGBT part
E-mail : th.jang@lge.com

AlGaN/GaN HFET(Hetero-structure field-effect transistor)는 AlGaN/GaN 사이에 형성된 이차원 전자가스(two-dimensional electron gas, 2DEG)에 의해 높은 항복전압과 낮은 on 저항을 가지는 차세대 고출력 스위칭 소자이다[1]. 하지만 normally-off 특성 구현을 위해 제작된 p-GaN gate HFET[2]의 경우 스위칭 동작 시 항복 전압이 낮아진다는 단점이 있다. 이 경우, 전력부하가 포함된 스위칭 회로를 구성하여 소자를 보호하거나 소자 자체의 gate 누설전류를 감소시켜 개선이 가능하다.

본 논문에서는 normally-off p-GaN gate HFET 의 gate 누설전류 감소를 통해 스위칭 동작 시 항복 전압 특성을 개선하였다. 먼저 시뮬레이션을 통해 p-GaN gate 위에 고안된 layer 가 삽입된 소자의 gate 누설전류 특성을 확인하였고, 그 후 6 인치 GaN 전력 소자 공정을 사용하여 소자를 제작하고 전기적 특성을 평가하였다. 개선된 p-GaN gate HFET 의 경우 문턱전압(threshold voltage, V_{th}) 및 drain 전류 특성은 기존의 소자 특성과 동일하게 유지되면서 gate 의 누설전류만 낮아지는 특성을 보였고, gate 누설전류가 100 배 이상 감소한 경우 스위칭 동작 시 항복 전압은 2 배 이상 증가하였다. 이를 통해 가전용 고신뢰성 p-GaN gate HFET 를 구현할 수 있을 것으로 예상된다.

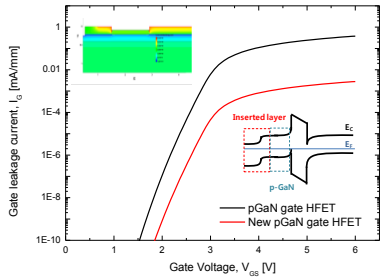

그림 5 p-GaN gate HFET 시뮬레이션 및 밴드구조

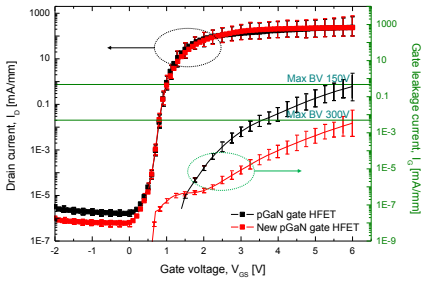

그림 6 p-GaN gate HFET 의 I_D-V_{GS} 특성

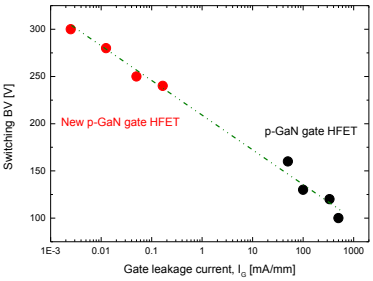

그림 7 gate 누설전류에 따른 스위칭 항복전압 특성

[1] S. Keller, Y-F. Wu, G. Parish, et al., IEEE Trans. Electron Devices 48 (3) (2001) 552-559.
[2] Y. S. Eum, W. S. Kim, J. H. Park, E. J. Hwang, K.C. Kim and T. Jang, SSDM F-9-3 (2012)

Home appliance용 AlGaN/GaN HFET의 Au-free 공정 적용에 대한 연구

조영제, 고화영, 박진홍, 이호중, 장태훈*
IGBT part, System IC R&D, LG Electronics, Korea
E-mail : th.jang@lge.com

AlGaN/GaN HFET(Hetero-structure field-effect transistor)는 높은 항복전압과 낮은 Ron 을 가지는 차세대 고출력 스위칭 소자로 각광을 받고 있다[1,2]. 일반적으로 AlGaN/GaN HFET 의 오믹 금속 물질은 Ti/Al 기반에 Ni/Au, Mo/Au 또는 Pd/Au 등 Au가 포함된 구조로 구성되는데 Au가 포함될 경우 고온의 열처리를 통해 낮은 ρ_c 특성을 나타내어 소자에서 높은 전류 밀도를 얻을 수 있다는 장점이 있다[3]. 하지만, Au 금속 사용의 경우 고가격 및 cross-contamination 으로 인한 기존 CMOS(Complementary metal-oxide semiconductor) 공정 라인으로 호환 불가 등의 문제가 있어 개선이 필요하다.

본 논문에서는 AlGaN/GaN HFET 소자의 전극에 Au-free 공정을 적용하여 기존의 Au가 포함된 오믹 구조와 동등한 수준의 전류 밀도를 확인하였다. 먼저 Au-free 공정의 문제점인 높은 ρ_c 을 해결하기 위하여 ohmic 접합 영역의 식각 깊이, 금속의 종류 및 두께에 대한 평가를 진행하였고, 그 후 기존방식 및 Au-free 공정을 적용하여 소자를 제작하였다. 제작된 소자는 Au 의 유무와 상관없이 +0.9V 의 문턱전압과 600V 이상의 항복전압 특성을 나타내었으며, ρ_c 값은 Au가 포함된 구조와 동등한 수준을 나타내었다. 이를 통해 home appliance 용 AlGaN/GaN HFET 제조에 있어서 가격 경쟁력 및 라인 호환성이 우수한 Au-free 공정을 확보하였다.

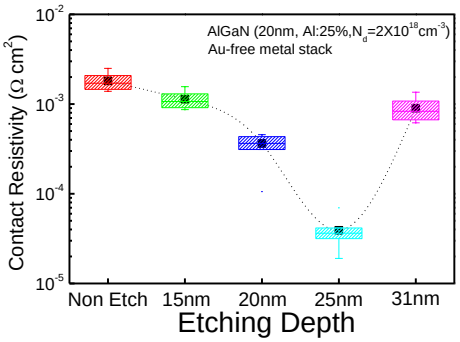

그림 1. Recess 식각 깊이에 따른 ρ_c 특성

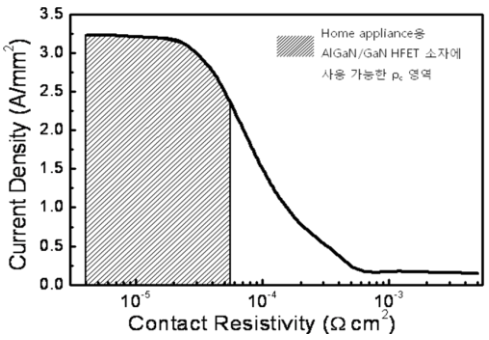

그림 2. 10A 급 HFET 소자를 위한 커런트밀도와 ρ_c 특성

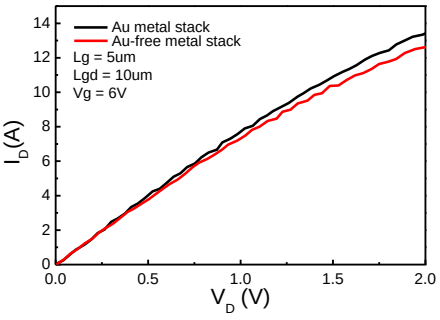

그림 3. Au 유무에 따른 I_D-V_D 특성

[1] U. K. Mishra, P. Parikh, and Y. –F. Wu, Proc. IEEE **90**, 1022(2002).
[2] Y. S. Eum, W. S. Kim, J. H. Park, E. J. Hwang, K.C. Kim and T. Jang, SSDM F-9-3 (2012).
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Role of Thin Al_2O_3 Dielectric Layer in AlGaN/GaN-based MISHFET as Gate Insulator and Surface Protection Layer during RTP

V. Sindhuri, Do-Kywn Kim, Dong-Seok Kim, Chul-Ho Won, Jun-Hyeok Lee and Jung-Hee Lee

School of Electronics Engineering, Kyungpook National University, Deagu, 702-701, Korea.

E-mail : jlee@ee.knu.ac.kr

To improve device performances of an AlGaN/GaN HFET, such as transconductance and cut-off frequency, a thin AlGaN barrier is required [1]. This is because a thinner barrier layer suppresses the short channel effect for the device. However, the thin AlGaN barrier can be easily damaged after rapid thermal process (RTP) which results in increased sheet resistance of the 2 DEG channel and hence increased access resistance of the device. Therefore, the surface protection of the thin AlGaN/GaN HFET is necessary to prevent the degradation of sheet resistance. In this work, we have employed a thin Al_2O_3 dielectric layer for the fabrication of the AlGaN/GaN MISHFET, with varying the thickness of the dielectric layer from 5 to10 nm (sample B (5 nm), C (8 nm), and D (10 nm)). The Al_2O_3 layer serves as the gate insulator of the device as well as the surface protection layer during RTP, which is important in the point of device fabrication because it does not require additional deposition step for the gate dielectric and thus it effectively simplifies the fabrication process. For comparison, sample A was also fabricated without Al_2O_3 layer. Two-step RTP was initially carried out at low temperature of 500 ℃ (20 sec) and then at higher temperature of 800 ℃ (30 sec). Figure 1 shows the degradation in sheet resistance according to Al_2O_3 thickness, where the sheet resistance is rapidly increased to1643 Ω/□ when no protection layer (sample A) is applied. On the other hand, the sheet resistances of the devices with the protection layer (sample B, C, and D) remain almost unchanged from the original sheet resistance of the 2 DEG channel (~ 400 Ω/□), regardless of the thickness of the protection layer, since the surface protection effectively prevents the surface damage after RTP and neutralizes the acceptor-like state on the AlGaN surface [2].

Figure 2 shows the static transfer characteristics, which clearly exhibits the device performance is strongly dependent on the thickness of the Al_2O_3 layer. The lowest subthreshold swing (SS) of 80 mV/dec, close to the ideal value (60 mV/dec) of Si-based device, was obtained from sample C due to lower gate leakage current. Also, sample C shows much higher I_{on}/I_{off} ratio (over 9 orders) compared to other devices. Above results demonstrates that the optimized thickness for the Al_2O_3 layer is approximately 8 nm. Very low I_{on}/I_{off} ratio for sample D with 10 nm-thick Al_2O_3 layer is because the phase of the layer changed from amorphous to poly-crystalline state after annealing [3] which rapidly increases the gate leakage current.

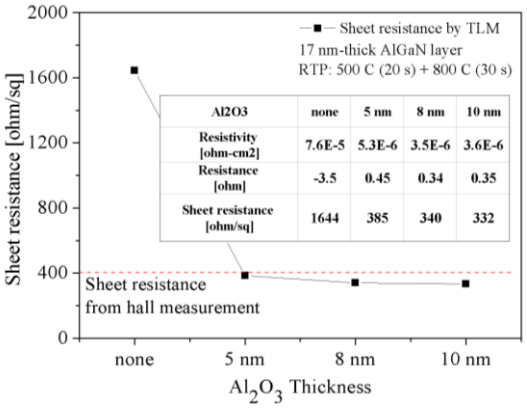

Fig.1. Sheet resistance according to Al_2O_3 thickness

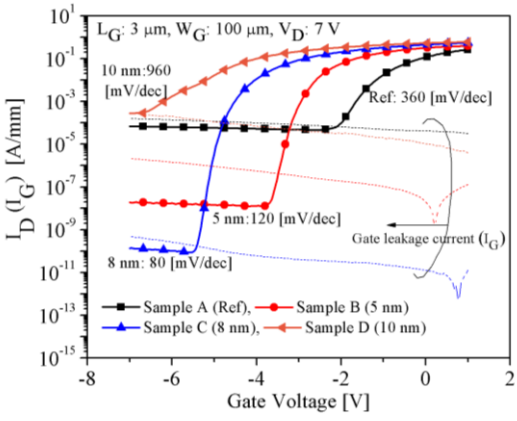

Fig.2. Drain current and gate leakage current with varying Al_2O_3 thickness

[1] P. Waltereit et al. Journal of Applied Physics 112, 053718 (2012).

[2] B. Jogai et al. Journal of Applied Physics, 93, 1631 (2003).

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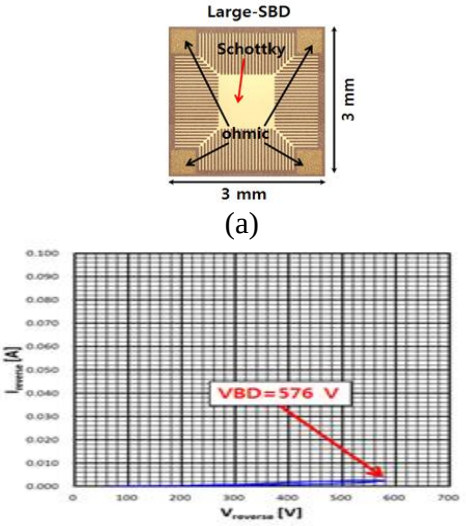
Large GaN-SBD with a symmetric electrode structure using an ohmic recess process and Si ohmic metal

W.Y. Jang[1,2], H.G. Jang[1,5], J.H. Na[1], S.C. Ko[1], Y.R. Park[1], J.J. Kim[1,3], W.J. Jang[1], S.B. Bae[1], C.H. Jun[1], S.H. Moon[1], D.K. Kim[2], J.K. Mun[1], H.M. Park[4], and E.S. Nam[1]

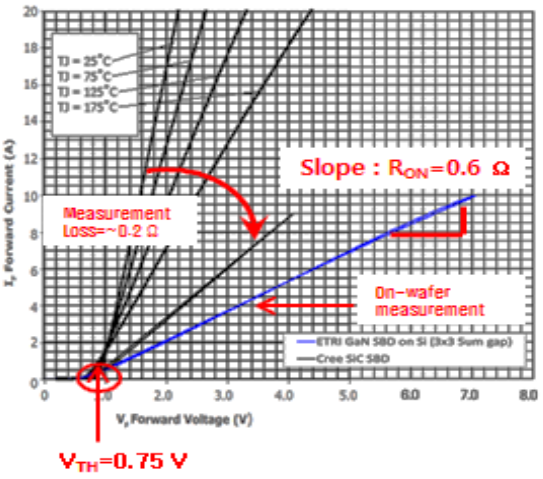
[1]*ETRI*, [2]*Sejong Univ.*, [3]*Chunbuk N. Univ.*, [4]*Dongguk Univ.*, [5]*Univ. of Sci. &Tech.*

E-mail : janghg@etri.re.kr

In this paper, we present electrical charateristics of Schottky Barrier Diode (SBD) based on AlGaN/GaN-on-silicon wafer. The recess process was proceeded to reduce ohmic contact resistance. Si/Ti/Al/Mo/Au was used as an ohmic contact metal. In metal-AlGaN junction structure, Si was used as a n^+-dopant to increase the workfunction of AlGaN/GaN. And Ni/Au was used as a schottky contact metal. Figure 1 (a) shows the large GaN-SBD based on AlGaN/GaN-on-Si with size of $3\times3mm^2$. Figure 1 (b) shows breakdown voltage of the fabricated large GaN-SBD. The reverse breakdown voltage was 576 V. Figure 1 (c) shows I-V characteristics for SiC-SBD (CREE) and fabricated GaN-SBD. The on-resistance was about 0.6 Ω and the turn-on voltage was 0.75 V for fabricated GaN-SBD. The forward current was 3 A at 2 V (SiC-SBD, CREE), 2A at 2V (fabricated GaN-SBD), respectively. In Figure 1(c), we confirmed the probe station has probe contact resistance of 0.2 Ω. We expect that the forward electrical characteristics of the fabricated GaN-SBD will be improved after TO-220 package process. Namely, the on-resistance of the packaged GaN-SBD will be 0.4 Ω, down from 0.6 Ω of the unpackaged GaN-SBD.



(a) (b)



(c)

Fig 1. (a) Photo of the fabricated GaN-SBD, (b) Reverse breakdown voltage and (c) Comparison of forward characteristics with fabricated GaN-SBD and SiC-SBD(CREE)

SiGeSn ternary system for next-generation electronic and photonic devices

Seongjae Cho[1], Byung-Gook Park[2,*], and James S. Harris, Jr.[3]
[1]*Department of Electronic Engineering, Gachon University, Gyeonggi-do 461-701, Republic of Korea*
[2]*Inter-university Semiconductor Research Center (ISRC) with Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-744, Republic of Korea*
[3]*Department of Electrical Engineering, Stanford University, CA 94305-4075, USA*
[*]E-mail: bgpark@snu.ac.kr

Implementing Si-compatible photonic devices is a key to the monolithic integration of electronic and photonic circuits and an enabling technology for group-IV optical interconnects. Although there have been successful demonstrations of Ge photonic devices [1–3], the range of wavelength is largely constrained by the direct-bandgap energy of Ge, which can be slightly extended by application of the tensile strain induced by Sn in the Ge matrix [4]. As the result, the Γ-valley energy bandgap of GeSn is varied from 0.81 eV (pure Ge) down to 0.08 eV (α-Sn: bulk grey tin) [5]. Further, incorporating Si will relax the strain and the SiGeSn ternary system separates the bandgap energy modulation effect from strain-induced lattice mismatch, which realizes the Si-compatible photonic devices with direct energy bandgap. Moreover, the theoretically predicted electron mobility of SiGeSn exceeds that of Ge at 300 K (~3,900 $cm^2/V \cdot s$), by which SiGeSn would be at the same time a superb channel material for high-speed transistors. In this talk, an introduction will be made on the underlying physics on bandgap engineering to obtain direct bandgap and lattice match with Si and recent achievements in active and passive devices making use of group-IV alloys toward the convergence of electronics and photonics as a solution for Si technology extension.

Acknowledgments This work was supported by the Center for Integrated Smart Sensors funded by the Korean Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186) and in part by Advanced Photonic Integrated Circuits (APIC) Corp.

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Optimization of integration process for stabilized graphene MOSFET

김윤지, 이영곤, 강창구, 정욱진, 이상철, 이상경, 이병훈

School of Materials Science and Engineering, Gwangju Institute of Science and Technology, Oryong-dong 1, Buk-gu, Gwangju, Korea, E-mail : bhl@gist.ac.kr

CVD graphene 의 경우 매우 높은 defect density 때문에 전사 과정 중 발생하는 오염, 기판의 영향 등 환경의 영향을 많이 받게 되어, 안정적으로 동작하는 graphene MOSFET 을 구현하는 것이 매우 어려운 상황이다[1]. 이를 개선하기 위하여 그림 1 에 보인 것과 같이 graphene MOSFET 의 집적공정을 최적화 하였고, 각 공정 단계별로 공정의 최적화가 소자 특성에 미치는 영향을 전기적으로 분석하였다. 그 결과로 Dirac voltage 의 이동을 0V 근처로 최소화할 수 있었고, hysteresis 도 대폭 감소하는 결과를 얻었다. Field-effect mobility 또한 증가되어, CVD graphene 에서도 4000cm^2/Vs 이상의 mobility 를 달성할 수 있었다(그림 2). 순차적인 소자 특성 개선과정을 pulsed I-V, discharging current analysis 등 graphene 소자를 위해 새로 개발된 측정 방법들을 이용하여 깊이 있게 분석함으로써, 특성 열화 mechanism 을 상세하게 규명할 수 있었다[2].

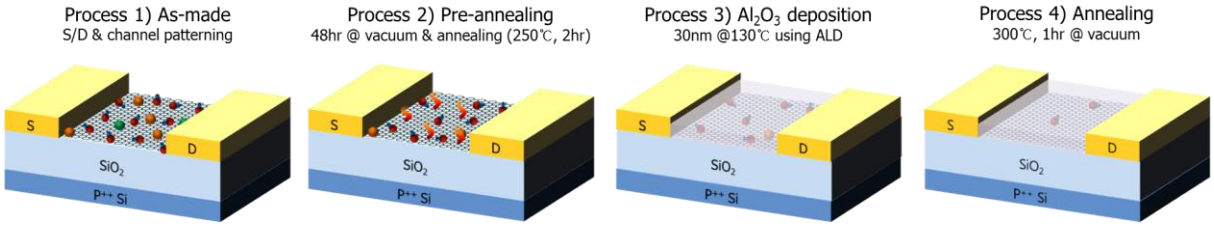

Fig 2. 직접공정 순서와 공정의 최적화에 따른 graphene 표면 변화

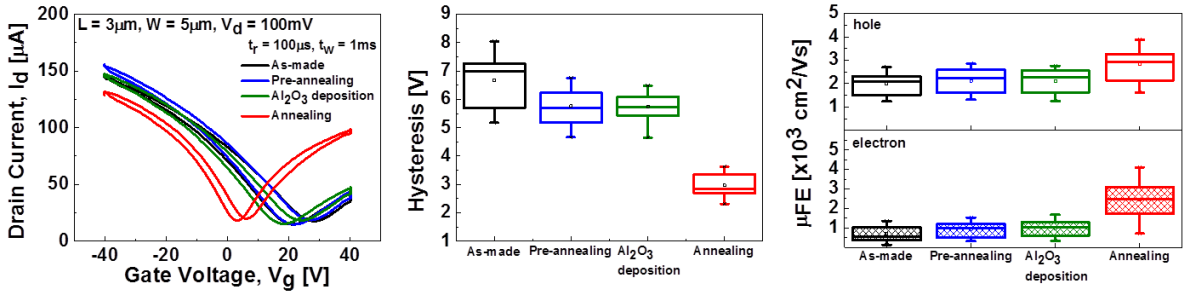

Fig 3. 최적화에 따른 전기적 특성 변화 (a) pulsed I_d-V_g , (b) hysteresis, (c) field effect mobility

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Integrate-and-Fire Neuron Circuit and Synaptic device with Floating body MOSFETs

Min-Woo Kwon, Hyungjin Kim, Jungjin Park, and Byung-Gook Park*
ISRC and Department of Electrical and Computer Engineering, Seoul National University,
E-mail : kmw1224@naver.com

Recently, interest in biological system has increased and many researchers attempt to emulate neural networks that are characterized by parallel processing and low power consumption. We propose I&F neuron circuit and synaptic device with the floating body MOSFETs. The synaptic devices consist of a floating body MOSFET. The synaptic learning is performed by hole accumulation [1]. When the input voltage is applied to the gate and drain, the holes are accumulated in the floating body by impact ionization. Then, threshold voltage is decreased and current drivability is increased. I&F neuron circuit consists of a floating body MOSFET and CMOS circuit. Integration is performed by the hole accumulation in the floating body. The inverters make the circuit fire, which means the circuit generates output pulse. The circuit is initialized by the feedback [2]. In the Fig 2, the output voltage of the synapse is increased by every input pulse, which means synaptic learning. Each synapse output pulses are integrated in the floating body MOSFET and then the neuron fires. After the synaptic learning, the frequency of the neuron firing is increased. We can emulate characteristics of the neuron and synapse, reducing power consumption and neuron circuit cell size by removing the capacitor for integration.

Acknowledgement

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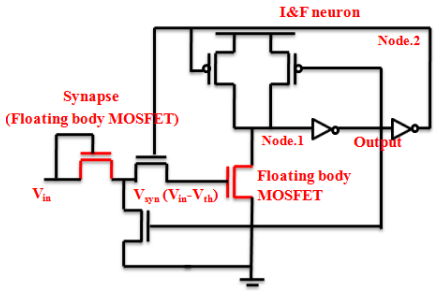

Fig 1. I&F neuron and synapse circuit diagram

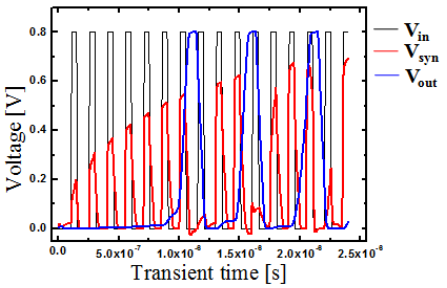

Fig 2. Circuit simulation result

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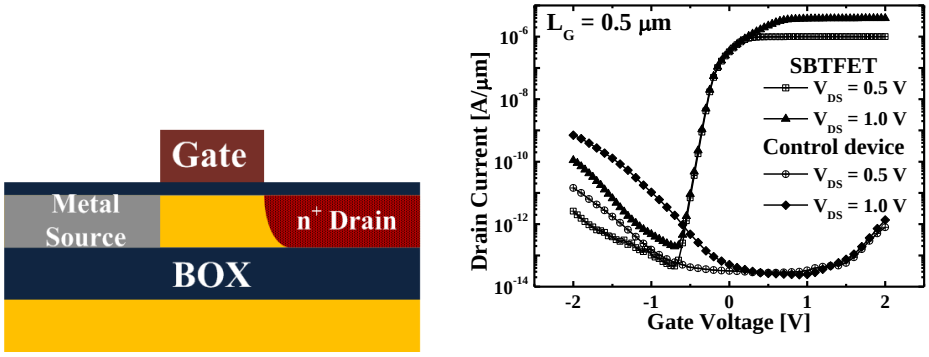
Schottky Barrier Tunneling Field-Effect Transistor using Spacer Technique

Hyun Woo Kim, Jong Pil Kim, Sang Wan Kim, Min-Chul Sun, Garam Kim, Jang Hyun Kim, Euyhwan Park, and Byung-Gook Park
Department of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-744, Republic of Korea
E-mail : hyunoo1218@snu.ac.kr

As Complementary MOS (CMOS) devices are scaled down to 20 nm technology node, the power dissipation in integrated circuits has been increased. In order to overcome power consumption issue, tunneling field-effect transistor (TFET) has been studied as a candidate for low operating power device [1]. However, TFETs have some disadvantages, small on-current by large tunneling resistance and ambipolar behaviors by tunneling between the channel region and the drain region. In addition, since TFET has an asymmetric source/drain region, it is difficult to fabricate short-channel TFET due to misalignment problem.

In this study, a TFET using Schottky barrier (SBTFET) is introduced to improve current drivability as shown in Fig. 1. This structure has a metal source region unlike the conventional TFET with a doping source region. Thus it is expected that large on-current is induced by smaller tunneling resistance. Moreover we firstly fabricated short-channel TFET with self-aligned source/drain region by using spacer technique [2].



(a) (b)

Fig 1. (a) Cross-sectional view of the SBTFET and (b) transfer characteristisc

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"This work was supported by the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186)."

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A Novel Characterization Technique for Location of Laterally Distributed Grain Boundary in Polycrystalline Silicon Thin-Film Transistors

Jaeyeop Ahn, Hagyoul Bae, Hyunjun Choi, Jun Seok Hwang, Jungmin Lee, Sung-Jin Choi, Dae Hwan Kim and Dong Myong Kim

School of Electrical Engineering, Kookmin University, 861-1 Jeongneung-dong, Seongbuk-gu, Seoul 136-702, Korea

E-mail : dmkim@kookmin.ac.kr

Polycrystalline silicon thin-film transistors (Poly-Si TFTs) with a large grain size has attracted since electron mobility increases with the grain size. There have been a lot of research and development activities to enlarge the grain size [1]. Recently, due to the strong dependence of transistor characteristics, characterization of the grain-boundary location in the channel of poly-Si TFTs is known to be very important [2]. As a convenient novel technique, we employed the gate-to-drain and gate-to-source capacitance-voltage characteristics for the poly-Si FFTs to obtain the grain boundary location. When the channel is more conductive by the gate bias, the effective channel length is increased and the change of the capacitance is modulated by the trapped charges at the grain boundary. This causes irregular decrease or increase in the measured C-V characteristics. Therefore, the grain boundary location can be detected by the correlation between the effective channel length and the grain boundary location. This result will be helpful in the development of robust large grain Poly-Si TFTs and in the characterization of device reliability.

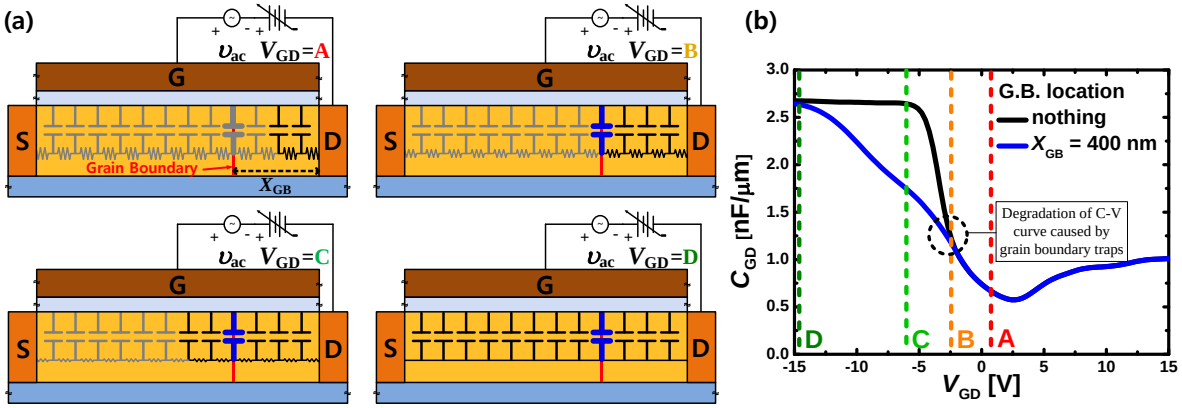

Fig 1. (a) A cross sectional view with gate-to-drain capacitance-voltage simulation setup and equivalent circuit model (b) C_{GD}-V_{GD} characteristic in p-channel Poly-Si TFT

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The Effect of Passivation on the Positive Bias Stress-Induced Instability of Polymer Thin-Film Transistors

Jaewook Lee, Jaeman Jang, Hyeongjung Kim, Chunhyung Jo, Sungwoo Jun, Kyung Min Lee, Dong Jae Shin, Juntae Jang, Sungju Choi, Sung-Jin Choi, Dong Myong Kim and Dae Hwan Kim[a)]

School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea

[a)]E-mail : drlife@kookmin.ac.kr

Organic electronic technology has been extensively developed to be used in the various applications [1]. However, issues on the enviromental effect and long term reliability of polymer thin-film transistors (PTFTs) remained not fully elucidated yet. In particular, the proper use of the passivation process is indispensible in the solution-based process of PTFTs because PTFTs are known to be vulnerable to water molecules and ions.

In this work, we report the effect of passivation on the positive bias stress (PBS)-induced instability of PTFTs by comparing electrical characteristics of two cases with and without passivation. The instability mechanisms of PTFTs are also investigated under the PBS. Consistent with the investigation for the passivation layer on the effective reduction of the ion migration from the back channel [2], it was observed that the passivated devices showed more stable characteristics than the non-passivated devices as shown in Fig. (b). It was attributed to the reduced trapping of polar molecules and ions into the gate insulator. In particular, the non-passivated device shows more stable characteristic with applying the bias stress in a vacuum rather than in atmosphere. This means that the most probable origin of the PBS instability is an ion migration followed by the charge trapping into the gate dielectric as shown Fig. (c). Theses results imply that the passivation against the exposure to air is very important for the stability-booster in the development of PTFTs as main building blocks of the printed electronics.

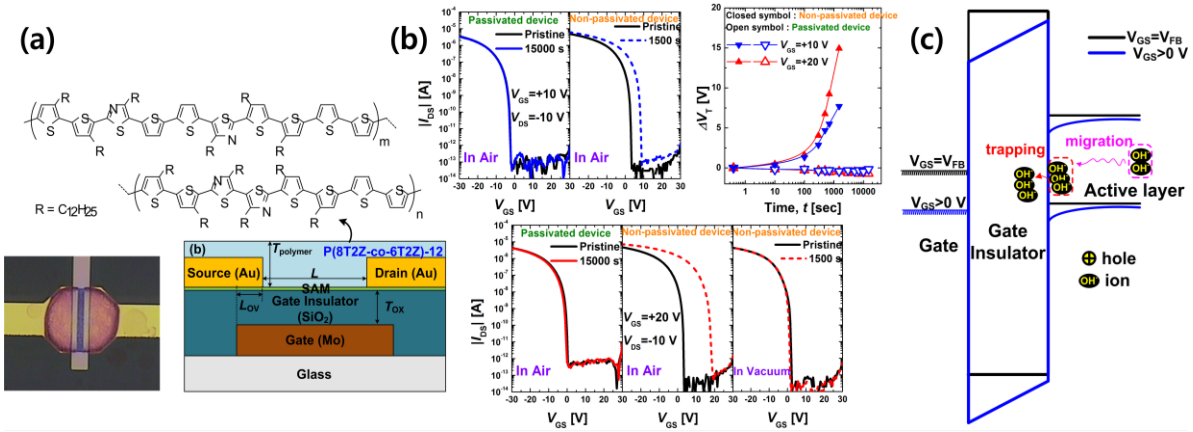

Fig. (a) Cross-sectional schematic of the fabricated PTFT and its chemical structure. (b) Measured t_{PBS} evolutions of I_{DS}-V_{GS} curve in log scale and PBS-induced ΔV_T. (c) Energy band diagram at PBS (non-passivated device).

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Capacitance-Voltage Technique for Extraction of Intrinsic Subgap DOS in AOS TFTs with Bias-Dependent Channel Conduction Factor Model

Hyunjun Choi, Hagyoul Bae, Jaeyeop Ahn, Jun Seok Hwang, Jungmin Lee, Sung-Jin Choi,
Dae Hwan Kim, and Dong Myong Kim
School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : dmkim@kookmin.ac.kr

For consistent characterization and modeling of amorphous oxide semiconductor TFTs, extraction of the subgap density-of-states (DOS) over the bandgap (E_V<E<E_C) is very important for electrical properties and long-term instability [1]. When extracting the subgap DOS per unit volume through the capacitance-voltage (C-V) measurement, it is necessary to normalize the result by the effective volume considering the metallurgical channel length (L_m), the width (W), and the active layer thickness (T_{IGZO}) regardless of the gate voltage [2]. However, the minimum total capacitance under V_G(<<V_{OFF} (V_{OFF} as the cut-off voltage)) strongly depends on the configuration and the active region is partially conductive or fully depleted by the gate bias. On the other hand, the maximum total capacitance is independent of the configurations for the C-V measurement. Therefore, the normalization should be performed by the V_G-dependent effective volume (υ_{eff}) considering the conductivity of the active region. Consequently, these approaches improves the accuracy of the extracted subgap DOS and robust characterization and modeling of TFTs.

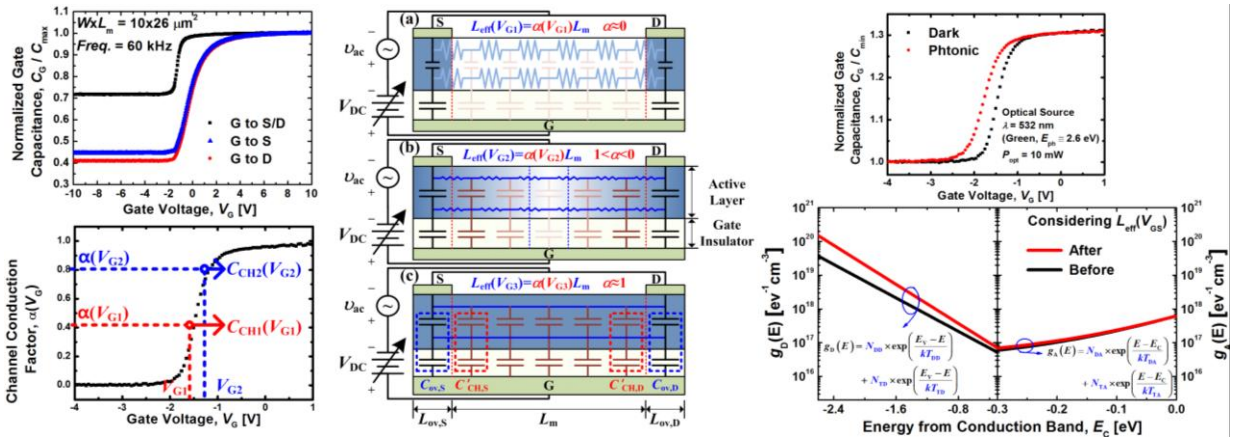

Fig 1. C-V characteristics, proposed model, distributed model and its electrical data

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Prediction Technique and Mechanism for PCB Pattern Crack in NAND Package of SSD

JungHoon Kim, JinYoung Choi, JaeWoo Jeong, Jin-Hyuk Lee, JongYun Yun, JoonHee Lee
Solution Development Team, Samsung Electronics, Hwaseong-si 445-701, Korea
E-mail : jh56.kim@samsung.com

This study is about the development of a prediction technique and mechanism analysis for the present invention of defect occurrence relates to the pcb pattern crack in NAND package of SSD. SSD products developed 8 array pcb(both sides) from 3 array pcb(single side) for the purpose of cost reduction through the evaluation of thermal cycle reliability at first-time mass production. It is possible to make a significant contribution to management in cost savings of SSD set through the development of new products that reduce pcb size. The general failure types of Thermal Cycle(TC) reliability was Solder Joint Crack(SJC) of the package and board side, this product also passed both 3 array and 8 array in TC prior reliability and qualify evaluation of development stage. However, the failure of 8 array products occurs in TC at the first-time mass production. If the upper side of SJ is strong and package substrate is weak, the possibility of pcb pattern crack in NAND package increase than SJC failure. The fatigue life of the defective products using NAND package applied the 3 layer pcb reduced than that of 2 layer pcb in bending load test[1]. Also, the prediction method of the pcb pattern crack in NAND package developed. The strength of pcb core applied the 3 layer pcb is 70MPa, the strength of pcb core applied the 2 layer pcb is 210MPa in bend test. The principal stress of pcb core applied the 3 layer pcb is 134MPa, the principal stress of pcb core applied the 2 layer pcb is 121MPa with a prediction technique. Therefore, fatigue life of 8 array product applied 3 layer pcb reduced that of 2 layer pcb. TC reliability passed qualify criteria by applying package pcb 2 layer which is the improvement scheme of 8 array product[2]. The set level reliability verification and methods obtained with strengthen the prior reliability evaluation and design phase. The strengthening scheme of the prior reliability and failure mechanism of pcb pattern crack currently developed, and contributed business profit and production with high reliability of product.

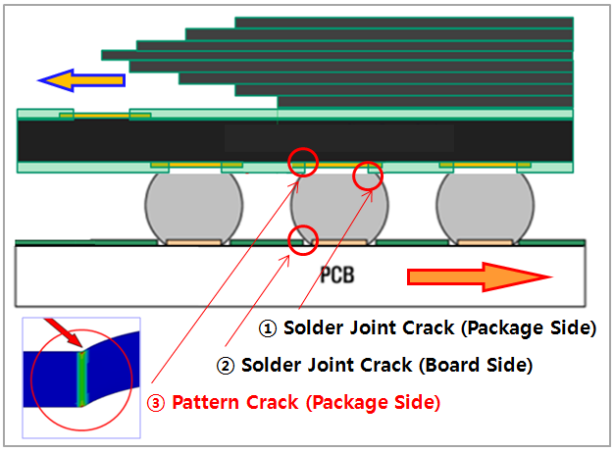

Fig 1. Test and simulation of package pcb pattern crack.

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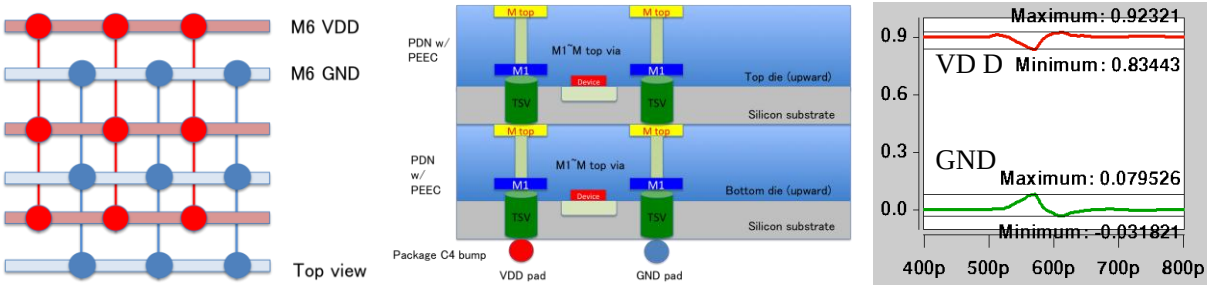
Analysis of Power Integrity of Multi-layer 3D IC with PEEC-based PDN

Seungwon Kim, Ki Jin Han, and Youngmin Kim
School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, Korea
E-mail: youngmin@unist.ac.kr

Recently, 3D IC stacking technology has been proposed and considered as a promising solution for more than Moore era. 3D IC effectively reduces propagation delay by shortening wirelengths with vertical interconnections (e.g., TSVs). However, TSV related power integrity issues still require accurate understanding in the multi-layers stacking [1]. In this study, we investigate the power delivery network of the 3D IC stacking structures. The on chip metal PDN is extracted with PEEC-based equivalent models [2] and frequency-dependent TSV parameters including C4 bumps are generated by EM modeling method [3]. We combine the on-chip PDN and TSV in multi-layer 3D IC for power integrity analysis of static and dynamic voltage drop. We vary the number of stacking layers to identify the impact of the multi-layer on the power integrity. The nominal C4 bumps structure is shown in Fig. 1 (a). And TSV-based 3D IC stacking methodology is shown in Fig. 1(b). The multiple dies are stacked in a way of face to back bonding. The results of the IR drop related voltage fluctuation of on-chip PDN with single layer TSV are shown in Fig 1(c). As can be seen from the figure, there are up to 10% and 11% voltage droop from power supply source (C4) to the final current sink (M1) and GND bump, respectively.



(a) (b) (c)

Fig 1. (a) The nominal VDD/GND structure. (b) Conventional face-2-back bonding. (c) Transient analysis results of the VDD droop and GND bump.

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Gyroscopes Using Surface Acoustic Waves for High Shock Tolerance

Sang Sik Yang
Department of Electrical and Computer Engineering, Ajou University, Suwon 443-749, Korea
E-mail : ssyang@ajou.ac.kr

This paper presents a surface acoustic wave(SAW)-based gyroscope having high sensitivity and high shock tolerance. There has been a great demand for smaller and inexpensive gyroscopes like MEMS gyroscopes. MEMS gyroscopes are categorized into several groups according to their working principle such as Coriolis gyroscope, levitated rotor gyroscope, and Sagnac gyroscope [1]. In comparison with MEMS gyroscopes, SAW gyroscopes have some attractive advantages. They have inherent tolerance to high shock and vibration owing to the absence of the suspended structure in MEMS gyroscope. The fabrication process is so simple, which only involves lithography and metallization. In addition, they spend low power to operate and can be mass produced using conventional CMOS process [2].

The proposed SAW gyroscope is based on Coriolis force inducing interference effect between SAWs. Vibration masses on the SAW delay line enhance the Coriolis force which is given by $F_{Coriolis} = 2m(v \times \Omega)$, where m is the mass, v is velocity, and Ω is the rotation rate. Using the theoretical backgrounds, we have developed SAW gyroscopes with three different structures [3-5]. Type 1, Type 2, and Type 3 are based on standing wave, progressive wave, and a one-port reflective delay line, respectively. We designed parameters for each type using coupling of modes (COM) method prior to fabrication. All the three-type SAW gyroscopes with an 80MHz operation frequency are characterized on a rate table. We obtained the maximum sensitivity of 172 Hz/ (deg/s) at the angular rate change of 0~500deg/s in the case of the type 1 device with Au/Cr vibration mass. Moreover, the vibration test proves that the SAW gyroscopes have excellent robustness up to 15,000g [3]. Type 3 having one port reflective delay line can be used for wireless measurement [5]. Consequently, a set of performance evaluations verified the feasibilities of the proposed SAW gyroscopes with three different structures.

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Graphene oxide coupled sandwiched immunoassays based on surface plasmon resonance biosensing

Yeonsoo Ryu, Seyoung Moon, Youngjin Oh, Yonghwi Kim, Taewoong Lee, and Donghyun Kim
School of Electrical and Electronic Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : kimd@yonsei.ac.kr

Surface plasmon resonance (SPR) biosensing has drawn tremendous interests due to the label-free nature and real-time capability. However, a SPR biosensor suffers from moderate detection sensitivity. Recently, graphene and graphene oxide (GO) have been considered to improve the detection characteristics of SPR biosensors because of the unique electronic and optical properties [1,2]. Here, we investigate SPR detection characteristics of GO-coupled structure (inset of Figure 1) for an antigen-antibody interaction between human and antihuman immunoglobulin in a sandwiched assay. We have attempted to take advantage of functional groups of GO, which was prepared in Langmuir-Blodgett method on gold and dielectric surface. Theoretical and experimental data suggest that a thicker dielectric spacer reduces resonance shifts for GO-coupled SPR detection (Figure 1). Peak resonance shift obtained with GO-coupled SPR detection was enhanced as 113% compared to conventional thin film-based SPR detection.

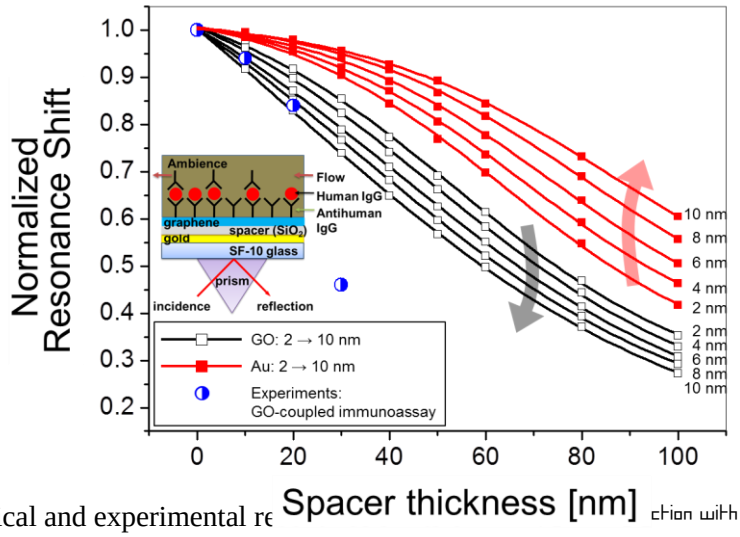

Fig.1. Theoretical and experimental results with respect to the spacer and GO thickness. (inset) Schematics of GO-coupled SPR structure

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Optical and Electrical Characterization of Hydrogen Peroxide Cytotoxicity using Indium Tin Oxide Electrode

Yonghyun Choi[1], Jaeyoung Kim[2], and Sungbo Cho[1,*]
[1]*Department of Biomedical Engineering, Gachon University, Incheon 406-799, Korea*
[2]*Department of Biological Science, Gachon University, Incheon 406-799, Korea*
[*]E-mail : sbcho@gachon.ac.kr

For the optical and electrical characterization of DNA, protein or cells, it is increasingly required to employ transparent electrodes. In this study, the transparent indium tin oxide (ITO) electrode was fabricated and evaluated as a cell-based assay for hydrogen peroxide (H_2O_2) cytotoxicity. H_2O_2 is produced via cell metabolic process and dissociated into water and oxygen by catalase. H_2O_2 induces growth stimulation, temporary growth arrest, or necrotic cell death according to its concentration [1]. The effect of H_2O_2 with different concentration on the growth of 293/GFP cells was monitored by the lock-in amplifier based impedance measurement system [2]. By monitoring the impedance magnitude (|Z|) at 21.5 kHz, it was able to detect the cell detachment from ITO electrode caused by the application of H_2O_2 with a concentration higher than 5 mM and the corresponding decrease in |Z| as shown in Fig. 1. The fabricated ITO electrode-based sensor is suitable for optical and electrical analysis of cells.

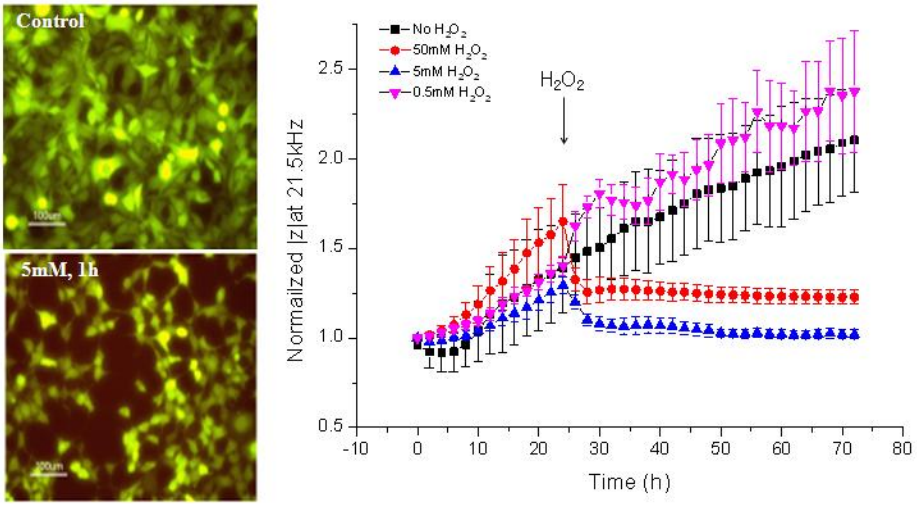


Fig 1. Optical (left) and impedance characterization of GFP cells on ITO after H_2O_2 application

[1] J.R. Stone and S. Yang, Antioxid. Redox Signal. 8, 243 (2006).
[2] H.S. Jun, L.T.M. Dao, J.-C. Pyun and S. Cho, Enzyme Microb. Technol., 53, 302 (2013).

Plasma enhanced chemical vapor deposition of amine layer on polycarbonate

[1]Dong-Ho Han, [3]Jung-Hwan Lee [1]Heon-Yul Ryu, [1]Si-Hyeong Cho, and [1, 2]Jin-Goo Park*

[1]Department of Bionano Technology and [2]Materials Engineering, Hanyang University, Ansan 426-791, Korea

[3]NanoBioSys Inc.

E-mail : jgpark@hanyang.ac.kr

Amine group is one of the common functional group which is widely used in the field of biotechnology and biomedical engineering. Conventional method for the modification of the surface with amine group is the liquid-SAM(Self-Assembled Monolayer). But this method has some limitation for the mass production because it requires various precursors and pre-treatments according to the substrate material. In this research, we deposited the amine group on PC (polycarbonate) substrate by using PE-CVD (plasma-enhanced chemical vapor deposition) method [1]. Ammonia(NH_3) gas was used as a plasma source. RF power, gas flow rate, temperature and gas pressure were controlled to optimize the deposition process. By changing the process conditions, the effect of each variable on the quality of amine layer was probed. Amine group on the PC substrate was confirmed qualitatively by contact angle and FT-IR analysis. Fluorescence analysis with immobilization of streptavidin-FITC was used for quantitative analysis. Fluorescence intensity was increased with temperature and inversely proportional to RF power. As a result, amine modified PC substrate which has high quality amine layer was successfully made by PE-CVD.

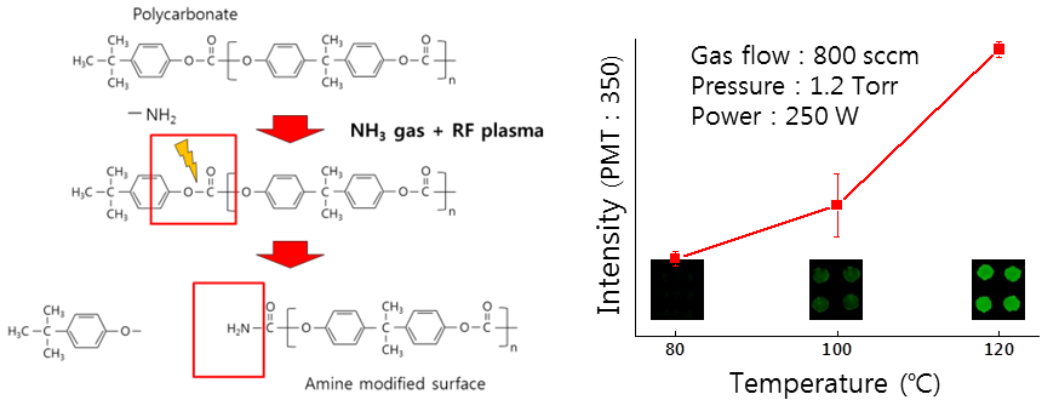


Fig 1. Amine modification mechanism on PC substrate and results of fluorescence analysis

[1] C. Jama, O. Dessaux, p. Goudmand, B. Mutel, L. Gengembre, B. Drevillon, S. Vallon and j. Grimblot, POLYMER, **29** 998 (1988)

Solution-Based Synthesis of Anisotropic Metal Chalcogenide Nanomaterials and the Challenges

Unyong Jeong
Department of Materials Science and Engineering, Yonsei University, Seoul 120-745, Korea
E-mail : ujeong@yonsei.ac.kr

Although it was only recent that anisotropic metal chalcogenide (MC) nanocrystals have been investigated with much interest, remarkable advances have been made in diverse areas of modern technology. This presentation will review recent advances in solution phase synthesis to generate 1-D and 2-D anisotropic MC nanostructures with a focus on using different growth mechanisms to control the shapes of the MCs. I will summarize current understanding of the thermodynamic and kinetic aspects associated with the mechanisms of forming these anisotropic MC nanostructures. I will discuss on the challenges to be investigated thoroughly in the solution-based synthesis of anisotropic nanomaterials, which includes surface energy control, correcting the nucleation & growth mechanism, removal of organic surfactant, kinetic study on the chemical transformation, scale-up of production, and eco-friendly synthesis.

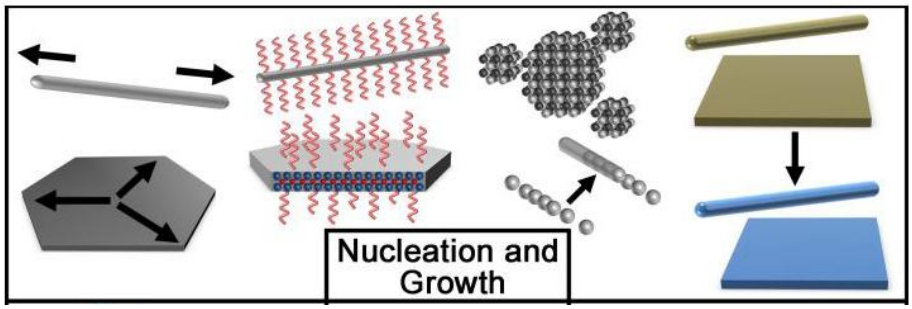
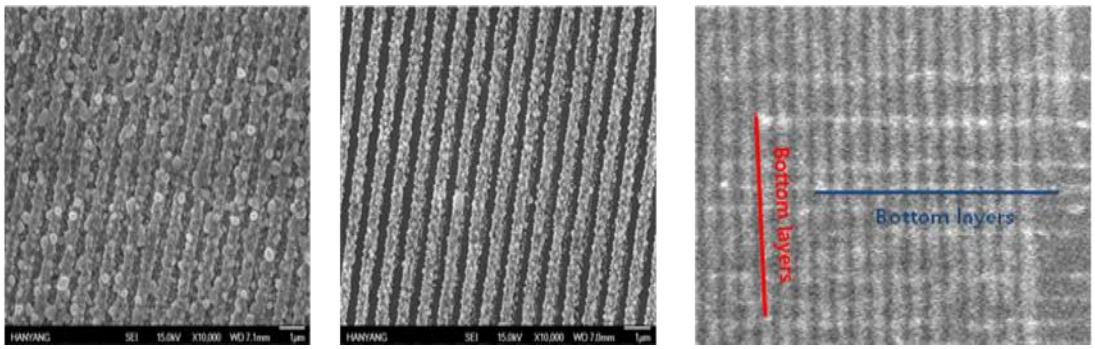


Fig 1. Synthetic strategies to obtain anisotropic metal chalcogenide nanomaterials

Nano-Imprinted Metal Electrode By Solution-Based Ag Nano Particles with Methanol Capillary Force Effect

Youngin Gil, DoHyung Kim, Changhwan Choi*
Division of Materials Science & Engineering, Hanyang University, Seoul 133-791, Korea
*E-mail address: cchoi@hanyang.ac.kr

Nano-imprint lithography (NIL) has continuously drawn huge attention from the point of production due to its potential advantages such as high efficiency, low cost, high-resolution, large-area coverage, and a simple process. For metal line formation using NIL, vacuum process such as evaporation or sputtering was typically adopted. However, it usually requires additional residual metal etching process. To skip this abundant residual metal etching step, we proposed a solution based metal pattern formation with NIL using capillary force effect. In this study, a silver ink (particle diameters of 40-50 nm) containing metal particles prepared by non-vacuum metal deposition process was first implemented, and then a reverse-transferred electrode was formed on the substrate through a nano-imprint process. Complete metal residual removal between NIL based line patterns is a challenging issue not to be interconnected each other. We adopted the capillary phenomena [2] with methanol used as a solvent of ink to remove any residues. First of all, a PUA (Polyurethane acrylate: PUA) was dropped over the silicon mold (master template line width: 800 nm), and then a cured PDMS (Polydimethylsiloxane: PDMS) was put in order to get the replicated mold with an exposure of UV light (365 nm) for 2 hours. Second, silver ink was dropped over the replicated mold. Then, the patterns were filled by nano silver particles with a needle. The following soft baking (80℃, 10 minutes), residual removal by methanol using spin-coating steps and the curing steps were performed. Finally, metal line was formed with the nano-imprint condition under 12 bar of pressure at 100℃. The experimental method aforementioned can be implemented to form the MIM structured metal cross-array elements such as ReRAM. Our study provides one to understand the principle of a solution-based electrode formation utilizing NIL method without unnecessary chemical etching process.



(a) (b) (c)

Fig1. Line patterns with (a) and without (b) residues, and cross-array patterns (c)

[1] Kyung S Park, Jeong M Dang, Myung M Sung and Soon-min Seo Park et al. Nanoscale Research Letters 7:351(2012)

[2] Jae K. Hwang, Sangho Cho, JeongM. Dang, Eun B. Kwak, Keunkyu Song, Jooho Moon and Myung M. Sung, Nature Nanotech. 175 (2010)

This research was supported by the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Science, ICT & Future Planning (2012-0009460).

The relationship between adsorption thickness of polymer layer on ceria and dishing in shallow trench isolation chemical mechanical planarization

Kijung Kim[a], Jihoon Seo[b], Sunho Moon[b], and Ungyu Paik[a,b*]

[a]*Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Korea*

[b]*WCU Department of Energy Engineering, Hanyang University, Seoul 133-791, Korea*

E-mail : upaik@hanyang.ac.kr

Dishing which reduces the final thickness of field oxide in STI structure and degrades the planarity of the wafer's surface has become more important due to the steady shrink of device geometry and channel length [1]. In general, the use of passivation agent has been considered to be one of the promising methodologies to prevent the dishing [2]. Especially, the polymers with high affinity for nitride film used as an auto-stopping layer in STI structure have been employed for preventing the dishing [3]. However, recently the gap-filling material becomes soft to fill extremely deep and narrow trench as aspect ratio has been getting higher. So it is inevitable to develop new approaches to prevent the dishing. Here, we suggest one of the prospective approaches to prevent the dishing. we controlled adsorption thickness of polymer layer on ceria to soften the ceria surface because the soft surface is better for preventing the dishing. To soften the ceria surface, we used poly acrylic acid (PAA) with different molecular weight. PAA with higher molecular weight makes the ceria surface more soft by thicker polymer layer. As a result, we could achieve enhanced dishing rate as the adsorbed polymer layer becomes thicker and obtain similar results with different line width and pattern density.

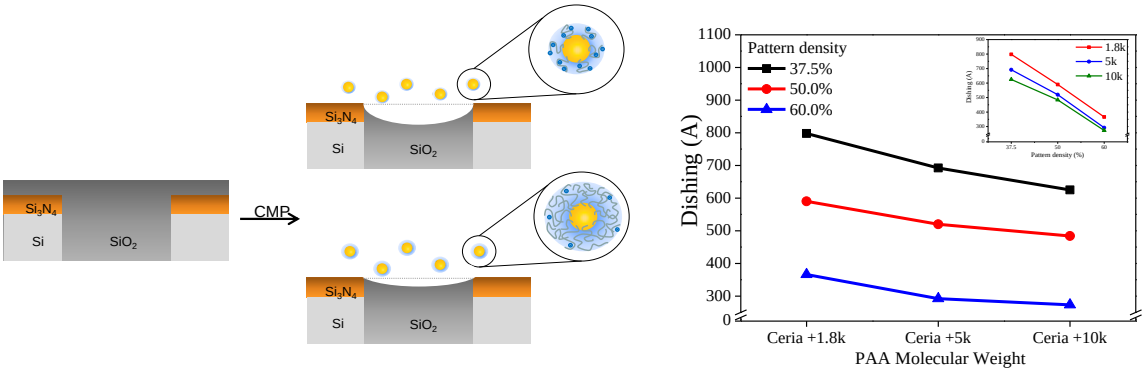


Fig 1. Graphical abstract and its dishing data

[1] S.H. Chang, Microelectronic engineering, 82 (2005) 136-142

[2] J.H. Park, H. Cui, J.Y. Cho, H.S. Hwang, W.J. Hwang, U. Paik, H.G. Kang, N.J. Kwak, J.G. Park, J Electrochem Soc, 157 (2010) H607-H612.

[3] Y.H. Kim, S.M. Lee, K.J. Lee, J.G. Park, U. Paik, J. Mater. Res, 23 (2008) 49-54

Nano-embossing Ceria Abrasive with Polishing Rate Accelerator for Scratch-less Poly-Si Stop CMP Application

Sang-su Yun, Eun-bin Seo, Hao Cui, Jin-Hyung Park, and Jea-Gun Park*

Advanced Semiconductor Materials & Device Development Center,

Hanyang University, Seoul 133-791, Korea

E-mail : Parkjgl@hanyang.ac.kr

As the device design rule shrinked below the 20 nm technology node, Scratches problem has became the most critical issue in polysilicon stop chemical mechanical planarization (CMP) using a conventional dry ceria slurry. To solve the scratche issue, the ceria particle was synthesized by the wet chemical precipitation method to precisely control size, shape and morphology of the particle instead of the conventional solid-state displcement method. In this study, we synthesized the wet ceria particle with various primary sizes from 5 to 65 nm. And, for the primary size of greater than 40nm, we changed the shape of the wet ceria particle from the polydral to the nano-embossing structure. It was observed that the polishing rate was lenearly proportional to the primary size of the ceria particle regardless of the accelerator. In this study, various organic additives were investigated to increase the polishing rate. It was found that only some of organic additives works as the accelerator. Therefore, we report how our nano-embossing ceria abrasive affects the decrease in the scratch generation and the mechanism of accelerator in the wet ceria slurry analyzed with the characteristics of the slurry and the dissociation behavior of the organic additive.

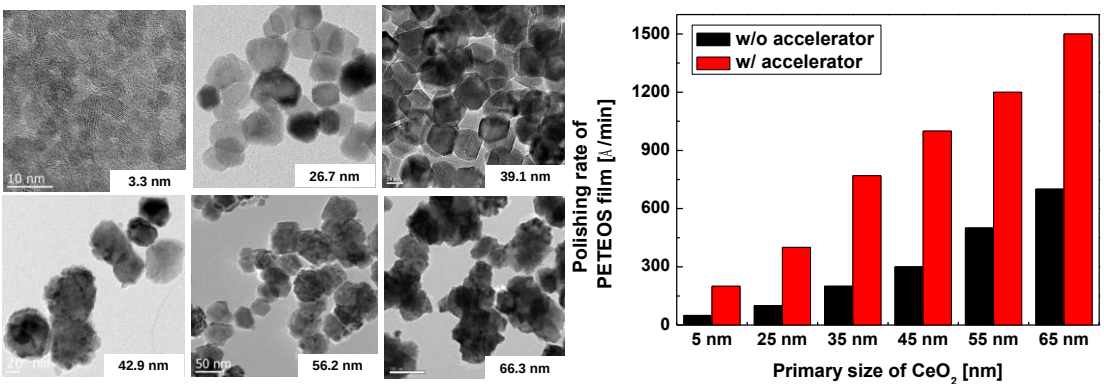


Fig 1. TEM image of CeO_2 particle with various primary sizes and its corresponding polishing rate of PETEOS film without or with rate accelerator.

[1] J. Y. Bae, J. H. Seo, K. W. Park, J. O. Moon, H. B. Park, U. Park, ICPT, #2503, (2012).

Acknowledgement

This investigation was financially supported by UB materials Inc. and the Post Brain Korea 21 Project in 2013. We also thank Sumco Corp. for helping us with the experiments

TSV Bumping 공정을 위한 저온 Nitride & Oxide 필름 개발 및 특성 연구

(Study on the Characteristics of Low Temperature Chemical Vapor Deposited Silicon Nitride and Silicon Oxide Film in Through Silicon Via Bumping Process)

양주헌, 최동진, 정래형, 김진평, 이웅선, 서민석, 변광유
Advanced PKG Development Team, Skhynix
E-mail : juheon.yang@sk.com

TSV 를 이용한 적층 구조의 경우 front & back side bump 형성 후 bump 간의 접합을 통해 chip 간의 전기적 연결을 형성하게 된다. 기존 polymer 계열의 passivation layer 를 적용한 'BD1' backside bump 구조의 경우 기계적 신뢰성 및 Cu 오염에 대한 문제점들을 가지고 있어, 이를 해결하기 위한 신규 'T-shape' backside bump 구조가 제안되었다. 한편, 신규 backside bump 구조 구현을 위해서는 신규 passivation layer 개발이 필요하며, PKG 공정에서 적용하기 위해 저온 공정에서 형성이 가능해야 한다. 또한, backside bump 공정은 wafer thinning 이후 공정을 진행하기 때문에 WSS (Wafer Support System)을 필수적으로 사용해야만 하는데, Si 과 WSS 간의 접합을 위해 사용되는 접착제의 경우 열 공정에 취약한 단점을 가지고 있어 공정 온도가 낮을수록 공정 안정성을 확보할 수 있다. 따라서 본 논문에서는 PKG 공정에서 적용하기 위한 저온 공정에서 형성 가능한 신규 passivation layer 를 개발하여, 'T-shape' backside bump 구조를 완성하여 기존 문제점들을 극복하고, 공정 온도 하향을 통해 WSS 에 적용되는 접착제에 기인한 다양한 불량 개선을 통해 해결하여, TSV 개발 제품에 대한 신뢰성을 확보하였다.

Electrical resistance evolution of Cu electroplated on a Si interposer

Wan-Gyu Lee
Department of Nanodevice, National NanoFab Center, Daejeon 305-806, Korea
E-mail : wangyulee@nnfc.re.kr

3-D integration of stacked chips has continuously attracted a lot of attention due to its capability to extend Moore's law beyond its expected limits [1]. We investigated the changes in electrical and structural properties of electroplated Cu films on a Si-interposer substrate. When Cu films were exposed in an air environment after electroplating on SiO_2/Si-substrate as a Si interposer, the resistance increased slightly until 7 days with a uniform distribution of it, and then increased very rapidly after 19 days with broader resistance distribution than those of the initial 7 days. The increase in electrical resistance of electroplated Cu films can be significantly influenced by the microstructural changes of electroplated Cu film with time, redistribution of impurities in electroplated Cu film, and oxidation behavior of electroplated Cu film in an air environment. These phenomena can be explained by the ionic neutrality due to the oxidation of electroplated Cu on the surface of electroplated Cu film and the microstructural changes with time at room temperature caused by recrystallization of electroplated Cu film. This study will be helpful in understanding the necessity of passivating or encapsulating the electroplated Cu film and will also give guidance to the 3-D integration of stacking many chips on a Si interposer [2].

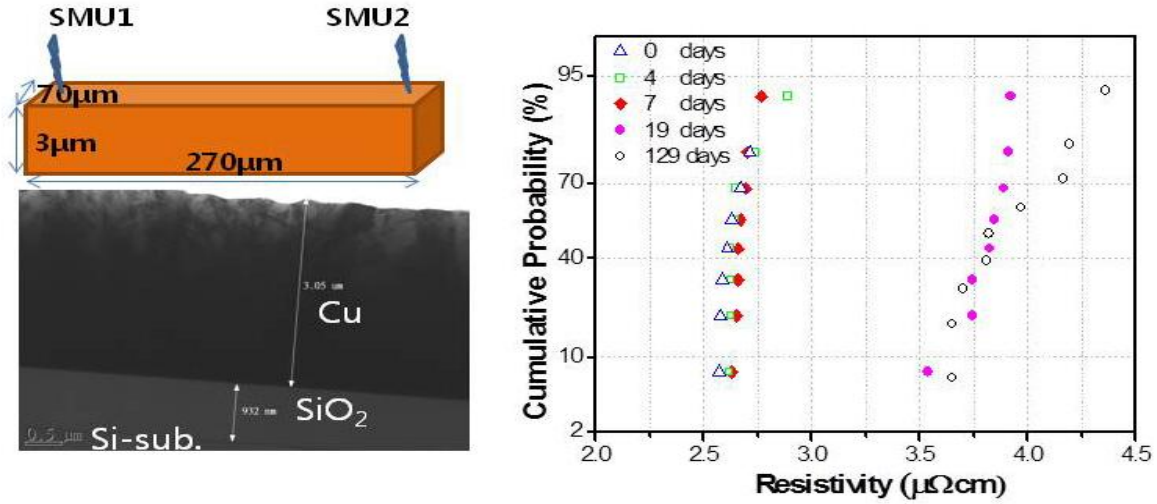


Fig 1. XTEM of patterned Si interposer and its electrical data

[1] IBM Press Release, http://www-03.ibm.com/press/US/on/inde, wss April 2007.
[2] G. Pares et. al., IEEE Electronic Components & Technology Conference 305 (2013).

Through-Silicon-Via(TSV) Filling by Electrochemical Deposition with High Frequency Pulsed-Current

Sanghyun Jin[1], Geon Wang[1], Sungho Seo[2] and Bongyong Yoo[1,2*]
[1]*Department of Materials Engineering, Hanyang University, Republic of Korea*
[2]*Department of Bionanotechnology, Hanyang University, Republic of Korea*
E-mail : byyoo@hanyang.ac.kr

TSV interconnection provides the 3D interconnection between the 2D silicon based integrated-circuits(IC). Especially, electrochemical deposition of Cu was core process in the TSV interconnecting process. However, several issues were discussed such as low throughput caused by slow deposition rate of Cu in the TSV and formation of a void which causes the serious electrical and mechanical problems.

In this study, TSV filling process was investigated by electrochemical deposition with high frequency pulsed current. Figure 1. Shows the cross-sectional images of Cu filled TSV by direct-current(DC) and pulsed-current(PC) with various frequency. In this result, more stable and faster TSV filling was achieved by the PC with fastest frequency(4444 Hz) compared to DC.

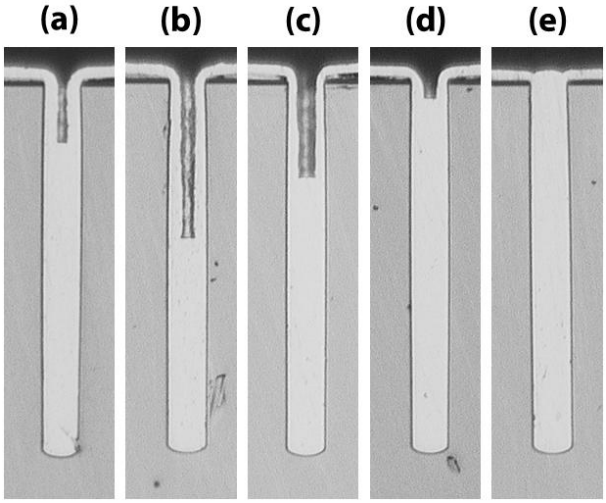


Figure 1. Cross-section images of Cu filled TSV by (a) DC and PC with frequency of (b) 898 Hz, (c) 1481, (d) 2222 Hz and (e) 4444 Hz with same average current density and processing time to 2 mA/cm^2 and 30 minute, respectively.

Effect of design on thermo-mechanical stress in through-silicon via

Joo-Sun Hwang, and Won-Jun Lee
INAME, Faculty of Nanotechnology and Advanced Materials Engineering, Sejong University, Seoul 143-747, Korea
E-mail : wjlee@sejong.ac.kr

Copper is the most popular filling metal in through-silicon via (TSV), owing to its low resistivity and the compatibility with interconnects. Due to the difference between silicon and copper in the coefficient of thermal expansion, thermo-mechanical stress evolves by changes of temperature, resulting in several issues such as cracking of silicon substrate or degradation of device properties. The failure of dielectric liner under bias-temperature stress was also observed, and was explained by the concentrated stress in the oxide liner at the top corner of TSVs [1]. In the present study, we report the effect of the design of TSV structure, such as geometry or dielectric liner, on the thermo-mechanical stress distribution in the TSV structure. A two-dimenesional finite element model with cylindrical coordinates was constructed and analyzed using ANSYS^{TM}. The maximum tensile stresses in silicon was calculated at the bottom corner of TSV, whereas the maximum tensile stress in dielectric liner evolves at the top corner. The tensile stresses in both silicon and dielectric liner increase with increasing via diameter and that the effect of aspect ratio is negligible for a fixed via diameter. Both stresses also increase with decreasing the thickness of dielectric liner.

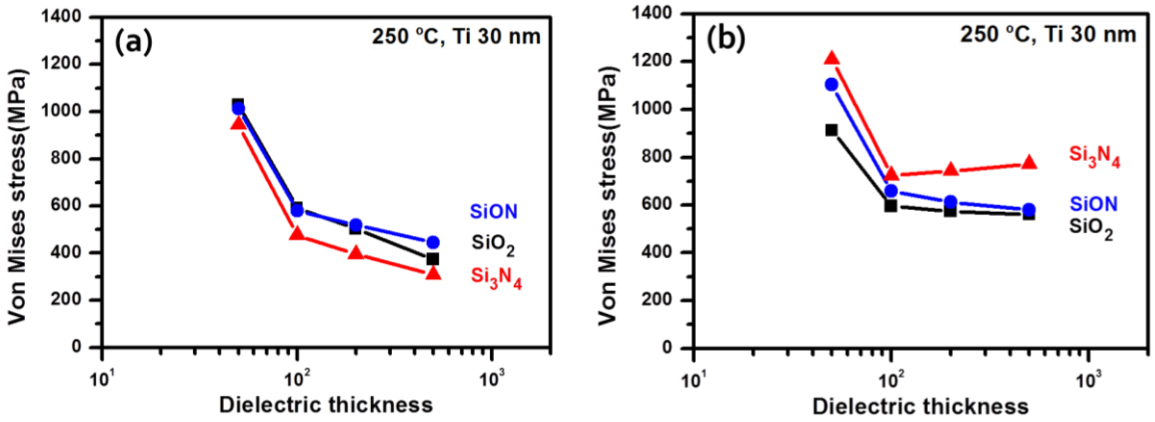


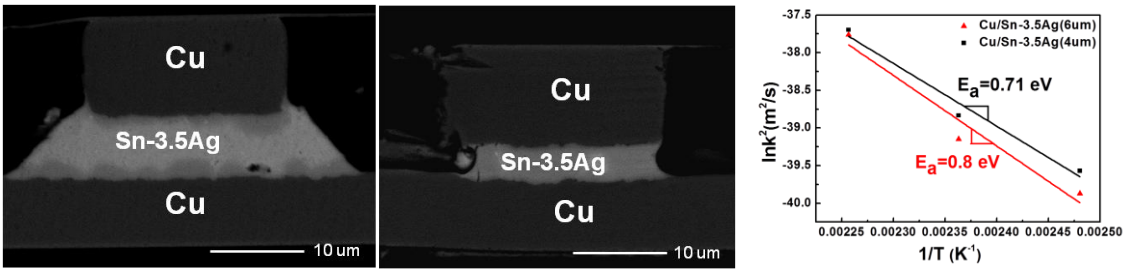
Fig.1. The effects of liner thickness and materials on the maximum tensile stresses in (a) silicon substrate and (b) dielectric liner

[1] S-H Seo, J-S Hwang, J-M Yang, W-J Hwang, J-Y Song, and W-J Lee, Thin Solid Films, 546, 14 (2013).

Solder Thickness Effect on the Interfacial Reaction Characteristics of Cu/Sn-3.5Ag Micro-bump for 3D Integration

Byeong-rok Lee[1], Young-ki Ko[2], Chang-woo Lee[2], and Young-bae Park[1*]
[1]*School of Materials Science and Engineering, Andong National University, Andong, Korea*
[2]*Micro-Joining Center, Korea Institute of Industrial Technology, Incheon, Korea*
E-mail : ybpark@andong.ac.kr

Recently smart phone, tablet and clouding computing environment intensify the needs of high performance and low power semiconductor device. A traditional approach to achieve market requirements is shrinking process, but we need breakthrough of technology to overcome limitation of the traditional approach. We believed that packaging technology with through-silicon-via (TSV) is one of the key.[1] Among all interconnection technologies, especially TSV provides the shortest length and the highest density which lead to significantly reduced signal delay and power consumption. TSV integration is stacked using micro-bumps and through Si via. Micro-bump is one of the key enabling technologies for 3D integration where high I/O count devices and interposers are interconnected with hundreds of thousands of micro-bumps.[2] There are several important issues such as current crowding, joule heating, thermomigration. And excessive intermetallic compound (IMC) growth and Kirkendall void formation in micro-bump can degrade the mechanical reliability of solder joints. Therefore, it is essential to understand the fundamental growth mechanisms of IMC and Kirkendall void. In this study, annealing and solder thickness on the IMC growth kinetics were quantitatively evaluated. We performed kinetic studies on the micro-bump system in order to quantify the amount of IMC by using in-situ annealing test in a scanning electron microscope chamber at 130 ~ 170℃. And also, activation energy values were derived.[3] The activation energies were 0.8 and 0.72eV for the Cu/Sn-3.5Ag(6um) micro-bump and Cu/Sn-3.5Ag(4um) micro-bump, respectively.[3]



(a) (b)

Fig 1. Cu/Sn-3.5Ag(6um) micro-bump and Cu/Sn-3.5Ag(4um) micro-bump; (a) bump structures and (b) the activation energy.[3]

[1] Ha-Young You, Yuchul Hwang, Jung-Woo Pyun, Young-Gyun Ryu, and Hyoung-Sub Kim, Proc. 62th Electronic Components and Technology Conference 2012, 315 (2012).
[2] Hsiao-Yun Chen, Da-Yuan Shih, Cheng-Chang Wei, Chih-Hang Tung, Yi-Li Hsiao, Douglas Cheng-Hua Yu, Yu-Chun Liang and Chih Chen, Proc. 63th Electronic Components and Technology Conference 2013, 49 (2013).
[3] Byeong-Rok Lee, Jong-Myeong Park, Young-Ki Ko, Chang-Woo Lee and Young-Bae Park, J. Microelectron. Packag. Soc., 20(3), 45 (2013).

∗ Acknowledgements: This work was supported by joint research project of Korea research council for industrial science and technology of Korea Ministry of Knowledge Economy.

Applications of nano-hybrid structures for improvement of light extraction efficiency in light emitting didoes

Jinsub Park
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea
Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jinsubpark@hanyang.ac.kr

Until now, to improve the device performance including optical and electrical properties of commercialized GaN-based light-emitting diodes (LEDs), great efforts have been made. Especially, to obtain the improved the internal quantum quantum efficiency and light extraction efficiency (LEE), promising approaches are suggested by using a patterned sapphire substrate (PSS) [1], surface morphology modification [2], nano-pit embedded LED structures [3], and spherical typed nanostructures [4]. Although the suggested methods are effective to improve the LEE, some techniques are required complex process and expensive steps which can be the critical issues to reduce the cost in LEDs to replace with the current solid state lighting source.

In this study, we report on the possible methods to improve the light extraction efficiency in GaN-based LED structures by using the combination various nanohybrid structrues such as ZnO nanostrucutres, polystyrene/SiO_2 core-shell nanospheres, and surface nano-pit formation. The observed experimental reuslts show the enhancement of light extraction efficiency in LED with help of nanohybrid structures. The mechanism of enhancement of photoluminescence and electroluminescence intensity using the various nanohybird structures formed on LED surface can be explained by the improvement in extraction efficiency by both increasing the probability of light escape by reducing Fresnel reflection and by multiple scattering within the applied nanospheres. The theoretical analysis using the finite-difference time-domain (FDTD) simulation correponds to experimental results. Finally the electrical properties and current issues reltated to LEDs will be discussed.

[1] H. Gao, F. Yan, Y. Zhang, J. Li, and Y. Zeng, Solid-State Electron 52, 962 (2009).
[2] H. W. Huang, C.C. Kao, J.T. Chu, and H.C. Kuo, IEEE Photonics Tech Lett. 17, 983 (2005).
[3] K. Koike et al., IEEE Photonics Tech Lett. 17, 983 (2012).
[4] S. Yeon and J. Park, J. Nano Sci. And Tech 13, 7653(2013).

Acetone-Derived Graphene: Synthesis and Seawater Corrosion Application

Jae-Hoon Huh, [a,b] Seung Hyun Kim, [c] Jae Hwan Chu, [a] Sung Youb Kim, [a,b] Ji Hyun Kim, [c,*] and Soon-Yong Kwon*

[a] *School of Mechanical and Advanced Materials Engineering, Ulsan National Institute of Science and Technology, Ulsan 689-798, Korea*

[b] *Opto-Electronics Convergence Group & Low Dimensional Carbon Materials Center, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, South Korea*

[c] *Interdisciplinary School of Green Energy, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, South Korea*

E-mail : kimjh@unist.ac.kr, sykwon@unist.ac.kr

An intense effort is underway to find coatings that inhibit the process of metal corrosion.[1-2] Graphene, consisting of a monolayer of graphite, is of major attraction as a two-dimensional atomic layer with functional application, for example anti-corrosion coating.[3] We show that acetone-derived graphene coating can effectively enhance the corrosion efficiency of copper (Cu) in a seawater environment (0.5-0.6 N (~3.0-3.5 %) sodium chloride). Scheme of Figure 1a illustrates graphene synthesis and seawater corrosion application process for monolayer graphene layers converted from a drop of acetone on Cu. Using a drop of acetone (20 μl/cm^2) on Cu, rapid thermal annealing allows the facile and rapid synthesis of graphene films on Cu surfaces with monolayer coverage of almost close to ~100 %. Experimental studies show that the catalytic Cu surface induces the spontaneous decomposition of acetone molecules into carbon-containing functionalities even at room temperature, facilitating the formation of graphene-coated Cu during short-period, high temperature annealing over 800 ^{o}C. Figure 1b shows the results of Raman spectra of the resulting film on a Cu surface after the RTA process at temperatures in the range between 800 and 1,050 ℃ for 3 min under vacuum. The Raman spectra show three primary features: a D band at ~1,349 cm^{-1}, a G band at ~1,593 cm^{-1}, and a 2D band at ~2,687 cm^{-1}: all of which are expected peak positions of graphene.[4] Electrochemical impedence spectroscopy (EIS, Figure 1c) of graphene-coated Cu follow the trend of large capacitive impedance behaviour, which is capable of protecting against penetration of the attractive active species because graphene coating decreases the probability of dissolved oxygen, water, and chloride ions penetrating onto the Cu surface. The resulting graphene-coated Cu exhibits 37.5 times higher corrosion resistance as compared to that of uncoated Cu. Further, an investigation into the role of graphene coating on Cu suggests that the outstanding corrosion inhibition efficiency (IE) of 97.4 % is obtained by protecting the underlying Cu against the penetration of both dissolved oxygen and chlorine ions thanks to the closely-spaced atomic structure of the graphene sheets. The increase of graphene coating thickness results in

the enhancement of the overall corrosion IE up to ~99 %, which can be attributed to the effective blocking of the ionic diffusion process via grain boundaries. Overall, our results suggest that the acetone-derived graphene film can effectively serve as a corrosion-inhibiting coating in seawater level and that it may have a promising role to play for industrial coating.

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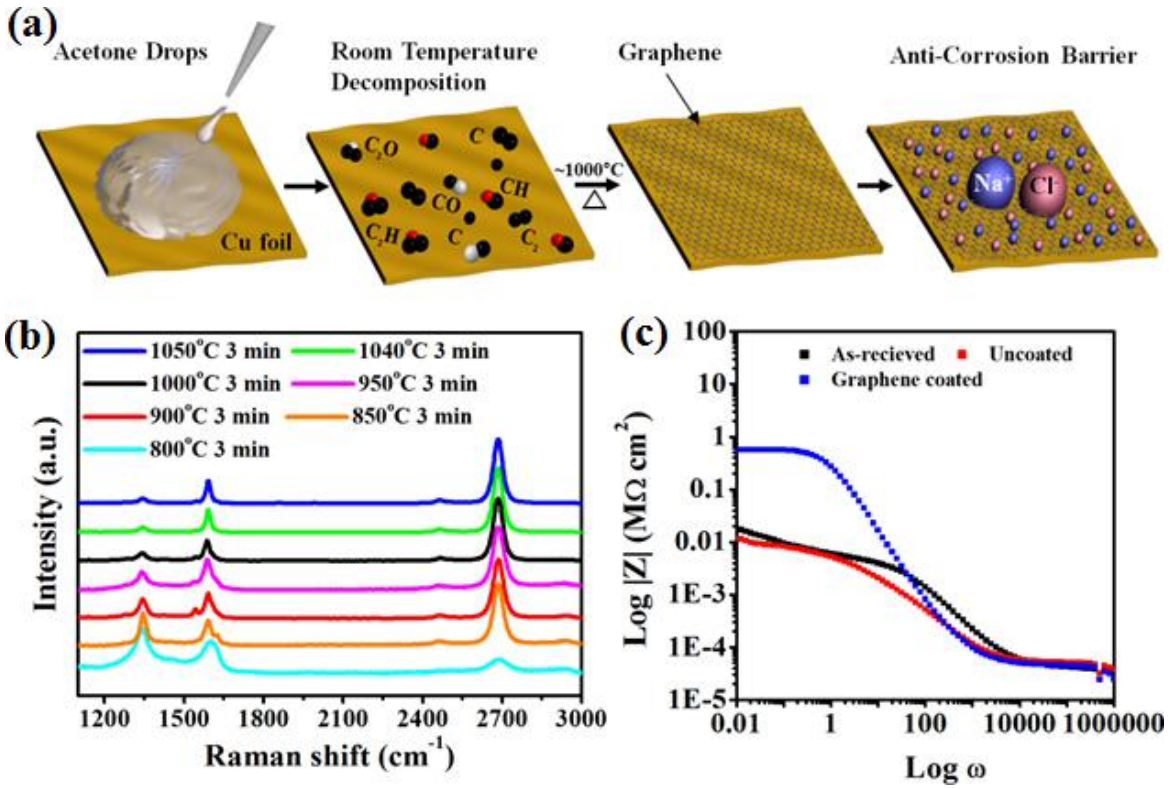

Figure 1. (a) Schematic illustration of graphene growth converted from acetone drops as anti-corrosion barrier, (b) Raman spectra of graphene films with temperature variation measured after transfer to a 300 nm SiO_2/Si surface, (c) EIS Bode plot of as-received, uncoated and graphene coated Cu in 3.5 % NaCl solution.

Fabrication of Ohmic contact using Graphene insertion between AlGaN and Ni/Au in AlGaN/GaN structures.

Yoonhyung Kim, Minjun Kim and Jinsub Park
Department of Electronics Computer Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jinsubpark@hanyang.ac.kr

AlGaN/GaN hetero-structures are very attractive system to be used in high electron mobility transistor(HEMT) and Schottky diode due to high mobility of carriers and high saturation velocity in channel formed by the spontaneous and piezoelectric polarization[1]. In order to obtain the high performance of electronic devices using the AlGaN/GaN, the high quality Ohmic contact is the essential issue [2].

In this study, we reported the formation of Ohmic contact in AlGaN/GaN structures using the graphene insertion between AlGaN and Ni/Au metal stacks. In addition, to improve the Ohmic properties of Au/Ni/graphene formed on AlGaN, the rapid thermal processes were conducted with various temperatures under nitrogen ambient. For the possible mechanism of Ohmic contact formation, we suggested the energy band structure related to the reduction of Schottky barrier height through thermionic emission by insertion of graphene. The combination of metal/graphene can be a promising electrode to improve the electrical characteristics in AlGaN/GaN based optoelectronic devices.

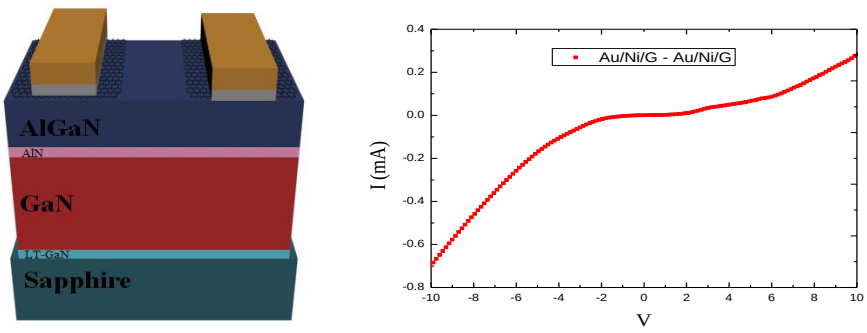

Fig 1. AlGaN/GaN structures and electronic characteristics

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Effects of nickel cobalt oxide nanoparticles on luminous efficiency of light-emitting-diodes.

Do-Hyun Kim , G.Mohan Kumar, Jinsub Park
Department of Electronics Computer Engineering, Hanyang University, Seoul 133-791,Korea
E-mail : jinsubpark@hanyang.ac.kr

In order to use the light-emitting diodes (LEDs) as solid state lighting sources, the improvement of light extraction and internal quantum efficiency is essential factors for high brightness LEDs [1].

In this study, we suggested nickel cobalt oxide nanoparticles (NPs) as a transparent conducting material[2] formed on blue LED epi-structures. Nickel cobalt oxide ($Ni_{1-X}Co_XO$) is representative p-type oxide material consisted of CoO and NiO system. To form the NiCoO hemisphere lens structures on p-GaN layer which is the topmost layer of blue emission LEDs epi-structures. The UV-visible absorption spectrum shows that synthesized NiCoO has 2.0~4.0eV band gap measured at room temperature. After fabrication of NiCoO hemisphere lens array on blue LEDs by using the spin-coating method of colloidal NPs, the electroluminescence (EL) measurements are conducted to investigate of electrical properties including wavelength conversion of emission wavelength from blue through the using the NiCoO layer. From the photoluminescence and EL measurements, we can observe the enhancement of light extraction from the blue LEDs using the NiCoO hemisphere lens array. Finally, the combination of ZnO nanorods on NiCoO hemisphere lens shows the dramatical improvement of light extraction comparing to the LED with NiCoO lense.

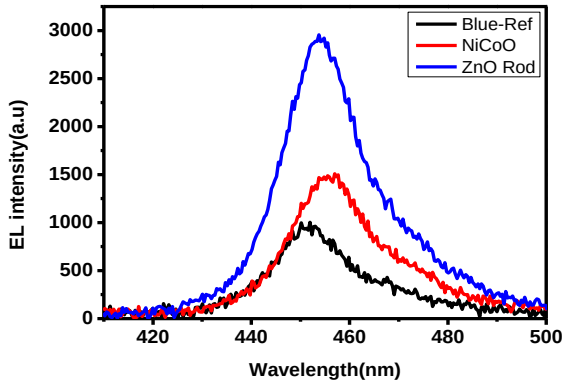

Fig.1 EL spectra obtained the blue LEDs with different surface nanostructures.

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[2] F. Iacomi et al. / Thin Solid Films 520 651–655 (2011)

Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature

Min Hyuk Park, Han Joon Kim, Yu Jin Kim, Woongkyu Lee, Taehwan Moon and Cheol Seong Hwang
WCU Hybrid Materials Program, Department of Material Science & Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea.
E-mail : pmh1983@snu.ac.kr

Recently, it was reported that HfO_2 thin films can be ferroelectric when they are doped with various elements, such as Si, Y, Al, and Zr.[1] The ferroelectricity of HfO_2-based films is believed to result from the formation of non-centrosymmetric $Pbc2_1$ orthorhombic phase (o-phase). However, the systematic study on the phase evolution of ferroelectric doped HfO_2 films are still missing. In this presentation, the effects of annealing temperature (T_{anneal}) and film thickness (t_f) on the crystal structure and ferroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ films are reported. The $Hf_{0.5}Zr_{0.5}O_2$ films consist of grains having tetragonal, orthorhombic, and monoclinic structures. The orthorhombic phase content, which is responsible for the ferroelectricity in this material, is almost independent of T_{anneal}, but decreases with increasing t_f. In contrast, increasing T_{anneal} and t_f monotonically increases (decreases) the amount of monoclinic (tetragonal) phase, which coincides with the variations in the dielectric constant. The remanant polarization was determined by the content of orthorhombic phase as well as the spatial distribution of other phases.

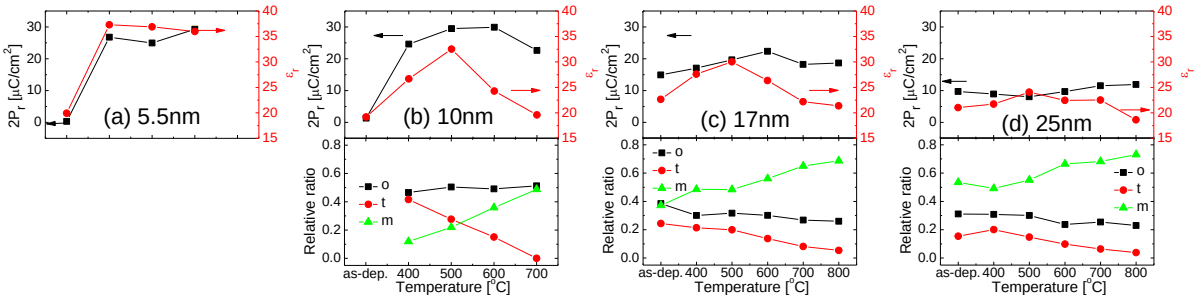


Fig 1. The change of $2P_r$ and ε_r (upper panel) and that of the relative ratio of o-, t-, and m-phases (lower panel) as a function of annealing temperature of (a) 5.5-nm-thick, (b) 10-nm-thick, (c) 17-nm-thick, and (d) 25-nm-thick HZO films.

[1] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon and C. S. Hwang, Appl. Phys. Lett. 102, 242905 (2013).

A New Chemical Route for Vapor Phase Deposition of GeTe for Phase Change Memory

Taehong Gwon[1], Taeyong Eom[1], Sijung Yoo[1], Moo-Sung Kim[2], Iain Buchanan[3], Manchao Xiao[3], and Cheol Seong Hwang[1*]

[1]Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea.

[2]Air Products Korea, 15 Nongseo-dong, Giheung-gu, Yongin-si, Gyeonggi-do 446-920, Korea

[3]Air Products and Chemicals, Inc., 1969 Palomar Oaks Way, Carlsbad, CA 92011, USA

E-mail : cheolsh@snu.ac.kr

Phase change random access memory (PCRAM) appears to be one of the strongest candidates for next-generation high density non-volatile memory. In fabricating PCRAMs with a design rule under 20nm, atomic layer deposition (ALD) of the phase changing chalcogenide materials is necessary. The authors reported ALD of materials with compositions lying on the $GeTe_2$-Sb_2Te_3 pseudo binary tie line using $Ge(OCH_3)_4$, in which Ge is in the +4 oxidation state, and $((CH_3)_3Si)_2Te$ as the Ge-and Te-precursors, respectively [1].

In this report, a new chemical route to deposit GeTe thin film from the vapor phase was examined. $Ge(N((CH_3)_3Si)_2)_2$, in which Ge is in the +2 oxidation state, and $((CH_3)_3Si)_2Te$ were used as novel Ge- and Te-precursors, respectively. GeTe films were deposited using a shower-head type 6-inch-scale ALD reactor at a wafer temperature of 70°C. $Ge(N((CH_3)_3Si)_2)_2$ showed low reactivity toward ALD-type reaction with $((CH_3)_3Si)_2Te$ at such a low temperature, and even passivation effect (no film growth) on substrates and chalcogenide film surfaces. Therefore, to improve the reactivity between Ge- and Te-precursors, methanol vapor was co-injected with the Ge-precursor and Te-precursor to form reactive Ge- and Te-intermediates. The precursor injection sequence consists of methanol injection/Ge-precursor and methanol co-injection/methanol injection/purge/methanol injection/Te-precursor and methanol co-injection/purge pulses without any oxidation/reduction gases. This chemistry-specific ALD process successfully deposit films with various composition including GeTe with good reproducibility, and very low impurity concentration.

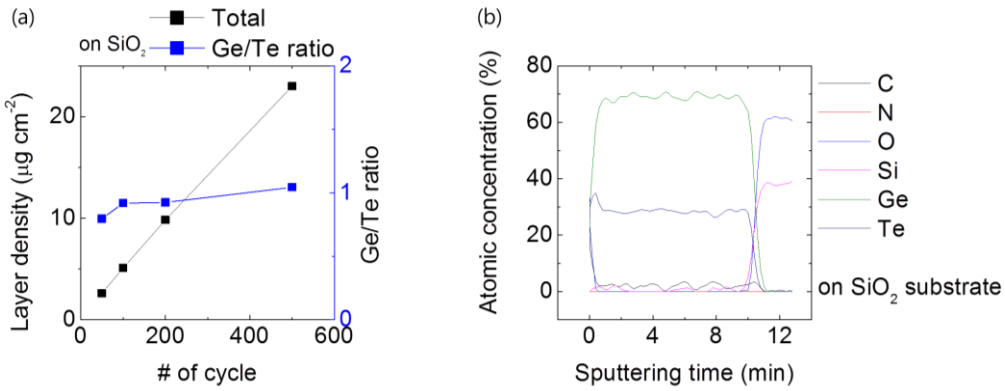


Fig 2. (a) Growth rate and (b) depth profile of GeTe films deposited

[1] Eom, T. et al., *Chem. Mater.*, 24, 2099 (2012)

Kinetic analysis of atomic layer deposition process of $(GeTe_2)_{(1-x)}(Sb_2Te_3)_x$ layers for phase change memories

Taeyong Eom[1], Taehong Gwon[1], Sijung Yoo[1], Moo-Sung Kim[2], Iain Buchanan[3], Manchao Xiao[3], and Cheol Seong Hwang[1*]

[1]*Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea.*

[2]*Air Products Korea, 15 Nongseo-dong, Giheung-gu, Yongin-si, Gyeonggi-do 446-920, Korea*

[3]*Air Products and Chemicals, Inc., 1969 Palomar Oaks Way, Carlsbad, CA 92011, USA*

E-mail : cheolsh@snu.ac.kr

Phase change random access memory (PCRAM) is one of the strongest candidates for next-generation high density non-volatile memory. The fabrication of ultra-high density phase change memory (>> 1 Gb) depends heavily on the thin film growth technique for the phase changing chalcogenide material, most typically Ge-Sb-Te compounds. Atomic layer deposition (ALD) at low temperatures is the most preferred growth method for depositing such complex materials over surfaces possessing extremely narrow holes.

In this study, $[(CH_3)_3Si]_2Te$ and stable $Ge(OCH_3)_4$, $Ge(OC_2H_5)_4$, and $Sb(OC_2H_5)_3$ metal-organic precursors were used to deposit various layers with compositions lying on the $GeTe_2$–Sb_2Te_3 tie line at substrate temperatures ranging from 50 to 150 ℃ using a thermal ALD process. The ALD specific saturation behavior of Ge precursor during the purge process was not observed due to the weak interaction force between substrate and Ge precursors while the saturation with respect to the pulse time was achieved.. The deatiled study on the dynamic balance between the adsorption and desorption kinetics of the Ge precursors showed that an ALD-like saturation behavior regarding the precursor injection time could be achieved even when multilayer formation of the physisorbed $Ge(OC_2H_5)_4$ molecules occurred. The behaviors in the growth rate with the variations in the substrate temperature and precursor bubbling temperature can also be quantitatively predicted using the physisorption model based on the Brunauer-Emmett-Teller (BET) theory

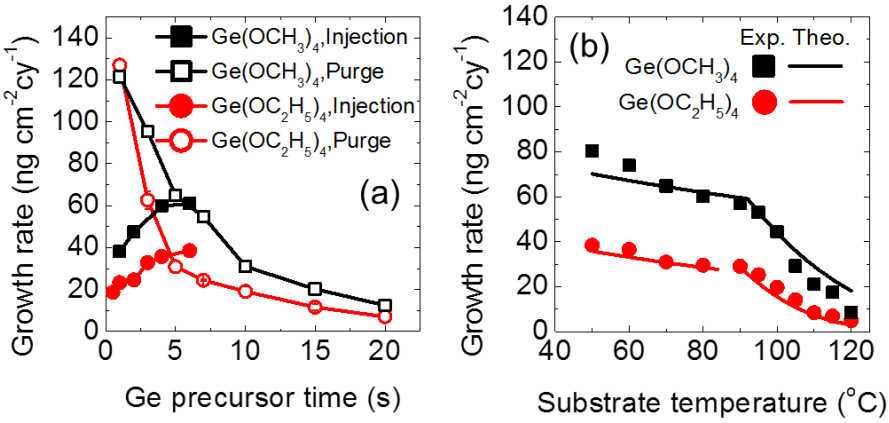


Fig 1. Influence of the process condition on the $GeTe_2$ growth rate of the processes using the $Ge(OCH_3)_4$ and $Ge(OC_2H_5)_4$ precursors: (a) influence of the Ge precursor injection and purge time in the Ge-Te cycle (b) influence of substrate temperature

Evaluating the change in electrical conduction mechanism and dielectric properties of TiO_2 thin-film by Al doping

Woojin Jeon*, Woongkyu Lee, Yeon Woo Yoo, Cheol Hyun An, and Cheol Seong Hwang
WCU Hybrid Materials Program, Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, 1 Gwanak-ro, Gwanak-gu, Seoul, 151-742, Republic of Korea
E-mail : wjjeon@snu.ac.kr

TiO_2는 높은 유전율[1]과 공정의 용이함으로 인해 차세대 DRAM capacitor dielectric 후보 물질로써 각광을 받고 있다. 하지만 좁은 band-gap과 oxygen vacancy로 인한 n-type 특성으로 dielectric으로 사용하기엔 지나치게 높은 누설전류특성을 가지고 있어 실제 device 사용에 어려움을 겪어왔으며, 따라서 대부분의 TiO_2 관련 연구는 누설전류를 감소시키기 위한 방향으로 연구가 진행되어 왔다. 그 중에서 Al을 doping한 Al-doped TiO_2의 경우 TiO_2 대비 10^5 배 누설전류를 감소시킨다는 결과가 보고된 바 있다 [2]. 하지만 Al doping 시 유전율이 60 정도로 감소하는 문제점을 가지고 있다.
본 연구에서는 Al doping 으로 인한 TiO_2의 누설전류 및 유전율 감소 등의 전기적 특성 변화가 어떤 mechanism으로 이루어지는지에 대해 규명해보았다. 누설전류 특성 분석을 통해 Al이 TiO_2에 doping 되었을 때 Schottky emission에 의한 누설전류가 크게 감소하는 것을 확인할 수 있었다. 이는 XPS를 통해 확인한 valence band offset 변화와 잘 일치하는 결과이다. XPS를 통해 doping된 Al의 화학 상태를 분석해 보았을 때, doping된 Al이 Al_2O_3 상태가 아닌 TiO_2 격자 내 치환된 상태로 존재함을 확인할 수 있었다. 또한 Al doping 과정에서 doping layer 주변 TiO_2의 결정성이 크게 저하 되었으며, 이러한 결정성 저하가 Al doping 시 전체 박막의 유전율이 pristine TiO_2 박막에 비해 감소하는 원인임을 알 수 있다. 이를 통해 Al-doped TiO_2에서 전기적 특성 변화 mechanism을 실험적으로 규명할 수 있었다. 또한 이를 활용하여 DRAM capacitor dielectric 물질로 적합한 Al-doped TiO_2의 특성을 더욱 향상시킬 수 있었다. 이와 같은 과정을 통하여 0.8V의 인가 전압에서 누설전류 밀도가 10^{-7} A/cm^2 이하의 특성을 만족 시키는 등가 산화막 두께를 0.4nm 이하로 확보 할 수 있었다.

[1] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys., 89, 5243 (2001).
[2] S. K. Kim, G.-J. Choi, S. Y. Lee, M. Seo, S. W. Lee, J. H. Han, H.-S. Ahn, S. Han, and C. S. Hwang, Adv. Mater., 20, 1429 (2008).

An Investigation of Electrical Characteristics in TiO_x Thin Film by Controlling Oxygen Vacancy

Jaesung Park, Daeseok Lee, Jiyong Woo, Euijun Cha, Sangheon Lee, Kibong Moon, Yunmo Koo, Jeonghwan Song and Hyunsang Hwang

Department of Materials and Science Engineering, POSTECH, Pohang, Gyeongbuk, Korea

E-mail : hwanghs@postech.ac.kr

Titanium oxide is an attractive meterial for ReRAM application because it has not only resistive switching but also selection characteristics such as non-linearity and metal-insulator-transition (MIT) by amount of oxygen vacancy [1]. In this paper, we investigate how can change electrical characteristics of thin film TiO_x about oxygen vacancy utilizing structural optimizaition.

To investigate the thin film TiO_x electrical characteristics about oxygen vacancy, we deposited TiO_x layer on a via-hole structure with a 250-nm diameter using Ti_4O_7 target. To control oxygen vacancy minutely, TiO_x layer thickness was varied from 2nm to 15nm and Ta was used top electrode due to absorbing oxygen vacancy.

The electrical characteristics of devices is shown in Fig. 1. Ta/TiO_x/Pt device which TiO_x thickness is 2nm has a resistive switching while 15nm TiO_x device has non-linear characteristics and occasionally shows MIT [2]. According to XPS depth profiling results, as shown in Fig. 1, 2nm TiO_x device has lower oxygen distribution than 15nm TiO_x device. It means that oxygen vacancy is important factor to determine electrical characteristics of thin film TiO_x.

In conclusion, electrical characteristics of thin film TiO_x depends on oxygen vacasncy. Thus, we can select a TiO_x based ReRAM or MIT selection device by controlling oxygen vacancy.

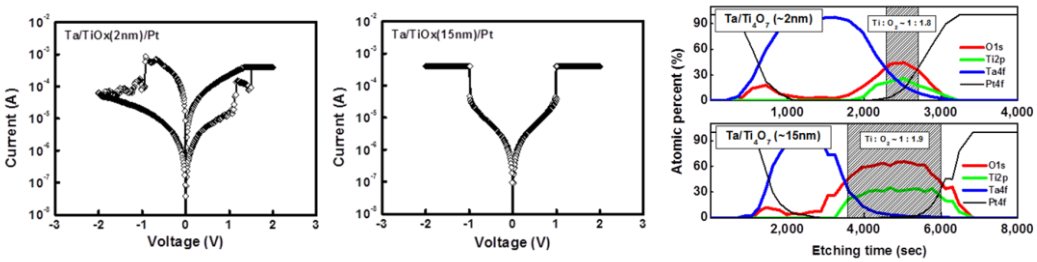


Fig. 1 Electrical characteristics of thin film TiO_x depending on thickness and XPS depth profile results of 2nm and 15nm thick TiO_x deivces

[1] K. Szot et al, Nanotechnology 22 254001 (2011)

[2] Daeseok Lee et al, will be presented at IEDM (2013)

Acknowledgement

This work was supported by POSTECH-Samsung Electronics ReRAM Cluster Research, R&D program of Ministry of Knowledge Economy, and the Pioneer Research Center Program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (2012-0009460).

Recent Advances in Terahertz Electronics

Munkyo Seo[1], Miguel Urteaga[2], and Mark Rodwell[3]
[1]*College of Information and Communication Engineering, Sungkyunkwan University, Korea*
[2]*Teledyne Scientific Company, California, USA*
[3]*University of California, Santa Barbara, USA*
E-mail : mkseo@ieee.org

Recent advances in semiconductor technologies have enabled design and implementation of very high-frequency ICs. Specifically, using advanced CMOS and InP HBT technologies, ICs operating beyond 100 GHz and 300 GHz have been recently demonstrated, respectively, opening a pathway to fully integrated terahertz systems for imaging, radar and communication applications. At these frequencies, we face several fundamental design challenges: available active device gain is relatively low, while losses from passive devices are relatively high. Local interconnects become an essential circuit element, as overall circuit sizes are relatively large compared to a wavelength. Traditional analog-IC design style may not directly scale to sub-millimeter-wave frequencies, while traditional RF design style may not be optimal in terms of circuit size and operating bandwidth. For a successful IC design, a holistic design approach is therefore necessary, where device, circuit, and their electromagnetic environment are altogether considered from the early design phase. In this presentation, recent trends and terahertz IC results in CMOS and HBT technologies will be reviewed, as well as their future applications. Then, the design and implementation of millimeter-wave and sub-millimeter-wave ICs using InP HBT technology will be presented to illustrate such a design approach, including various transceiver building blocks and a single-chip phased-locked loop operating at 300 GHz and beyond.

THz Varactors based on III-V High Electron Mobility Transistor Structures

Seung Heon Shin, Dae-Myeong Gum, and Jae-Hyung Jang
School of Information and Communications, Gwangju Institute of Science and Technology
1 Oryongdong, Gwangju 500-712, South Korea
E-mail : jjang@gist.ac.kr

Metal-semiconductor-metal (MSM) varactor diodes on top of a 2-dimensional electron gas (2DEG) based on III-V semiconductor-based heterostructures have been demonstrated in recent years. MSM-2DEG varactors have various advantages such as easy integration with high electron mobility transistor (HEMT) circuits and binary capacitance switching characteristics. The capacitance switching ratio, C_{max}/C_{min}, of the MSM-2DEG varactor was much higher than those of conventional p-n, heterostructure diodes, and Schottky diodes. Moreover, its bistable capacitance switching behavior is more suitable for binary frequency shifting circuits.

Terahertz (THz) electronics, which can generate, control, and detect THz signals, is getting more interests due to the emerging applications such as THz security, bio-imaging, and communication. In order to achieve a cutoff frequency that corresponds with the THz range from MSM-2DEG varactors, devices should have very low parasitic capacitance and very low parasitic resistance within the device.

Among HEMT structures, InP-based HEMT structures have shown outstanding performance in millimeter and sub-millimeter wave applications such as LNAs, OEICs, power amplifiers, and oscillators because of their excellent high frequency characteristics and low noise performance originating from high electron mobility, high saturation velocity, low effective electron mass, and high sheet charge density. In the meantime, the advent of InAlN/GaN HEMT structures have also been spot lighted as a next generation low power ultra-high speed electronics due to the excellent material characteristics such as lattice-matched heterostructures and high sheet carrier densities leading to the high output power.

In this presentation, design criteria of the MSM-2DED varactors by introducing figure of merit (FOM), which is defined as $f_o \cdot C_{max}/C_{min}$, where f_o is the cutoff frequency of the varactors. The critical parameters determining the FOM will be identified and the design examples of high cutoff frequency above 1 THz within the limit of the same FOM will be given.

Recently demonstrated high performance varactors based on InP/$In_{0.52}Al_{0.48}As$/$In_{0.7}Ga_{0.3}As$ HEMT structure with FOM higher than 1 THz and varactors on InAlN/GaN heterostructures will also be presented.

[1] MSM Varactor Diodes Based on In0.7Ga0.3As HEMTs with Cut-off Frequency of 908 GHz, S. H. Shin, D. M. Geum, and J. H. Jang, IEEE Electron. Dev. Lett., in press.

Improved current collapse phenomenon in AlGaN/GaN HEMTs on Si substrate by using SiNx re-deposition process

Minseong Lee, Donghwan Kim, Sukeun Eom, and Kwangseok Seo
Department of Electrical Engineering and Computer Science, *Seoul National University, Seoul 151-747, Korea*
E-mail : beterang83@snu.ac.kr

AlGaN/GaN HEMTs have great potential in high power microwave applications [1]. Despite the remarkable improvement in GaN-device technology, the "current collapse" issue has not been completely solved yet, which plays an important role in RF performance. It has been reported that optimizing a surface passivation process can diminish the current collapse phenomenon [2]. In this study, we developed a SiNx re-deposition process to further improve the current collapse phenomenon. A pre-passivation process started with SiN_x deposition at 350 ^{o}C using a remote ICP-CVD system in order to protect the surface during device fabrication. The key difference in the re-deposition process was that the SiN_x pre-passivation layer was removed after high-temperature ohmic annealing by using a CF_4/O_2-based dry etching method and a new SiN_x film was re-deposited on the entire surface before continuing the process. No significant difference in drain current density was observed between re-deposited and control devices whereas great improvement in pulse characteristics was observed for the re-deposited device. The SiN_x pre-passivation layer was not removed for the control devices. The current collapse in pulse characteristics ($V_{DS.Q}$ = 30 V and $V_{GS.Q}$ = -5 V) decreased from ~33% to less than 8% when the re-deposition process was employed. It is speculated that the surface, even with the pre-passivation layer, was damaged during high-temperature ohmic annealing (800 °C, in N_2 ambient). Removing the pre-passivation layer and re-depositing the fresh SiN_x film turned out to be a very effective way to recover the damaged surface. As a result of the improved pulse characteristics, the re-deposited device exhibited superior characteristics to the control device; an output power density of 6.3 W/mm and PAE of 53.5% with the drain bias of 15V at 9.3 GHz.

[1] Mishra, U.K., Parikh, P., and Yi-Feng Wu: 'AlGaN/GaN HEMTs-an overview of device operat ion and applications', Proc. IEEE., 2008, 90, (6), pp. 1022-1031.
[2] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," IEEE Electron Device Lett., vol. 21, no. 6, pp. 268–270, Jun. 2000.

Performance Optimization Study of FinFETs Considering Parasitic Capacitance and Resistance

SoYoung Kim
Department of Semiconductor Systems Engineering, Sungkyunkwan University, Suwon, Korea
E-mail : ksyoung@skku.edu

Devices with nonplanar gate structures such as double gate transistors, FinFETs and gate-all-around transistors were once considered the next generation devices. Recently, the first generation FinFET based microprocessors are being mass produced, and scaling of FinFET transistors is ongoing. Traditional capacitance and resistance models cannot be applied to nonplanar gate transistors like FinFETs. Although scaling of nanoscale FinFETs may alleviate electrostatic limitations, fringe capacitances increase due to the close proximity of the source/drain (S/D) selective epitaxial growth (SEG) region to the gate, and series resistances increase due to the narrow finwidth [1].
In this study, we will review the analytical modeling approach of parasitic capacitance and resistance for FinFETs[2]. Then, we will introduce simulation methods to evaluate their impact on circuit-level performance metrics such as digital circuit delay and analog/RF performance. The impact of layout-dependent three dimensional parasitics and technology scaling on the circuit performance metrics will be investigated, and the relevant tradeoffs will be discussed.

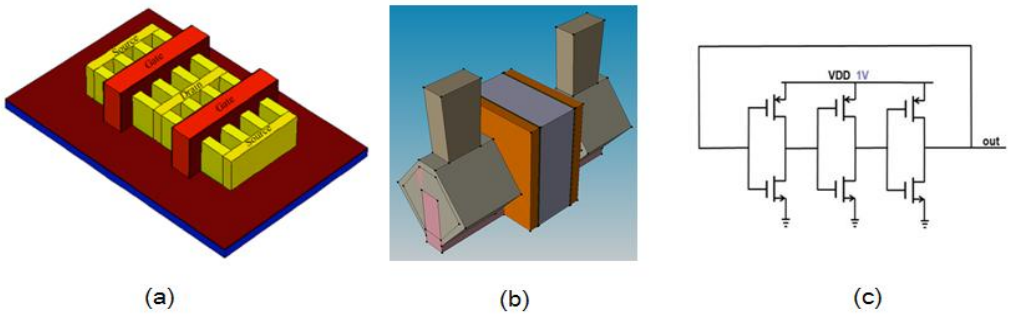


Fig 1. (a) Multifin FinFET structure. (b) S/D SEG region. (c) Ring oscillator circuit.

[1] Chang-Woo Sohn et al., “Device Design Guidelines for Nanoscale FinFETs in RF/Analog Applications, ” IEEE Trans. Electron Devices, vol. 33, no. 9, pp. 1361-1370, Sept. 2012.
Electron Devices, vol. 33, no. 9, pp. 1361-1370, Sept. 2012.
[2] K. Lee, T. An, S. Joo, K.-W. Kwon, and S. Kim, “Modeling of Parasitic Fringing Capacitance in Multifin Trigate FinFETs,” IEEE Trans. Electron Devices, vol. 60, no. 5, pp. 1786-1370, May 2013.

Effect of Hydrogen Induced Gettering on Sensing Margin Enhancement of Si CMOS Image-sensor Contaminated with Cu and Ni

Il-Hwan Kim, Seung-Hyun Song, Joo-Hyeong Park, Gon-Sub Lee and Jea-Gun Park*
Advanced Semiconductor Materials and Device Development Center,
Department of Electronics and Communication Engineering, Hanyang University,
Seoul 133-791, Republic of Korea
E-mail : parkjgl@hanyang.ac.kr

With expanding the use of mobile devices such as cellular phones and digital cameras, CMOS image-sensor (CIS) has been attracting a great deal of attention. As the pixel size in CIS has scaled less than 1.1 μm, it is important to maintain the sensitivity of the photodiode of a CIS cell. To improve photo sensitivity in CIS, the achievement of a lower dark current is essential. Thus, we investigated the dependency of the properties of CIS on metallic contamination. For metallic contaminants, especially Ni and Cu, the minority-carrier recombination lifetime decreased with increasing a metallic contaminant concentration. These contaminations result in degradation of sensitivity of photodiode and sensing margin of CIS. In our study, we applied a gettering method using hydrogen ion implantation by forming nano-cavities close to the device region (Fig. 1). It was confirmed that the sensing margin of CIS was dramatically improved, as shown in Fig. 2. We will present the effect of hydrogen induced gettering on sensing margin enhancement of Si CIS contaminated with Cu and Ni and suggest an extremely proximity gettering method for reducing metallic contaminants for CIS.

* This work was financially supported by the Brain Korea 21 Plus Program in 2013 and SiWEDS (Silicon Wafer Engineering and Defect Science), an Industry/University Cooperative Research Center under the National Science Foundation Grant.

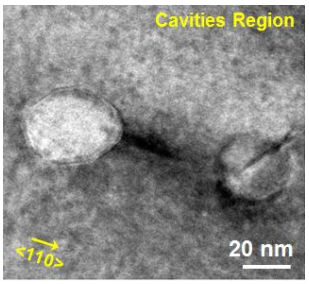


Fig 1. Cavities region formed by hydrogen ion implantation

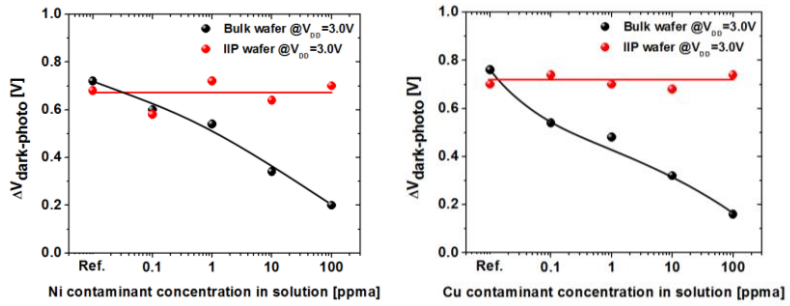


Fig 2. Sensing margin of CMOS-image-sensor after metallic contamination: bulk wafer vs. hydrogen ion implanted wafer

[1] F. Domengie, J. L. Rrgolini, and D. Bauza, *J. Electron. Mater.*, 39, 6 (2010) 625

Optimization of 7V to 60V Low Vgs nLDMOS with Enhanced Specific On-resistance

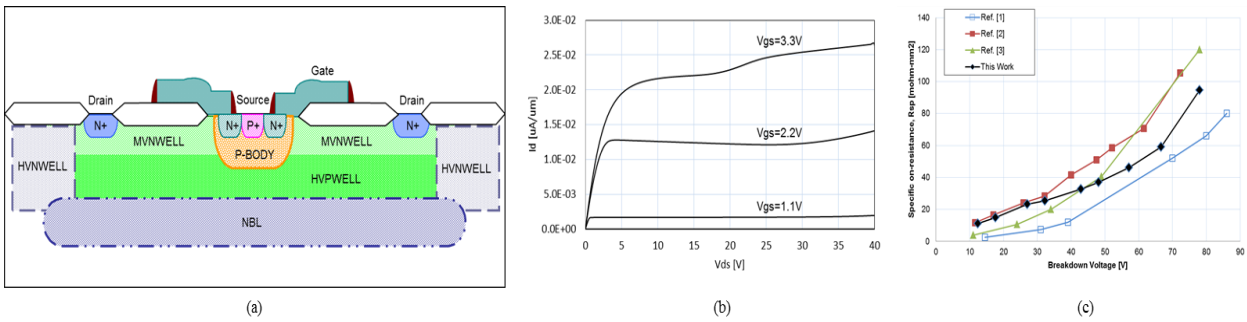
Min-Woo Kim, Cheol-Ho Cho, Choul-Joo Ko, Min-Seok Kim, Hyung-Gyun Jung, Hee-Bae Lee, Sun-Kyung Bang, Han-Geon Kim, Sung-Mo Gu, Sun-Kyoung Kang and Jung-Ho Kang

Product Integration Team, Dongbu Hitek, Bucheon 420-712, Korea

E-mail : minwoo.kim1@dongbuhitek.com

최근, BCDMOS(Bipolar–CMOS–DMOS) 공정은 LED Driver, Switching Regulator, Audio Amplifier, Motor Driver, Power Management 제품 등의 application market 에서 광범위하게 사용되고 있으며, Cost-effective BCDMOS 공정은 Power Management 분야에서 높은 성장을 이끄는 역할을 하고 있다. 기존 BCDMOS 공정은 Analog 를 구동시키는 LDMOS 영역과 Digital 의 고속 연산을 하는 CMOS 영역의 GATE 전압 Level 이 달라 Interface 시 Voltage Level 차이가 발생하고, 이로 인해 Voltage Buffer 역할을 하는 Function Block (level shifter, charge pump 등)이 추가로 필요하기 때문에 비용 및 크기가 제한된다. 이러한 문제를 해결하기 위해, 본 논문에서는 0.35um BCDMOS 공정을 이용하여 LDMOS 와 CMOS 영역의 GATE 전압 Level 을 동일하게 하고 nLDMOS 의 Rsp 를 향상시킨 구조를 제안하였다. 제안된 40V nLDMOS 소자의 경우 BV_{DSS}=54V, Rsp=47.3 mΩ•mm^2 로 기존 Low Vgs nLDMOS 소자 대비 23.3%의 Rsp 감소 효과를 얻을 수 있었다. 이러한 Rsp 감소는 0.18um 급 BCDMOS 공정과 비교해도 매우 경쟁력 있는 결과이다.

LDMOS 소자 제작을 위해 본 논문에서는 P+ substrate 에 P-epi 를 epitaxially 증착시킨 wafer 를 사용하였으며, Gate Oxide 두께는 Digital CMOS 영역과 동일한 77 Å으로 제작하였다(Vgs=3.3V, 0.35um BCDMOS process). Fig. 1(a)는 40V High-side nLDMOS 소자의 단면도이며, 제안된 nLDMOS 소자는 높은 doping 농도를 갖는 MVNWELL 과 HVPWELL 로 인해 더 낮은 Rsp 를 구현할 수 있었다. Fig. 1(b)는 40V High-side nLDMOS 소자의 I_{DS}-V_{DS} 특성을 보여준다. I-V 특성은 높은 Gate 전압과 Drain 전압에서 Kirk-Effect 현상을 보이는데, 이것은 Drain 영역에서 impact ionization 에 의해 generation 된 electron-hole pair 때문이다 [1]. Fig.1(c)는 Breakdown Voltage 와 Specific On-resistance 사이의 trade-off 특성이며, 본 실험을 통해 제작된 7V~60V nLDMOS 소자의 Rsp 는 기존 Low Vgs nLDMOS 소자 대비 약 5%~40% 감소하였다.



(a) (b) (c)

Fig 1. Schematics of the (a) Cross-sectional view, (b) experimental I_{DS}-V_{DS} and (c) trade-off characteristics

[1] H. L. Chou, et all, “0.18um BCD Technology Platform with Best-in-Class 6V to 70V Power MOSFETs”, ISPSD, pp. 401-404, 2012.

[2] C. J. Ko, et all, “A New 8V-60V rated Low Vgs NLDMOS Structure with Enhanced Specific on-Resistance”, ISPSD, pp. 245-248, 2010.

[3] D. Riccardi, et all, “BCD8 from 7V to 70V: a new 0.18um Technology Platform to Address the Evolution of Applications towards Smart Power ICs with High Logic Contents”, ISPSD, pp. 70-76, 2007.

Proposal of 90V rated High-side n-type LDMOS utilizing double-epi process

Joowon Park, Kwangsik Ko, Soonyeol Park, Daehoon Kim, Jina Eum,
Kuemju Lee, Sekyung Oh, Sanghyun Lee, Inwook Cho and Kyungdong Yoo
Technology Development team, SK hynix Inc, Cheong-ju, South Korea
E-mail : joowon.park@sk.com

In this study we proposed new type 90V rated High side nLDMOS(n-type Lateral Double-diffused MOS) device in 0.13um BCD process[1], and proved it by 2-dimensional device simulation. To achieve up to 90V BV(Breakdown voltage) in high side LDMOS with junction isolation, we should use sufficient thickness of epi layer to get BV between P-BODY and NBL(n-type buried layer). But thick epi layer demands high energy implant and long time drive-in to make Deep N-Well it works to link drain junction with NBL. And it derives bigger chip size because of lateral diffusion. In case of Low side nLDMOS, low doped Deep N-Well and PBODY meets vertically, so thick epi layer is not needed. But in High side nLDMOS, high doped NBL is necessary, so it needs thick epi layer. To overcome this, we scheme out a double epi process[2], and to use resurf technology effectively, we added P-type buried layer(PBL) between 1st and 2nd epi layer. And then we designed layout split of PBL, to find best combination of charge balance between Deep N-Well with PBL. (PBL doping concentration controled by implant open size split.) And we use floating poly plates to improve BV without Ron(on-resistance) increase, and for that we optimized poly plate length on STI. Figure.2 shows that adapting floating poly plates disperse impact ioniazation peak point into 3spots, and cause BV increase. Finally We got BV=132V, Ron.sp=210mohm*mm2 in High-side nLDMOS using double epi process, PBL and floating poly plates. (in case of Low-side nLDMOS, we got BV=134V, Ron.sp=190mohm*mm2 using same process).

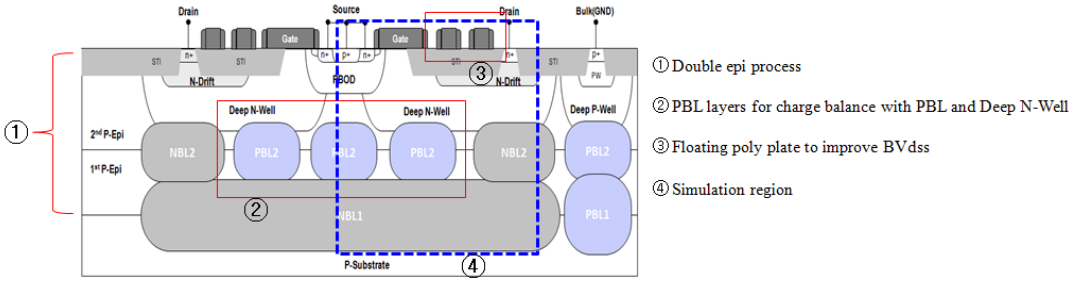


Figure.1 Proposed structure of 90V rated HS nLDMOS

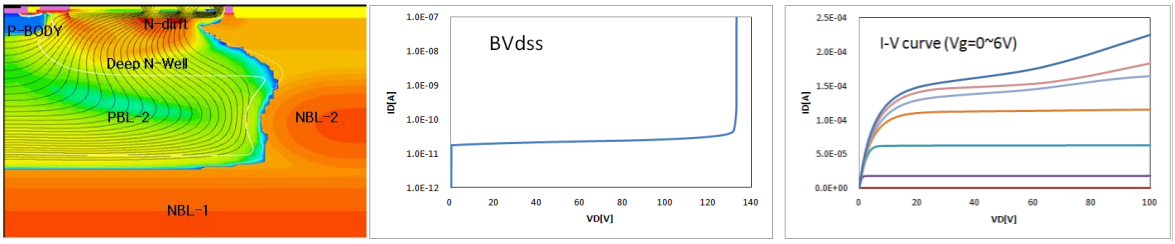


Figure.2 Simulated Potential Contour, Impact ionization, depletion, BVdss & I-V characteristcs

[1] K.S. Ko, "HB1340- Advanced 0.13um BCDMOS Technology of Complimentary LDMOS...", p159-162, ISPSD 2013

[2] "새로운 고내압 LDMOS High Side 소자제작" 출원번호 : 20130107448, 발명번호 : IVX000133839

GPS와 Compass를 위한 이중 채널용 GNSS 수신기의 설계 기법

정연재
㈜ 지씨티리써치, 아날로그 부서

최근 스마트폰을 비롯한 여러 전자기기에서 위치 정보를 활용하게 되면서, 세계 여러 나라들은 고유의 GNSS(Global Navigation Satellite Systems)를 개발하고 있다. 미국의 GPS 와 더불어, 러시아의 GLONASS, 유럽연합의 Galileo, 중국의 Compass(또는 Beidou)가 이에 해당한다. 서로 다른 GNSS 신호를 동시에 수신할 수 있게 되면, 정확도 및 위치 획득 시간을 개선할 수 있을 뿐 아니라, 보다 양질의 신호를 선택할 수 있는 이점이 있다.

기존의 연구 결과로 발표된 이중 채널용 GNSS 수신기의 설계 방식은 다음과 같다.
- 모든 개별 블록이 독립적으로 동작하는 두 개의 수신기를 집적하는 방식[1]
- 주파수 합성기를 공유하는 두 개의 수신기를 집적하는 방식[2]
- 단일 수신기로 구현하되, 채널 분리는 digital baseband 에서 구현하는 방식[3]

본 논문에서는, 각 구현 방식의 장단점을 알아보고, 최근의 초미세 공정 사용에 따른 향후 연구 방향을 제시하고자 한다.

[1] D. Chen *et al.*, "Reconfigurable dual-channel multiband RF receiver for GPS/Galileo/BD-2 systems," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 3491-3501, Nov. 2012.
[2] N. Qi *et al.*, "A dual-channel Compass/GPS/GLONASS/Galileo reconfigurable GNSS receiver in 65nm CMOS with on-chip I/Q calibration," *IEEE Trans. Circuits and Systems-I*, vol. 59, pp. 1720-1732, Aug. 2012.
[3] C. G. Tan *et al.*, "A universal GNSS (GPS/Galileo/Glonass/Beidou) SoC with a 0.25mm^2 radio in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 334-335.

Baseband block control for low power consumption in broadcasting RF receiver system

Huijung Kim, Sanghoon Kang, Hyeongseok Jeong, Soo-Young Kim, and Chaehag Yi
M&C development, System LSI business, Samsung Electronics, Young-In 446-711, South Korea
E-mail : huijungsk.kim@samsung.com

모바일 기기에서 제한된 배터리 용량으로 인해, 모바일 통신에 필수적인 RF 수신기의 파워를 줄이고자 하는 노력은 계속 되고 있다. 본 연구에서는 추가적인 회로 없이 모바일 채널 환경을 추정(estimation)하고, 추정된 채널 환경을 바탕으로 RF 수신기의 전력 소모를 줄이는 방법에 대해 알아보고자 한다. 그림 1 은 일반적인 RF 수신기의 block diagram 이다 [1]. 그림 1 에서 Mixer 의 출력에 TIA(Trans Impedance Amplifier) 블록에서 R_{TIA} 와 C_{TIA} 는 1st order RC LPF (Low Pass Filter)를 구성한다. 이때 C_{TIA} 가 있고 없고 에 따라 TIA 의 특성이 LPF 혹은 APF(All Pass Filter)의 mode 로 바뀐다. 즉 C_{TIA} 를 통해 TIA 의 transfer function 을 바꿀 수 있으며 이를 이용해서 통신 채널을 추정할 수 있다. 즉 통신 신호에 interfere 가 있는 경우라면, APF 와 LPF 로 mode 를 바꾸었을 때 modem 에서 측정하는 SNR 에 변화가 있을 것이고, 반대로 통신신호에 interfere 가 없는 경우라면 APF 와 LPF 로 mode 를 바꾸었을 때 SNR 의 변화가 없을 것이다. 이러한 특성을 이용해서 통신 채널을 추정하고 추정한 채널을 바탕으로 interfere 가 없는 채널이 확인되면 전류소모가 큰 Channel Selection Filter 대신에 상대적으로 전류소모가 적은 VGA 회로로 대체하면 RF 수신기의 전류소모를 줄일 수 있다. 그림 2 는 이러한 시나리오에 대한 flow chart 를 보여준다. 비록 이러한 동작은 수신하는 신호의 SNR 이 통신에 필요한 SNR 보다 큰 방송(Broadcasting signal) 신호에 적합하다는 단점은 있다.

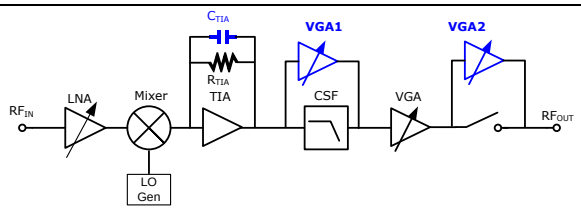


Fig 1. RF receiver block diagram for small power consumption

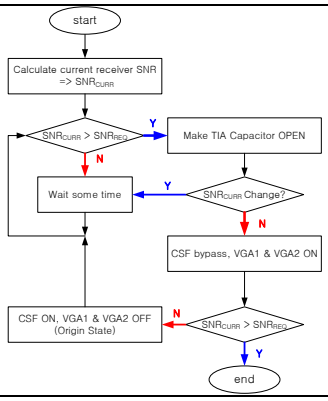


Fig 2. Flow-chart for reduction of power consumption

[1] B. Razavi, *RF Microelectronics*, second edition. Prentice-Hall, 2011.

Quantum-dot sensitized metal oxide semiconductor hybrid phototransistor for near infrared detection

Do Kyung Hwang,[1] Hee Sung Lee,[2] Yun Jae Lee,[1] Won Kook Choi,[1] and Seongil Im[2]
[1]*Interface Control Research Center, Korea Institute of Science and Technology, Seoul 136-791, Korea*
[2] *Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea*
E-mail : dkhwang@kist.re.kr

Solution processed colloidal quantum dots (QDs) have unique properties that can lead to cost-effective and printable optoelectronic applications such as light emitting diodes, photodetectors, and photovoltaic cells. In particular, lead sulfide (PbS) QD has been extensively studied with much attention because it is highly desirable as light absorber for harvesting sunlight energy or for near-infrared (NIR) photo-detection.[1] Here we introduce new approach of three-terminal PbS QD/InGaZnO (IGZO) hybrid phototransistor for NIR detection wherein colloidal PbS QDs play a role of NIR sensitized layer and can be easily formed on the top of IGZO thin film transistors (TFTs) array. This hybrid phototransistor responded to NIR light up to 1400 nm. The photo-generated electrons from the PbS sensitized layer can be transferred to the IGZO channel and consequently induced significant negative threshold voltage shift on the TFT. To further evaluate the real potential towards the development of more practical applications, a photo gating resistive-load inverter was implemented by connecting a unit phototransistor to an external load resistor. The photo-induced threshold voltage shifts of the hybrid phototransistor led to certain output voltage signals in static and dynamic characteristics of this photo-inverter. We expect that this hybrid phototransistor can be simply integrated on glass or plastic substrates that can be applied to pixels on flat panel photo imaging applications or building blocks on complex photo gating logic circuits.

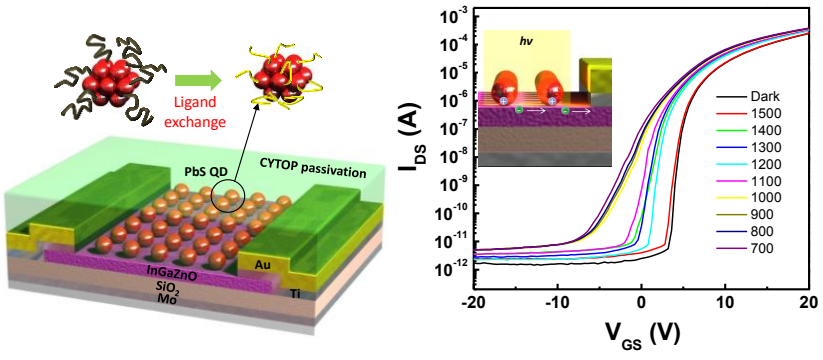


Fig 1. PbS/IGZO hybrid phototransistor and its photo induced transfer characteristics.

[1] J. Tang *et al*., *Nat. Mater.* **10**, 765 (2011).

Development of low-cost and high speed coincidence count unit using FPGA

Byung Kwon Park, Min-Soo Lee, Min Ki Woo, Il Young Kim, Osung Kwon,
Yong-Su Kim, Sang-Wook Han, Sung Moon
Center for Nano & Quantum Information research, Korea Institute of Science and Technology (KIST), Seoul, 136-791, Korea
E-mail : H13006@kist.re.kr

A Coincidence Counting Unit(CCU) is a module that counts the coincidences of two or more inputs. Since many intersting characteristics of quantum entanglement are usually measured by a two-photon interference which requires a coincidence detection between two single-photon detectors, CCUs are widely used for quantum optics and quantum information experiments. One easy way to implement a CCU would be using Time-to-Amplitude Converters(TACs), however, it is usually expensive and bulky. On the other hand, a Field Programmable Gate Array(FPGA) can be an inexpensive and simple option to implement a CCU. In the Ref. [1], the authors developed a CCU with an inexpensive FPGA. They utilized AND gates of the FPGA and could achieve 7 ns of coincidence window.

Here, we introduce a new CCU with an FPGA which has better performances. Fig 1 (left) shows a block diagram of the CCU. For better performances, we employ not only AND gates but also JK Flip-Flops, EX-ORs, and delay buffers. With a new scheme, the coincidence window can be less than 1.6 ns. Note that the small coincidence window is crucial for many quantum optics experiments to reduce the background noise. Furthermore, the delays of each input can be independently adjustable up to 100 ns that is convenient for users. The delay adjustment resolution is about 1ns. The maximum counts and coincidence counts are more than 100MHz due to the smaller coincidence window, see Fig 1 (right). Detailed scheme and characteristics will be presented.

The work was supported by the IT R&D program of MSIP/KEIT. [10044559, Development of key technologies for quantum cryptography network]

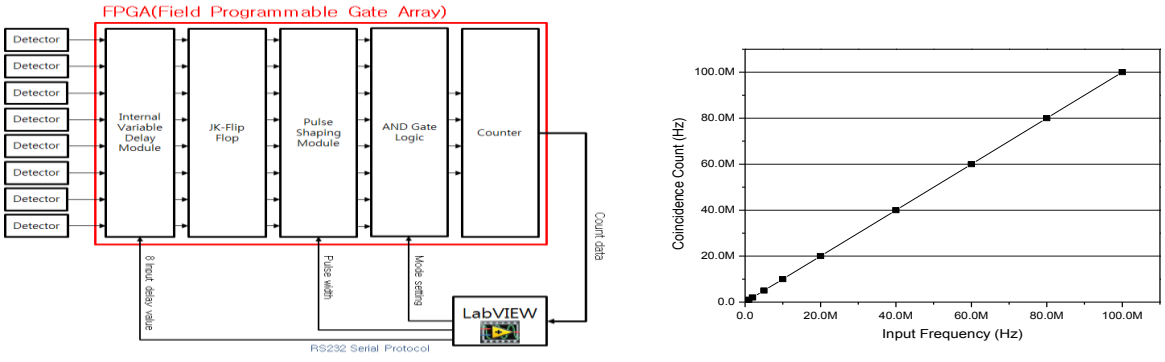


Fig 1. Block diagram of CCU and performance graph

[1] Branning D., Bhandari S., and Beck M., Am. J. Phys 77, 667-670 (2009).

Temperature characteristics of dark and afterpulse noise in single photon detector using InGaAs/InP avalanche photodiode

Minsoo Lee, Byungkwon Park, Minki Woo, Il-young Kim, Osung Kwon, Yong-su Kim, Sang-wook Han and Sung Moon

Nano & Quantum Information Research Center, Korea Institute of Science and Technology, Hwarangno 14-gil 5, Seongbuk-gu, Seoul 136-791, Republic of Korea

E-mail : lms0408@kist.re.kr

Nowdays, many research groups are working to reduce the noise of single photon detector using InGaAs/InP avalanche pohoto diode(APD)[1]. There are two major noise sources that are dark count and afterpulse. The dark count can be easily reduced by cooling APD. In contrast, the afterpulse increases shaply in low temperature condition because the reduction of APD temperature causes rising of detrap time of carriers in APD[2]. We had developed the single photon detector using the integrator method to reduce afterpulse and acheived less 2 % afterpulse probability at quantum efficiency(QE) of 15.6 %[3]. In this paper, we have focused on finding the temperature characteristics of two major noise souurces. As shown in Fig 1. and Fig. 2, the integrator scheme has an low noise performance versus QE and temperature, respectively, in the measurement condition of 0.1 photons input and 25MHz operation. It shows clearly that the optimal operation temperature is -10 degree. But the optimal point varies in the diffenent measurement conditions since the operation conditions affect the dark and the afterpulse noise differently. In the conference, we will present the measurement results in various conditions versus temperature that can indicate the optimal point in specific application of single photon detector.

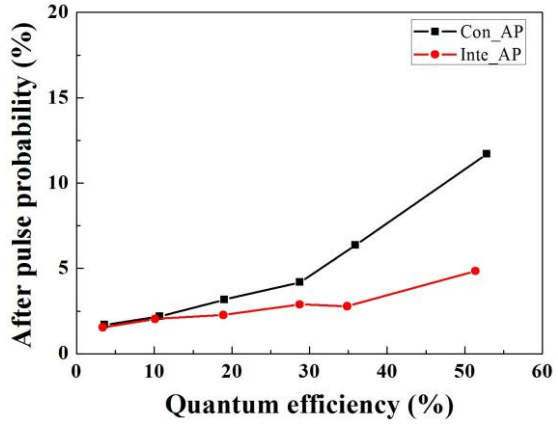


Fig 1. After pulse probability vs quantum efficiency

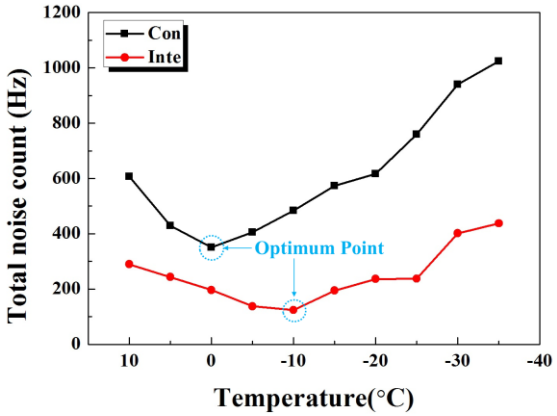


Fig 2. Optimum point of total noise in APD

ACKNOWLEDGMENTS

The work was supported by the IT R&D program of MSIP/KEIT. [10044559, Development of key technologies for quantum cryptography network]

[1] Z.L Yuan, B. E. Kardynal, A.W. Sharpe, A and J.Shields, Applied Physics Letters 91, 041114 (2007)

[2] Y. Kang, D.S. Bethune, W.P. Risk and Y.-H. Lo, SPIE Vol. 5246 (2003)

[3] Abdessattar Bouzid, Sang-Wook Han, Min-Soo Lee, and Sung Moon, Applied Physics Express 6, 052201 (2013)

Noise reduction in graphene nanopores

Ashvani Kumar, Kyeong-Beom Park, Hyun-Mi Kim, and Ki-Bum Kim

Department of Materials Science and Engineering, Seoul National University, Seoul 151-742, Korea

E-mail: kibum@snu.ac.kr

Among various biological and solid state nanopores, graphene nanopores provide the possibility for futuristic sequencing technology because of atomically thin and mechanically robust graphene membrane [1]. In spite of the possibility of enhanced resolution and sensitivity to the small structural change of the molecule passing through the graphene nanopore, high level of ionic current noise limits their applications and is responsible for degraded spatial and temporal resolution [2]. Here, we descriptively investigate the impact of different substrate materials (Si and Quartz) and membrane thicknesses on noise characteristics of graphene nanopore devices. To mitigate the membrane fluctuations and pin-hole defects, a SiN_x membrane is transferred onto the substrate and a pore of approximately 70 nm in diameter was perforated prior to the graphene transfer. Comprehensive noise study reveals that the few layer graphene transferred onto quartz substrate possesses low noise level and higher signal to noise ratio as compared to single layer graphene without deteriorating the spatial resolution. The findings here point to improve the graphene based nanopore device for exciting opportunities in futuristic single-molecule genomic screening devices.

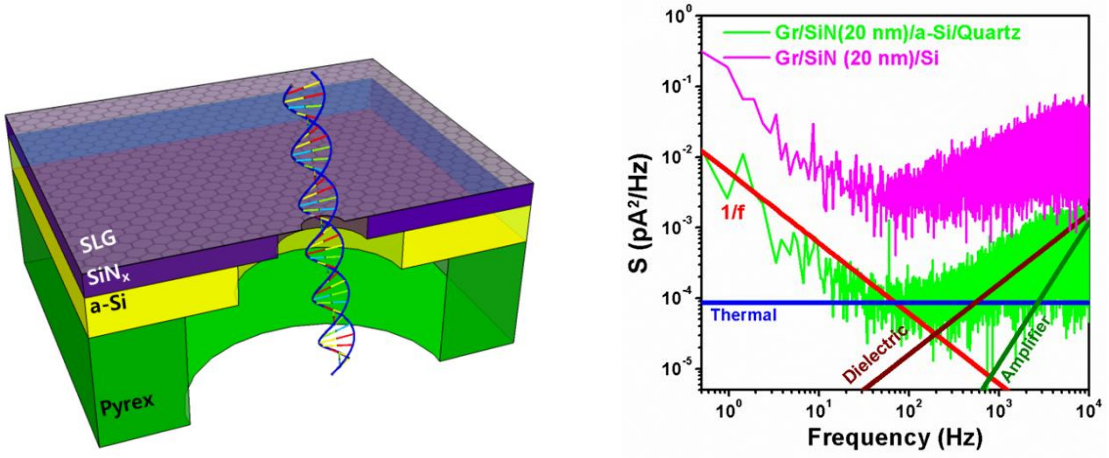


Fig 1. Schematic diagram and the noise data corresponds to Quartz and Si based graphene nanopores.

[1] S. Garaj, W. Hubbard, A. Reina, J. Kong, D. Branton and J. A. Golovchenk 2010 Nature 467, 191-94.

[2]Merchant C A, Healy K, Wanunu M, Ray V, Peterman N, Bartel J, Fischbein M D, Venta K, Luo Z, Johnson A T C and Drndic M 2010 Nano Lett. 10 2915-21.

The fabrication method of tungsten oxide-based sensors using laser-induced oxidation

Jaeho Shim, Jeong Oen Lee, Kyungmook Kwon, Minkyung Kim, Jun-Bo Yoon, and Kyoungsik Yu
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea
E-mail : ksyu@kaist.edu

Among various metal oxide semiconductors, tungsten oxide (WO_x) has been extensively investigated due to its properties that can be used for a number of applications, such as gas sensing and nonvolatile memories [1-2]. For facile fabricatoin of tungsten oxide-based devices, we propose a localized laser heating method in which tungsten metal is chemically converted into tungsten oxide at a specific location illuminated by the focused laser spot. We experimentally demonstrate a real-time laser-induced oxidation process to selectively convert the tungsten metal bridge into a W-WO_x hybrid within a sub-micron length scale. Computer simulations based on the finite element method suggest that the heated temperature near the laser spot is high enough to oxidize the 40-nm-thick tungsten material within a few seconds. The current-voltage curves also show the conductivity change due to the oxidation. The proposed method will find a number of applications in studying/making tungsten oxide-based devices, such as humidity sensors.

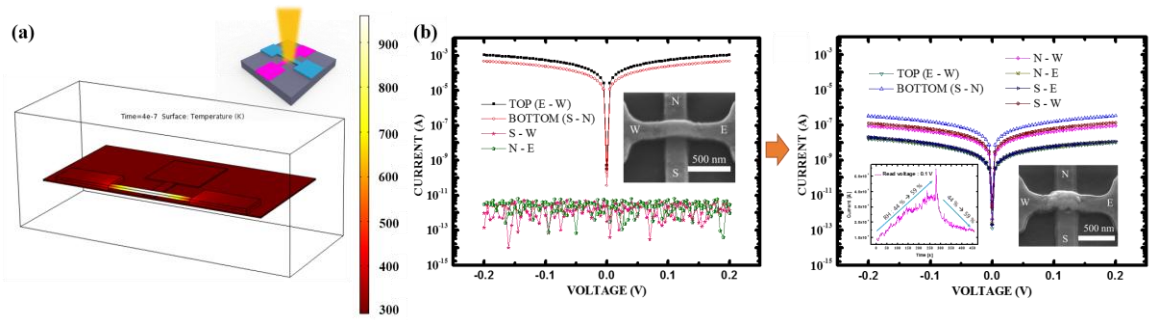


Fig 1. (a) Laser heating simulation and (b) current-voltage curves before and after laser heating. The inset shows the change of current depending on the relative humidity.

[1] A.J.T. Naik, M.E.A. Warwick, S.J.A. Moniz, C.S. Blackman, I.P. Parkin, R. Binions, J. Mater. Chem. A, 1, 1827 (2013).
[2] D. S. Shang, L. Shi, J. R. Sun, B. G. Shen, F. Zhuge, R. W. Li, and Y. G. Zhao, Applied Physics Letters 96, 072103 (2010)

Nanophotonic Devices for NT-IT Convergence

Chang-Won Lee, Yeonsang Park, Young-Geun Roh, Jineun Kim, and Sangmo Cheon
Frontier Research Lab, Samsung Advanced Institute of Technology, Yongin 446-712, Korea
E-mail : chang-won.lee@samsung.com

Recent progress in nanophotonics promises bright future of new devices by merging nanotechnology and information technology [1,2]. Here, we report two preliminary plasmonic device prototypes. First, a two color surface plasmon polariton launcher is demonstrated in the visible by utilizing locally embedded semiconductor nanocrystal (NC) clusters. The nanocrystals were chemically synthesized and located inside a metal trench for efficient SPP generation. Second, an optical nano-antenna is presented by utilizing magnetic dipole radiation (instead of electric dipole radiation) as a feed element based on weak Babinet's principle. Different from rod-type optical Yagi-Uda antenna, slot-type antenna shows different optimization principle based on surface plasmon coupling rather than photonic coupling between antenna elements. These devices would provide a platform for future integrated-nanophotonics-based IT technology.

[1] R. Zia, J. A. Schuller, A. Chandran, and M. L. Brongersma, Mater. Today **9**, 20 (2006).
[2] E. Ozbay, Science **311**, 189 (2006).

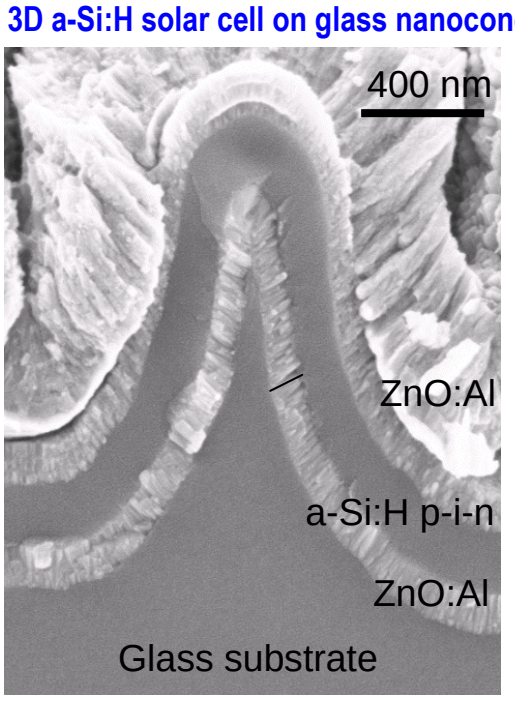
Three-dimensional nanostructures for photovoltaic applications

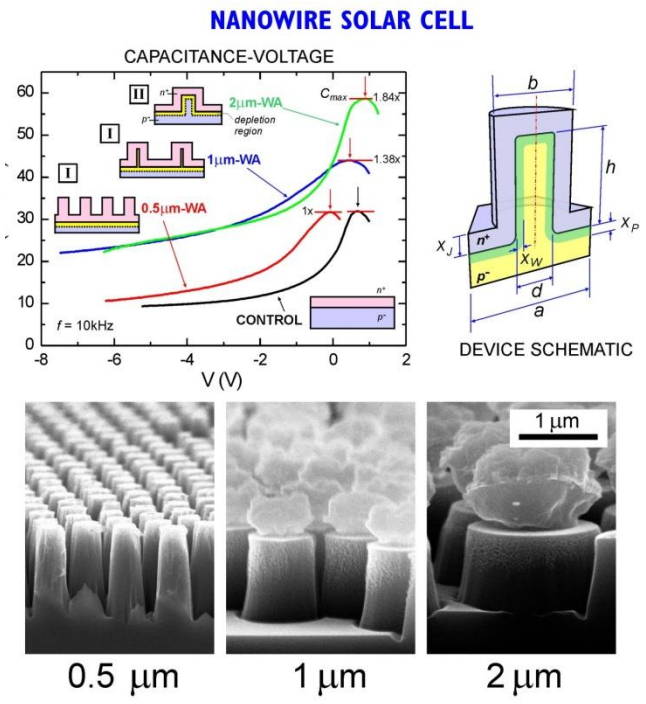
Jeehwan Kim,[2] Oki Gunawan,[2] Byungha Shin,[1,2] Jae-Woong Nah,[2] George Tulevski,[2] Augustin Hong,[2] Devendra Sadana,[2] Supratik Guha[2]

[1] *Department of Materials Science and Engineering, KAIST, Daejon 305-701, Korea*

[2] *IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, U.S.A.*

Three-dimensional (3D) solar cells have attracted great attention over conventional two-dimensional planar solar cells because of their potential output efficiency improvement through enhanced light absorption and collection efficiency. In this talk, I will present two examples of a litho-free method of forming 3D arrays of nanostructures—nanocones and nanowires—for photovoltaic applications. In the first example, we employed self-assembled Tin (Sn) nanospheres as an etch mask. Etching through the self-assembled Sn nanospheres with a broad size range allows for patterning glass substrates into glass nanocones with various dimensions. The performance of a-Si:H solar cell p-i-n stacks built on the 3D-structured glass will be presented in comparison to that of planar solar cells. In the second example, we demonstrated technologically-viable wire-array solar cell fabrication using microspheres lithography. I will present the basic concepts, experimental realization and electrical characteristics of Si solar cells based on this nanostructure.





A facile synthesized 3D silicon nano membrane for lithium ion anode materials

Fan Xia, Jung Min Lee, and Won Il Park
Division of Material Science and Engineering, Hanyang University, Seoul, 133791, Korea
E-mail : wipark@hanyang.ac.kr

Silicon (Si) is of the largest known theoretical capacity (about 4200 mAh/g) that makes it one of the most promising candidate for the anode materials in lithium ion batteries. However, volume expansion up to as much as 400% during the reaction with Li caused particle pulverization and fracture, resulting in rapid capacity fading. In this work, we propose a facile method to synthesis a novel Si membrane structure with good mechanical strength and three-dimensional configuration that is capable of accommodating large volume changes associated with lithiation in batteries applications. In specific, the cycliability and rate capability are promoted based on the merits of this membrane nanoarchitecture, that is, pre-defined interior spaces within the capped hexagonal nanowalls as well as the exterior spaces between them can effectively accommodate the reversible volume change. In addition, the underline layer not only interconnects the current collectors but also clamps the end of every hexagonal nanowall so that it ensures robust electrical and mechanical connection. Additionally, such a Si membrane can be transferred anywhere, which makes its latent functions to be exploited in the following days.

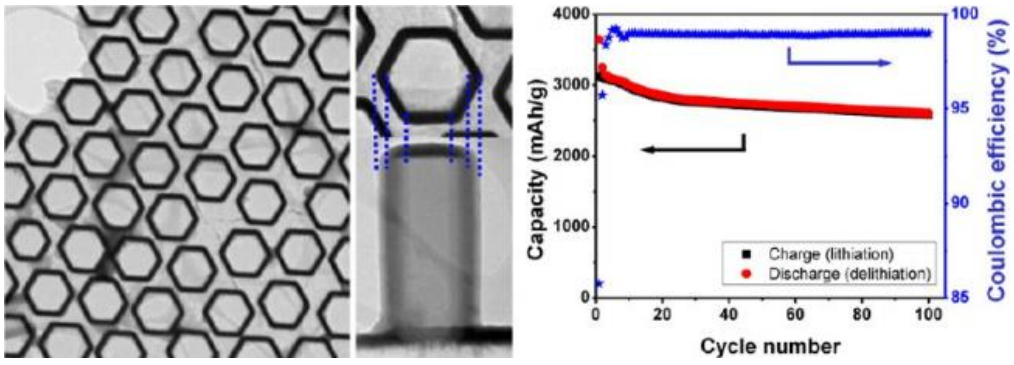


Fig 1. Si nano membrane and its electrochemical test data

Write-traffic-aware cache management for phase-change memory*

SeunghoonYoo[1], Eunji Lee[2], and Hyokyung Bahn[3]
[1]*Korea Air Force Academy,* [2] *Samsung Electronics,* [3]*Ewha University*
E-mail: bahn@ewha.ac.kr

Phase-change memory (PCM) is anticipated to be adopted as main memory of computer systems, but it has some weaknesses such as long write latency and limited endurance. We present a novel cache management policy for PCM memory by the fine-grained dirtiness management of a cache block. Our policy keeps track of the dirtiness of a cache block at the granularity of a cache line and replaces blocks with less dirty lines preferentially. This technique, which we call LDF (less dirty first), is effective in reducing write traffic to PCM significantly by replacing blocks incurring small writes. Nevertheless, LDF does not degrade the cache performance as it is incorporated into existing replacement policies aiming at reducing cache misses. Specifically, we incorporate LDF into two well-known replacement policies, NRU (not recently used) and RRIP[3] (re-reference interval prediction), which have good abilities in estimating the re-reference likelihood of cache blocks. LDF maintains a dirty bit for each cache line to quantify the expected write traffic when evicting a block. LDF sets the reference bit[4] of a *block* to 1 when the block is accessed, and it also sets the dirty bit of the referenced *line* when the access is write. The reference bits of all blocks in the cache are cleared periodically as is done by NRU. In order to reduce the number of cache misses, LDF restricts victim candidates to those blocks with the reference bit of 0. To reduce the write traffic as well, LDF checks the dirty bits of these candidate blocks and selects the block with the minimum number of dirty lines as a victim block. This policy allows blocks referenced recently to remain in the cache, while reducing the write traffic by evicting a block that does not incur much PCM write. Fig. 1 shows the PCM write traffic of LDF relative to NRU when SPEC CPU2006 is used. LDF reduces the write traffic by 25.5% on average and up to 51.6% compared to NRU. Fig. 2 shows the average memory access time of LDF in comparison with NRU. The performance degradation of LDF is very small (less than 1% for all cases). LDF also extends the lifetime of PCM by 36.2% on average. Similar results were observed when LDF is adopted to RRIP.

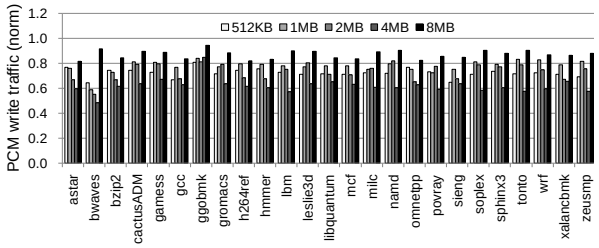


Fig. 1 Write traffic of LDF relative to NRU

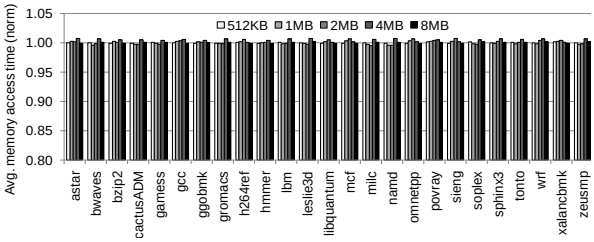


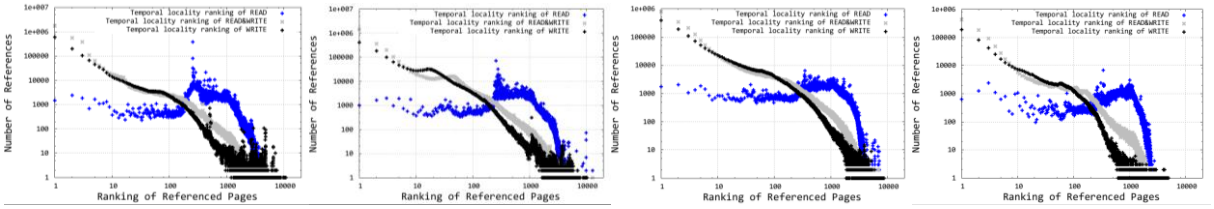
Fig. 2 Avg. mem. access time of LDF relative to NRU

* This work was supported by the IT R&D program MKE/KEIT (No.10041608, Embedded System Software for New-memory based Smart Devices) and the National Research Foundation (NRF) grant funded by the Korea government (No. 2011-0028825).
[3] A. Jaleel et al., "High Performance Cache Replacement Using RRIP," ISCA, pp. 60-71 (2010).
[4] If RRIP is used, multiple reference bits are set. (eg., 2-bit RRIP sets the bits to 11 in this case.)

Characterizing Memory References for Smartphone Applications

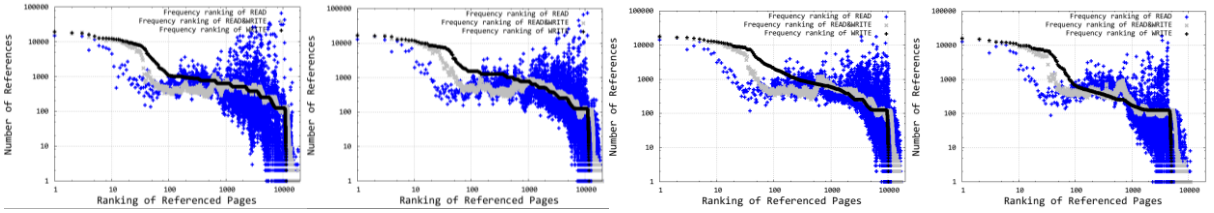
Soyoon Lee and Hyokyung Bahn
Department of Computer Science & Engineering, EWHA Womans University, Seoul 120-750, Korea
E-mail : bahn@ewha.ac.kr

As smartphones support a variety of applications and their memory demand keeps increasing, design of an efficient memory management policy becomes imporant. In particular, as nonvolatile memory (NVRAM) technologies such as PCM and STT-MRAM have emerged and will be adopted in smartphones in the next few years, write references in memory should be carefully managed. This is due to long write latency and/or large energy consumption during write operations in NVRAM. For the deep understanding of memory access features in smartphones, this paper performs comprehensive analysis of memory references for various smartphone applications. Specifically, we focus on the estimation of future write references by quantifying the effects of recency and frequency properties. Through this analysis, we found three noticeable phenomena. First, in terms of recency, exploiting both read and write histories performs the best in estimating future write references. Second, in terms of frequency, exploiting write history alone performs the best in estimating future write references. Third, except for uppermost a few hot pages, frequency is a better estimator than recency in predicting future write references. Through this analysis, we expect that an efficient memory management policy for smartphones can be designed[1].



(a) angrybird (b) mx player (c) youtube (d) facebook

Fig. 1. Number of write references that occur versus recency ranking of read, write, and total references.



(a) angrybird (b) mx player (c) youtube (d) facebook

Fig. 2. Number of write references that occur versus frequency ranking of read, write, and total references.

[1] This research was supported by Basic Science Research Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Education (2013060548).

Page caching of Web browser using NVRAM

Taeho Nam and Taeseok Kim
Department of Computer Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail : thn7440@gmail.com

Non-volatile random-access memory (NVRAM) is a kind of memory that retains its information when power is turned off [1]. Many studies about NVRAM was focused on system on chip (SoC), operating system and etc. We will study NVRAM focused on application, especially web browser which is the most used by the people. The wide prevalence of NVRAM will change the modern computer architecture. The study will give a useful method for executing web browser on the changed architecture. Fig 1 shows the general process that a web page is rendered by web browser. After loading some HTML and CSS from the Internet, web browser parses the HTML and CSS as a DOM tree and style rules respectively. Then the styles are applied to the elements in the DOM tree by the "style formating" process. A data structure called a render tree can be obtained through the process. Next, the render tree goes through a "layout" process. This means giving each node exact coodinates where it should appear on the screen. Finally, each node in the render tree is rendered to the screen by the "painting" process. Outputs such as DOM tree and render tree are usually kept on DRAM, but we can expect some advantages by caching them on NVRAM. There are three possibilities to cache data in the general web page rendering process. One extreme is caching render tree immediately after layout process. However, this cache is invalid even if only the window size changes. Other extremes are caching DOM tree and render tree. These caches are effective for a web page do not changes frequently such as web applications. We will propose a scheme that caches render tree rather than DOM tree into NVRAM. By doing so, Already browsed web pages can be re-rendered and unfinished activities on the pages can be continued. In addition, web page loading time can be reduced by omitting the loading, parsing and style formatting process for rendering web pages.

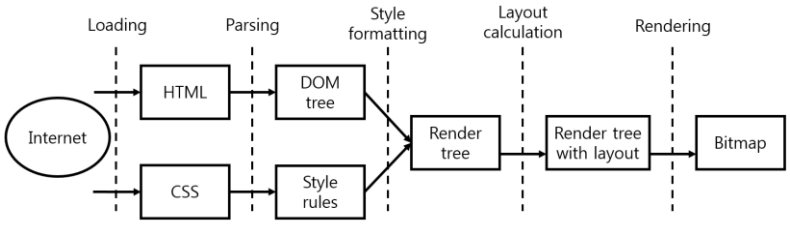


Fig 1. General web page rendering process.

[1] E. Lee, H. Bahn, Sam H. Noh, "Unioning of the Buffer Cache and Journaling Layers with Non-volatile Memory." (2013)
[2] Baron, D. "Faster HTML and CSS : layout engine internals for web developers." (2008)

Efficient Metadata Management Method for Flash Memory based Filesystem using BPRAM

Jinsoo Yoo, and Youjip Won
Department of Software Engineering, Hanyang University
E-mail : {jedisty | yjwon}@hanyang.ac.kr

A number of work suggested to use Byte Addressable NVRAM (BPRAM) to reduce the mount latency of NAND Flash based file system. CMFS [1] which is a byte addressable NVRAM filesystem based on YAFFS2 [2] saves compressed metadata (checkpoint) for mounting filesystem in BPRAM. We attach 8MByte FRAM which is a type of BPRAM to the memory extension pin on SMDK2440 embedded board. The overall structure is illustrated in Fig 1. We measure mount time of CMFS and YAFFS2 in various partition size which is shown in Fig 2. The partition size of NAND Flash memory is increased from 50Mbyte to 100Mbyte with no data. We assume that checkpoint is valid and is used for mounting filesystem. When the partition size is bigger than 70MByte, the mount time of CMFS is lower than that of YAFFS2. Although there is checkpoint decompression overhead, CMFS can reduce the mount time by reading checkpoint from the FRAM. When the partition size is 100MByte, the mount time of CMFS is reduced by 16%.

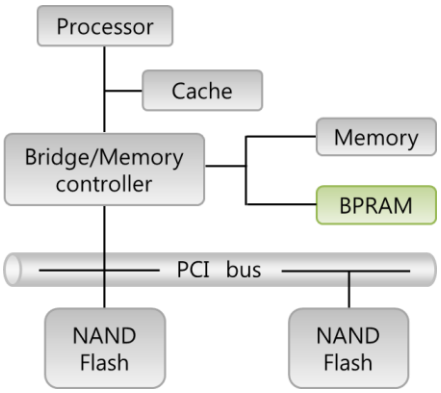


Fig 3. Hierarchical Storage Organization

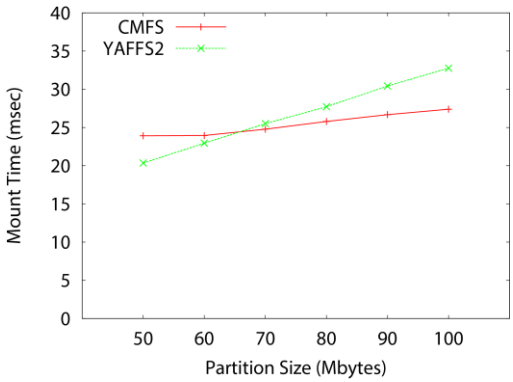


Fig 4. Mount Latency

[1] Quan Taizhong, Jinsoo Yoo, Jaemin Jung, Youjip Won, "Addressing Scalability and Consistency Issues in Hybrid File System for BPRAM and NAND Flash", 7th IEEE International Workshop on Storage Network Architecture and Parallel I/O (SNAPI 2011), Denver, Colorado, USA, May 25, 2011
[2] Aleph One Limited, "Yet Another Flash File System", http://www.yaffs.net/

Single Crystalline Ge Heteroepitaxy on Hastelloy Substrate via Laser-induced Melting and Solidification

Yong-Hoon Son, Sangsoo Lee, Euijoon Yoon
Department of Materials Science and Engineering, Seoul National University, Seoul 151-747, Korea
E-mail : sonyh0325@snu.ac.kr

Since the advent of Si on insulator (SOI) or Si on sapphire (SOS) devices, there have been ever-increasing attempts for acquiring the greater single crystallinity of Si. Accordingly, over the last few decades the microelectronics community has continuosly provided the various methods that enable to form the single crystalline Si with simple and cheep procedures. One way to form the SOI quality single-crystal Si is to use the melt-mediated recrystallization with the laser irradiation or the halogen heating source radiation. While further single crystallinity may be possible especially in utilizing substrate as a seed during melting and solidification, additional integration stepes such as lithography processes or limitations of applicable devices need to be necessary granted [1-2].

In this paper, laser-induced recrystallization of Ge on metal hastelloy substrate was performed with (100) biaxially textured metal oxide layers which served as a seed for Ge epitaxial growth during melt-mediated recrystallization. The biaxially textured metal oxide layers were sequentially deposited on hastelloy substrate in order for the lattice-matched system with Ge. The extent of melting depth of Ge was monitored by an in-situ transient reflectivity beam system. The complete melting of Ge layer led to (100) epitaxial growth from underlying textured metal oxide such as CeO_2. The crystallinity of epitaxially grown Ge was investigated by TEM, EBSD and RAMAN spectroscopy. Experimental details will be shown later.

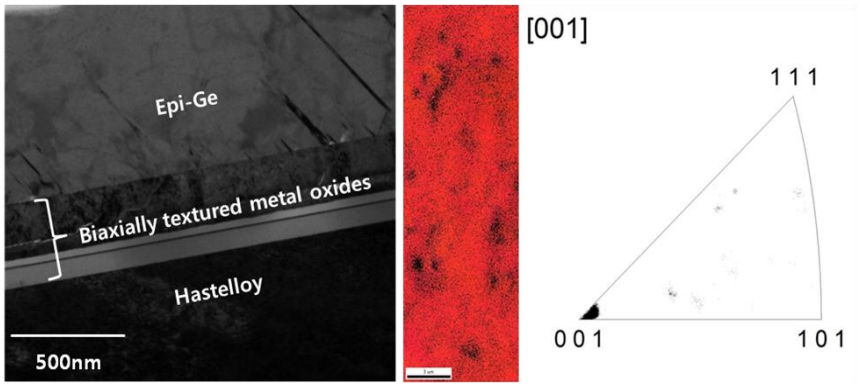


Fig 1. TEM microscope image and EBSD data of epitaxially grown Ge

[1] Y.-H. Son, S. J. Baik, S. Jeon, J.-W. Lee, G. Hwang, Y.G. Shin, E Yoon, IEEE Trans. on Elec. Dev. 58, 3863 (2011)
[2] Y.-H. Son, S. Lee, K. Hwang, S. J. Baik, E. Yoon, JSS, 2. 230 (2013)

Seed Shape Dependence of Ingot Crystalline Characteristics in Single-Crystal Sapphire Ingot Grown by Kyropoulos Method

Jun-Seong Park, Il-Hwan Kim, Gon-Sub Lee, and Jea-Gun Park*
Advanced Semiconductor Materials and Device Development Center,
Department of Electronics and Communication Engineering, Hanyang University, Seoul 133-791, Republic of Korea
E-mail : parkjgl@hangyang.ac.kr

Single crystal sapphire has been an important material for opto-electronics due to strong physical property, high chemical stability, good light transmission, and good electrical insulation. However, the difficulty in the growth of high quality sapphire ingot requires huge time and production cost. Therefore, we described the influence of seed shape on the heat transfer and fluid flows in order to develop a large diameter pure sapphire ingot grown with a Kyropoulos method. Numerical parameters, Al_2O_3 melt convection, temperature distribution in ingot grower, consumption of heating power, melt/crystal interface shape, and stress distribution were tested by varying a seed diameter and a length. The previously simulated results suggested that the increase in a seed diameter led to larger temperature gradient and distribution of temperature gradient at the ingot center. In addition, the increased seed length induced smaller distribution of temperature gradient, interface deflection and consumption of heater power. In this work, we report the influences of seed ring shape on crystal ingot by performing computational simulation, along with the ingot crystalline characteristics of single-crystal sapphire ingot grown by a Kyropoulos method.

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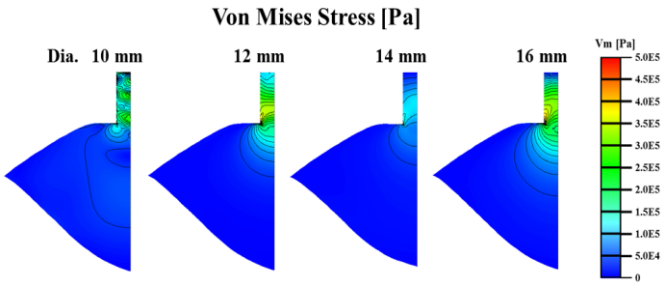

Fig 1. Analysis of Crystallization Front Shape and Von Mises Thermal Stress

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Strained Si:C Epi 층에서 Dopant 가 Carbon 고용도에 미치는 영향 분석

Taeone Youn[a)], Taekwon Lee[a)], Jaegeun Oh[b)], Juhee Lee [a)], Sujin Kong [a)], Won Kim [a)], and Hojoung Kim [a)]

Analysis Team[a)], NMProcess S-Team[b)], SKhynix, 2091 Gyeongchung-daero Bubal-eub Icheon-si Gyeonggi-do, Korea

E-mail : taeone.youn@sk.com

메모리 소자의 고집적화에 따른 구동 전류 감소를 극복하기 위해 격자 상수가 Si 보다 작은 C 원소를 source/drain 에 주입하여 strained nMOS 를 형성하였다[1]~[3]. Strain 의 형성 정도는 Si 과 치환되는 C 의 고용도 (Solubility) 에 의해 결정되므로 이를 평가하기 위해 High Resolution X-ray Diffraction (HR-XRD) rocking curve 으로 측정하였으며 실제 구동 전류 측정 결과와 비교하였다. C 고용도는 dopant 를 추가 주입하지 않은 경우가 추가 주입한 조건 대비 약 3.7 배 높으며 구동 전류도 증가하는 것으로 나타났다. 이는 추가 주입된 dopant 가 C 보다 Si 내 고용도가 높아서 후속 열 공정 시 Si 격자에 위치한 C 원자를 침입형 (interstitial) 위치로 빼냄으로써 C 고용도가 낮아진 것으로 판단된다.

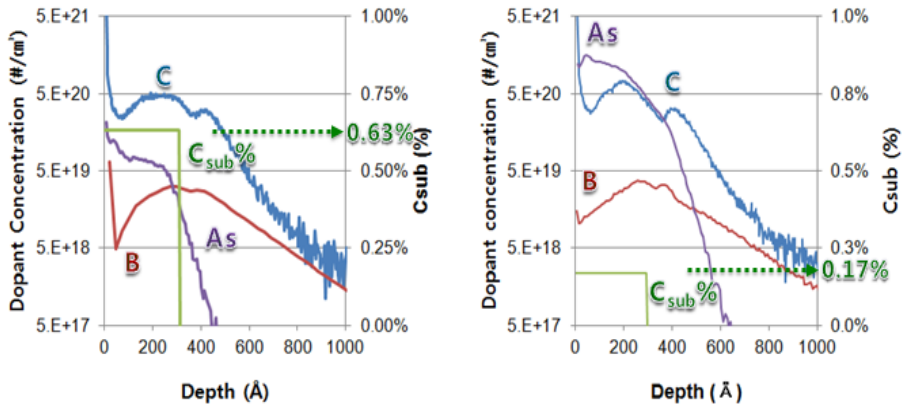

Fig 1. As 추가 주입 전후의 치환형 Carbon 의 고용도 비교

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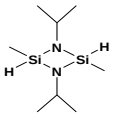
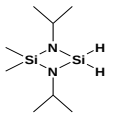
Plasma Enhanced Atomic Layer Deposition of Low Temperature Silicon Oxide Using New Cyclodisilazane Structure Precursors

김성기, 양병일, 장세진, 김종현, 김도연, 조성우, 석장현, *이상익, 김명운
대전광역시 대덕구 대화로 132 번길 142 ㈜디엔에프
E-mail: sgkim@dnfsolutin.com, *silee@dnfsolution.com

반도체 소자 제조공정에서 산화규소(SiO_2) 박막은 gate oxide, field oxide, pad oxide, masking oxide, interlayer dielectric (ILD), capacitor dielectric, tunneling oxide 등의 다양한 용도로 사용된다.[1] 최근 반도체 소자의 초미세화에 따라 점차 공정온도 측면에서 문제점이 지적되고 있어, 각각의 반응 기체들을 순차적으로 펄스 형태로 공급하여 기판표면에서 자기제한적인 (self-limiting) 표면 반응을 통해 박막을 형성하는 ALD 방법을 적용하면 박막의 두께 균일도 및 물성을 향상시키고 공정 온도를 낮추게 되어 반도체 소자의 특성을 향상시킬 수 있다.[2,3] 특히 매우 얇은 두께에서 우수한 물성 및 step coverage가 요구되는 gate의 spacer의 경우에 매우 효과적인 적용이 기대된다.[1] 더욱이 플라스틱을 기판으로 사용하는 플렉시블 (flexible) 디스플레이 및 집적회로 소자 분야에서는 플렉시블한 특성을 유지하기 위해서 매우 얇은 두께로 수분의 확산을 막을 수 있는 고밀도의 산화규소(SiO_2) 확산방지막 (moisture barrier)이 필요하다.[4,5] 따라서 저온에서 고밀도 산화규소 박막을 형성하기 위해 플라즈마강화 원자층증착 (Plasma Enhanced Atomic Layer Deposition : PEALD)기법을 사용하여 신규한 사이클로다이실라잔 (cyclodisilazane) 형태의 실리콘 전구체와 O_2/Ar 플라즈마 사용하여 실리콘 기판 위에 ALD 특성을 나타내는 산화규소 박막을 증착 하였다. 사이클로다이실라잔 화합물은 Si-N 결합을 가지는 안정한 사각 고리 화합물로 치환 그룹에 따른 화합물의 대칭과 비대칭성을 조절하여 반응성을 조절할 수 있는 장점을 가지고 있으며, 이를 통해 박막 성장 속도 및 형성된 박막의 물성에 영향을 미칠 수 있음을 확인 하였다.

(a)

	CSN-2	CSN-3
Structure		
Chemical name	1,3-Di-isopropylamino-2,4-dimethylcyclosilazane	1,3-Di-isopropylamino-2,2'-dimethylcyclosilazane
Molecular weight	202.44 g/Mol	202.44 g/Mol
Boiling Point	175℃	175℃

(b)

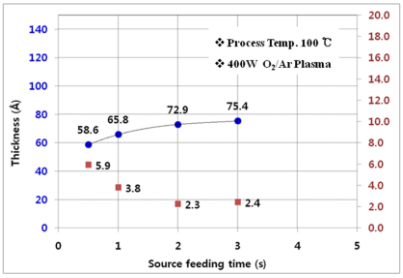


Figure 1. (a) Chemical structures and properties. (b) Thickness and uniformity data of CSN-3 by feeding time.

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Electrical Properties of ALD La_2O_3-Capped High-K/Metal Gate Device

Donghwan Lim[1], Woosuk Jung[1], Moon-Suk Choi[1], Dohyung Kim[1], Youngil Gil[1], Chulwon Chung[2] and Changhwan Choi[1,*]
[1]Division of Materials Science and Engineering, Hanyang University, Seoul, 133-791, Republic of Korea
[2]Department of Energy Engineering, Hanyang University, Seoul, 133-791, Republic of Korea
*E-mail: cchoi@hanyang.ac.kr

Since high-k/metal (HKMG) gate technology was successfully implemented into manufacturing logic devices, HKMG technology and its derivative have been also adopted into other applications such as dynamic random access memory (DRAM). However, device requirements for peripheral transistor in DRAM are not as strict as logic transistor. Nonetheless, HKMG technology is still challenging to achieve higher performance and low power consumption for advanced DRAM. In order to attain low and symmetric threshold voltage (V_{TH}), various materials and process integration schemes were proposed. From cost perspective, gate-first (GF) is still favorable for DRAM. However, post high temperature thermal step during Metal-Insulator-Metal (MIM) capacitor process significantly affects on HKMG gate stack in peripheral transistor leading to device performance degradation (i.e., V_{TH} roll-off, increased inversion layer thickness(T_{inv})) because capacitor is processed later after transistor formation. Therefore, material-oriented solution was reported. Among them, it was reported that Group IIA in periodic table such as La can induce negative flat-band voltage shift (i.e., lower V_{TH}) for GF-nMOS device because diffused La elements through high-k gate dielectric during thermal process cause dipole formation at the Si substrate and interfacial layer.

In this study, we have studied ALD La_2O_3 capping on the high-k gate dielectric to tune work-function, which is compatible with GF nMOS device. Two different La precursors - ① $La(fAMD)_3$ and ② $La(thd)_3$ - were chosen for ALD capping layer. Deposition temperatures were 175℃ and 275℃ for ①, ② precursors, respectively. It is shown that both precursors induce more V_{FB} shift as increasing capping thickness, but more shift is observed with $La(fAMD)_3$ (Figure 1). At 1.5 nm thickness, $La(fAMD)_3$ causes about 200 mV while $La(thd)_3$ 130mV. V_{FB} shift behaviors on Si-containing HfO_2 gate dielectric (i.e., $HfSiO_x$ and HfSiON) are similar to HfO_2 only case (Figure 2). EOT is scaled down to 1.15 nm and 1.25 nm for ①, ② precursors, respectively. Interface state density (D_{it}) increases with increasing ALD capping regardless of precursor types (Figure 3). However, $La(fAMD)_3$ show lower D_{it} than $La(thd)_3$. Charge trapping characteristics are compared by time-dependent V_{FB} shift during stress. For either 1.1V or 1.6V as for stress voltage, improved charge trapping behavior is shown with $La(fAMD)_3$ (Figure 4). These electrical improvement with $La(fAMD)_3$ aforementioned are attributed to lower deposition temperature, shorter oxidation pulse time, and lower carbon in the precursor matrix compared with $La(thd)_3$.

We investigated V_{FB} shit, EOT scaling and charge trapping on ALD La capped HKMG device. Our result suggests that beside process optimization, precursor is also important to attain improved electrical properties of GF-based nMOS device applications.

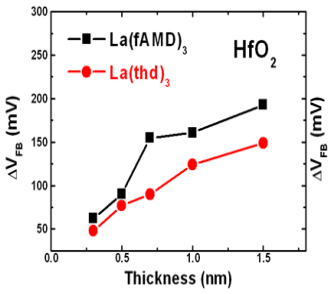

Fig 1. V_{FB} shifts of ALD La capped HfO_2 MOS devices with two different La precursors.

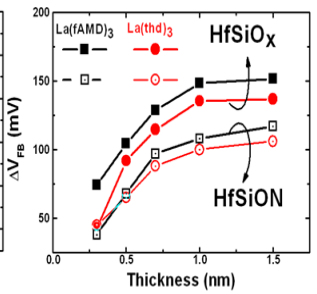

Fig 2. V_{FB} shifts of ALD La capped Si containing HfO_2 MOS devices with two different La precursors.

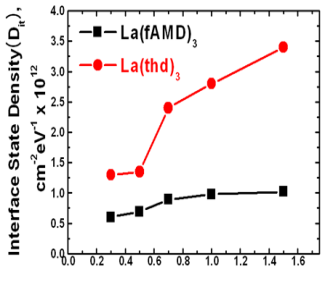

Fig 3. D_{it} shifts of ALD La capped with two different La precursors.

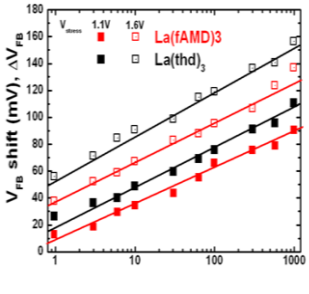

Fig 4. Charge trapping behaviors of ALD La capped with two different La precursors.

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Oxidizing Agent Effects in Atomic Layer Deposition of $Hf_xZr_{1-x}O_2$ Thin Films with High Dielectric Constant

최민정,[1,2] 박형호,[2] 김성근 [1]
[1] *한국과학기술연구원 (Korea Institute of Science and Technology), 전자재료연구센터*
[2] *연세대학교, 신소재공학과*
E-mail : T12541@kist.re.kr

DRAM 은 셀의 동작을 위해 셀의 크기에 관계없이 25 fF/cell 이상의 정전용량을 갖는 커패시터를 요구한다. 최근 DRAM 소자의 고집적화에 대한 요구는 커패시터의 표면적을 지속적으로 감소시켜, 제한된 면적 내에서의 충분한 정전용량 확보가 차세대 DRAM 소자 개발에 가장 큰 걸림돌이 되고 있다. 현재 사용하고 있는 ZrO_2 박막의 경우 tetragonal/cubic 상에서 약 40 의 유전율을 보이나 0.5 nm 이하의 등가산화막두께에서는 누설전류의 급격한 증가로 10 nm 급 차세대 DRAM 커패시터에 적용하기 어려워, 새로운 유전체 개발이 요구되고 있다. 게이트 절연막으로 주로 이용되는 HfO_2 박막은 약 15 정도의 낮은 유전율로 DRAM 커패시터의 유전물질에 적합하지 않는 물질로 알려져 왔으나, 최근 10 nm 이하의 극박막에서 새로운 결정 구조가 발견되었으며, 높은 유전율을 기대할 수 있을 것으로 예측된다. 따라서 본 연구에서는 새로운 결정 구조를 가지는 $Hf_xZr_{1-x}O_2$ 박막을 원자층증착법을 이용하여 형성하였다. 특히 유전박막의 누설전류에 영향을 미치는 산소 공공 농도의 영향을 파악하고자 서로 다른 산화력을 갖는 두 산화제 H_2O 와 H_2O_2 를 이용하여 $Hf_xZr_{1-x}O_2$ 박막을 형성하였다. 또한 각 산화제를 이용하여 성장한 박막의 물리적, 화학적 성질을 평가하고, 나아가 커패시터를 제작하여 전기적 특성 또한 비교하였다.

Stabilization of negative capacitance in ferroelectric thin films

Yu Jin Kim, Min Hyuk Park, Han Joon Kim, Tae Hwan Moon, and Cheol Seong Hwang
WCU Hybrid Materials Program, Department of Material Science & Engineering and Inter university Semiconductor Research Center, Seoul National University, Republic of Korea,
E-mail : uzinknig@snu.ac.kr

Although ferroelectric switching is one of the most significantly researched topics in solid state physics, it is still an intriguing research topic for modern electronic devices. One of the most arguable comments reported recently is the involvement of the negative capacitance (NC) effect in the ferroelectrics in a dielectric (DE) – ferroelectric (FE) stacked system [1]. The NC effect of the FE can be stabilized by the DE, but can also be destabilized by the formation of FE domains [2]. Even though their experimental verification at high temperature has been reported [3], direct observation of negative capacitance at room temperature is yet to be made. In this research, therefore, the authors took a completely different approach to achieve NC in $Pb(Zr,Ti)O_3$ (PZT) layers at room temperature by invoking a method that makes the polarization of FE *mono-stable* but still switchable by applying electric field. First, we proposed that mono-stable and reversibly switchable polarization could be achieved where trapped charges (Q_t) are involved at the DE/FE interface, which could be derived from the well-established Landau-Ginzburg-Devonshire theory. As a result, infinite capacitance could be observed at a certain thickness condition of DE/FE structure, but the maximum achievable charge density was limited $2P_r$ of the FE layer irrespective of the thickness of DE and FE layers. Based on the theory, we conducted experiments as follows. Thin DE layer (SiO_2 or Al_2O_3) was deposited on top of the PZT FE layer, and the transient current response of this DE/FE system when a dc pulse voltage was applied was monitored. The capacitance values of the DE/FE system were extracted from the transient current flow, and were compared with the capacitance values of single DE or FE layers which can be estimated from the standard (static) capacitance – voltage measurement. The measured values were higher than that of the single DE or FE layers. Also, the difference in charging capacitor charges between NC mode and non-NC mode of DE/FE capacitor was clearly observed through pulse charging measurement. However, the highly concentrated electric field in DE layer make trapped charge prone to dissipation during NC, which is detrimental to NC effect. Finally, we'll suggest that several approaches to sustainable NC operation.

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Effect of NH_3 Plasma Treatments on Deposition of Nickel Film by Chemical Vapor Deposition

Jingyu Park[1], Heeyoung Jeon[1], Hyunjung Kim[1], Jinho Kim[2], Woochool Jang[2] and Hyeongtag Jeon[1, 2]
[1]*Department of Nano-scale Semiconductor Engineering, Hanyang University, Seoul, 133-791, Korea*
[2]*Department of Materials Science and Engineering, Hanyang University, Seoul, 133-791, Korea*
E-mail : px26@hanyang.ac.kr

Recently, 3-dimensional structures with high aspect ratio have become important in DRAM and multi-stacked flash memory devices. Therefore, source/drain and its contact must be vertically fabricated. In microelectronic devices, metal silicides like $TiSi_2$, $CoSi_2$, NiSi are most used. Among these silicides, NiSi is the most promising material due to its low sheet resistance, low silicon consumption, and low thermal budget. Although PVD (physical vapor deposition) method like sputtering or evaporation is considered to be good method to deposit thin Ni metal, it cannot be used in deep trench structure because of poor step coverage. Thus, the usage of chemical based deposition such as CVD (chemical vapor deposition) or ALD (atomic layer deposition) is inevitable. In this study, we deposit nickel film by CVD and make NiSi by annealing. Characteristics of films are investigated using several analysis equipment such as X-ray sepctroscopy (XPS) field emission scanning electron microscope (SEM), Auger electron spectroscopy (AES), four point probe (FPP), and X-ray diffraction (XRD)

Ni film was deposited on Si substrate by CVD using new Ni precursor (Bis(1,4-di-isopropyl-1,3-diazabutadienyl)nickel, $Ni(iPr\text{-}DAD)_2$) and NH_3 gas as a reactant at 250℃ for 30min. In order to investigate the properties of phase transformation, we annealed the Ni thin films deposited on Si at various temperatures.

Before Ni film deposition, NH_3 plasma pre-teatment was performed to enhance thermal stabilty of NiSi films. We separted the flow rate of NH_3 plasma into three conditions (20, 100, 200sccm) to control the amount of hydrogen and nitrogen molecules. The XPS spectra show that the higher flow rate of NH_3 plasma was used, the large amount of nitrogen atoms were inserted in Si substrate. There were no significant difference in as-deposied Ni films irrespective of the flow rate of NH_3 plasma. The as-deposited Ni films exhibit relatively low sheet resistance around 12 Ω/□ and contain 20% carbon impurities. After annealing 500℃ sheet resistance of Ni films was drastically decreased due to formation of low resistive NiSi phase without respective to NH_3 flow rates. However, NiSi films which NH_3 plasma pre-treated with 200sccm has the lowest sheet resistance overall ranges because this sample exhibit smooth interface without any Si exposed regions. Therefore, nitrgoen atoms were effective to reduce interface roughness of NiSi films.

Analysis of a reaction mechanism of oxide layer removal using reactive gas

Hyuntae Kim[1], Jungsoo Lim[1], Min-Su Kim[1], and Jin-Goo Park[1,2,†]

Department of Bionano Technology, Hanyang University[1], Department of Materials Engineering, Hanyang University[2], Ansan 426-791, Korea

E-mail : jgpark@hanyang.ac.kr

The size of semiconductor device has been reduced; cleaning process is more important in semiconductor fabrication process. To improve device yield reduction, the removal of the various contaminants and control of the surface roughness are very essential. In general, wet cleaning processes have been used in semiconductor cleaning process for removal of thin film layer. In this way, rinse and dry process repeated. Therefore the pattern collapse is generated by high surface tension of cleaning solution and over etching of pattern. [1] For this reason, dry cleaning process is the most promising technique. However, conventional dry cleaning process has some problems such as low selectivity, anisotropy the etching method and surface damage by radiation from plasma. To solve these problems, we studied, to attain high removal efficiency and high selectivity reactive gas was created by plasma. Particularly, for the removal of oxide layer, we adopted plasma dry cleaning process instead of buffered oxide etchant (BOE) wet cleaning process. [2] The designed process was achieved high removal rate of oxide layer by using NH_3/NF_3 gas. The reaction mechanism and oxide layer surface were analyzed by optical microscopy, SEM, and FT-IR respectively. In this study shows, the removal efficiency mainly depends on the reaction mechanism and effect of the product.

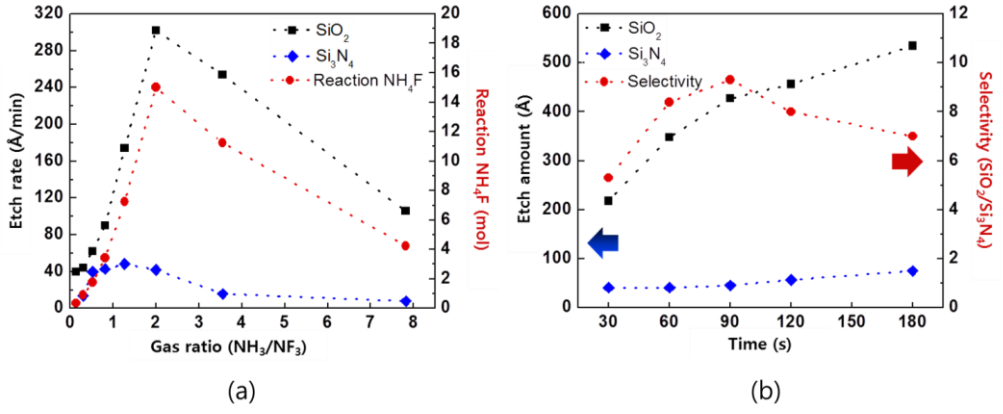


Fig 1. Result of (a) etch rate with NH_3 gas ratio and (b) selectivity of Si_3N_4 and SiO_2

[1] H. Nishino, et al, J.Applied Physics., 74 (2), pp1345-1348 (1993)

[2] B. Du Bois, et al., Dutch National Sensor Conference, pp.131-136 (2001)

Graphene-silver nanowire hybrid structure as a transparent and current spreading electrode in ultraviolet light emitting diodes

Tae Hoon Seo, Ah Hyun Park, Bo Kyoung Kim, GangU Shin, Seul Bee Lee, Gun Hee Lee, and Eun-Kyung Suh*

School of Semiconductor and Chemical Engineering, Semiconductor Physics Research Center (SPRC), Chonbuk National University, Jeonju 561-756, Korea

*E-mail : eksuh@jbnu.ac.kr

The indium tin oxide (ITO) layer has appeared to be increasingly problematic due to limited transparency in the ultra-violet (UV) region. However, graphene has been attracting much attention owing to its physical properties such as a high intrinsic mobility and high transparency in the UV ranges [1]. We report a device that combines graphene film and Ag nanowires (AgNWs) as transparent and current spreading electrodes for UV light emitting diodes (LEDs) with interesting characteristics for the potential use in the deep UV region. The current-voltage (I-V) characteristics and electroluminescence (EL) performance show that graphene network on AgNWs well-operates as a transparent and current spreading electrode in UV LED devices due to the reduced sheet resistance and the effective current spreading. This result shows that graphene network on AgNWs can provide efficient current diffusion pathways and are able to provide injected current to the active junctions of LED through *p*-GaN layer.

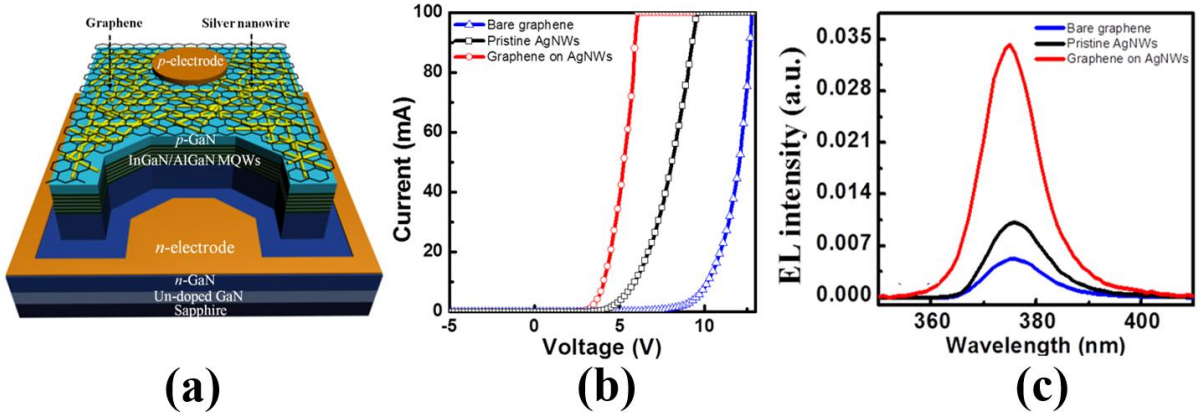


Fig 1. The schematic diagram of UV LEDs with graphene-silver nanowire hybrid structure, I-V curves and EL of GaN-based LEDs with graphene electrode, pristine AgNWs, and graphene-silver nanowire hybrid structure.

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov: Science **306** 666 (2004).

Tapered laser diode with linear effective-refractive-index variation waveguide

Duchang Heo*[1], Seongche Jeon[1], Yun-Seok Kwak[2], Seong-Wook Ryu[2] and Tae-kyung Kim[2]
[1]*Korea Electrotechnology Research Institute, Ansan 426-170, Korea*
[2]*QSI laser Co., Ltd., Choenan, 331-836, Korea*
E-mail : dcheo@keri.re.kr

Recently, high power laser diodes (HPLDs) have enlarge the field of applications from industry to medicine. There are two kinds of HPLDs; one is bread area LD and the other is tapered LD. Taperd LD has more stable beam profile by maintining the stable single mode profile from single mode ridge section [1]. The tapered LDs are categorized into gain-guided and index-guided tapered strcuture for from a few to a few decade W and ~ a few hundred mW respectively. In this work, we propose the novel design concept of index-guided taper section in the index-guided tapered LDs. Figure 1 shows the comparison with both linear geometric tapered structure and linear effective-refractive-index variation structure, which are desinged by calculating effective refractive inex of multilayer using Helmholtz equation [2]. Figure 2 shows the proposed linear effective-refractive-index variation waveguied structure and stable near-field image and far-field pattern. The linear effective-refractive-index variation waveguide is helpful to make more stable optical mode profile by desiging waveguide in the point of view of beam propagation.

(a)

(b)

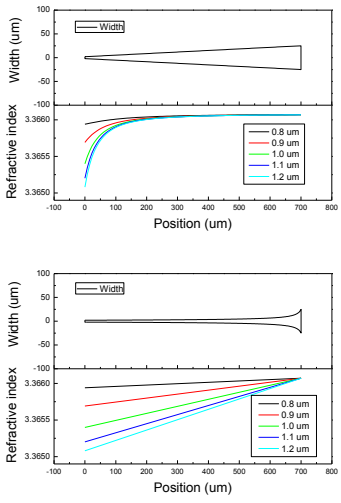


Figure 1 (a) conventional tapered structure (b) proposed linear effective-refracive-index variation structure

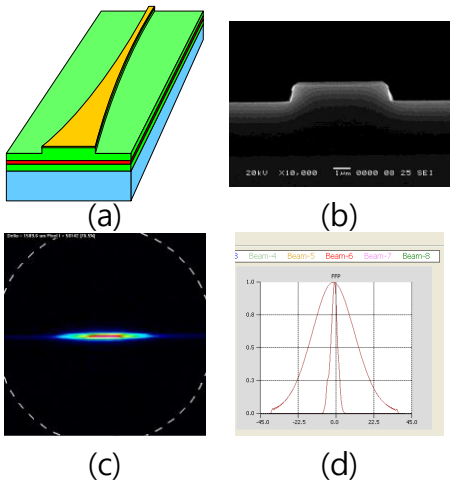


Figure 2 (a) device schematics (b) SEM image of front facet (c) near-field image (d) far-field pattern

[1] D. Heo, I. K. Han, J. I. Lee and J. Jeong, *J. Kor. Phys. Soc.*, 43, 352 (2003)
[2] D. Heo, J. D. Song, I. K. Han, W. J. Choi, and Y. T. Lee, *IEEE J. Quantum Electron.* 49, 24 (2013)

Current Crowding Improvement of InGaN-based Blue Light-Emitting Diodes by Modifying Metal Contact Geometry

Garam Kim, Jang Hyun Kim, Euyhwan Park and Byung-Gook Park
Department of Electrical Eng. and Computer Sci. (EECS), Seoul Nat. Univ., Seoul 151-742, Korea
E-mail : garami21@hanmail.net

InGaN-based blue light emitting diodes (LEDs) are the most promising candidates to replace the conventional fluorescent lamp in the market of the back light unit of display and the general lighting application, due to its advantages such as relatively long lifetime and high energy efficiency. In order to improve the internal quantum efficiency and the negative-voltage Electro-Static Discharge (ESD) problem of InGaN-based LEDs, it is important to analyze the effect of the current crowding problem [1,2]. In this paper, by using photon emission microscope and thermal emission microscope measurement, we confirmed that the electric field and the current of the InGaN-based LED sample are crowded in specific regions where the distance between p-type metal contact and n-type metal contact is shorter than other regions. To improve this crowding problem of electric field and current, modified metal contact geometry having uniform distance between the two contacts is proposed and verified by a numerical simulation. It is confirmed that the proposed structure shows better current spreading, and for this reason, higher internal quantum efficiency and reduced reverse leakage current can be obtained.

Acknowledgement : This work was supported by Samsung Electronics Co., Ltd. and the Center for Integrated Smart Sensors funded by the Ministry of Science, ICT & Future Planning as Global Frontier Project (CISS-2012M3A6A6054186)

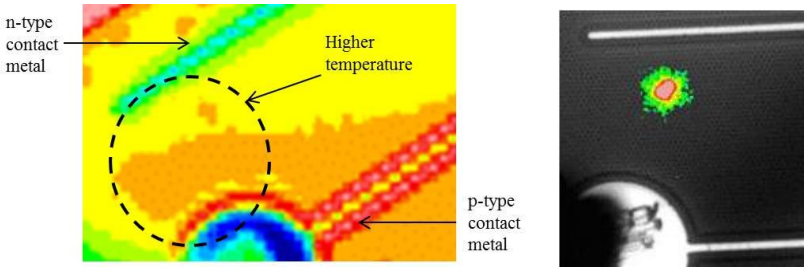


Fig 1. The surface temperature distribution of the prepared LED sample and the light emitting pattern of the breakdown sample.

[1] V. K. Malyutenko, S. S. Bolgov, and A. D. Podoltsev, Applied Physics Letters 97 (25), 251110 (2010).
[2] S. Hwang and J. Shim, IEEE Transactions on Electron Devices, 55 (5), 1123 (2008).

Role of V-defect on internal quantum efficiency of InGaN LEDs

Yong-Hee Cho, Mun-bo Shim, Sangheum Hwang, Sungjin Kim
Computational Science Group, SAIT, Samsung Electronics, Yongin 446-712, Korea
E-mail : yonghee2.cho@samsung.com

A large number of threading dislocations (TDs) are naturally generated due to the large lattice mismatching between GaN layer and sapphire substrate in GaN based LEDs with acting as non-radiative sinks. V-defects are known to suppress the non-radiative recombination to TDs in the lateral direction of quantum well [1]. Even if V-defects play an important role of enhancing the quantum efficiency in the active layers of InGaN/GaN quantum well, a proper theoretical model can be rarely found. Here we show an unusual three dimensional modeling of quantum well, which can describe both the in- and out-of-plane quantum well. Thus it can accomodate a V-defect and TD system.

As a result, we show that our sophistcated model induces a simple phenomenological relation among the effective non-radiative domain size, carrier density injected, and local V-defect barrier originated from its facets, for explaining the non-radiative recombination. Also, we discuss a V-defect condition for more efficient screening of non-radiative carrier capture.

[1] A. Hangleiter, F. Hitzel, C. Netzel, D. Fuhrmann, U. Rossow, G. Ade, and P. Hinze, Phys. Rev. Lett. 95, 127402 (2005).

Effects of surface damage on Raman spectrum of etched InSb(100) surface

Chulkyun Seok[1], Minkyung Choi[2], Jinwook Jung[1], Sehun Park[1],
Yongjo Park[3], In-Sang Yang[2], and Euijoon Yoon[1,*]
[1]*Department of Materials Science and Engineering, Seoul National University, Seoul 151-742, Korea*
[2]*Department of Physics, Ewha Womans University, Seoul 120-750, Korea*
[3] *Advanced Institutes of Convergence Technology, Suwon 443-270, Korea*
E-mail : eyoon@snu.ac.kr

Recently, Indium antimonide (InSb) has attracted a lot of attention due to its electrical properties such as narrow bandgap and high carrier mobility. For the fabrication of high performance InSb devices, reducing dark current is required. Especially, surface damage induced by plasma etching makes the dark current increase and the device performance degrade. In this respect, a research on the damage-measuring method is required to evaluate the etched InSb surface for the optimization of plasma etching.

In this work, we have examined ion-induced structural damages on the etched InSb surface by Raman scattering for the first time. Ar ions with high energy cause structural damages near the ion-bombarded surface. Such structural changes, undetectable even by AFM, may cause significant alteration in the electronic structure of the InSb surface. Raman scattering measurements for the etched InSb surface show that the splitting between longitudinal optical (LO) and transverse optical (TO) phonon modes are drastically enhanced as the energy of the RF power increase. Furthermore, bombarded ions cause point defects on the etched surface. As a result, the integrated area ratio of I_{TO}/I_{LO} and the FWHM of LO peak are proportional to the applied RF power, which is proportional to the energy of the Ar ions. Our results prove that Raman analyses can characterize the structural damages effectively induced by the energetic Ar ions bombarded onto the InSb(100) surface.

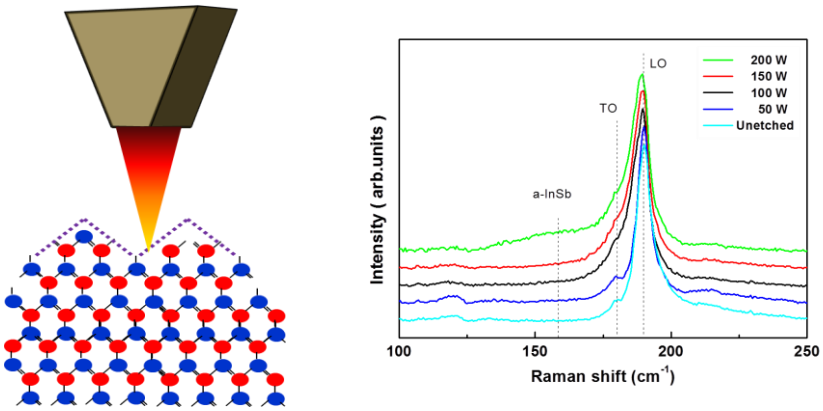


Fig 1. (a) Schematic of Raman measurement (b) Raman spectrum of etched InSb(100) surface

HyperX 구조를 이용한 저전력 256-Radix Crossbar Switch 의 -설계

백승헌, 김재하
서울대학교 전기정보공학부, 반도체공동연구소
E-mail : shbaek@mics.snu.ac.kr

다중 코어 프로세서의 사용 및 그 코어의 수가 늘어나는 추세에 따라, 코어들 사이의 연결선 네트워크를 이루는 핵심 요소인 크로스바 스위치의 포트 수, 즉 radix 를 늘이면서도 지연시간 및 소비전력을 줄여야 하는 필요성이 부각되고 있다. 가장 기본적인 매트릭스 구조의 크로스바 스위치는 radix N 이 증가함에 따라서 지연시간과 소비전력이 N^2에 비례하여 증가하는 문제점이 있고, 이를 해결하기 위하여 기본 구조에 계층 개념을 도입한 구조들이 제안되었으나, 더 향상된 성능이 요구되고 있다.

본 연구에서는 HyperX 네트워크 구조를 크로스바 스위치 설계에 도입하여 지연시간 및 소비전력을 획기적으로 절감한 결과를 소개한다. 그림 1 의 HyperX 구조에서는 전체 네트워크가 지역 네트워크들로 분할되어 있는데, 한 지역 네트워크내의 라우터들은 서로 모두 연결되어 있으나, 다른 지역 네트워크들간에는 등위의 라우터들끼리만 연결되는 성질이 있다. 이 HyperX 구조를 크로스바 스위치에 적용하되, 이에 추가로 다음의 규칙을 도입하면 각 경로의 branch factor 를 줄일 수 있고, 이에 따라 지연시간 및 소비전력의 절감을 이룰 수 있다. 첫째, 전송 순서를 지역 네트워크 내부 이후 외부의 순서로 제한한다. 둘째, 한 네트워크의 여러 입출력 신호를 한 스위치에서 처리하는 대신, 각 신호에 순번을 매겨 같은 순번끼리의 신호들만 동일한 스위치에서 처리하도록 한다. 셋째, 열간의 데이터 이동을 대각선 방향의 이동으로 대체하여 여러 개의 경로를 하나로 병합한다.

표 1 은 제안하는 각 규칙들을 단계적으로 사용하였을 때 CMOS 65 나노 공정에서 설계한 256-radix, 16-bit 크로스바 스위치의 지연시간과 소비전력이 향상되는 시뮬레이션 결과를 보여준다. 기본 구조에 비교할 때, 지연시간은 13.5 배, 소비전력은 5.3 배로 감소하였다.

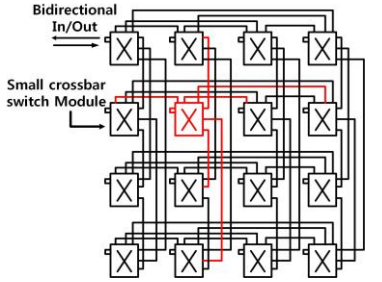


그림 1. HyperX crossbar

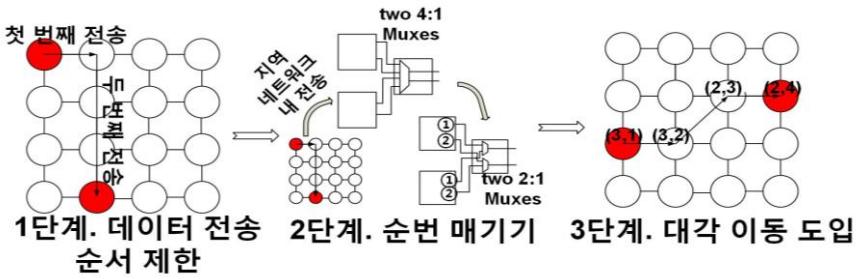


그림 2. 각 규칙 단계의 구현

	delay(ns)	power(mW)
Hyper X	26.26	9.830
전송 순서 제한	9.285	2.884
순번 지정	6.918	1.622
대각 이동	1.195	1.848

표 1. 시뮬레이션 결과

[1] J. Ahn, S. Choo, and J. Kim, “Network within a Network Approach to Create a Scalable High-Radix Router Microarchitecture,” in HPCA, 2012.

[2] J. Ahn, Nathan Binkert, et al., “HyperX Toplogy, Routing, and Packaging of Efficient Large-Scale Networks,” in SC, ACM, 2009.

The new test method for flip-flops

김아름, 박진수, 정건옥, 김민수, 김태형, 김정희, 김용걸, 한상신, 조욱래, 신영민
Samsung Electronics, Giheung-gu, Yongin-si, Gyeonggi-do 446-711, Korea
E-mail : ar83.kim@samsung.com

최근 휴대용 전자 기기의 종류 및 사용량이 증가함에 따라 휴대용 전자 기기의 성능에 대한 관심이 높아지고 있다. 특히 고성능 기기의 구현에 있어 필수 요소인 프로세서의 동작 클락 주파수를 높이기 위해 파이프라인 단의 개수가 늘어나고 있는 추세이다. 이에 따라 클락 동기화 저장 요소 (clocked storage elements)인 플립플롭과 래치의 사용량이 증가하고 있으며, 플립플롭과 래치가 시스템 성능에 미치는 영향 역시 커지고 있다[1].

일반적으로 플립플롭의 성능을 측정할 때 동작(writeablity), 타이밍(Clock-Q/D-Q delay, setup/hold time)을 중요하게 다룬다[2]. 특히 타이밍 측정은 플립플롭의 성능을 결정하는 중요한 요소인데, 그 단위가 ps 로 매우 작아 실리콘으로 만들어진 후 측정하기가 쉽지 않다. 또한 플립플롭은 VLSI 시스템 내에서 여러 가지 로직 게이트로 이루어진 콤비네이션 블록과 함께 사용되고 있다. 따라서 실제 수 백만개의 플립플롭이 사용되는 VLSI 시스템과 유사한 환경에서 플립플롭을 테스트해봄으로써 제품으로 구현되었을 때의 플립플롭의 성능 및 문제점을 미리 예측하는 것이 매우 중요하다. 본 논문에서는 플립플롭이 사용되는 실제 환경과 유사한 대량의 플립플롭을 동시에 테스트 할 수 있는 모듈을 제안하고자 한다. 제안하는 테스트 모듈은 28nm CMOS 공정을 이용하여 설계 및 테스트를 진행하였다.

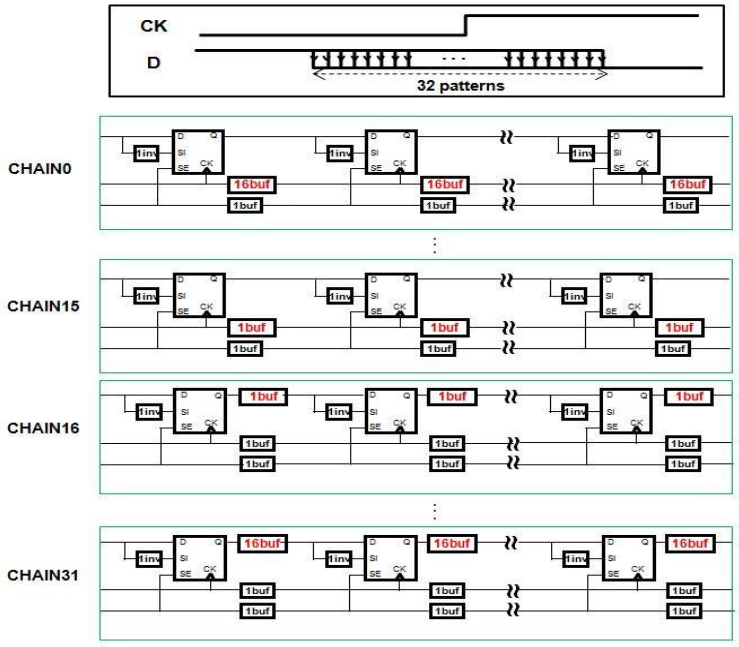


Fig 1. Proposed flip-flop test module

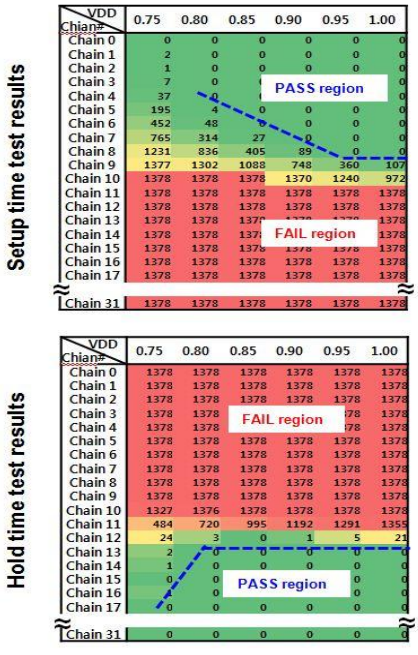


Fig 2. DQ type flip-flop test results

[1] V. G. Oklobdzija, in *Proc. 23rd IEEE Int. Conf. Microelectronics*, vol. 2, pp. 561-568, May. 2002.
[2] V. Stojanovic and V.G. Oklobdzija, *IEEE J. Solid-State Circuits*, vol. 34, pp. 536-548, Apr.1999.

Adaptive Tracking Algorithm of Autonomous Power Management

Soo-Yong Kim[1,2], Chaehag Yi[1], Huijung Kim[1], Keunhwi Koo[2], Sang Woo Kim[2], and Suk Won Kim[1]
[1]*Modem and connectivity Business Team, System LSI Business, Samsung Electronics Co., Korea*
[2]*Department of Electrical Engineering, Pohang University of Science and Technology, Korea*

E-mail : odin.kim@samsung.com

기존의 전력 관리 기법들은 특정 시나리오 상황에서만 유효한 것들이 많다 [1], [2]. 주어진 상황이라 하더라도, 전력 소모를 관측하는 창(window)를 좁혀서 관찰해 보면, 최적화 기법을 통하여 구한 최적의 시간 문턱치(time-threshold level)가 항상 전력 소모의 최소값을 보장하지 못한다.

이러한 문제점을 해결하기 위하여 시간 문턱치의 실시간 보정 기법을 제안한 바 있다[3]. 이 알고리듬은 자율전력관리를 탑재하여, 각 시스템의 전력 모드를 근거로 소비 전력을 측정하고, 다음의 시간 문턱치를 계산하는 법이다. 본 논문에서는 효과적인 시간 문턱치의 실시간 보정 기법의 구조에 대하여 아래와 같이 제안한다.

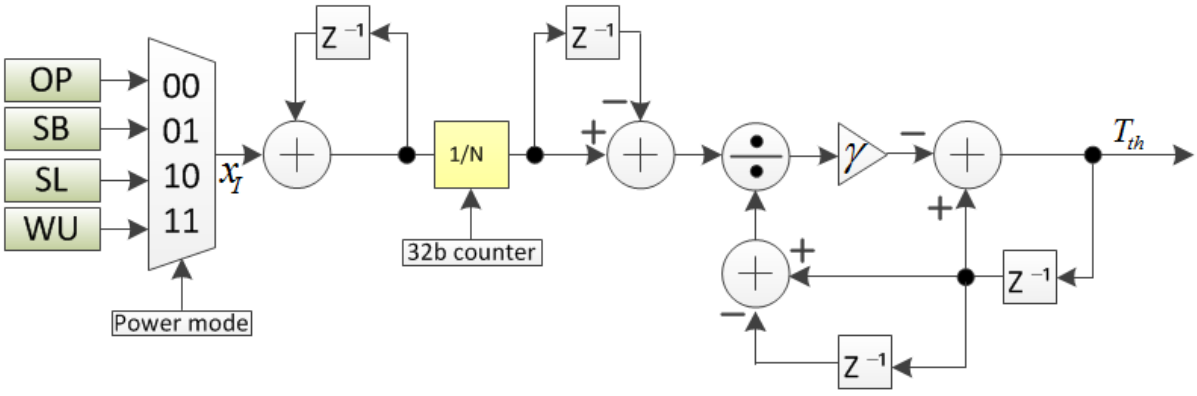


Fig 1. Structure of Adaptive tracking algorithm

[1] Soo-Yong Kim, Keunhwi Koo, and Sang Woo Kim, "Time-based power control architecture for application processors in smartphones," Electron. Lett., vol. 48, no. 25, pp. 1632-1634, Dec. 2012.
[2] Soo-Yong Kim et al., "High-performance low-power application processor integrated with modem processor," in Int. Soc Design Conf., Nov. 2013.
[3] Soo-Yong Kim *et al.*, "Real-time adjustment of power management policy for time-based power control architecture," in IEEE IECON2013, Nov. 2013.

A Dual-Retention Time Architecture towards Secure and High Performance STT-RAM Main Memory Subsystem

Taemin Lee, Sungjoo Yoo, and Sunggu Lee
Department of Electrical Engineering, POSTECH, Pohang 790-784, Korea
E-mail: ltmin@postech.ac.kr

Spin-transfer torque RAM (STT-RAM) is considered to be a strong candidate of large capacity cache and main memory as DRAM faces its scaling limit [1]. STT-RAM based main memory can suffer from a security problem due to its non-volatility. Data encryption, which can be applied to resolve this problem, can incur significant performance degradation due to the additional latency of decryption/encryption in each main memory access. We propose an STT-RAM architecture where two regions have different retention times [2]. A small short retention (SR)-time region, which works as a write-through cache, keeps data unencrypted thereby avoiding the additional latency. The short retention time also makes the memory chip secure by decaying data fast in case of sudden power off. The large long retention (LR)-time region contains the original version of main memory data in the encrypted form thereby providing full security. Experimental results, with SPEC2006 benchmarks, show that the proposed method offers 17.1%~36.3% improvement in memory access latency. For 10 memory-intensive programs, we can obtain average 15.3% improvement in total execution cycles.

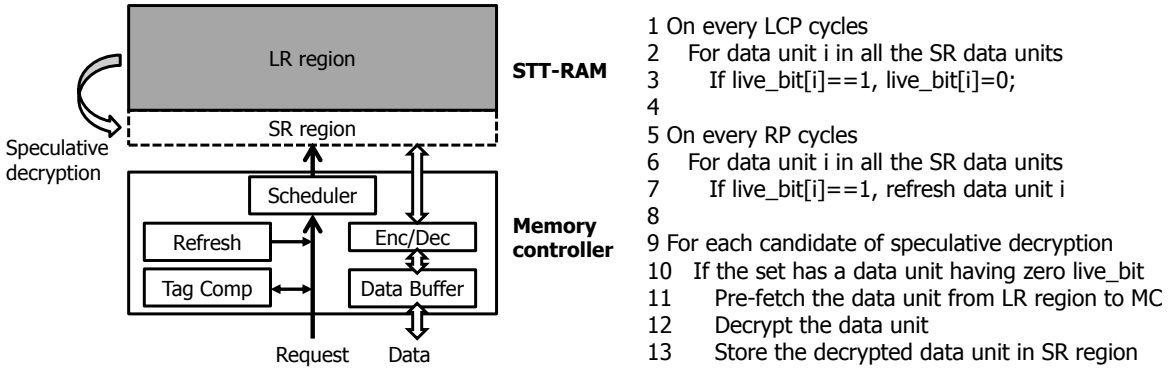


Fig. 1. Memory subsystem for dual-retention time STT-RAM and pseudo code of selective refresh

The memory controller consists of cache tag storage for SR region (rectangle denoted with 'Tag Comp' in the figure), data buffer, request scheduler, refresh manager ('Refresh'), and encryption/decryption engine ('Enc/Dec'). On an incoming request from the on-chip bus, the memory controller performs tag comparison to see if the required data can be found in the SR region. The SR region requires refreshes because it has a short retention time (e.g., 1 second). Thus, the memory controller periodically generates refresh requests for the SR region. In order to reduce the long latency to access the LR region, the memory controller performs *speculative decryption* which issues prefetch requests to the LR region and stores the decrypted prefetch data in the SR region. In order to avoid cache pollution in the SR region, speculative decryption is triggered only when there is available space in the SR region (i.e., enough space occupied by dead data) and prefetch conditions (we use strided prefetch) are met.

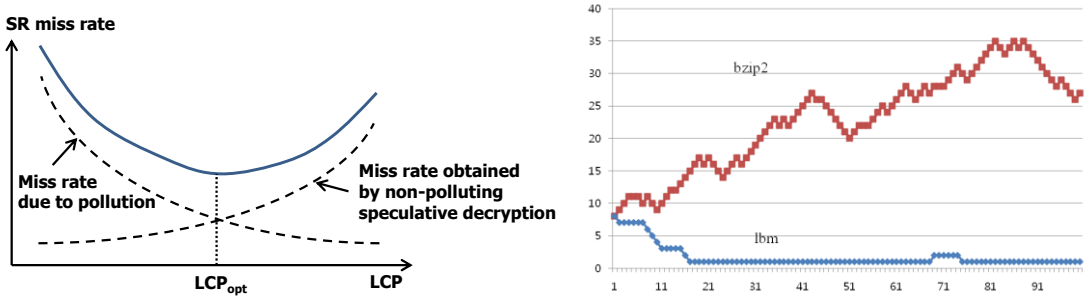


Fig. 2. SR miss rate vs. LCP (left) and LCP (y axis) vs. time (x10^7 instructions) (right)

The effectiveness of speculative decryption varies across programs and program phases (Fig. 2, right). Thus, we propose a runtime adaptive method to adjust the aggressiveness of speculative decryption (how much data are speculatively decrypted) in order to minimize average memory access latency. Periodically, at every LCP cycles (where LCP is the liveness check period), a data unit in the SR region is selected and its live bit (which is set on every access) is reset (Fig. 1, right). A small LCP allows us to eliminate dead data more aggressively from the SR region thereby enabling speculative prefetches. A large LCP enables us to keep data for a long time in the SR region. The large LCP can be useful especially when the speculative decryption is not effective and it is better to keep once-used data in the SR region expecting future re-references. The LCP is adjusted with temporal sampling.

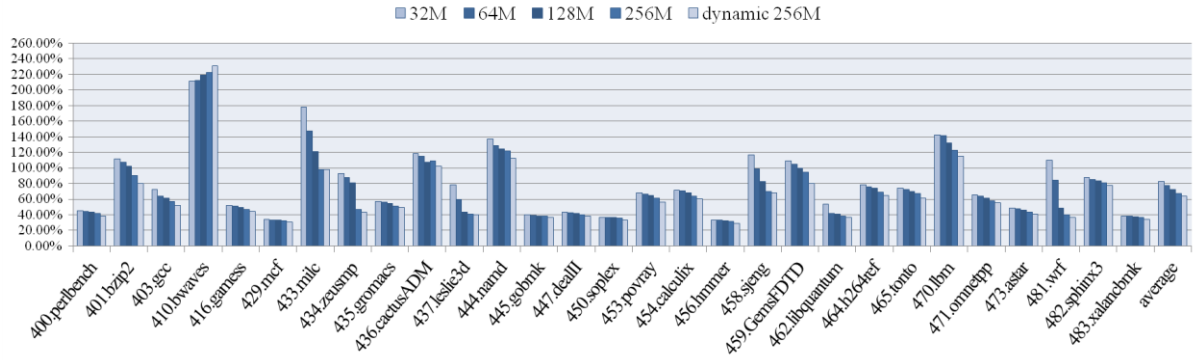


Fig. 3. Average memory access latency (SR region size in bytes varies)

We did experiments by running SPEC2006 benchmarks on an architecture model, McSim (2GB 400MHz DDR2 STT-RAM with 8 banks/1KB rows, SR refresh period of 64ms, 512KB 16-way L2 cache with 6 cycles/64B lines, and 32KB 4-way L1 I/D cache, 2GHz in-order x86 CPU). Fig. 3 shows the impact of SR region size on memory access latency. As SR region size increases, memory access latency decreases. The trend is different across programs. Our experiments show that the proposed method offers average 6.7% (15.3% for 10 memory-intensive programs) and 36.3% improvement in total execution cycles and memory access latency, respectively.

[1] International Technology Roadmap for Semiconductors (ITRS), available at www.itrs.net.

[2] Z. Sun, et al., “Multi Retention Level STT-RAM Cache Designs with a Dynamic Refresh Scheme,” Proc. MICRO, 2011.

LPDDR2-NVM 기반의 상변화 메모리 시스템 설계

Jaehyun Park and Naehyuck Chang
Department of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-747, Korea
E-mail : naehyuck@elpl.snu.ac.kr

Phase change memory (PCM) has received considerable attention as a promising next generation non-volatile memory (NVM) because of its scalability, and it is being commercialized in LPDDR2–NVM standard by a semiconductor manufacturer [1]. Researchers have explored the possibility of utilizing PCM in the memory hierarchy, but there is not enough research that really implements a PCM memory system. In this paper, we focus on the implementation of a PCM with LPDDR2-NVM standard compatible controller and its verification system. We design a row buffer management mechanism considering the row buffer structure and three-phase addressing of PCM, which do not exist in conventional DRAMs [2]. Our controller is capable of managing the activated rows to reduce the access latency. The controller performs address phase skipping when the address and/or data is already in the buffers. A round-robin buffer replacement algorithm is implemented. We also design a PCM SODIMM and verification system on the FPGA and verify the operation of PCM with LPDDR2-NVM standard.

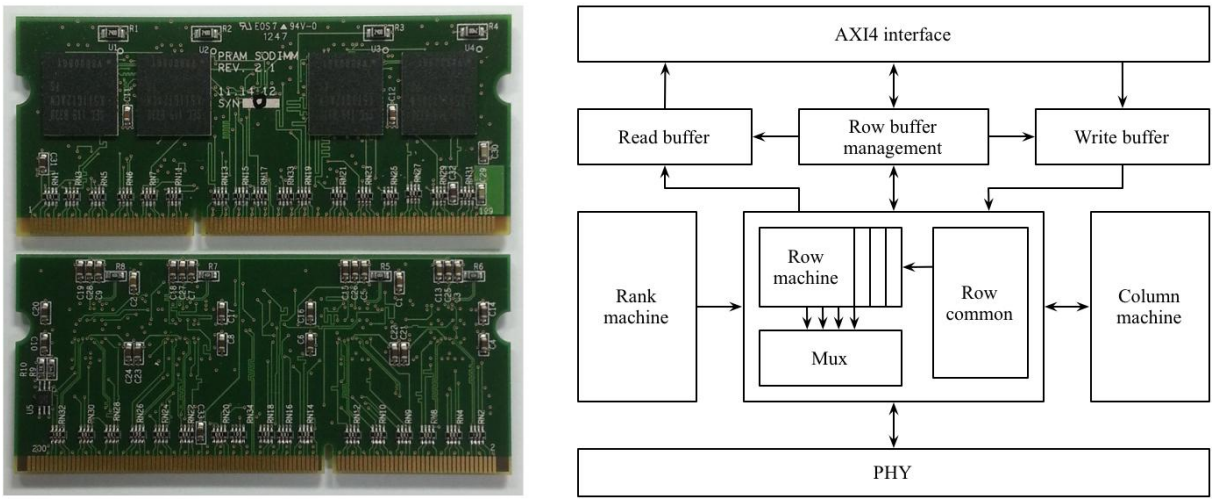


Fig 1. PCM SODIMM board and PCM controller structure

[1] Y. Choi et al., ISSCC (2012), p. 46-48.
[2] JEDEC, JESD209-2E, (2011).

New Processing Element for Imperfect Nested Loops on Coarse Grained Reconfigurable Architecture

Seongseok Seo, Hyeonuk Sim, Jongeun Lee
School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology, Ulsan 689-798, Korea
E-mail : jlee@unist.ac.kr

대부분의 하드웨어 컴파일러들은 높은 병렬성을 위해 loop pipelining 을 적용 한다. 하지만 nested loop 에서의 loop pipelining 은 innermost loop 에만 제한적으로 적용 할 수 있다는 문제점이 있고 이러한 문제는 CGRA (Coarse Grained Reconfigurable Architecture) 에서도 그대로 나타나게 된다. 그중에서도 특히 imperfect nested loop 의 경우 FPGA 와 같은 fine grained 아키텍쳐에서는 Single-dimension Software Pipelining (SSP) [1]와 같은 방법을 이용하여 이러한 문제를 해결 할 수 있지만 loop level 의 개수만큼의 하드웨어 컨트롤러가 필요하다 [2]. 따라서 이러한 방법만으로는 CGRA 에서 임의의 loop level 을 가지는 nested loop 을 지원하는 데에 문제가 있다.

본 논문에서는 이러한 문제를 해결 하기 위해 기존 CGRA 에서 PE (Processing Element)를 확장함으로써 이러한 imperfect nested loop 에 대한 문제를 해결하고자 한다. SSP 와는 다르게 loop 을 flattening 하는 방법을 적용하고 이에 따라 발생하는 추가 노드와 conditional branch 를 효율적으로 제거할 수 있는 Programmable Regular Iterator Generator 아키텍쳐를 제안한다.

StreamIt [3] 에서 사용되는 여러 Stream 어플리케이션의 경우 많은 nested loop 을 포함하고 있어서 실험에 사용 되어 졌다. StreamIt benchmark 에 포함된 벤치마크 중에서 FFT, DCT, Bitonic Sort 를 이용하여 실험을 하였다. 실험은 아무런 코드 수정을 하지 않고 innermost

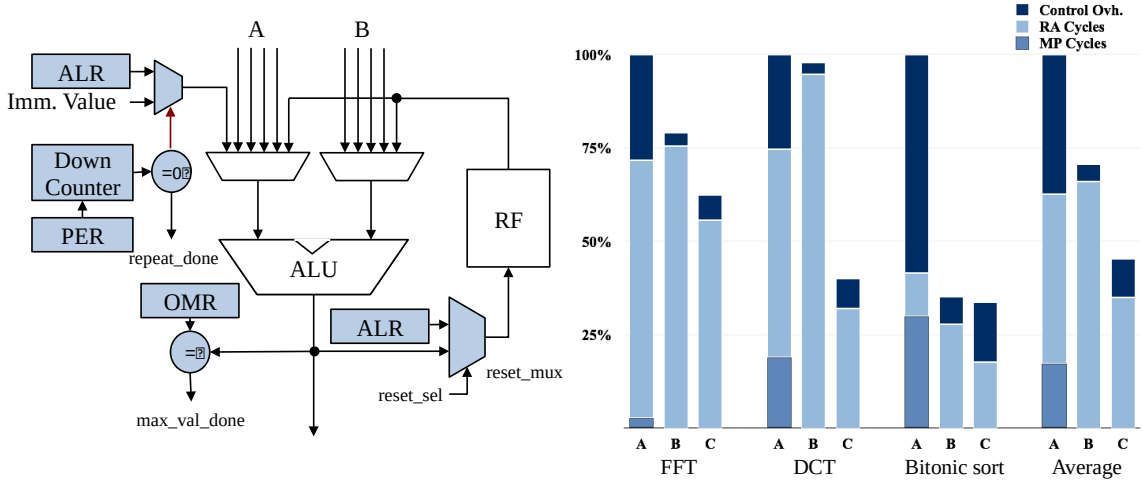


Fig 1. Extended PE Architecture (left) and Experiment Result (right).

Table 1. Information of nested loop in each benchmarks

	Nested depth	Iterations	Imperfect	Recurrent
FFT	2	8(64,64)	Yes	Yes
DCT	2	8(8)	Yes	Yes
Bitonic sort	3	4(2(2))	Yes	Yes

loop 을 커널로 만드는 방법 (naïve), 소프트웨어만을 이용해 flattening 하는 방법, 그리고 flattening 후 확장된 PE 를 이용하는 방법으로 진행 되었다. 모델링된 시스템에서 메인 프로세서는 720Mhz 로 동작하고 32kB L1 cache 와 128kB l2 cache 를 가진다. RA control overhead 의 1 store 사이클은 평균 6 사이클이며 cache through 로 되어있고, CGRA 는 520Mhz 으로 동작한다.

소프트웨어만을 이용한 flattening 실험에서는 메인프로세서에 의해 제어되어야 하는 부분이 대부분 감소 하고 중복 호출에 의한 컨트롤 오버헤드는 상당량 감소 하였다. 하지만 컨디셔널 브렌치의 추가와 이터레이터 생성을 위한 노드의 추가로 인해 mapping 결과가 나빠짐을 확인 할 수 있었다. 결과 적으로 소프트웨어만을 이용한 flattening 은 메인 프로세서 사이클은 대부분 감소 하고 control overhead 는 87.39%가 감소하였지만 RA cycle 은 45.15%가 오히려 증가 된다는것을 확인 할 수 있었다.

두번째 실험에서 소프트웨어 flattening 을 수행한 후 확장된 PE 가 지원하는 새로운 인스트럭션을 이용해 매핑을 하였다. 확장된 PE 를 사용하는데에 필요한 store 사이클이 컨트롤 오버헤드로 추가 되었다. 이 확장된 PE 를 사용함으로써 소프트웨어 flattening 으로 인해 증가된 노드를 상당수 줄일 수 있었다. 그 결과 소프트웨어 flattening 에 비해 RA cycle 이 46.81% 감소한다는 사실을 확인 할 수 있었다.

결과 적으로 naïve mapping 대비 확장 PE 를 이용한 경우를 비교해 보았을때 실험 결과 각각 메인프로세서 사이클은 대부분 감소 하고 RA 사이클은 22.79%, 콘트롤 오버헤드는 72.53%가 감소 하였다. Naïve 매핑대비 전체 커널 수행 시간은 54.67% 감소 하였다.

[1] Kieron Turkington, George A. Constantinides, Konstantinos Masselos, Peter Y. K. Cheung, "Outer Loop Pipelining for Application Specific Datapaths in FPGAs," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.16, no.10, pp.1268,1280, Oct. 2008

[2] Hongbo Rong, Zhizhong Tang, R. Govindarajan, Alban Douillet, and Guang R. Gao, “Single-dimension software pipelining for multidimensional loops.” ACM Trans. Archit. Code Optim. 4, 1, Article 7, March. 2007

[3] William Thies, Michal Karczmarek, and Saman P. Amarasinghe, “StreamIt: A Language for Streaming Applications.” In Proceedings of the 11th International Conference on Compiler Construction, 2002

Intra/Inter-CGRA Co-Reconfiguration for Efficient CGRA-based Multi-Core Architecture[5]

Heesun Kim, Seungyun Sohn, and Yoonjin Kim
Department of Computer Science, Sookmyung Women's University, Seoul 140-742, Korea
E-mail : {khs9101, kjkj35, ykim}@sookmyung.ac.kr

Coarse-grained reconfigurable architecture (CGRA) has emerged as a suitable solution for embedded systems but there is a limit as to what a CGRA can improve performance. This is because single CGRA is sequentially optimized for the parallelized computations in a kernel at a time whereas the entire speedup of the applications can be achieved by kernel level parallelism (KLP) that several kernels concurrently run [1]~[4]. Therefore, CGRA-based multi-core architectures have appeared to support diverse KLPs. However, the existing CGRA-based multi-core architectures suffer from much energy and performance bottleneck because the existing multi-CGRA structures are not flexible enough to adaptively support various cases of the KLP. It means that the resources in the multi-CGRAs cannot be efficiently utilized under monotonous aggregation of several CGRAs. For improving their flexibility, we introduce a novel intra/inter-CGRA co-reconfiguration technique based on a ring-based sharing fabric (RSF) focusing on the kernel-stream type of the KLP.

We make use of the multi-CGRA in Fig 1 as base architecture for comparison with proposed architecture. It is composed of a general purpose processor (GPP), a DMA, four CGRAs, and on-chip communication which couples them. Single CGRA consists of PE array (PA), data buffer (DB), configuration memory (CM), and execution controller (EC). The proposed RSF based on four CGRAs connects all of the PAs through single-cycle interconnection and a DB (or a CM) is

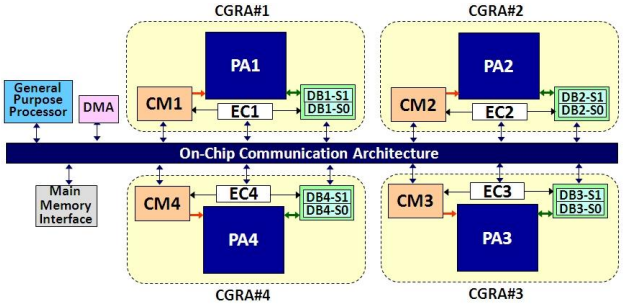


Fig 1. CGRA-based multi-core architecture.

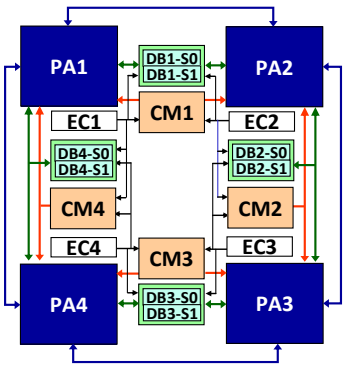


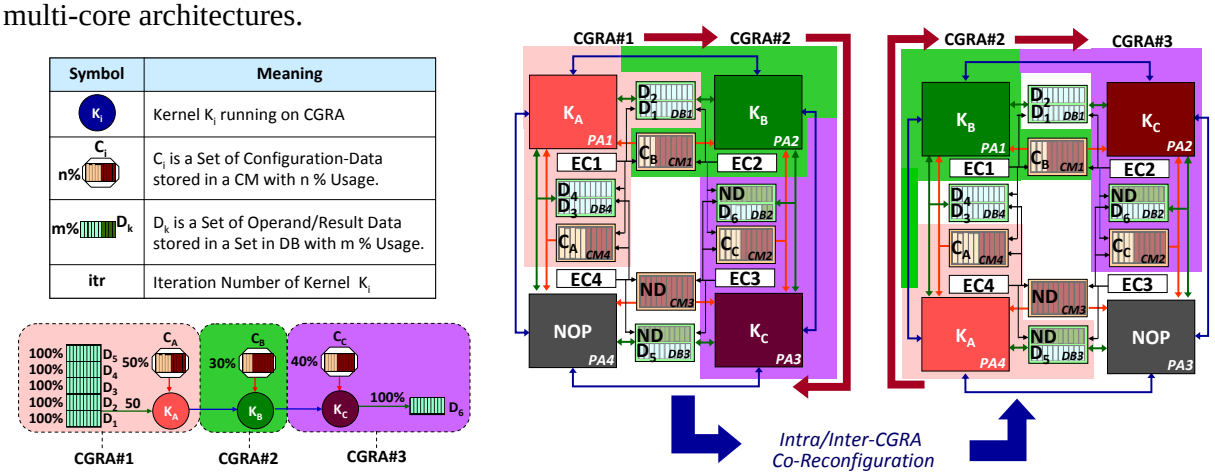
Fig 2. Ring-based sharing fabric.

[5] This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2011-0013282) and by IC Design Education Center (IDEC).

shared by two adjacent PAs as Fig 2. Such connectivity shows minimal interconnection overhead even though the number of CGRAs increases because the design overhead is only interconnections and switching logics between two adjacent PAs.

In order to show the process of the proposed co-reconfiguration technique, we assume an example that the pipelining of kernel-stream requires three DBs (500%) and it iteratively runs on the RSF at 50 times iterations as Fig 3 (a) – each data-set (100%) includes operand-data for the iterative running at 10 times. In this example, base architecture should be sequentially performed with DMA transfer because of insufficient DB capacity. It causes much energy and performance bottleneck. The lack of DB resources may be also exposed on the RSF but we can alleviate the limitation of the RSF by shifting configuration of kernel-stream on the RSF. Fig 3 (b) shows initial configuration of the kernel-stream that PA1 utilizes DB1 (D_1 and D_2) and DB4 (D_3 and D_4) for the running of 40 iterations. Then the RSF can be configured as Fig 3 (c) that shows the utilization of one more DB (DB3) for the remaining 10 iterations. The utilization of DB3 (D_5) can be achieved by shifting the configurations of PAs from 'PA1->PA2->PA3' to 'PA4->PA1->PA2'. In this case, the intra-CGRA reconfiguration means that PA1 and PA2 are reconfigured twice in order to perform K_A/K_B and K_B/K_C. On the other hand, the inter-CGRA reconfiguration enables that three CGRAs are configured with different number of CMs/DBs and connected through the direct interconnections. Such a co-reconfiguration can start immediately because each CM is shared by two adjacent PAs that are dynamically reconfigurable. It means that the pipelining of the kernel-stream continually runs on the RSF without stall as shown in Fig 4.

Experimental results show that the proposed approaches improve performance by up to 50.62 times and reduce energy by up to 50.16% when compared with the conventional CGRA-based multi-core architectures.



(a)Pipelining of kernel-stream with 3 DBs (b) Configuration#1 (c) Configuration#2

Fig 3. Intra/inter CGRA co-reconfiguration for the kernel-stream with three DBs on the RSF.

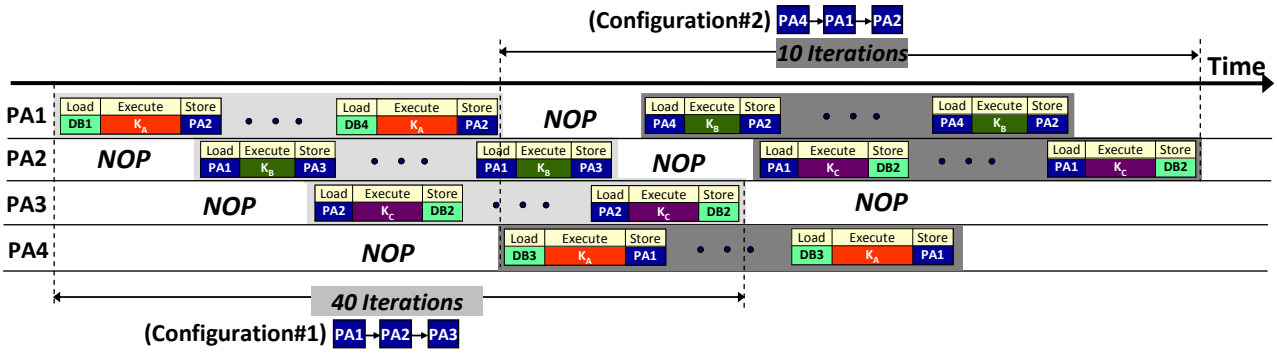


Fig 4. Pipeline-scheduling on the RSF according to two cases of configurations.

1. Aaron Wood, et al, "Multi-kernel floorplanning for enhanced CGRAs," in *Proc. of IEEE Int. Conf. on Field-Programmable Logic and Application (FPL),* pp. 157-164, Aug. 2012
2. Minsoo Kim, et al, "Hybrid Partitioned H.264 Full High Definition Decoder on Embedded Quad-core," in *Proc. of IEEE Int. Conf. on Consumer Electronics (ICCE),* pp. 279-280, Jan 2012.
3. Kosuke Nishihara, et al, "Parallelization of H.264 video decoder for embedded multicore processor," in *Proc. of IEEE Int. Conf. on Multimedia and Expo,* pp. 329-332, April 2008.
4. Minsoo Kim, et al, "H.264 decoder on embedded dual core with dynamically load-balanced functional partitioning," in *Proc. of IEEE Int. Conf. on Image Processing (ICIP),* pp. 3749-3752, Sept 2010.

FPGA Prototyping of Programmable Regular Iterator Generator

Hyeonuk Sim, Seongseok Seo, Jongeun Lee

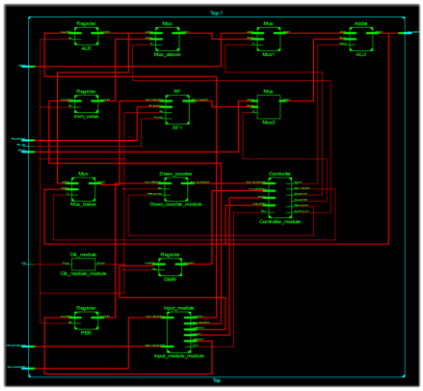
School of Electrical & Computer Engineering, Ulsan National Institute of Science and Technology, Ulsan 689-798, Korea

E-mail : jlee@unist.ac.kr

기존의 CGRA(Coarse-Grained Reconfigurable Architecture)는 오직 innermost loops 만을 지원한다. 우리는 이를 각 PE(Processing Element)에 대한 아키텍처 확장을 통해 outer loop 특히 imperfect 구문을 포함하는 outer loop 에도 효율적인 연산을 이루도록 설계해보았다 [1]. 그리고 최종적으로 loops 상황에 따라 4 가지 새로운 instruction 을 지원하도록 하였다.

1 번 instruction 은 resetting accumulator 로 매 II cycle 마다 지정된 연산을 수행하다가 특정 cycle 이 되면 지정된 값으로 초기화를 하게 된다. 이는 innermost loop 의 iterator generator 로 사용될 수 있다. 2 번 instruction 은 resetting accumulator with another PE as operand 이다. 이 연산은 위의 resetting accumulator 과 동일 하지만 지정된 연산에 사용되는 operand 가 다른 PE 의 출력을 사용한다는 점이 다르다. 이 연산은 매 iteration 마다 값을 누적해야 하는 명령에 사용될 수 있다. 3 번 instruction 은 leaping accumulator 이다. 이는 매 II cycle 마다 연산을 수행하다가 특정 cycle 에 특정한 다른 operand 값을 이용해 연산을 한다. 이 연산은 fission 으로 인해 dependency 가 문제가 되는 buffer index striding 문제를 해결 할 수 있다. 마지막 instruction 은 resetting accumulator with periodic update 이며 이는 평소에 기존 값을 유지하고 특정사이클에만 연산을 수행한다. 그리고 출력 값이 특정 값에 도달하게 되면 출력 값을 지정된 값으로 reset 하게 된다. 이 연산은 nested loop 처음과 끝이 아닌 depth 의 iterator generator 사용될 수 있다.

이를 우리는 Verilog 로 구현하여 Xilinx FPGA Virtex-5 330 에 구현하였다. 그 결과 확장된 PE 하나당 323 개의 slice register 와 423 개의 LUT 가 사용되었고, 3bit Input_direction 과 32bit Input_data 를 통해 6 번 cycle 만에 valid 출력 값이 정확히 출력되기 시작하는 것을 확인할 수 있었다 (그림 1 참조).



Logic Utilization	Used
Number of Slice Registers	323
Number of Slice LUTs	423
Number of fully used LUT-FF pairs	167
Number of bonded IOBs	133
Number of BUFG/BUFGCTRLs	5

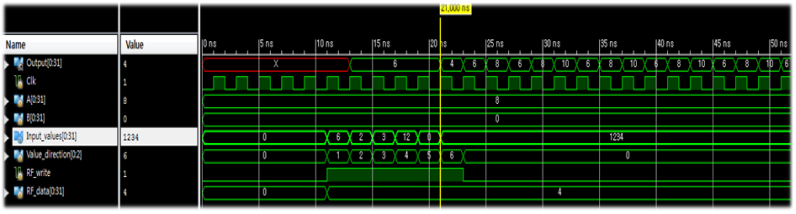


Fig 1. Extended PE RTL diagram (left), Logic Utilization and Simulation Result for instruction 1 (right).

[1] Sungsok Seo, Yeonghun Jeong, and Jongeun Lee, “Mapping DSP Loops to Reconfigurable Processor Accelerators”, *the 20th Korean Conference on Semiconductors*, February, 2013.

Excellent Non-linear I-V Characteristics of Ti/HfO_x ReRAM with Ultrathin TiO_y Tunnel Barrier for Cross Point Memory Application

Nusrat Tamanna, Saiful Haque Misha, Amit Prakash, Daeseok Lee, Jiyoung Woo, Euijun Cha, Jeonghwan Song, Moon Kibong and Hyunsang Hwang.
Department of Materials Science and Engineering, Pohang University of Science and Technology,Gyeonbuk,Korea
E-mail: hwanghs@postech.ac.kr

ReRAM is one of the proposed candidate due to its excellent scalability, simple structure, multi-level stacking and compatible with the CMOS processes compared to other conventional memory devices for cross-point architecture [1]. The non-linear I-V characteristic in LRS state of ReRAM is the most important device parameter for cross-point memory applications. In this paper, the main objective was to establish high non-linearity (the ratio of I @ V_{LRS} to I @ $^1/_2V_{LRS}$) in LRS regime by TiO_y tunnel barrier layer on top of Ti/HfOx/Pt ReRAM (shown in Fig. 1(a)) where 250 nm hole structure substrate was used. Because, it is reported that TiO_x embedded devices are producing non-linear current-voltage region [2, 3]. Also, the conduction mechanism (Fig. 1(b)) of LRS in positive bias is extensively investigated where we proposed direct tunneling at low voltage regime and trap assisted tunneling at high voltage regime. Through the introduction of MATLAB model, we verified our experimental data to describe the improvement of nonlinearity which predicts two important key parameters thickness and trap density (Fig. 1 (c) and (d)). By control film thickness and trap density, we could obtain non-linearity values over 30 which are necessary for cross-point ReRAM applications.

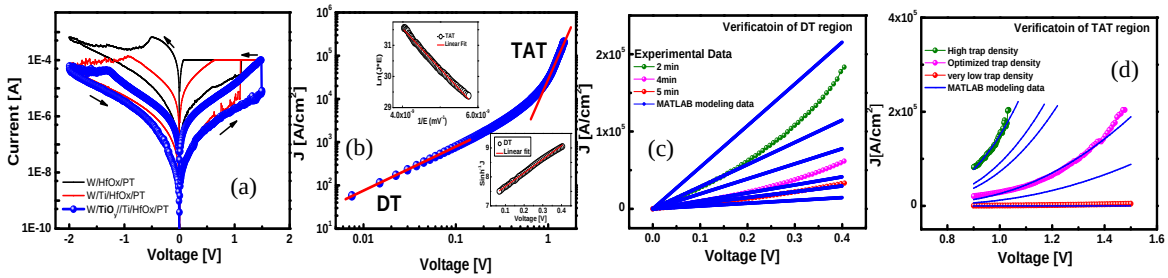


Fig 1. (a) Typical I-V switching characteristics of ReRAM devices, (b) Verified conduction mechanism for LRS region in Positive bias where low voltage region is dominated by DT and high voltage region is dominated by TAT, (d) and (e) Verification of MATLAB modelling data and experimental data for DT and TAT respectively.

Acknowledgement: This work was supported by R&D program of Ministry of Knowledge Economy.

[1] H. Akinaga and H. Shima, “Resistive random access memory (ReRAM) based on metal Oxides,” Proc. IEEE , vol. 98, no. 12, pp. 2237–2251,Dec. 2010. [2] J. J. Yang, M. X. Zhang, M. D. Pickett, F. Miao, J. P. Strachan,W. D. Li, W. Yi, D. A. A. Ohlberg, B. J. Choi, W. Wu,J. H. Nickel, M. R. Gilberto and R. S. William,Appl. Phys.Lett., 2012,100, 113501. [3] Beomyong Kim_, Wangee Kim, Hyojune Kim, Kyooho Jung, Wooyoung Park, Bomin Seo, Moonsig Joo, Keejeung Lee, Kwon Hong, and Sungki Park, Japanese Journal of Applied Physics 52 (2013) 04CD05,2013.

Characterization of γ-Fe_2O_3 memristors via physics-based empirical I-V model

Yun Hyeok Kim,[1] Dae Guen Kim,[1] Jae-Deuk Kim,[2] Sung-Jin Choi,[1] Dong Myong Kim,[1] Tae-Sik Yoon,[2] and Dae Hwan Kim[1,*]

[1]*School of Electrical Engineering, Kookmin University, Seoul, 136-702, Korea*

[2]*Department of Materials Science and Engineering, Myongji University, Gyeonggi-do 449-728, Korea*

[*]E-mail : drlife@kookmin.ac.kr

Recently, memristor has been studied as one of the most promising candidates for next generation nonvolatile-memory due to its fast write/read speed, superior scalability, compatibility with CMOS technology and multi-bit storage potential [1]. We here represent the empirical current-voltage (*I-V*) model to explain the Pt/γ-Fe_2O_3/Pt (Fig. 1 (a)) memeristive switching behaviors based on the variation of the state variables. Noticeably, physical mechanisms such as tunneling [2] and back-to-back Schottky characteristics are taken into account (Fig. 1(b)). In addition, we show that the proposed empirical *I-V* model can be successfully incorporated into the SPICE model using Verilog-A (Fig. 1(c)). Our model has a distinguished merit in perspective of the opimization of material, process, and memeristive device in that it is able to be identified by the resistance variation of ON state in the formula and without any fitting parameter in the OFF state. This study would be helpful in understanding of the memristive behaviors and also give insight into the design for innovative memristor-based circuit applications.

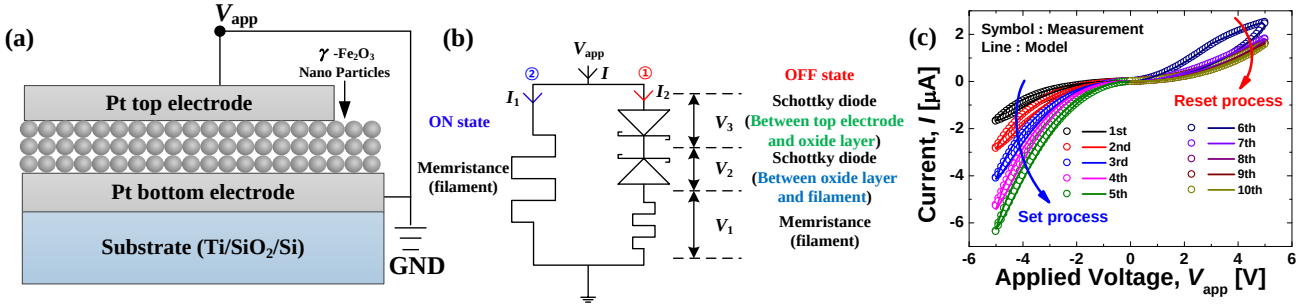


Fig 1. (a) Schematic of the Pt/γ-Fe_2O_3/Pt memristor, (b) equivalent circuit of the memristor, and (c) comparison of empirical *I-V* model on the measured *I-V* characteristics.

[1] Y. S. Chen, H. Y. Lee, P. S. Chen, C. H. Tsai, P. Y. Gu, T. Y. Wu, K. H. Tsai, S. S. Sheu, W. P. Lin, C. H. Lin, P. F. Chiu, W. S. Chen, F. T. Chen, C. Lien, and M.-J. Tsai, *in IEDM Tech. Dig.*, pp. 31.3.1-31.7.4, 2011.

[2] K. Eshraghian, O. Kavehei, K. R. Cho, J. M. Chappell, A. Iqbal, S. F. Al-Sarawi, and D. Abbott, *proc. IEEE*, vol. 100, no. 6, pp. 1991-2007, Jun. 2012.

Identification of controlling parameters on self-compliance resistive switching in a Pt/TaO_x/Ta_2O_5/Pt Structure

Taehyung Park, Seul Ji Song, Jun Yeong Seok, Jung Ho Yoon, Kyung Jean Yoon, Dae Eun Kwon and Cheol Seong Hwang

Department of Material Science and Engineering, Seoul National University, Seoul 151-747, Korea

E-mail : dobig2@snu.ac.kr

전이금속 산화물 기반의 저항변화메모리(ReRAM) 소자는 외부에서 전압을 인가하여 저항 상태를 가역적으로 바꿀 수 있는 현상을 적용한 차세대 비휘발성 메모리이다. ReRAM 은 높은 저항 상태를 낮은 저항 상태로 전환하는 SET 동작 중에 급격한 current jump 가 나타나기 때문에 소자의 절연파괴를 방지하기 위해 추가적인 current compliance element 가 필요하다. 최근에는 메모리 소자가 자체적으로 SET 전류를 제한할 수 있는 self-compliance 거동이 보고되고 있으나 동작 원리에 대해서는 아직 잘 알려져 있지 않다.[1-2] 본 연구에서는 self-compliace 저항변화특성을 평가하기 위하여 Pt/TaO_x/Ta_2O_5/Pt 구조의 ReRAM 소자를 제작하였고, [그림 1]과 같이 안정적인 self-compliance 거동을 확보할 수 있었다. 또한 self-compliance 동작 메커니즘을 규명하기 위해 oxygen vacnacy migration 과 schottky conduction mechanism 모델을 사용한 시뮬레이션을 진행하였고, 실제 실험 결과를 근사하게 모사한 결과를 얻을 수 있었다. 위와 같은 모델을 적용하여 self-compliance 거동에 직접적인 영향을 미칠 수 있는 인자들을 파악함으로써 근본적인 동작 메커니즘을 확인하고, 소자의 동작 특성을 개선 할 수 있을 것으로 기대된다.

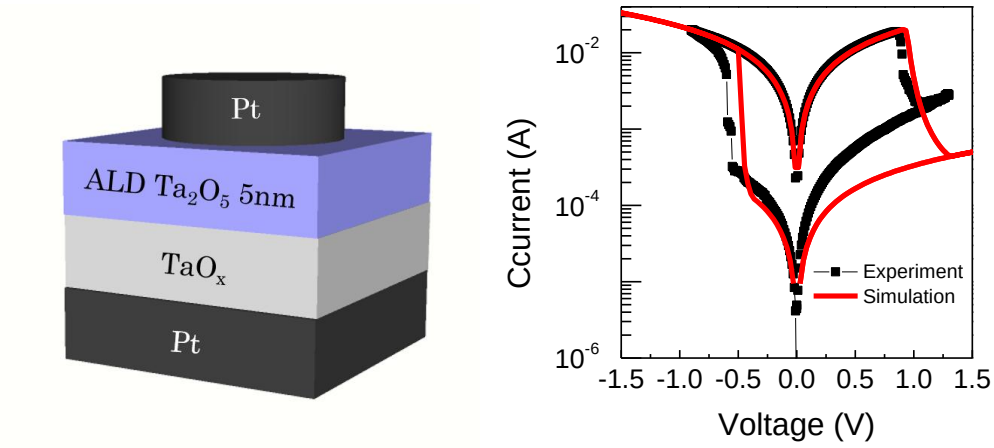


그림 1. (좌) 제작된 ReRAM 소자의 모식도와 (우) 전기적 특성평가 및 시뮬레이션 결과

[1] TSENG et al, Electron Device Letters, IEEE, 34[7], 858 (2013)

[2] Myoung-Jae Lee et al, Nature Materials 10, 625–630 (2011)

Cu_2O-based conductive bridging random-access-memory

Ki-Hyun Kwon[1], Hyun-Min Seung[1], Kyoung-Cheol Kwon[2], Jong-Sun Lee[1], Myung-Jin Song[1], Han-Vit Jeoung[1], Young-Hye Son[1] and **Jea-Gun Park[1,2]***
[1]Department of Electronics and Computer Engineering,
[2]Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Republic of Korea
Tel : +82-2-2220-0234, Fax : +82-2-2296-1179
E-mail : parkjgL@hanyang.ac.kr

Conductive bridge random access memories are highly promising as one of next-generation memories due to high current density, high speed, simple structure, and low power consumption [1]. In this work, we present the electrical features of p-type Cu_2O layer, working as a solid electrolyte [2], where the Pt/Cu_2O/Ag configuration with a 250 nm-hole pattern size was prepared. The thickness, O_2 flow rate, and N_2-annealing temperature were varied for the optimized device performance. Typical electrical characteristics displayed the set voltage of 0.2 V, the reset voltage of –0.6 V, high resistance state current at 0.1 V of 6.94×10^{-7} A, and low resistance state current at 0.1 V of 10^{-3} A. Moreover, stable endurance and retention at 35 nm thick Cu_2O after N_2-annealing at 250 ^oC were observed with the properties of endurance of 7.0×10^3 cycles with a margin (Ion/off) of 7.27×10^2 and retention of 10^5 sec with a margin of 8.89×10^2. Finally, the role of Cu_2O thickness, O_2 flow rate, and N_2-annealing temperature on the electrical features was described.

**This work was financially supported by the Industrial Strategic Technology Development Program(10039191, The Next Generation MLC PRAM, 3D ReRAM, Device, Materials and Micro Fabrication Technology Development) funded by the Ministry of Trade, Industry and Energy (MOTIE) and the Brain Korea 21 Plus, Republic of Korea.*

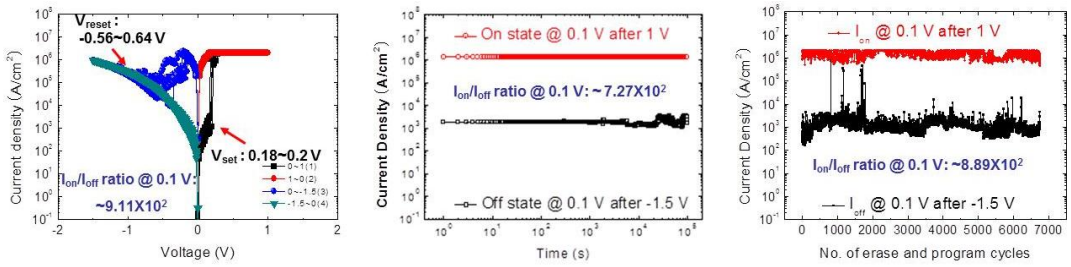


Fig 1. The NVM characteristics of Cu_2O based CBRAM

[1] K. H. Kim, S. H. Jo, S. Gaba, and W. Lu, Appl. Phys. Lett. 96, 053106 (2010).
[2] H. Raebiger, S. Lany, and A. Zunger, Phys. Rev. B, 76, 045209 (2007).

Evolution of the shape of the conducting channel in complementary resistive switching transition metal oxides

Kyung Jean Yoon, Seul Ji Song, Jun Yeong Seok, Jung Ho Yoon, Tae Hyung Park, Dae Eun Kwon and Cheol Seong Hwang
Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea
E-mail: rodwls88@snu.ac.kr

Resistive switching phenomenon has been rigorously studied over recent years amid the great expectations for their potential use as the non-charge based non-volatile memory as well as an element in the artificial neuromorphic circuits (i.e. memristor). Transition metal oxides have been known to be the most promising resistive switching materials owing to the naturally inherent high non-stoichiometry within themselves. According to these studies, unipolar resistive switching (URS) phenomena in this material, where set operation occur under the same bias polarity, is attributed to the formation and rupture of local conducting filaments, which is proven to be basically composed of the metallic oxygen-deficient Magnéli phases (Ti_nO_{2n-1}, where n = typically 4 or 5). Bipolar resistive switching (BRS) is characterized with the opposite bias polarity when performing the set and reset switching, and has been so far ascribed to the localized drift of oxygen vacancies along the direction of electric field, which causes the Schottky barrier modulation at the electrode/thin film interface.

Making use of the BRS at the filament ruptured region, this paper suggests a system, where ultimate control of the defect distribution and local conduction path in a BRS Pt/TiO_2/Pt sample, which was in a unipolar reset state, is provided by means of voltage pulsing. Combined analysis upon the time-transient current during the voltage pulsing and the resistance status obtained in the voltage sweep mode confirms and gives the detailed physical reasoning and kinetic behaviors for the desired phenomenon in the system. The power consumption during the ion migration-based resistive switching is the key determinant of the conduction states, or the resistance of the memory. The data retention of the on-state in the BRS was critically dependent on the shape of the rejuvenated conduction channel. The required time to lead the rejuvenation of the conducting channel was ~70-100 ns when the threshold voltage for the BRS set of ~1 V was applied.

Basically, the limited amount of oxygen vacancies in this system allowed reversibly switching-diode-like current-voltage curves, which was also confirmed in another Magnéli-phase-containing Pt/WO_3/Pt sample. Such careful control of the defect distribution allowed the achievement of a complementary resistive switching (CRS) curve even from a single switching layer. The unlimited vacancy source in the Pt/TiO_2/TiO_{2-x}/Pt sample did not allow switching-diode type and the CRS behavior.

Heater-less operation of chemoresistive sensors based on thin film nanostructures: extremely low power consumption for mobile applications

Ho Won Jang
Department of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea
E-mail : hwjang@snu.ac.kr

Here we present what we confidently view as a major breakthrough in the development of chemoresistive sensors. We have realized all oxide transparent chemoresistive sensors with a combination of ultrahigh sensitivity, extremely low power consumption and excellent long-term stability by utilization of uniquely nanostructured metal oxide thin films [1,2]. These devices are readily self-activated with sub-μW power levels, orders of magnitude lower than the best micromachined devices. At the same time they exhibit remarkably high sensitivities to toxic chemicals such as NO_2, SO_2, CO, and VOCs for which detection limits are well below international air quality standards. This remarkable device performance, achieved with a facile fabrication process, considerably broadens the potential application of chemoresistive sensors to transparent electronics and highly miniaturized mobile devices. Finally we briefly present sub-nW power consumption of ultrasensitive and reliable grapheme-based sensors with high transparency and flexibility [3].

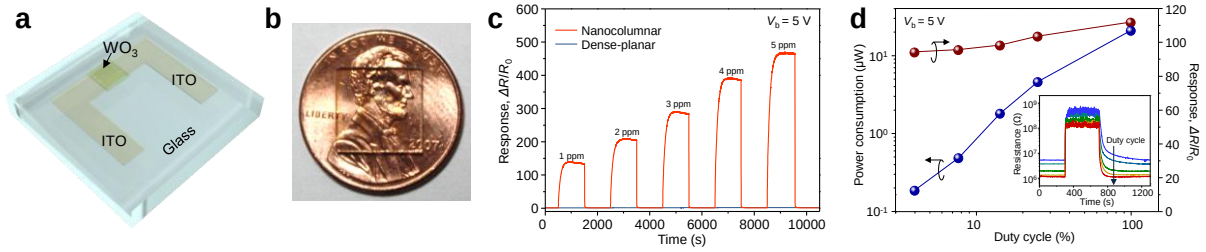


Fig 1. (a) Illustration of sensor structure. (b) Photograph of a fabricated sensor. (c) Response to 1–5 ppm NO_2 and (d) power consumption of heater-less chemoresistive sensors without external heating.

[1] H. G. Moon *et al.*, *Sci. Rep.* **2**, 588 (2012).
[2] H. G. Moon *et al.*, *ACS Appl. Mater. Interfaces*, DOI: 10.1021/am402456s .
[3] H. G. Moon, Y. R. Choi, *et al.*, *submitted*.

The study of thermoelectric properties in n- and p-type silicon nanowire thermoelectric devices

Soojung Kim [1,2], Hyojin Jeon[1,2], Wonchul Choi [1,3], Dongsuk Jun[1], and Moongyu Jang[1,2,*]

[1]*Novel Materials and Devices Research center, ETRI, Daejeon 305-700, Korea*

[2]*Department of Advanced Device Technology, UST, Daejeon 305-350, Korea*

[3]*Department of Electrical Engineering, KAIST, Daejeon 305-701, Korea*

**E-mail address: jangmg@etri.re.kr*

Thermoelectric power devices as energy conversion technology require materials with good electrical conductivity and Seebeck coefficient but low thermal conductivity. Therefore, the bulk silicon is a poor thermoelectric material due to high thermal conductivity, ~150$Wm^{-1}K^{-1}$ at room temperature, giving ZT= 0.01 value [1, 2]. In the low dimensional structures, such as nanowires and nanotubes, the thermal conductivity is expected to decrease by phonon scattering elements. Thus silicon is a valuable thermoelectric material because nanostructure could be easily implemented with well-developed semiconductor process technology. In this study, we evaluated the thermoelectric properties of 50 nm wide silicon nanowires (SiNWs) with different doping types, length (10um, 40um) and number of wires (1, 6 wires). For the measurement of Seebeck coefficients and power factor of SiNWs, we fabricated SiNW test structure including micro-heaters, temperature sensors and SiNWs. It takes advantages of using the semiconductor device manufacturing process. SiNWs have 50 nm wide which is smaller than the mean free path of the phonons (~ 100nm) and yet larger than that of electrons (~ 5nm). The optimized doping concentrations of SiNWs are ~1.2×10^{20} cm^{-3} and ~3.5×10^{20} cm^{-3} for n- and p- type, respectively. Thermoelectric properties with variable factors, i.e., wire doping type, length, number and temperature differences will be discussed.

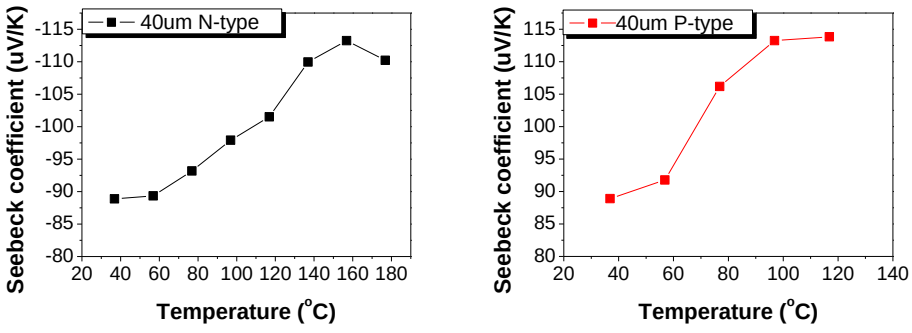


Figure 1. Seebeck coefficient of 50nm wide and 40um long N-type and P-type silicon nanowires with temperature

[1] Boukai A I et al, *Nature.* **451**, 168-71 (2008)
[2] Hochbaum A I et al, *Nature.* **451**, 163-8 (2008)

수직자기이방성을 갖는 MgO/Co/Pd 구조에서 열처리를 통한 계면 구조 변화가 스핀-궤도 결합에 미치는 영향

김민석, 김상훈, 홍종일*
연세대학교 공과대학 신소재공학과, 서울특별시 서대문구 신촌동 134, 120-749

최근 들어 스핀-궤도 토크 효과, Dyaloshinskii-Moriya interaction (DMI)와 같은 물리적 현상들은 강자성체의 자화 반전을 일으키는 임계 전류 감소에 큰 영향을 미치기 때문에 p-MTJ, 자구벽 메모리 소자와 같은 응용분야에서 많은 주목을 받고 있다[1,2]. 이러한 현상들은 스핀-궤도 결합과 밀접한 관련이 있으며 특히 강자성체와 인접한 물질과의 계면 구조가 가장 큰 영향을 미치는 요소들 중 하나이다. 이러한 중요성에도 불구하고 계면의 구조 변화와 스핀-궤도 결합간의 상관관계에 대해서는 자세한 연구가 부족한 상황이다. 본 발표에서는 수직자기이방성을 갖는 MgO/Co/Pd 구조에서 열처리를 통해 MgO/Co, Co/Pd 계면의 구조변화를 일으키고 이러한 변화가 스핀-궤도 결합에 미치는 영향에 대해서 논의한다. MgO 5/Co t/Pd 3(nm) 구조를 갖는 박막을 초고진공 스퍼터링 시스템(<2.0×10^{-9}torr)을 이용하여 증착하였으며, 수직자기이방성 특성을 확인하기 위해 Co 층의 두께 t 를 0.8 nm 부터 2.4 nm 까지 0.2 nm 씩 증가시켰다. 열처리에 따른 수직자기이방성 및 계면 구조의 변화를 관찰하기 위하여 200, 300, 400 ℃ 에서 각각 1 시간 동안 4.5 kOe 의 일정한 외부 자기장을 가하며 진공(<5×10^{-7}torr)열처리를 진행했다. 자기적 특성의 변화는 VSM (vibrating sample magnetometer)을 통하여 확인하였으며, 계면의 구조변화와 스핀-궤도 결합 특성은 XRD (X-ray diffraction)및 XMCD (X-ray magnetic circular dichroism) 측정으로 관찰하였다. VSM 측정을 통해 얻은 자기이력곡선을 면적차이 계산을 통하여 분석한 결과, 열처리 온도가 높아짐에 따라 수직자기이방성이 증가되는 것을 확인하였다. 단 열처리 온도가 400 ℃ 일 때 포화 자화 값은 열처리 전 1,400 emu/cc 보다 작은 1,200 emu/cc 를 가지는데 이는 높은 열처리 온도로 인하여 Co/Pd 계면에서 CoPd 합금 형성의 결과로 여겨지며 동일 시편의 XRD 측정을 통해 CoPd (002) peak 을 검출로 확인할 수 있었다. 계면에서의 합금의 형성이 열처리 후 포화 자화 값을 낮추는 원인으로 분석된다. 열처리를 통한 계면 구조의 변화가 스핀-궤도 결합에 미치는 영향을 확인하기 위하여 XMCD 측정 결과를 바탕으로 sum rule 을 이용해서 궤도 모멘트 기여도를 정량적으로 분석했다. 열처리 온도가 증가함에 따라 궤도 모멘트 기여도가 높아지는 것을 알 수 있었으며, 열처리 온도 400 ℃ 의 경우에는 열처리 전과 비교하여 궤도 모멘트 기여도가 160% 높아지는 것을 확인하였다. 궤도 모멘트의 기여가 스핀-궤도 결합과 밀접한 관련이 있다는 것은 400 ℃ 열처리 시편의 계면에서 강한 스핀-궤도 결합이 형성되어 있음을 의미한다 [3]. 다만 이러한 결과를 실제 소자에 적용시켜 CoPd alloy 가 형성됨에도 높은 스핀-궤도 토크를 갖는지는 추가적으로 확인이 필요하다.

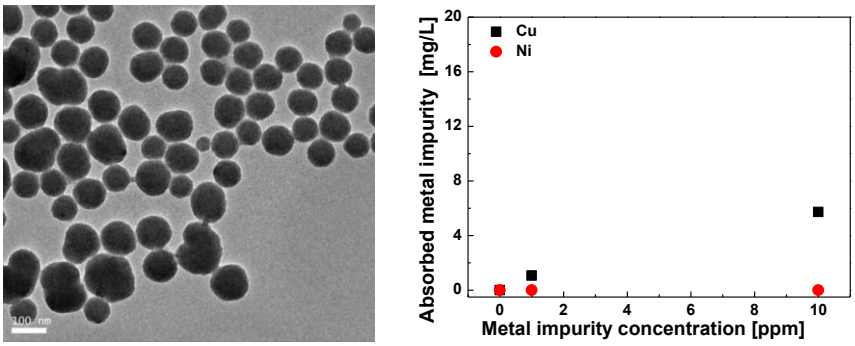
[1] E. Martinez et al Appl. Phys. Lett. **103**, 072406 (2013)
[2] S. Emori et al. Nature Mater. **12**, 611 (2013)
[3] C. T. Chen et al. Phys. Rev. Lett. **75**, 152 (1995)

Influence of Ni and Cu Contaminants in the Colloidal Silica slurry for Efficient Silicon Wafer Polishing

Eun-Bin Seo, Hao Cui, Jin-Hyung Park and Jea-Gun Park*
Advanced Semiconductor Materials and Devices Development Center
Department of Electronic Engineering, Hanyang University, Seoul 133-791, Republic of Korea
E-mail : parkjgL@hanyang.ac.kr

As the design rule of memory devices has shrink, metal contaminants in the silicon wafer surface are becoming one of critical issues. In particular, Cu and Ni contaminants on the silicon wafer surface easily induce the leakage current and early breakdown of gate oxide.[1-2] In this work, we describe the absorption behavior of Ni and Cu contaminants in a silicon wafer polishing slurry and then possible chemical additives are proposed to reduce the metal contaminants after silicon wafer polishing. The adsortion features of Ni and Cu contaminants onto the colloidal-silica abrasive surface in a silicon wafer polishing are analyzed by utilizing the pourbaix diagram of Ni and Cu and zeta potentials of abrasives, as shown in Fig.1(b). In addition, we observe the effect of an additive, such as carboxyl, amine and hydroxyl functional gourp additives on the reduction of Ni and Cu contaminants during polishing. Experimental observations indicate that appropriate addition of chemical additive into the slurry can reduce the amounts of Ni and Cu contaminants on the silcion wafer surface.

* This study was financially supported by Semiconductor Industry Collaborative Project between Hanyang University and LG Siltron, and the Brain Korea 21 Plus Project in 2013, Republic of Korea.



(a) (b)

Fig 1. Absorbed amount of Ni and Cu onto the abrasive in the silicon wafer polishing slurry as a function of metal contaminants concentration; (a) TEM image of abrasive, (b) absorbed amount of metal contaminant

[1] M. Miyazaki, M. Sano, S. Sumita, and N. Fujino, Jpn. J. Appl. Phys. 30, 2B, 295-297 (1991)
[2] T. Fukami, T. Takaku, US patent 6,060,396 (2000)

Clone-Resistant Identity for Non-Volatile Self-Reconfiguring SoC Units

W. Adi , S. Zeitouni
University of Braunschweig, Germany
E-mail : {w.adi, s.zeitouni} @tu-bs.de

Non-volatile Self-reconfiguring VLSI units with System-on-Chip (SoC) architecture are emerging as solutions for many modern single chip applications. In this work, we propose a practical and low-cost technique to create physical clone-resistant units. The resulting system security is manufacturer-resistant and even trusted-authority (TA)-resistant. A Trusted Authority authenticates a "post-manufacturing" self-created random unknown Hardware-Software (HW-SW) secret digital function (SUCF) in each SoC unit as shown in Fig.1. The unknown secret function, being implemented as a non-volatile structure, can serve as a permanent electronic-DNA to securely identify each unit by a single one-time consultation of the public trusted authority as shown in Fig. 2. By using such clone-resistant identification infrastructure, a TA can help to establish a secured peer-to-peer link between any two such SoC units. Both trusted authority and SoC manufacturer have a temporary pure helping task without being able to clone units or later intercept identities. No keys are stored permanently; the keys reside in unknown individually self-created structures. The key usage lifetime is kept as short as possible. As a result, keys are not repeatable and can entirely be removed from the device after a secure session is completed. This makes the system more immune against Side Channel Attacks (SCA). The proposed system is low-cost, with scalable security and complexity. As all practical security systems its security is not perfect, however offers a valuable practical pragmatic security. The system was originally proposed in [1] and later refined in [2] for modern SoC units. The system may be occasionally integrated in existing systems with minor changes.

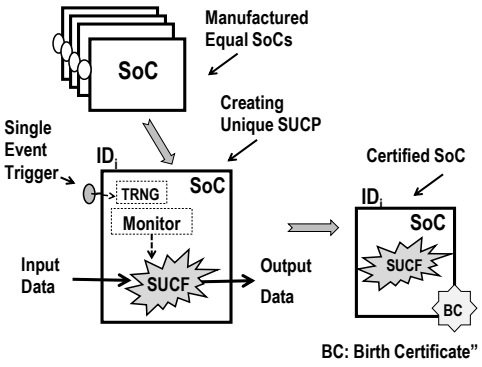


Fig. 1 Clone-resistant Identity Creation Concept

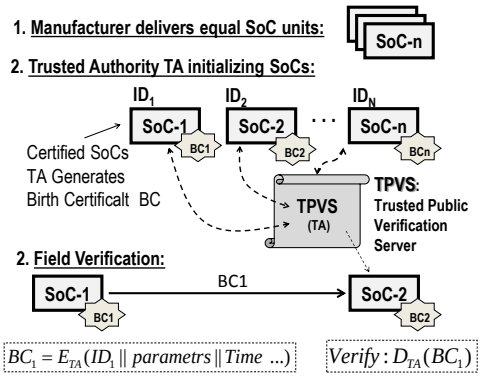


Fig. 2 System Setup and Usage

[6] Wael Adi, Noureddine Ouertani, Abdulrahman Hanoun, Bassel Soudan: "Deploying FPGA self-configurable cell structure for micro crypto-functions". IEEE, ISCC 2009: 348-354

[7] M. Fyrbiak, C. Kison, M. Jeske, W. Adi, "Combined HW-SW Adaptive Clone-Resistant Functions as Physical Security Anchors," in Adaptive Hardware and Systems (AHS), 2013, 2013, pp. 130–137.

Reverse Engineering Essential SSD Characteristics

Seongjin Lee and Youjip Won
Department of Electronics and Computer Engineering, Hanyang University, Seoul 133-791 Korea
E-mail : {insight,yjwon}@hanyang.ac.kr

Recent advancement in NAND Flash memory technology in SSDs such as bits per cell [1] has lead to various applications in storage systems. Along with extending storage capacity of the device, SSDs actively exploit parallelism through channels and ways producing higher bandwidth which is the stepping stone for replacing mechanical storage device. It is true, however, the current computing system is designed with HDD devices in mind, which are not optimized for SSDs. Althouhg there are several issues that have to be addressed before software engineers can properly manuever and work around the issues to make SSDs widely accepted storage medium; however, one of the issues is that NAND characteristics such as size of page, blocks, and units of erase and garbage collection is not disclosed to the public. Flashbench provide a ways to figure out how SDcard is configured; however, since SSDs have more complex architecture, flashbench is insufficient in unmasking the characteristics, especially when SSDs exploit channels and ways to improve the performance. In this paper we propose a methods to expose the size of page and block of the SSDs, and also number of channels that a SSD utilizes. Fig 1 shows the result of finding the page size of a SSD.

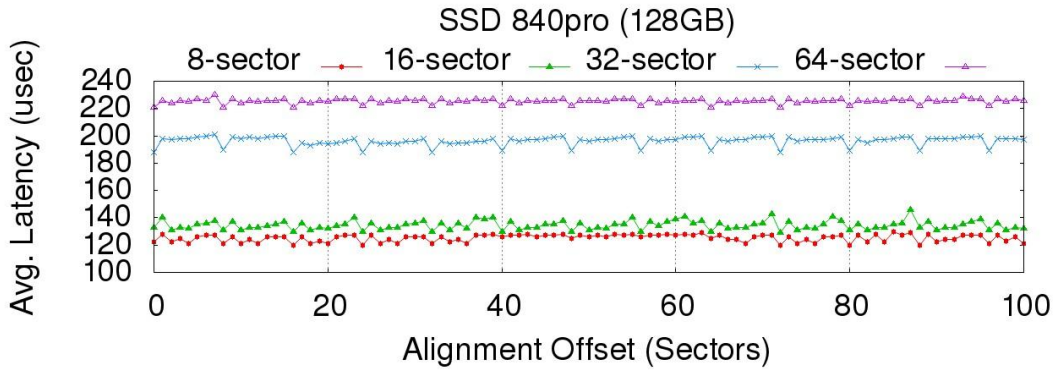


Fig 1. Finding Size of a Page in SSD

[1] GRUPP, L. M., CAULFIELD, A. M., COBURN, J., SWANSON, S., YAAKOBI, E., SIEGEL, P. H., AND WOLF, J. K. Characterizing Flash Memory: Anomalies, Observations, And Applications. In MICRO 42: Proceedings of the 42nd Annual IEEE/ACM International Symposium on Microarchitecture (New York, NY, USA, 2009), ACM, pp. 24–33.

Effect of Flash-based SSD in Virtualized Hadoop

Sangkyu Park, Jae-Ki Hong, Sungyong Ahn, Jongwon Yi and Wooseok Chang
DS Software R&D Center, Samsung Electronics Co.,
95, Samsung 2-ro, Giheung-gu, Yongin-si, Gyeonggi-do 446-811 Korea
E-mail : {skyu7.park, jaeki.hong, sungyong.ahn, jongwon_.lee, wooseok_chang}@samsung.com

Cloud computing is one of the major trends in the recent information technology, receiving attention because of the cost effectiveness and flexibility. The two representative technical paradigms highly related to cloud computing are Big Data and Virtualization. Virtualization is key technology to build infrastructure of cloud computing. It helps for cloud environment to utilize and consolidate various computing resources in a scalable manner. However, underutilization of big data clusters and unrivalled performance of solid state drives (SSD) reopen an opportunity of virtualization of Hadoop framework which is a de facto standard in the big data analytics. In this paper we demonstrate that SSD can not only deliver higher performance on a virtualized Hadoop cluster than a bare-metal Hadoop cluster built with hard disk drive (HDD) storage, but also enable more extensive performance optimizations both in the Hadoop and the hypervisor layer.

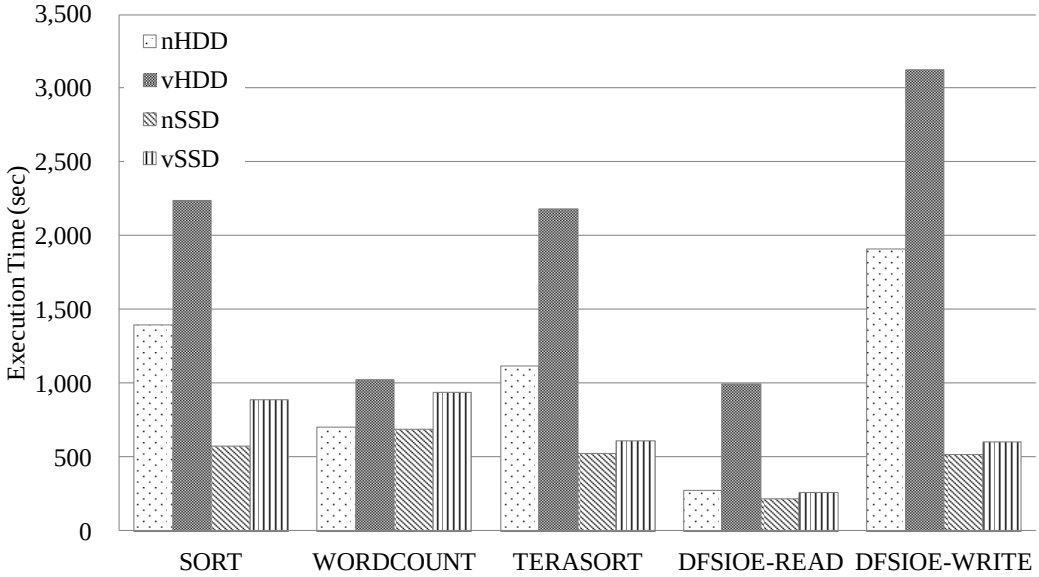


Fig 1. HiBench execution time comparison between bare-metal and virtualized cluster (HDD vs. SSD)

SSD를 위한 트랜잭션 기반 펌웨어 구현

정영진, 김종화, 최종무
Department of Computer Science, Dankook University, Yongin-si, Gyeonggi-do, 448-701, Korea
E-mail : cyj4369@gmail.com

최근 SSD 는 개인용 컴퓨터나 고성능 서버를 위한 용도로 사용량이 점점 늘어나고 있는 추세이다. 하지만, SSD 에 사용되는 플래시 메모리는 물리적 한계 때문에 셀의 마모, 전하의 누수 등 오류[1]가 발생하며 결국 데이터 유지의 문제가 발생한다. FTL 에서는 문제가 발생한 페이지들을 관리해야 하며 이를 위해 해당 페이지들의 위치를 정확하게 파악하고 있어야한다. 이에 따라 펌웨어는 처리된 요청에 대한 결과를 FTL 에 정확히 전달해야 하며, 플래시 메모리의 데이터 처리 실패로 인해 FTL 이 유지하는 매핑정보와 플래시 메모리상에 존재하는 데이터의 위치가 어긋나지 않도록 각 요청을 관리해야한다. 본 논문에서 펌웨어는 이를 효율적으로 수행하기 위해 각 요청에 대해 트랜잭션을 생성하고 전처리 과정과 후처리 과정으로 구분하여 수행한다. 읽기/쓰기 요청이 발생하면 펌웨어는 트랜잭션을 생성하고 FTL 로부터 물리 페이지 번호를 얻은 뒤 플래시 메모리에 명령을 보내는 전처리 과정을 수행한다. 명령이 완료되면 후처리 과정을 통해 각 트랜잭션마다 명령 수행 결과를 유지하여 성공적으로 읽기/쓰기가 수행되었을 경우에만 FTL 의 매핑 테이블이 업데이트될 수 있도록 관리한다. 만약 중간에 실패하는 경우 해당 트랜잭션에 이에 대한 정보를 유지하고 있으며 매핑 테이블은 업데이트 되지 않는다. 그리고 모든 과정이 종료되면 펌웨어는 해당 트랜잭션을 해제한다. 따라서 각 요청의 수행은 원자적으로 관리되며, 이를 통해 FTL 의 매핑 테이블과 물리적으로 저장된 데이터 사이에서 일어날 수 있는 매핑의 불일치를 막을 수 있다.

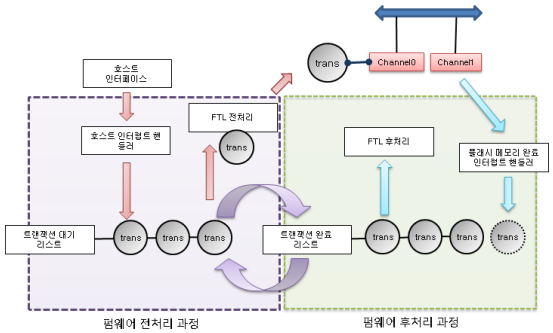


Fig 5. 펌웨어의 요청 수행 흐름

[1] Y. Cai et al., “Error patterns in MLC NAND flash memory: measurement, characterization, and analysis”, DATE 2012.

반도체 디바이스 전자빔 계측 검사 기술

권광민, 오재형, 마성민, 김성수, 유형원
SK Hynix, 2091 Gyeongchung-daero, Bubal-eub, Icheon-si, Gyeonggi-do, Korea
E-mail: gwangmin.kwon@sk.com

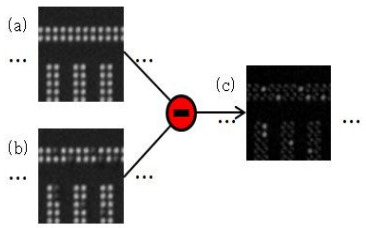
최근 반도체 디바이스 크기가 작아짐에 따라 반도체 공정 기술뿐만 아니라, 수율 저하 불량률을 낮추기 위한 계측 검사 기술도 빠른 속도로 발전해 오고 있다. 그러나, 디자인 룰이 20 nm 이하로 작아지고, 구조의 종횡비 (Aspect Ratio)가 40 이상 높아지며, 3D (적층)화 됨에 따라 일반적인 개념과 방법으로 계측 검사 기술을 조기에 확보하는데 많은 어려움이 발생하고 있다. 지금까지 광학 검사 장비는 미세 불량 검출을 위해 해상도를 높이기 위한 짧은 파장대역 광원에 대한 필요성이 대두 되었지만, 최근에는 수 um 깊이의 불량을 검출하기 위해 긴 파장대역 (700 nm 이상)에 이르는 폭넓은 대역을 활용 할 수 있는 장비가 필요하게 되었다. 마찬가지로 전자빔 계측 기술 분야에서도 기존에 정확한 CD 측정을 위해 해상도를 높이기 위한 기술 개발에서, 높은 종횡비를 가진 구조물의 하부 구조 영상을 확보하기 위해 가속 전압을 높이고 검출된 전자를 선택적으로 취득 제어하려는 노력들을 하고 있다. 전자빔 검사 기술에서는 Interconnection 전극의 크기가 작아짐에 따라 높은 저항 특성을 가지게 되었고 발생하는 불량을 검출하는데 어려움을 겪고 있으며, 이를 극복하기 위해 표면 전위를 조절하는 기술과 전자 취득 효율을 높이기 위한 외부 전위 조절 기술 개발이 진행되고 있다. 이러한 계측 검사 장비 개발과 더불어 시뮬레이션 기술의 접목을 통해 직접적으로 디바이스를 사용하는 손실을 최소화하고 조기에 기술을 확보 할 수 있을 것이다.

Wafer defect inspection by multi-level thresholding of SEM images

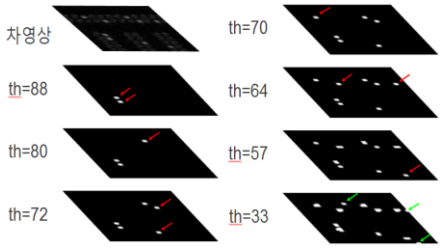
Sunghyon Kim[1], Minwoo Kim[2], and Ilseok Oh[1,2]
[1]*Department of Nano Technology*, [2]*Department of Computer Engineering*
Graduate School, Chonbuk National University, Korea
E-mail : starwise@jbnu.ac.kr

Fast and reliable inspection technology is essential for improvement of yield and productivity in semiconductor device fabrication. For this purpose various inspection technologies have been developed and used for silicon wafers[1]. Inspection of silicon wafers for defect identificaion is usually done by analyzing SEM images of the wafers, but diversity and irregularity of various defects, many sources of noise in SEM image generation, and unpredictable variation of device fabrication process make the image processing quite difficult.

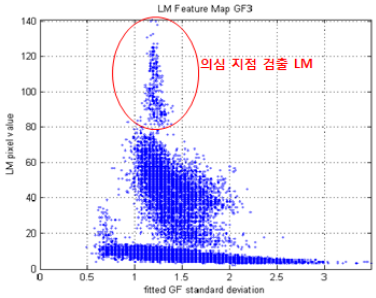
In this paper we present two methods for analyzing SEM images of silicon wafers for defect inspection. The first one is the method of multi threshold levels. In this method we change the threshold level and observe the change in difference images to identify the regions of suspicious defect. When such regions are identified, the intensity distribution of their neighbors is analyzed and find defect pattern. The second one is the method of Gaussian mapping to local maxima. After the mapping operation, the standard deviations of the mapped regions are extracted, which can be used as features representative of the statistical characteristics of various regions. By constructing the feature space and analyzing its spatial distribution we can identify the regions of potential defect.



[Fig 1] (a),(b) A part of wafer image
(c) difference iamge



[Fig 2] Result of multi-threshold processing
(th >=57: defect suspicious regions only appeared(red arrow)
th=33: the other regions appeared at first time (green arrow))



[Fig 3] feature space mapping of LM
(x label: standard deviation
y label: pixel intensity value)

[1] Bong-Jin Yum, Jae Hoon
in Semiconductor Manufacturing: A Bibliographical Review", IEEE International Conference on Automation Science and Engineering, August 20-24, 2012.

저전압 TEM 측정을 이용한 그래핀 형상 및 결정립 관찰

조영지 [1,3], 양준모 [1], Do Van Lam[2], 이승모 [2], 김재현 [2], 박윤창 [1], 장지호 [3]
[1] 나노종합기술원, [2] 한국기계연구원, [3] 한국해양대학교 응용과학과
E-mail : jmyang@nnfc.re.kr

그래핀은 탄소원자 한 층으로 이루어진 2 차원 물질로서, 강도, 열전도율, 전자이동도 등의 여러 가지 특성이 현존하는 물질 중 가장 뛰어나다. 2004 년에 발견된 이래 물리·화학·재료 분야에서 미래의 가장 주목할만한 신소재로 각광받으며 전세계적으로 연구개발되고 있고, 디스플레이, 이차전지, 태양전지, 자동차, 조명 등 다양한 산업에 응용될 것으로 기대된다[1]. 이러한 그래핀의 분석에는 라만분광법을 포함한 광학적 분석이 많이 이용되고 있고, 형상관찰을 위해서는 전자현미경, 원자힘현미경(atomic force microscopy) 등의 방법이 이용되고 있으나 그래핀의 두께는 수 Å 정도로 아주 얇기 때문에 측정하기가 매우 힘들다.

투과전자현미경(transmission electron microscopy: TEM)은 전자빔을 얇은 시료에 통과시켜 투과되거나 회절된 전자를 관찰하는 장비로 수 Å 단위까지 관찰이 가능하기 때문에 그래핀 형상관찰이 가능하다. 보통 TEM 은 200 kV 이상의 가속전압에서 작동하기 때문에 그래핀 관찰시 전자빔에 의해 데미지를 입어 관찰이 어렵다. 그러나 가속전압을 100 kV 이하로 낮추면 데미지를 최소한으로 줄일 수 있으므로 저전압 TEM 측정은 그래핀의 형상관찰에 가장 적합한 방법이다.

본 연구에서는 TEM 의 가속전압을 80 kV 로 낮추어서 그래핀을 관찰하였다. CVD 방법으로 Cu 기판 위에 성장한 그래핀은 기판식각 및 이동과정을 거쳐 Au 천공막 그리드 위로 옮겨졌다. 만들어진 그래핀 시편은 가속전압을 80 kV 로 낮추어서 TEM 영상 및 암시야상 측정으로 결정립을 관찰하였고, 고분해능 TEM 측정과 고속퓨리에변환(fast Fourier transform: FFT)을 통해 그래핀의 구조를 확인하였다.

감사의 글: 본 연구는 미래창조과학부 및 정보통신산업진흥원의 대학 IT 연구센터 육성지원 사업의 연구결과로 수행되었음(NIPA-2013-H0301-13-2009).

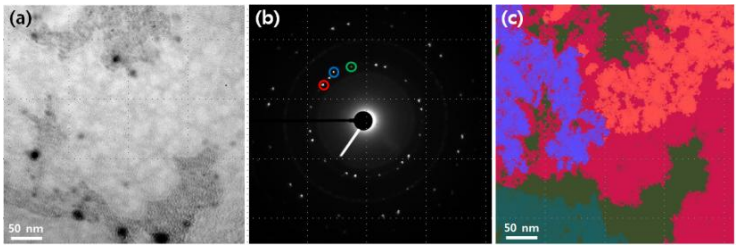


그림 9. 암시야상 TEM 측정을 이용한 그래핀 결정립 관찰.

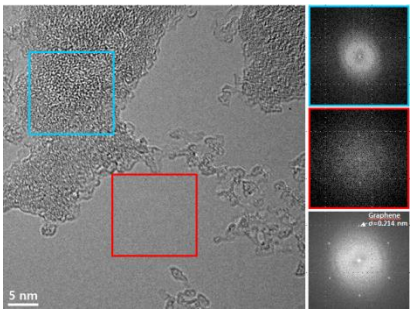


그림 8. 고분해능 TEM 및 FFT 영상.

[1] T. J. Booth, P. Blake, R. R. Nair, D. Jiang, E. W Hill, U. Bangert, A. Bleloch, M. Gass, K. S. Novoselov, M. I. Katsnelson and A. K. Geim, Nano Lett. 8, 2442 (2008).

Accelerating defect inspection technology by next-generation inspection platforms

Jeongho Ahn, Shijin Seong, Hyungseop Kim, Dong-Ryul Lee, Heewon Sunwoo, Dong-chul Ihm, and Soobok Chin

Process Development Team, Semiconductor R&D Center, Samsung Electronics Co., Korea

E-mail : bifidus.ahn@samsung.ac.kr

The shrink of design rule is one of main factors which drives the wafer inspection requirements. The cycle of the advent of new inspection tools is getting shorter due to a lot of requests from chip makers. However, we still do not know that we are fully ready for the next generation device development. The CDs and spaces are most critical in defect inspeciton. Therefore defect arrays are designed on a EUV patterned mask to evaluate the defect detection sensitivity for several optical and e-beam inspection tools. The inspection mode of each tool is optimized to enhance the detection sensitivity, and some simulation works were conducted to analyze the defect signals and further analysis. This result represents the capabilities and limitations of the current wafer inspection tools.

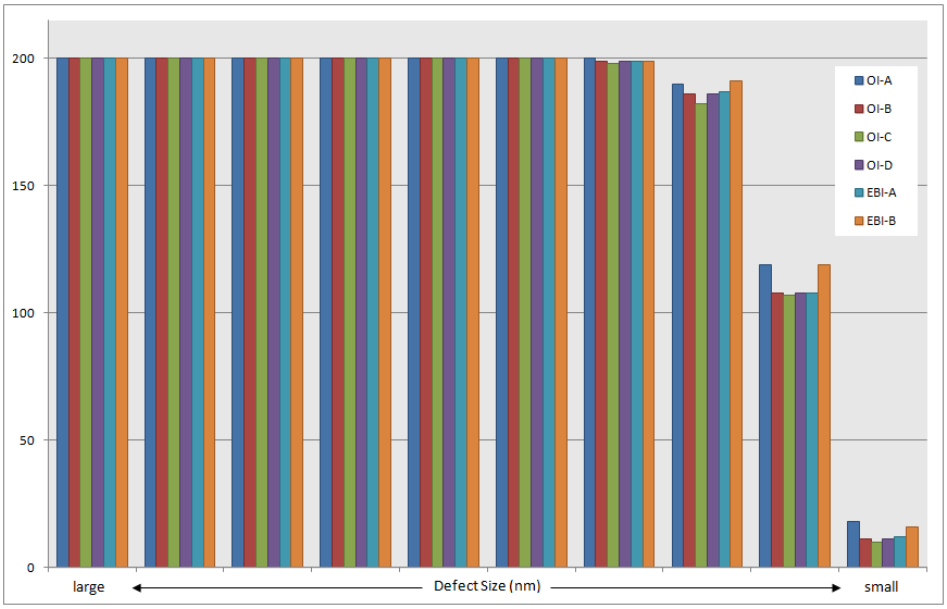


Fig 1. Pareto chart of detected defects on several inspection tools

[1] “Investigation of the performance of state-of-the-art defect inspection tools within EUV lithography”, Dieter Van den Heuvel, Proc. of SPIE Vol. 8324, 83240L (2012).

[2] “Transistor Architecture Impact on Wafer Inspection”, Timothy F. Crimmins, Proc. Of SPIE Vol. 8324, 83240C (2012).

A Robust DC-DC Converter Protection Scheme for Enhanced PMIC Reliability

Yoo-Jun Jeong, Sang-Ik Cho, Hyoung-Seok Oh, and Byeong-Ha Park

Power Device Development Team, System LSI Division, Samsung Electronics Co., Ltd.
E-mail : yoojun.jeong@samsung.com

Recently, DC-DC switching converts are widely used in various electronic systems for high efficiency, especially in mobile and display PMIC. And, the robustness of DC-DC converter has a critical impact on the reliability of whole system[1]. Thus, the converters must have the protection circuit which can protect itself and the application system from various fault conditions. The protection circuit must embody not only dynamic protection functions such as over current/voltage detection, but also static protections such as external component floating, pad-to-pad short and so on caused by the unwanted PCB board conditions. In this paper, the static protection circuit which can prevent the system failure due to the switch node-open/short without additional external components and power loss is proposed. The proposed protection circuit protect three fault conditions, inductor floating, swtich node-to-ground short, and switch node-to-VIN short, by sensing the switch node voltage (V_{SW}) in the initial state of starting the converter. The proposed protection circuit was simulated and fabricated using a 130nm CMOS process, and has been verified by the experiment with the DC-DC Buck converter.

Fig 1. Buck converter with the proposed protection circuit and its timing diagram.

(a) Inductor floating. (b) Switch node-to-V_{IN} short. (c) Switch node-to-ground short.

Fig 2. Experimental results of three protection cases.

[1] H. Sheng, F. Wang, and C.W. Tipton, "A Fault Detection and Protection Scheme for Three-Level DC–DC Converters Based on Monitoring Flying Capacitor Voltage," *IEEE Trans. Power Electron., vol. 27, no. 2,* pp. 685-697, Feb. 2012.

A Digitally-controlled, Glitch-free, 5-GHz Phase Interpolator

Chang Soo Yoon, Woorham Bae, and Deog-Kyoon Jeong
Department of Electrical and Computer Engineering, Seoul National University, Seoul 151-747, Korea
E-mail : csyoon@isdl.snu.ac.kr

Clock and data recovery (CDR) circuit is one of the most important circuits in receiver system and it should be designed properly for chip-to-chip communication. Phase interpolator (PI) based CDR whose block diagram is shown in the figure 1, is one kind of CDR for forwarded-clock system. PI, different from voltage controlled oscillator (VCO), can be controlled easily and high-order loop filter is unnecessary. To use PI in data recovery system, it should be able to do weighted summation of 2 input clocks. And those 2 input clocks should be overlapping clocks to prevent slew rate degrading. [1] So in this paper, proposed PI uses two neighboring, and overlapping, clocks of multi-phase clock that is selected by MUX. Proposed PI and MUX are controlled digitally and free from glitch. Simulation is performed in Samsung 65nm technology. 5-GHz, 8-phase clocks are used as input of MUX to generate 48 steps of output clock.

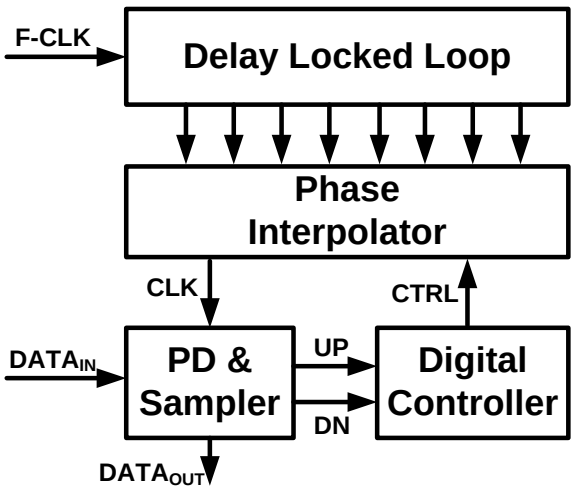


Fig 1. Phase interpolator based CDR

[1] Mohamed Benyahia, Jean Batiste Moulard, Franck Badets, Anouar Mestassi, Thomas Finateu, Lionel Vogt and Fabrice Boissieres, “A digitally controlled 5GHz Analog Phase Interpolator with 10GHz LC PLL”, Design & Technology of Integrated Systems in Nanoscale Era, 2007. DTIS. International Conference on.

저전력 대 출력 신호 스위치드 캐패시터 앰프 설계

이 현의*, 최 정환*, Masaya Miyahara**, Akira Matsuzawa**
삼성전자 메모리사업부 DRAM 설계팀*
동경공업대학교 이공학연구과 전자물리공학전공**
E-mail : hyunui.lee@samsung.com

앰프를 사용하는 아날로그 시스템을 설계할 때, 앰프의 소비 전력 및 출력 신호 범위는 시스템의 성능에 큰 영향을 미친다. 높은 이득을 얻기 위해 필수적인 캐스코드 구조의 앰프 중에서 폴디드 캐스코드 앰프는 출력 신호 범위가 넓지만 소비 전력이 크다는 단점이 있고, 텔레스코픽 앰프는 소비 전력은 낮지만 출력 신호 범위가 좁은 문제가 있다. 본 논문에서는 저 소비 전력 몇 대 출력 신호를 달성하기 위해 새로운 구조의 앰프를 설계하였다. 그림 1 에 메인 앰프의 회로도를 제시하였다. 설계한 앰프는 텔레스코픽 앰프를 베이스로 삼고 있지만 앰프의 바이어스 전류를 결정하기 위한 테일 트랜지스터를 제거하여 출력 신호 범위를 확대하였다. 테일 트랜지스터 대신에 앰프의 바이어스 전류를 결정하기 위해 M_{NB1}, M_{NB2} 를 추가하여, 전류를 미러링하는 방식으로 바이어스 전류를 결정하고 있다. 앰프의 입력은 CMOS 타입으로 설계하여 g_m 을 향상시켰으며, 전류를 결정하기 위한 피드백 루프 이외에 출력 신호의 코몬 레벨을 정하기 위한 피드백 루프도 형성되어 있다. 그림 2 에 구체적인 전류 바이어스 방법을 설명하였다. 우선 앰프에 필요한 바이어스 전류 ($2I$) 가 바이어스 회로로부터 공급된다. 이 전류는 M_{NB1} 과 M_{NB2} 에 각각 I 씩 흘러 들어간다. 이 때, M_{NB1} 과 M_{N3} 사이에 1:α의 사이즈 비율이 있다면, M_{N3} 에 흐르는 전류는 αI 가 된다. 이렇게 설정된 바이어스 전류를 일정하게 유지시키기 위해, 입력 NMOS 트랜지스터의 벌크 전위에 피드백 루프를 형성하였다. 이러한 원리를 통해서 설계한 앰프는 텔레스코픽 앰프의 저 소비 전력 특성 및 폴디드 캐스코드 앰프의 대 출력신호 범위를 동시에 달성하였다.

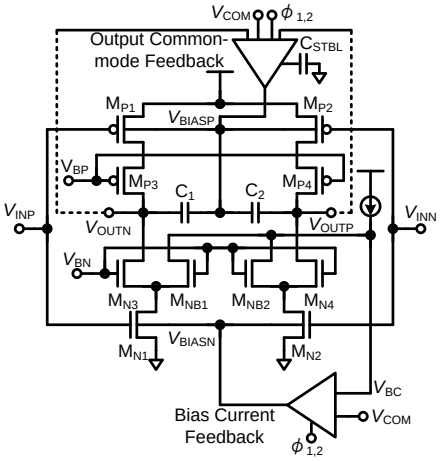


그림 1. 메인 앰프의 회로도

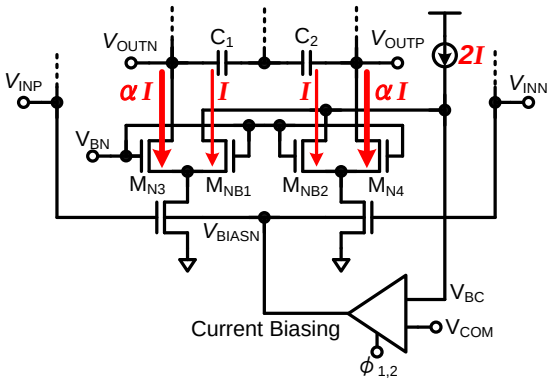


그림 2. 메인 앰프의 전류 바이어스 방식

A SUC-based 10 bit 1 GS/s Current Steering DAC in 0.042 mm^2

김시내, 김미란, 류승탁
한국과학기술원 전기 및 전자공학과
E-mail: sinai@kaist.ac.kr, kmeeran@kaist.ac.kr, stryu@kaist.ac.kr

고속 고해상도 current steering DAC 설계에 있어서 전류원 정합성을 충족시키며 작은 칩 면적을 구현하는 것은 가격경쟁력뿐만 아니라, 동적 선형성과 전력 소모 측면에서 매우 중요하다. 이차원의 단위 전류원 매트릭스 배열은 우수한 정적 선형성으로 인해 고해상도 DAC 설계에서 자주 사용된다. 그러나 넓게 퍼져있는 많은 전류원들 간의 연결과 이를 다시 캐스코드 트랜지스터까지 배선해야 하므로, 연결선의 길이는 매우 길어지고 복잡해지며 필연적으로 칩의 면적은 커지게 된다. 본 설계에서는 연결선의 길이를 최소화하기 위해서 단위 전류원과 입력 데이터를 제어하는 회로들을 일렬로 쌓아 올린 적층식 셀(Stacked Unit Cell)[1]을 사용하였고, 이 셀들을 선형으로 배치하여 배선을 짧게 하고 배선으로 인한 칩 면적의 증가를 최소화하였다. 또한, 5 bit MSB 와 5 bit LSB 분할 구조를 구현함에 있어 LSB 전류원을 병렬 연결하여 MSB 전류원을 구성하는 일반적인 설계 방법을 사용하지 않고, 그림 1 과 같이 MSB 의 단위 전류량(I_{MSB})을 분할하여 LSB 비트들을 구현함으로써 전체 전류원의 개수를 64 개로 크게 감소시켰다. 출력 임피던스의 정적 선형성을 보장하기 위한 요건을 만족시키기 위해, 전류원은 triple cascode 구조를 사용하였고 MSB 와 LSB 단위 전류원간의 출력 임피던스의 선형성을 유지하도록 설계 하였다. 전류원의 일차원 배치로 인한 선형성의 저하를 방지하기 위해서 MSB 영역은 hierarchical symmetric switching 기법을 적용하였고, LSB 영역에는 일차원 common-centroid 배치를 사용하였다. 제안된 10 bit DAC 는 0.18 μm CMOS 공정을 사용하여 설계되었고 그림 2 와 같이 레이아웃 되었다. State-of-the-art 수준의 0.13 μm CMOS 공정의 10 bit 설계[2]와 비교할 때, 코어의 면적은 91.6% 감소하였다. 동적 선형성을 검증하기 위한 모의실험 결과를 그림 3 에 나타내었다. 1GHz 의 샘플링 속도에서 Nyquist 출력신호 주파수까지 62dB 이상의 SFDR 성능을 확인 하였고, 최대 동작 속도에서 34.2mW 의 전력 소모량을 보였다.

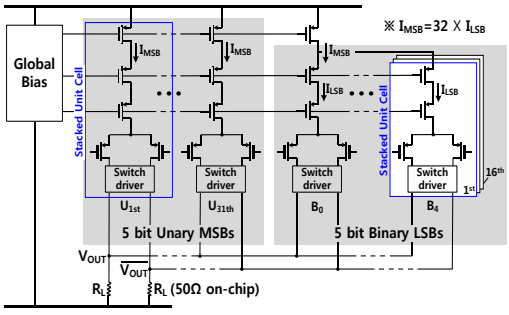


그림 1. MSB 와 LSB 단위 전류원

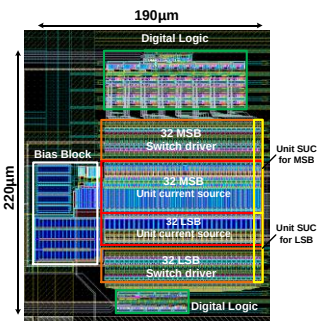


그림 2. DAC 의 레이아웃

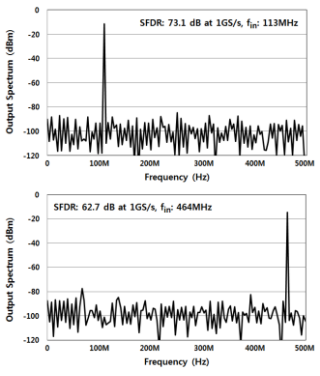


그림 3. 출력 스펙트럼

[1] Si-Nai Kim, Wan Kim, Chang-Kyo Lee, and Seung-Tak Ryu, JSTS (2012).
[2] Pieter Palmers, Michiel S. J. Steyaert, IEEE Trans. Circuits Syst. I (2010).

A Single-Inductor Multiple-Output (SIMO) DC-DC Converter with Wide Operation Voltage Range for Mobile Devices

Whan-Seok Seo, Hyun-A Ahn, Young-Ho Jung, Ki-Soo Nam, Jae-Hyung Jung, Seong-Kwan Hong, and Oh-Kyong Kwon

Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea

E-mail : okwon@hanyang.ac.kr

In mobile devices, the extension of the operating voltage range in power management block is an effective solution to prolong the operating time without adding the cost or sacrificing the performance [1]. In order to do this, the reliable output voltages have to be generated in power management block of mobile devices when the voltage of Li-ion battery is lowered. In this paper, the SIMO (Single-Inductor Multiple-Output) DC-DC converter is proposed to widen the operating voltage range. The operating modes of the proposed SIMO DC-DC converter are composed of buck mode and buck-boost mode and are determined adaptively according to input voltage. The proposed SIMO DC-DC converter is simulated by using a 0.18 μm CMOS process technology with high voltage devices of 5 V. It has maximum power efficiency of 92.4% and its minimum operating voltage decreases from 3.3 V to 3.0 V. Consequently, the proposed SIMO DC-DC converter is well suited to power management block in mobile devices.

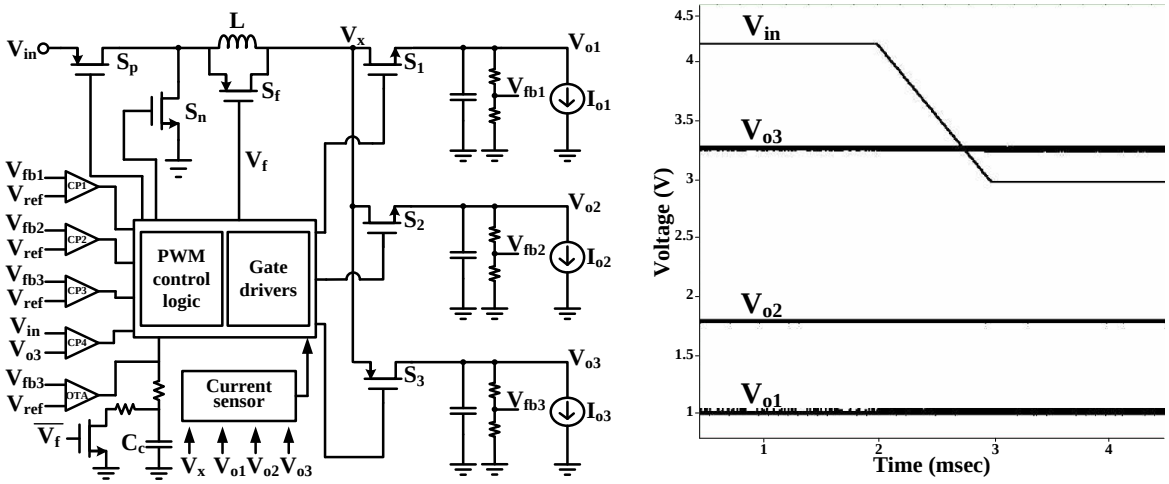


Fig. 1. Schematic diagram and simulated results of the proposed SIMO DC-DC converter.

[1] S. Nomura, F. Tachibana, T. Fujita, T. Chen Kong, H. Usui, F. Yamane, IEEE Int. Conf. IC Design and Technology, 129-134(2009).

HetNoC3D: A User Friendly Simulation Framework for Homogeneous and Heterogeneous 3D NoC Architectures

Michael Opoku Agyeman
School of Engineering and Built Environment, Glasgow Caledonian University, Glasgow, UK
E-mail : Michael.Agyeman@gcu.ac.uk

To meet the high design and validation cost of multi-core applications, simulators which facilitate the evaluation of best design options of systems before actual implementation have emerged as an inevitable solution in both research and industrial design flow [1]. This paper presents Heterogeneous 3D NoC simulator, HetNoC3D, a Graphical User Interface (GUI) based 3D NoC simulation framework for exploring the performance of homogeneous and heterogeneous on-chip networks. The simulator, developed in C++, serves as a user friendly cycle-accurate 2D and 3D NoC integrated evaluation tool which allows modeling of hardware modules including NoC components as well as routing and mapping algorithms for homogeneous and heterogeneous 3D NoCs of variable NoC dimensions. The simulator provides a real-time graphical update of network average packet latency and simulation progress for a given configuration.

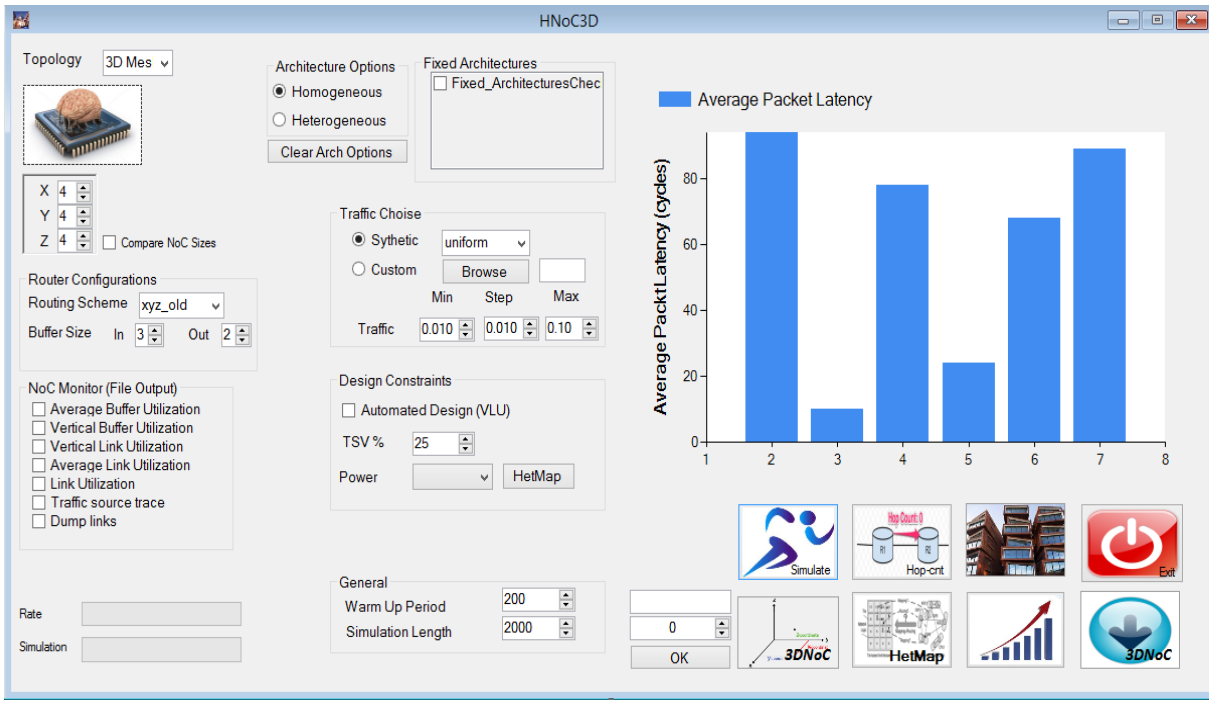


Fig 1. HetNoC3D Framework

[1] Micro Magic Inc, http://www.micromagic.com, [Online; accessed July-2010].

Database 성능 평가를 위한 SQLite Trace 추출 환경

이성광, 유승주, 이승구
Department of Electronic Engineering, POSTECH, Pohang 790-784, Korea
E-mail : gwangyi@postech.ac.kr

SQLite 는 별도의 서버를 두지 않고도 SQL 을 이용한 데이터베이스를 사용할 수 있다는 특징으로 인해 다양한 응용프로그램에서 사용되고 있다. 이는 모바일 시스템에서도 마찬가지로, 높은 시장 점유율을 보이고 있는 Android 시스템에서는 OS 에서 SQLite 지원을 제공하고 있는 실정이다.

하지만 SQLite 는 데이터베이스가 제공해야 하는 무결성을 만족시키기 위해 여러 번의 Synchronized Write 가 요구되며, 이는 전체적인 성능 저하를 야기하는 원인이 되고 있다[1]. 이를 해결하기 위해 다양한 방법들이 제안되고 있지만, Android 와 같은 모바일 환경에서는 일상에서 사용하는 응용프로그램들은 매우 높은 정도로 사용자와 상호작용을 하기 때문에 정적인 테스트 환경을 갖추기가 어려워 실험 결과를 분석하는데 어려움이 있었다. 특히, phase-change RAM (PRAM)과 같은 데이터의 값에 따라 다른 특성을 보이는 메모리를 활용하는 SQLite 구현을 평가하는 경우 SQLite 명령뿐 아니라 SQLite DB 및 journal 데이터 역시 재현 가능한 실험환경이 필요하다.

본 논문에서는 특별히 Android 시스템에서 수행되는 일상적인 응용 프로그램에서 SQLite 테스트를 위한 환경을 구축하기 위한 방법을 소개한다.

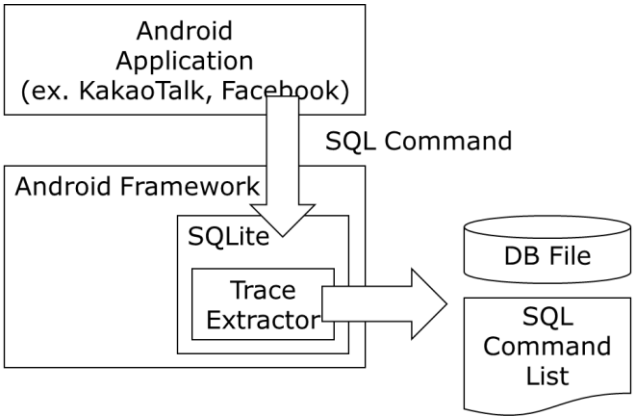


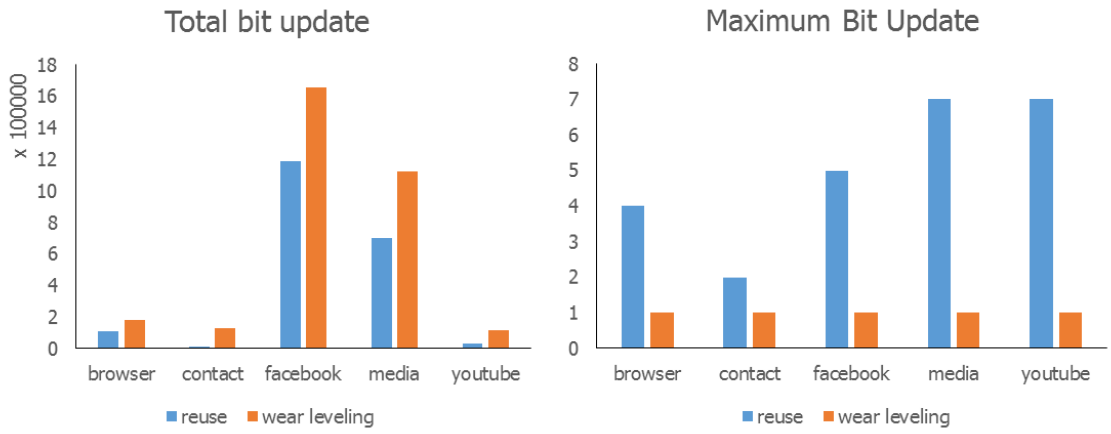
Fig 1. SQL Trace 추출 환경 구조

응용프로그램을 개별적으로 수정하는 것은 일반적으로 대부분의 응용프로그램이 소스코드를 공개하지 않고 배포되는 점과 일부 DB(연락처, 계정 정보 등)의 경우 응용프로그램에서 직접적으로 SQLite 를 사용해서 접근하지 않고 Android Framework 에서 제공하는 API 를 통해 접근하도록 되어 있다는 점에서 부적절하다. Android 의 경우 Open Source Project 로 각 개별 스마트폰 제조사에 접촉하면 Android Framework 소스코드를 얻을 수 있도록 되어 있다. 이를 통해 SQLite 라이브러리의 소스코드를 얻어 SQLite Trace Extractor 를 추가하여 스마트폰에 있는 기본 SQLite 라이브러리를 대체함으로써 Trace 를 얻는다. System wide SQLite 라이브러리를 교체함으로 인해서 Android 스마트폰에서 발생하는 모든 SQL 명령을 얻어낼 수 있다.

SQLite Trace Extractor 는 크게 두 부분으로 이루어져 있다. 첫 번째는 SQL command 를 추출하는 SQL command extractor 로,

SQLite 에서 모든 SQL command 를 수행하는 함수 뒤에서 수행한 SQL command 를 얻어내 Android Logcat 라이브러리를 통해 PC 로 전송한다. 보통 성능평가를 위해 사용하는 벤치마크 응용프로그램과는 달리, 일상적인 응용프로그램은 이전에 사용했던 패턴에 영향을 받는 경우가 많으므로 사용된 SQL command 만으로는 정상적인 실험 결과를 재생산할 수 없다. 따라서 두 번째 부분인 SQL DB file extractor 가 필요하다. 이 부분은 SQLite DB 파일을 열기 전에 미리 DB 파일을 Android 스마트폰 내의 특정 장소에 복사해둠으로써 SQLite command 가 적용되기 전의 원래 DB 파일을 백업해둔다. 백업된 DB 파일은 추출된 SQL command 를 재실행시킬 때 초기상태로 사용된다. 부가적으로, SQLite 는 동시에 여러 DB 파일을 작업할 수 있는데 연결된 DB 마다 유일한 ID 를 부여하여 각각의 SQL command 가 어느 DB 를 대상으로 작업했는지 볼 수 있도록 하였다.

구현한 SQL Trace Extractor 를 검증하기 위해 Android Application 중 5 개를 택하여 Trace 를 얻은 후 이를 이용해 SQLite DB Journaling 실험을 진행하였다. SQLite 에서 기본적으로 사용되는 Rollback Journal 구현은 journaling 을 위해 일반 파일로 journal 을 기록하는 형태로 구현되어 있다. 이를 주 메모리의 일부로 구현된 PRAM 에 저장한다고 가정한 뒤 PRAM 메모리 관리 방법에 따라 전체 bit update 가 얼마나 차이나는지, 그리고 메모리 각 셀당 최대 bit update 횟수는 얼마나 나오는지를 구해 보았다.



Reuse 는 이전에 사용했던 영역을 동일한 데이터가 journaling 될 때 재사용하는 구현이고 wear leveling 은 한번 사용한 메모리 영역은 다시 재할당하지 않는 구현이다. SQLite 는 특성상 데이터를 특정 단위로 I/O 를 하게 되는데, 메모리 영역을 재사용 하게 되면 자주 바뀌지 않는 부분은 값이 변하지 않은 채 써지므로 전체 bit update 를 최소화시킬 수 있었다. 반면에 빈번하게 재사용하게 되어 최대 bit update 횟수는 증가하는 것을 볼 수 있다. 이에 비해 wear leveling 의 경우 매번 모든 데이터를 다 메모리에 써야 하므로 전체 bit update 는 늘어나지만, 한번 사용한 뒤에 재사용하지 않기 때문에 최대 bit update 횟수는 1 로 균일한 것을 볼 수 있다.

우리는 이러한 방법으로 랜덤성이 강한 Android 어플리케이션에서 정적인 SQLite Trace 를 추출해 내고 이를 통해 어플리케이션에서 행했던 DB 접근을 재현해낼 수 있는 환경을 갖추었고, 간단한 실험을 통해 이 환경이 제대로 동작한다는 것을 볼 수 있었다.

[1] Lee, Kisung, and Youjip Won. "Smart layers and dumb result: IO characterization of an android-based smartphone." Proceedings of the tenth ACM international conference on Embedded Software. ACM, 2012.

Module Regrouping for Minimizing Wrapper Cells in SoC Testing

김상민 [1], 홍정민 [1], 배상민 [2], 신영수 [1]
[1]KAIST 전기및전자공학과, [2]LG 전자

SoC 는 테스트 복잡도를 줄이기 위해 칩을 모듈 단위로 분할하여 modular testing 을 주로 한다. 각 모듈의 입/출력은 F/F 이 아닌 경우 그림 1(a)과 같은 F/F 이 포함된 래퍼 셀을 추가하게 된다. 래퍼 셀의 개수를 줄이기 위해 [1]에서는 그림 1(b)와 같이 서로 연결된 모듈 사이의 두 래퍼 중 한쪽을 제거하고, 남아 있는 래퍼를 양쪽 모듈이 같이 사용하도록 하였다. 그러나 이 경우 두 모듈을 같이 테스트할 수 없게 되어 그림 1(b)와 같이 테스트 시간이 증가할 수 있다.

본 논문에서는 래퍼의 개수를 보다 더 줄이기 위해 그림 1(c)와 같이 모듈 regrouping 을 제안한다. 즉, 모듈 1 과 2 를 하나의 모듈로 취급하고 그 사이의 래퍼를 모두 제거한다. 두 모듈의 regrouping 여부는 두 모듈 사이의 래퍼 셀 개수와 regrouping 적용으로 증가하는 테스트 시간을 고려하여 결정한다. 또한, 테스트 시 사용할 수 있는 최대 테스트 핀의 개수에 의해서도 regrouping 대상이 한정된다. Regrouping 이 적용된 모듈들은 테스트 시간이 과다하게 증가하지 않도록 하는 것이 중요한데, 본 논문에서는 이를 위해 regrouping 이후 scan chain 을 새롭게 설계하고 래퍼를 입/출력마다 선택적으로 제거하도록 하였다. Memory controller 에 대해 제안하는 방법을 적용한 결과 래퍼의 개수는 24% 줄이면서 테스트 시간의 증가는 10%로 유지할 수 있었다.

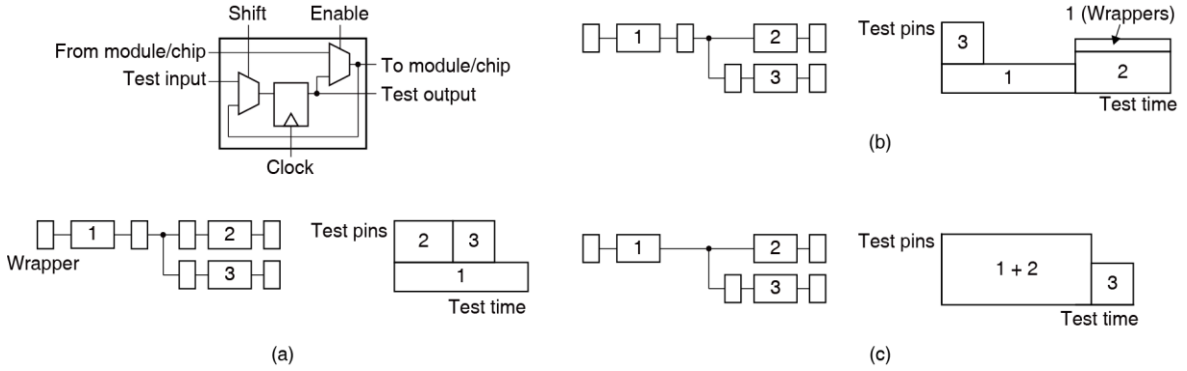


그림 1. (a) 래퍼 셀과 래퍼 셀을 사용한 예제 회로 및 테스트 scheduling, (b) 기존 래퍼 개수 감소 방법을 적용한 예제 회로 및 테스트 scheduling, (c) 제안하는 래퍼 개수 감소 방법을 적용한 예제 회로 및 테스트 scheduling.

참고문헌

[1] Q. Xu and N. Nicolici, “On reducing wrapper boundary register cells in modular SOC testing,” Proc. ITC, pp. 622-631, 2003.

Accurate Frequency Spectrum Analysis of Event-Driven Simulation Results of Analog/Mixed-Signal Circuits

Junsuk Kim, Ji-Eun Jang, and Jaeha Kim

Department of Electrical and Computer Engineering, Inter-university Semiconductor Research Center

Seoul National University, Seoul, Korea

E-mail: jskim@mics.snu.ac.kr

Frequency-domain spectrum analysis of time-domain continuous-time waveforms always involve approximation errors, since the waveform must be sampled in unform time steps and its discrete-time Fourier transform (DTFT) must be approximated with a discrete Fourier transform (DFT), also known as fast Fourier transform (FFT). For instance, the need for a uniform-time-sampled waveform means that the analog circuit simulator like SPICE can no longer exploit the variable time-stepping algorithm. Also, the waveform must capture the exact periodicity of the signal or various windowing methods must be employed in order to suppress various artifacts due to the differences between DFT and DTFT.

This paper demonstrates that the frequency spectrum analysis can be carried out directly in continuous-time domain when the simulated signal waveform is expressed in a functional form, for instance, as a series of $t^m exp(at) \cdot u(t)$ events. The frequency spectrum of the signal can then be computed over an infinite frequency range without sacrificing the simulation speed. It has been reported in [1]-[2] that when a waveform is expressed in this particular form, rather than as a series of time-value pairs, various circuits and systems including linear filters/ampfliers, switched-linear circuits such as buck/boost DC-DC converters, and circuits with large-signal nonlinear effects such as RF power amplifiers can be simulated in a purely event-driven fashion, enabling a fast and accurate simulation of complex mixed-signal systems on a single simulation platform like SystemVerilog. The experimental results with the case of estimating the spectral regrowth due to the nonlinearity in the RF power amplifier circuit show that the proposed spectrum analysis can achieve virtually perfect accuracy with 300× speed-up in the overall execution time (Fig. 1).

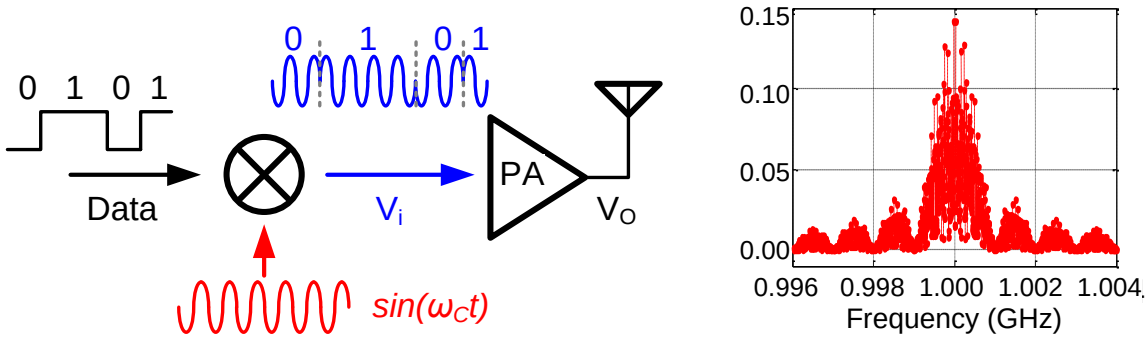


Fig. 1. Simulation and analysis of the spectral regrowth of an RF transmitted signal. The functional expression of the signal and event-driven simulation algorithm result in 300× faster simulation speed compared to HSPICE with almost ideal accuracy.

[1] J.-E. Jang, et al., "True Event-driven Simulation of Analog/Mixed-signal Behaviors in SystemVerilog: a Decision-Feedback Equalizing (DFE) Receiver Example," in IEEE Custom Integrated Circuits Conf. (CICC), pp. 1–4, Sep. 2012.

[2] J.-E. Jang, et al., "Event-Driven Simulation of Volterra Series Models in SystemVerilog," in IEEE Custom Integrated Circuits Conf. (CICC), pp. 1–4, Sep. 2013.

Highly uniform, electroforming-free, and self-rectifying resistive memory in $Pt/Ta_2O_5/HfO_{2-x}/TiN$ structure

Jung Ho Yoon,* Seul Ji Song, Il-Hyuk Yoo, Jun Yeong Seok, Kyung Jean Yoon, Tae Eun Kwon, Tae Hyung Park, and Cheol Seong Hwang

Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, (Korea)

*E-mail : yjh1309@snu.ac.kr

Although resistance switching random access memory (ReRAM) has attracted a great deal of attention as one of the most promising next-generation non-volatile memory devices, it has several obstacles to overcome presently to be used in mass-production. Among them, development of RS memory cell which contains rectification functionality in itself, highly reproducible RS performance, and electroforming-free characteristics are the impending tasks. The method for solving these problems can be generally stated as having a two-layered dielectric structure, where one layer (in this case HfO_2) works as the resistance switching layer by changing its chemical state, while the other dielectric layer (in this case Ta_2O_5) remained intact during the whole switching cycle, which provides the rectification. In addition, the RS layer should have lower dielectric constant compared with the rectifying oxide layer to make the integral part of voltage effectively applied over the RS layer. In addition, the energy gap of the RS layer should be higher than that of the rectifying oxide layer to make the carrier transport in the forward (or switching) bias polarity not to be disturbed by the conduction band offset between the two dielectric layers.

The present combination of Ta_2O_5 and HfO_2 layer which are in contact with the Pt and TiN electrode, respectively, nicely fits to the above mentioned conditions for achieving the desired multitude of functionality from one RS system. In addition, plasma-enhanced atomic layer deposition process for the Ta_2O_5 on the underlying HfO_2 makes the HfO_2 to have just enough density of oxygen vacancies to induce the fluent RS within the layer. The careful tunings of operation voltage and compliance current are another key ingredient to achieve the required functionality. With the optimized structure and operation conditions for the given materials, excellent RS uniformity, electroforming-free and self-rectifying functionality could be simultaneously achieved from the $Pt/Ta_2O_5/HfO_2/TiN$ structure.

S-doped TiO_2 as a selection diode for ReRAM

Dae Eun Kwon[1*], Jong Ho Lee[2], Jung Ho Yoon[1], Seul Ji Song[1], Kyung Jean Yoon[1], Tae Hyung Park[1], Tae Joo Park[3], and Cheol Seong Hwang[1]

[1]*Department of Materials Science and Engineering, Seoul National University, Seoul 151-747, Korea*

[2]*Department of Materials Science and Engineering University of Pennsylvania,3231 Walnut Street, LRSM 419 Philadelphia, PA 19104*

[3] *Department of Materials Engineering, Hanyang University, Ansan, 426-791, Korea*

[*]E-mail : comkdy@gmail.com

차세대 메모리 중 하나인 저항변화 메모리 (ReRAM : resistive random access memory)는 외부에서 전압을 인가함으로써 높고 낮은 저항상태를 전환하여 데이터를 쓰고 읽는 소자이다. 저항변화 메모리는 이상적으로 $4F^2$ 의 단위 소자 크기를 가지는 crossbar array 구조에서 동작 가능하므로 고집적화를 이루기 용이하다는 장점이 있어 크게 주목 받고 있다.[1] 하지만 crossbar array 구조에서 읽기, 쓰기 동작을 구현할 때 필연적으로 인접 소자로부터의 누설전류(sneak path current)가 간섭을 일으키는 문제점이 있어 이를 차단할 수 있는 선택소자가 필요하다. 특히 고집적 crossbar 소자 구현을 위해서는 메모리 소자의 저저항 상태를 고저항 상태로 전환시키기에 충분히 높은 전류밀도를 가지면서, 동시에 누설전류를 차단할 수 있는 우수한 정류 특성을 가지는 선택소자가 개발되어야 한다.[2]

본 연구에서는 정류특성이 우수한 선택소자 개발을 위해 Si/SiO_2(100nm)/TiO_2/Pt(50nm)기판상에 60nm 두께의 TiO_2 박막을 원자층 증착법을 이용하여 증착 한 후 H_2S 분위기에서 여러 온도(350℃ ~ 550℃)의 rapid thermal annealing 처리를 통해 TiO_2 박막에 부분적으로 S 를 도핑하여 Pt/S-doped TiO_2/TiO_2/Pt 구조를 갖는 소자를 제작하였다. 결과적으로, Pt/TiO_2/Pt 구조에 H_2S 열처리를 함으로 인해 정방향 전류밀도는 증가, 역방향 전류밀도는 감소하는 현상을 확인할 수 있었고, 450℃의 열처리에서 가장 좋은 선택소자로서의 특성이 보임을 확인할 수 있었다.

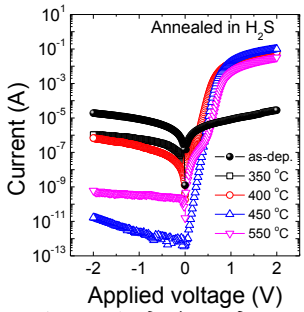


Figure 1.H_2S 열처리 전 TiO_2(as-dep)와 온도별 H_2S 열처리를 한 TiO_2의 I-V 특성

[1] Linn, E., Rosezin, R., Kugeler, C., Waser, R., Nature Materials 18 (2010)

[2] Chang S. H., Lee S. B., Jeon D. Y., Park S. J. Kim G. T., Yang S. M., Chae S. C., Yoo H. K., Kang B. S., Lee M., et al., Advanced Materials 23 (2011)

Metal-Insulator-Transition in nano scale $SmNiO_3$ for selector application with BEOL compatibility

Saiful Haque Misha, Nusrat Tamanna, Euijun Cha, Daeseok Lee, Amit Prakash, Jiyong Woo, Jeonghwan Song and Hyunsang Hwang

Department of Materials Science and Engineering, POSTECH, Pohang, Gyeongbuk, Korea

E-mail : hwanghs@postech.ac.kr

$SmNiO_3$ (SNO) is the most attractive material to study among all the Rare-earth nickeletes ($RNiO_3$), because it shows metal-insulator transition (MIT) above room temperature (400K) [1]. As $SmNiO_3$ is very unstable oxide compare with other sub-oxides (Sm_2O_3 , NiO_2 etc.), which are formed during deposition, so several studies have been conducted describing the stabilization of relatively thick SNO films [2]. In this study, we introduce the optimized condition for nanoscale SNO deposition to tune the MIT behavior which will be a strong candidate for the future selector materials for ReRAM application. Pt/SNO/Pt devices are fabricated by using 250 nm via- hole structures. The effects of temperature and Ar/O_2 ratio during deposition of SNO by using RF sputtering are observed and analyzed very carefully. Finally we found the resistance range for transition which can be maintain by very specific oxygen flow rate with 300 ^oC temperature during sputtering deposition, following no extra annealing. Fig 1 shows the electrical charecteristics of our device, measured under DC voltage which confirms the insulator to metal transition at -1.5 V. The Current distribution and the effect of oxygen flow rate are also shown in accordance with our experiment.The exact mechanism of MIT behavior of this nanoscale device is still unknown . Bias induced oxygen redistribution to reach the optimum condition for tuning MIT may be the one way to explain the mechanism.

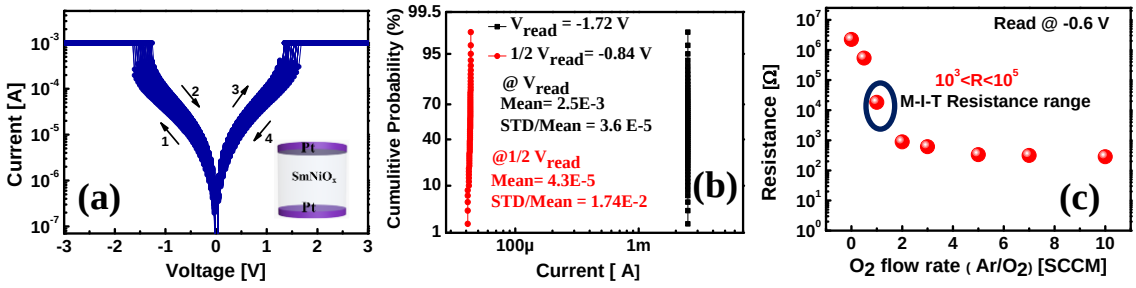


Fig 1. (a) Electrical data of Pt/SNO/Pt device, (b) Current distribution at V_{read} and ½ V_{read}, (c) the effect of O_2 flow rate on resistance to tune MIT.

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[1] Sieu D. Ha, B. Viswanath, and Shriram Ramanathan, J. Appl. Phys. 111,124501(2012);doi: 10.1063/1.4729490

[2] R. Jaramillo, Frank Schoofs, Sieu D. Ha and Shriram Ramanathan, J. Mater. Chem. C, 2013, 1, 2455.

Modeling of crystalline morphology in mixed-phase $Ge_2Sb_2Te_5$ from electrical characterization

Sanghyeon Lee, Gwihyun Kim, Seungwoo Hong, and Seung Jae Baik
Department of Electrical, Electronic and Control Engineering, Hankyong National University, Gyeonggi-do 456-749, Korea
E-mail : sjbaik@hknu.ac.kr

Control and understanding of resistance drift phenomena in $Ge_2Sb_2Te_5$ (GST) are crucial for the development of multi-level-cell phase change memories (MLC PRAM). This resistance drift phenomena are due to the meta-stability of amorphous states. Our objective of this work is to understand and improve the resistance drift in partially set states, where amorphous and crystalline phases are thought to be mixed. We have investigated line shapes of current-voltage characteristics, and their temperature dependence. To explain those, we suggest a model of crystalline morphology: (1) filamentary conduction in the fully set state [1] (2) thinner filamentary conduction in lower resistance region of partially set states (3) conduction through broken filaments in higher resistance region of partially set states. Comparison of this model with measured resistance drifts, and potential methods to control resistance drift will be given and extensively discussed.

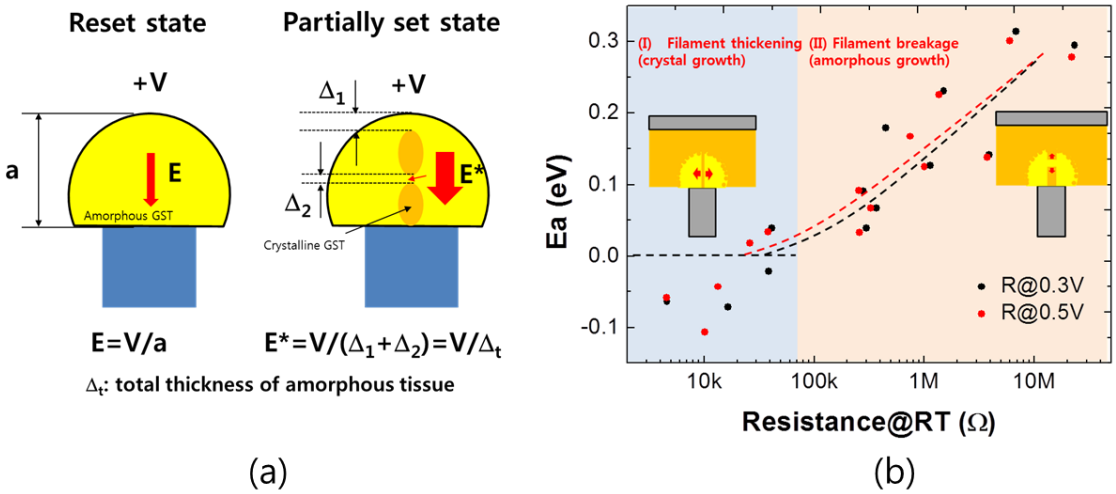

Fig 1. (a) Morphology model of reset and partially set state. E and E* denote electric field applied on amorphous region. (b) Conduction activation energy (E_a) for various resistance values of GST.

[1] V. G. Karpov, Y. A. Kryukov, I. V. Karpov, and M. Mitra, Phys. Rev. B. 78, 052201 (2008)

A 1.2-V 2T Embedded DRAM Macro in Generic Logic CMOS Technology

Weijie Cheng, Baolong Zhou, Huarong Zheng, and Yeonbae Chung
School of Electronics Engineering, Kyungpook National University, Daegu 702-701, Korea
E-mail: ybchung@ee.knu.ac.kr

Gain cell memories are receiving a growing attention due to their preferable embedded attributes over currently dominant 6T SRAMs and 1T/1C DRAMs. Featuring logic CMOS compatibility, compact bit-cell area, decoupled read-write path and non-destructive read-out, the gain cell memories are becoming a strong contender for future embedded appications [1-3]. In this work, we demonstrate an embedded DRAM utilizing hybrid 2T gain cell on 130 nm CMOS technology. The memory bit-cell, which can be implemented with standard twin-well logic process, consists of a high-threshold NMOS write transistor and a standard-threshold NMOS read transistor. The bit data are stored on parasitic capacitances of the cells. Combination of a low off-leakage device for write and a high mobility device for read provides much improved retention time and read performance in a compact bit area. The embedded macro operates with 32-kbit density, logic-compatible supply voltage, SRAM-like I/O interface, speed comparable to the 6T SRAM but 0.65× smaller cell area, and self-timed 128-row refresh. The random access time and active power have been measured to be 6.9 ns and 36.3 μW/MHz, respectively. The refresh power for 140 μs refresh rate is 4.4 μW/kbit at 1.2 V and 85 ℃. The retention time in a typical 32-kbit die at room temperature exhibits a cumulative average of 2.1 ms. The proposed embedded memory techniques in this work can be applicable to the more advanced CMOS technology.

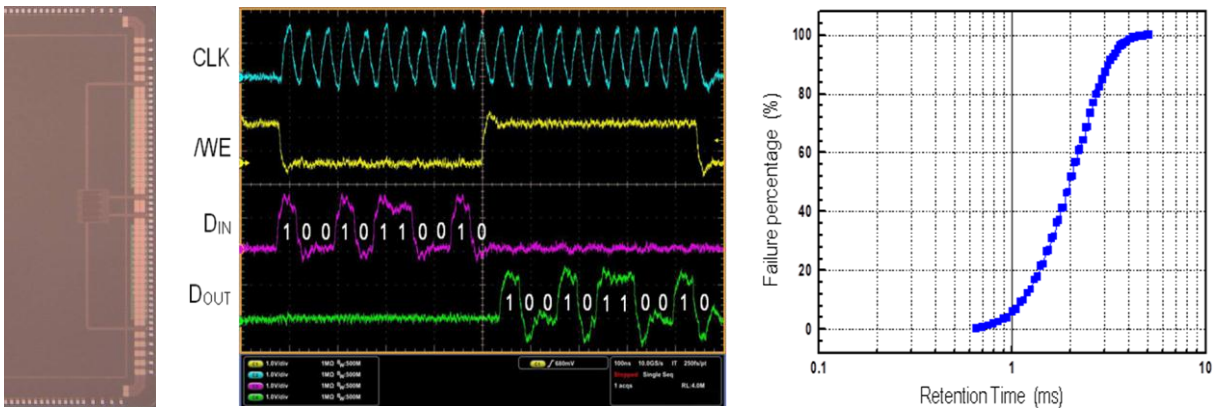

Fig. 1 Chip microphotograph, measured I/O waveforms, and retention time distribution.

[1] D. Somasekhar *et al*., "2 GHz 2 Mb 2T gain cell memory macro with 128 GBytes/sec bandwidth in a 65 nm logic process technology", *IEEE J. Solid-State Circuits*, vol. 44, pp. 174-185, January 2009.
[2] A. Vignon *et al*., "A low leakage 500 MHz 2T embedded dynamic memory with integrated semi-transparent refresh", *Solid-State Electronics*, vol. 75, pp. 55-62, September 2012.
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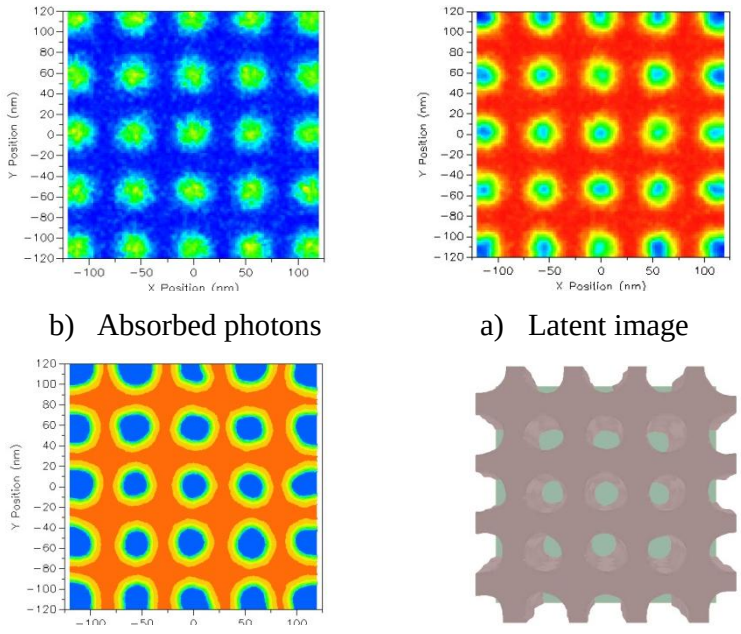
C/H pattern 의 photon shot noise effect 정량화를 위한 stochastic simulation

김정식 [1], 이재욱 [2], 홍성철 [2], 이승민 [2], 정시준 [3], 안진호 [1,2,3]
나노반도체공학과 [1], 신소재공학과 [2], 나노융합과학과 [3]
한양대학교
E-mail : jhahn@hanyang.ac.kr

Photon shot noise 광자와 포토레지스트 간 반응에 대한 확률 통계적인 효과로 빛 자체의 특성을 바꿀 수 없기 때문에 포토리소그래피에서는 피할 수 없는 noise 성분으로 작용한다. 이는 resist patterning 시 critical dimension uniformity(CDU), line edge roughness(LER) 및 circle edge roughness(CER) 등의 imaging performance 를 저해시키며 특히 광자의 개수가 작을수록 더욱 심하게 발생한다. 차세대 리소그래피로 주목받고 있는 극자외선 리소그래피(EUV Lithography)는 13.5nm 의 단파장을 사용함으로써 193nm 파장으로 노광하는 기존의 ArF Lithography 에 비하여 한계 해상력을 향상시켜 더욱 미세한 패턴을 구현할 것으로 기대된다. 그러나 짧은 파장을 사용하여 광자 한 개가 갖는 에너지가 약 14.3 배 더 강하므로 같은 exposure dose 량을 가해줬을 경우, ArF 에 비하여 EUV 광자의 개수가 훨씬 더 적어져 photon shot noise effect 가 심하게 작용할 것으로 예상된다. Stochastic 시뮬레이션을 통해 20nm 부터 32nm 까지의 half-pitch 를 갖는 contact hole 패턴에 대해서 dose-to-size, absorbed photons, generated acids 등의 photon latent image 결과 값들과 developed CD 평균값, CDU 3σ, CER 등의 imaging performance 시뮬레이션 결과 값들을 측정하여 photon shot noise effect 를 정량화 하였다. Source 모양은 기존의 circular 뿐만 아니라 annular, quadrupole 을 적용하였으며 EUV 마스크는 binary mask(BIM)와 attenuated phase shift mask(attenuated PSM)를 사용하여 시뮬레이션 평가를 진 행하였다.



b) Absorbed photons　　a) Latent image

d) Developed PR image　　c) 3D resist profile

Fig 1. Stochastic simulation images of C/H pattern

The suggestion of half-tone phase-shift mask for high-NA EUVL

Seongchul Hong[a], Seejun Jeong[b], Jae Uk Lee[a], Seung Min Lee[a], Jung Sik Kim[c] and Jinho Ahn[a,b,c]

[a]Department of Materials Science and Engineering, [b]Department of Convergence NanoScience
[c]Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jhahn@hanyang.ac.kr

It is expected that high-NA (numerical aperture of $\geq$ 0.45) with 4x lens reduction ratio will be adopted in EUV Lithography. In this case, broader range of incident angles of EUV light on mask is expected, and this will lead to several undesirable mask effects with current Mo/Si multilayers and Ta-based absorbers: decrease in reflectivity of multilayer mirror due to increased incident angle, and mask 3D effects such as obstructing of diffracted lights by thick absorber structure with shadowing patterns. These effects (especially shadowing effect) associated with the mask will have severe negative effect on overall patterning performance. Reducing the absorber thickness is the most effective and simplest method of minimizing the mask 3D effects such as shadowing effect. A simple thickness reduction, however, can lead to the deterioration of the imaging properties. Therefore, the phase-shift concept has been suggested as a potential method of extending the resolution limit in high-NA EUVL. This paper will focus on optimization of half-tone phase-shift mask (PSM) stack for high-NA scanner. The Mo/Si multilayer was re-designed to have sufficient reflectivity for broader range of incident angle. In addition, the proposed half-tone PSM consists of $Ta_8B_1N_1$ as an absorber layer and Mo as a phase shifter on Ru capped Mo/Si multilayers. This structure has ~6% reflectivity of absorber stack and 180±10° phase-shift. The lithographic properties of half-tone PSM were compared with those of conventional binary intensity mask (BIM) with a Ta based absorber for the 11 nm line and space (L/S) dense and isolate patterns with 0.45 NA (9° of AOI) off-axis illumination condition. The optical constants of materials were obtained from KLA-Tencor. The phase-shift and reflectivity were calculated by simulation using EM-Suite of Panoramic technology. Furthermore, imaging properties were evaluated by simulation using lithography simulation tool, PROLITH X4.2 of KLA-Tencor.

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Study of etching properties of Nickel absorber for EUV mask

Seejun Jeong[a], Seongchul Hong[b], Jae Uk Lee[b], Seung Min Lee[b], Jung Sik Kim[c] and Jinho Ahn[a,b,c]

[a]Department of Convergence NanoScience, [b]Department of Materials Science and Engineering,
[c]Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : jhahn@hanyang.ac.kr

For extreme ultraviolet (EUV) lithography mask applications, tantalum-based compounds have been developed as a absorber material. Due to the mild absorption coefficient of Ta (k~0.04 @13.5nm), relatively thick (~70nm) absorber layer is required which results in mask shadowing effect causing smaller printed space size on the wafer than compared to the designed space on the mask. It is expected that an higher incident angle of EUV radiation on mask is to have more acute shadowing effect when high-numerical aperture EUV lithography (NA $\geq$ 0.45) is considered. The most effective and simplest solution for this problem is to reduce the absorber thickness. A research has shown preferable imaging properties that includes contrast and NILS using Ni-based absorber. This paper will present optimization of chlorine-containing plasmas for Ni-based absorber. The dry etching recipe is optimized for a high etch rate and high selectivity with ruthenium capping layer. The results have been confirmed by transmission electron microscopy (TEM).

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Electron beam lithography on flexible polymer substrates using metal discharging layer

Joonhyung Cho[1], Hyungyu Lee[1] , Eunsuk Choi[1], Soonhyung Hwang[1], Hyunsuk Chun[1], and Seung-Beck Lee[1,2*]

1 Department of Electronic Engineering, Hanyang University, Seoul, 133-791, South Korea

2 Institute of Nano Science and Technology, Hanyang University, Seoul, 133-791, South Korea

E-mail address: sbl22@hanyang.ac.kr

Recently, many groups have researched on various flexible devices. These devices usually used polyethylene terephthalate (PET) or polyimide (PI) as a flexible substrate. Most devices on polymer substrates have commonly been fabricated on a micro-scale by optical lithography. To fabricate nano-scale pattern on polymer substrate, electron beam lithography (EBL) can be applied. However, the charging effect of polymer substrate during EBL causes the displacement and distortion of pattern. To define an exact nano-pattern on polymer substrate using EBL process, the electron charging effect should be eliminated. In this study, we have developed the discharging technique to reduce the electron charging effect of polymer substrate using various discharging metal layers on electron beam resist (EBR). The thick coating metal layer makes the charging effect efficiently reduced, but causes the high electron scattering effect and generates wider pattern than we design. To minimize both scattering and charging effect, the proper thickness of discharging metal layer should be proposed.

In this study, we present a discharging technique by various thicknesses of metal layers. We also derive the effect of thin metal deposition on the line width, clearing dose, and resolution of polymethyl methacrylate (PMMA) EBR on PET and PI substrate. Finally, we confirm effective EBL process on polymer by deposition thin metal layer as discharging layer.

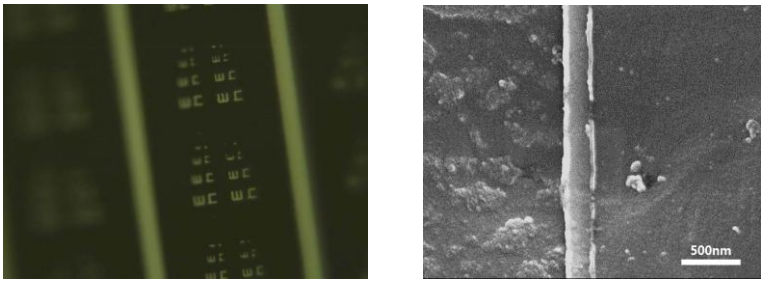

Fig 1. Platinum deposited pattern on PET using EBL. (a) Optical microscope image (1000x) (b) Scanning electron microscope

Comparison of High Density Plasma Etching of MgO Thin Films Using Cl_2, CH_3OH and CH_4 Plasmas

Il Hoon Lee, Su Min Hwang, Adrian Adalberto Garay, Ji Hyun Choi and Chee Won Chung*
Department of Chemical Engineering, Inha University, 100 Inharo, Nam-Gu, Incheon 402-751, Korea

MgO thin films have recently attracted a great attention as prominent candidates for a tunneling barrier layer in the MTJ stack instead of conventional Al_2O_3 films because they have a low Gibbs energy, low dielectric constant and high tunneling magnetoresistance value [1].

For successful etching of high density MRAM, the etching characteristics of MgO thin films as a tunnelling barrier layer should be developed. MgO thin films patterned with Ti (or TiN) hard masks were etched in high density plasma using Cl_2/Ar, CH_3OH/Ar and CH_4/Ar gases. As the gas concentration in Cl_2/Ar and CH_3OH/Ar gases increased, the etch rate of MgO thin films decreased and there was no enhancement in etch profile. On the other hand, in case of using CH_4/Ar gas, the etch selectivity was enhanced and the etch profiles were improved without redeposition with increasing CH_4 concentration.

For understanding the etch mechanism, optical emission spectroscopy (OES) and x-ray photoelectron spectroscopy (XPS) analyses were carried out and they showed that magnesium hydroxide was formed due to chemical reactions on the film surface under CH_4/Ar gas [2]. Based on these results, the MgO thin films were etched by a physical sputtering etching mechanism with the influence of a chemical reaction during the etching.

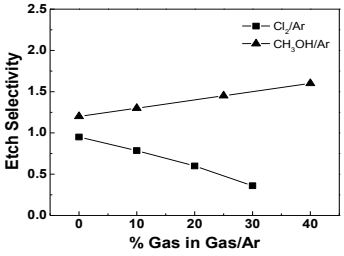

Figure 16. Etch selectivity of MgO films to Ti hard masks in Cl_2/Ar and CH_3OH/Ar gases.

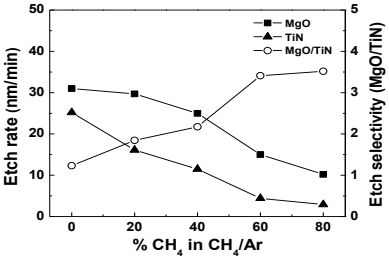

Figure 15. Etch rate of MgO thin films and TiN hard masks, and etch selectivity in CH_4/Ar gas.

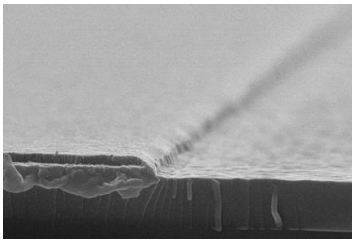

Figure 14. FESEM micrographs of MgO thin films with TiN hard masks etched in 40% CH_4/Ar

[1] R. W. Dave, G. Steiner, J. M. Slaughter, J. J. Sun, B. Craigo, S. Pietambaram, K. Smith, G. Grynkewich, M. DeHerrera, J. Å kerman, and S. Tehrani, IEEE Trans. Magn., **42**, 1935 (2006).

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Dry Etching of Magnetic Tunnel Junctions Stacks using a H_2O/CH_3OH based inductively coupled Plasma

Il Hoon Lee, Adrian Adalberto Garay, Su Min Hwang, Ji Hyun Choi and Chee Won Chung*

Department of Chemical Engineering, Inha University

100 Inharo, Nam-Ku, Incheon 402-751, Korea

As the society becomes technologically dependent; the need of nonvolatile, fast and high capacity semiconductor memory devices that replaces the current DRAMs is growing. Even though there are many other candidates to replace DRAMs as the next generation memory devices (PCRAM, ReRAM, etc.), magnetic random access memory (MRAM) has been considered as a viable option among the others; due to its many advantages including non-volatility, fast access time, unlimited read/write endurance, low voltage operation and high storage density [1].

The MRAM devices structure can be simplified and divided into a complementary metal-oxide semiconductor (CMOS) and a magnetic tunnel junction (MTJ) stack. Because the etching process of the MTJ stacks is one of the key processes in the fabrication of high density MRAMs, an appropriate dry etching process should be developed in order to overcome the difficulties that entail the etching of these materials. Since the MTJ stacks are mostly conformed of metals and magnetics materials that rarely react with reactive species produced in the plasma. Several methods have been tried such as Ion Beam etching [2, 3], chemically assisted ion beam etching [4] but they have not yielded satisfactory results. In order to produce a further improvement, reactive ion etching was introduced by employing Cl_2 and BCl_3 gas chemistries; but the heavy redeposition was encountered. Recently, in order to avoid this problem while improving the etching characteristics, Inductively Coupled Plasma Reactive Ion Etching (ICPRE) was employed to etch MTJ stacks using non corrosive gasses such as Co/NH_3, CH_3OH/Ar and $CH_4/O_2/Ar$ [5-7].

In this paper we investigate the dry etch characteristics and etch profile of the MTJ stacks with nanometer size patterns by means of a H_2O/CH_3OH gas mixture.

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Mask heating량 제어를 통한 Overlay margin 확보

김장선, 최진필, 강영석, 하헌환
E-mail : sunny_k@samsung.com

EUV 시대 연착에 따른 메모리 업체의 집적도 대한 고민은 날로 심화되고 있다. 현재의 기술력으로 최대의 생산 경쟁력을 확보하기 위해 DPT 공정 도입 등의 개선을 꾀하고 있지만 imaging 측면의 문제를 해결한다 하더라도 overlay margin 확보에 대한 어려움은 점점 심화되고 있으며 이를 해결하기 위해 업계의 수많은 resource 가 소모 되고 있는 실정이다. Overlay margin 확보에 있어 특히 intra field overlay 는 inter field overlay 에 비해 소면적 상에서(가로:26mm, 세로:33mm) margin 을 확보해야 하며 제어 불량 시 chip 단위 수율 저하가 아닌 wafer 단위의 수율 문제를 일으켜 제품 경쟁력을 저하 시키는 주요 문제로 대두되고 있다.
특히, Mask 원판의 노광 에너지 축적은 물리적인 신축을 유발하게 되어 Overlay 의 불량 인자로 큰 Portion 을 가지고 있으며 이를 제어 하기 위해 Mask 의 Heating 량을 측정하여 이를 Overlay 인자로 보정하는 기술이 도입되었다. 본 논문에서는 관련 기술에 대한 평가 및 보정 능력에 대한 검증을 통해 intra field overlay margin 개선량을 확인하였다.

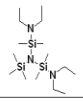
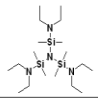
Keywords: Reticle heating control, TOP-RC, Reticle temperature sensor

Plasma Enhanced Atomic Layer Deposition of Low Temperature Silicon Nitride Using Ultra Conformal Silicon Precursors with New Chemical Structure Design

장세진, 이상도, 김종현, 김도연, 조성우, 석장현, *이상익, 김명운
대전광역시 대덕구 대화로 132 번길 142 ㈜디엔에프
E-mail : sjjang@dnfsolution.com, *silee@dnfsolution.com

질화규소 박막은 화학적으로 비활성 물질이며 산화규소 박막에 비해 높은 저항, 높은 유전 상수 및 뛰어난 기계적 강도를 가지는 중요한 소재이다. 반도체 및 디스플레이 산업에서 절연체 또는 확산 방지막으로 사용되며, 또한 뛰어난 전자 트래핑 능력으로 기인해 비휘발성 메모리장치에 사용된다. 질화규소 박막은 다양한 증착 기법을 이용하여 박막 형성이 연구되어 지고 있으며, 주로 저압화학증착 (Low Pressure Chemical Vapor Deposition : LPCVD) 및 플라즈마강화화학증착 (Plasma Enhanced Chemical Vapor Deposition : PECVD) 기법에 의한 박막 형성이 활발히 진행되었다[1]. 이러한 종래 기술의 단점은 높은 기판 온도, 박막 내의 수소 함량 및 질소와 규소의 정량적 비율 조절이 어렵다는 것이며, 더욱이 미세화에 따라 종횡비가 크게 증가되는 소자의 균일한 초박막 형성에 적용되기는 어려운 실정이다. 자기 제한적 표면 반응 (self limiting surface reaction)을 통해 균일하고 두께 조절이 용이한 플라즈마강화 원자층증착 (Plasma Enhanced Atomic Layer Deposition : PEALD)기법을 이용하여 트리실릴아민 (Trisilylamine) 유도체를 N_2/NH_3 플라즈마를 이용하여 실리콘 기판 위에 ALD 특성을 나타내는 질화규소 박막을 형성하였다. 트리실릴아민은 질소의 비공유전자쌍이 규소의 비어있는 d오비탈에 전자를 제공하는 (N pπ→Si dπ donation) Si_3N 시스템을 가지는 안정한 화합물이다 [2]~[3].

(a)

	DTDN-2	DTDN-3
Structure		
Chemical name	Bis(Diethylaminodimethylsilyl) (trimethylsilyl) amine	Tris(diethylaminodimethyl silyl) amine
Molecular weight	347.77g/mol	404.87g/mol
Boiling point	277°C	313°C

(b)

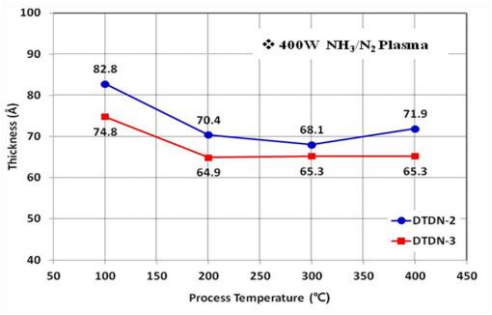


Figure 1. (a) Chemical structures and properties. (b) Thickness data of DTDN-2 and DTDN-3 by process temperature.

[1] A P Mousinho, R D Mansano, L S Zambom and A Passaro, J. Phys.: Conference Series 370 (2012) 012015

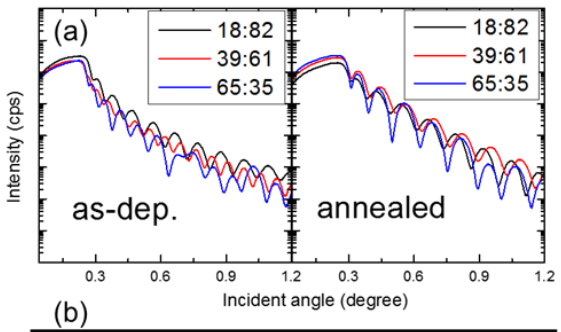
[2] B.W. Bush et al., Surf. Interface Anal. 2008, 40, 1402-1405

[3] R. P. Bush et al., J. Chem. Soc. (A). 1969, 253-257

Analytical Investigation on Electrical Properties of Atomic Layer Deposited amorphous Zinc Tin Oxide Thin Film

Jun Shik Kim, Un Ki Kim, Eun Suk Hwang, Lee Seung-Jun, and Cheol Seong Hwang*
WCU Hybrid Materials Program, Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea
E-mail : kykkysp@snu.ac.kr

Atomic layer deposition (ALD) method has received increasing attention over other deposition methods due to its superior conformality and exceptional controllability on film thickenss and elemental composition. These characteristics make the ALD optimal process technique for fabricatiing complex three-dimensional devices made of functional multi-component oxides at the atomic scale. In this study, zinc tin oxide thin films with different elemental compostions were prepared on Si substrate via ALD and annealed in furnace. All samples maintained amorphous phase even after annealing at 600 ^{o}C. However, it was observed that there is severe densification behavior through annealing process with volumetric contration of ~ 30%. It is believed that this volumetric contraction results from the low density of as-deposited samples, and it affects other film characteritics such as band gap, refractive index and absorption coefficient. Further investigation on electronic structures were also conducted for different Zn/Sn ratios. XPS spectra showed that oxygen-vacancy-related peak is strongest near the composition of Zn:Sn=0.4:0.6, which is in agreement with previously reported paper.[1] The electrical performance of thin film transistors (TFT) with ALD deposited zinc tin oxide showed lower quality compared with other TFTs



(b)

Zn:Sn(at.%)	as-dep. (g/cm^3)	Annealed(g/cm^3)	Ratio
18:82	2.86	3.66	78.1 %
39:61	2.7	3.79	71.2 %
65:35	3.16	3.66	86.3 %

Figure 1. XRR results with different Zn/Sn ratio and annealing condition; (a) intensity profiles and (b) measured densities

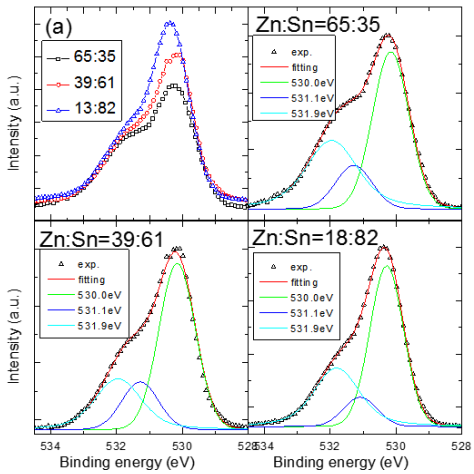


Figure 2. XPS spectra of oxygen 1s spectra; (a) oxygen-vacancy-related peak (531.1eV), and spectra of that Zn:Sn is (b) 65:35, (c) 39:61 and (d)18:82, respectively.

fabricated using chemical vapor deposited zinc tin oxide films.

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Large-area fabrication of Vertically oriented ZnO Hexagonal Nanotube-Rod Hybrids Applying a Two-Step Growth Method

Sungwoong Kim, Sun Sang Kwon, Won Woo Lee and Won Il Park
Division of Materials Science and Engineering, Hanyang University, Seoul 133-791, Korea
E-mail : wipark@hanyang.ac.kr

Zn-polar (0001) surfaces are more chemically reactive than other surfaces of Zinc oxide (ZnO) crystals [1-2] and trigger preferential anisotropic and asymmetric growth along the [0001] direction, which promotes growth of c-axis oriented, one-dimensional ZnO nanostructures. Therefore, capping the top (0001) surface of ZnO crystals can hinder c-axis growth and thus serve to modulate growth habits. Here we generated vertically aligned ZnO hexagonal nanotube-rod (h-NTR) hybrids by modulating growth habits during a second-stage process. Electron microscopy studies revealed the formation of very thin (10–20 nm) single-crystalline nanotube walls along the edges of underlying hexagonal rod tops capped with Si. In addition, spatially resolved investigation of ZnO h-NTR indicated an abrupt increase in the measured bandgap across rod-tube junctions, which was ascribed to a quantum confinement effect [3-5] and Burstein–Moss effect [6] of carriers within the very thin nanotube walls.

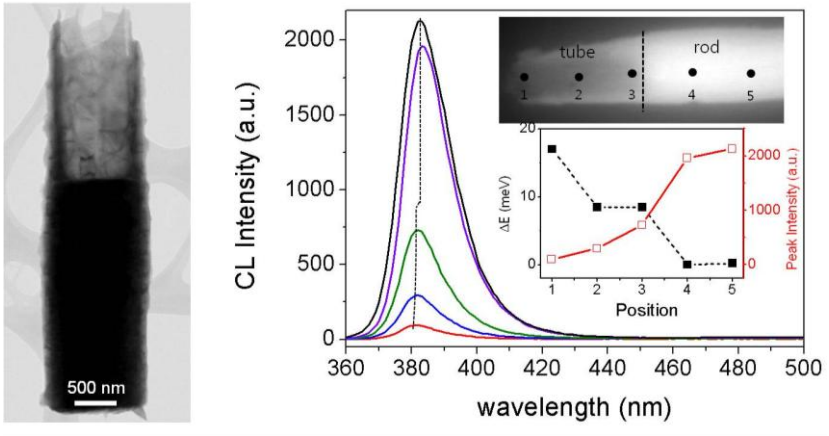

Fig 1. Transmission electron microscopy (TEM) images and Cathodoluminescence (CL) spectra of ZnO h-NTR

[1] T. Song, J. W. Choung, J. G. Park, W. I. Park, J. A. Rogers and U. Paik, Adv. Mater. 20, 4464 (2008).
[2] W. I. Park, Met. Mater. Int. 14, 659 (2008).
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[4] T. Song, J. W. Choung, J. G. Park, W. I. Park, J. A. Rogers, and U. Paik, Adv. Mater. 20, 4464 (2008).
[5] W. I. Park, J. Yoo, D. W. Kim, and G. C. Yi, J. Phys. Chem. B 110, 1516 (2006).
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Structural and perpendicular magnetic anisotropy features of novel $[CoO/Pd]_n/[Co/Pd]_m$ multilayer matrix for the STT-MRAM applications

JaBin Lee, GwangGuk An, SeungMo Yang, JaeHong Kim, and JinPyo Hong*
The Research Institute for Natural Science, Novel Functional Materials and Device Laboratory, Department of Physics, Hanyang University, Seoul, 133-791, South Korea
E-mail : jphong@hanyang.ac.kr

In past years, [Co/Pd] multilayer (ML) configurations and its alloys have been widely explored due to the large perpendicular magnetic anisotropy features [1-2]. This study examined the structural reconfiguration events of [Co/Pd] ML matrix under annealing. The initially formed Co-O bonding states *via* [CoO/Pd] spacer layer was broken by post annealing and oxygen diffusion event may lead to structural reconfiguration in the multilayer by supplying proper lattice strains. The ordinary ML matrix revealed an anisotropic energy of around 3 Merg/cc, while the modified [Co/Pd] ML matrix provided a significantly higher K_U value of 7.43 Merg/cc after annealing. The x-ray photoelectron spectroscopy suggests an evidence for the presence of Co-O bonding states and annealing dependent oxygen atom diffusion event, along with transmission electron microscopy images.

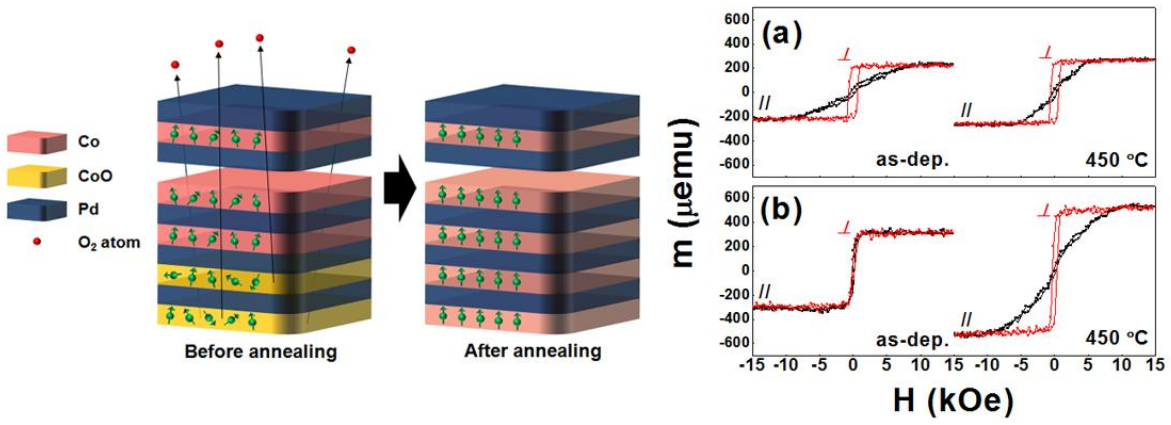

Fig 1. Possible structural reconfiguration and typical M-H loops for Samples (a) A and (b) B.

[1] P. F. Carcia, J. Appl. Phys. 63, 5066 (1988).
[2] S. Kim, S. Lee, J. Ko, J. Son, M. Kim, S. Kang, and J. Hong, Nat. Nanotechnol. 7, 567 (2012).

Quality Improvement of Epitaxial Graphene Grown on 4H-SiC Surface by Molybdenum Plate Capping during UHV Annealing

Han Byul Jin[1)], Youngeun Jeon[1)], Sungchul Jung[2)], Hun Han Yoon[1)], Hyun Suk Kang[3)], Byung Cheol Lee[3)], Jae-Hyeon Ko[4)], Hyung-Joon Shin[5)], Jung-Woo Yoo[5)], Sung Youb Kim[5)], Soon-Yong Kwon[5)], Daejin Eom[6)], and Kibog Park[1,2)*]

[1)] School of Electrical and Computer Engineering, KIER-UNIST Advanced Center for Energy, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, Republic of Korea

[2)] Department of Physics, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, Republic of Korea

[3)] Korea Atomic Energy Research Institute, Daejeon 305-353, Republic of Korea

[4)] Department of Physics, Hallym University, Chuncheon Gangwondo 200-702, Republic of Korea

[5)] School of Mechanical and Advanced Materials Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 689-798, Republic of Korea

[6)] Korea Research Institute of Standards and Science, Daejeon 305-340, South Korea

*E-mail: kibogpark@unist.ac.kr

It is found that the quality of epitaxial graphene (EG) grown on a C-face 4H-SiC substrate can be improved greatly by having the substrate in contact with a molybdenum plate (Mo-plate) during vacuum annealing. The controlled experiments demonstrating the effects of Mo-plate capping on EG growth were performed as shown in Fig. 1. The structure of EG layer grown with Mo-plate capping was analyzed by Raman spectrum measurements. The significant reduction of D-peak and increase of 2D-peak in the measured spectrum confirm the quality improvement of the grown EG layer in comparison with the EG layer grown without Mo-plate capping. The sheet resistance of the EG layer grown with Mo-plate capping was found to be ~663 Ω/sq by performing circular transfer line method (CTLM) measurements.

Mo-plate capping is believed to reflect the thermal radiation from the 4H-SiC substrate (radiation mirroring effect), increasing the surface heating efficiency, and also slow down Si atom sublimation on the surface, which would be the main contributors of quality improvement [1]. This Mo-plate capping can be used as a very efficient experimental supplement of reducing the number of defects and making grains larger to other known methods for growing wafer-scale uniform EG layers on SiC surface [1,2]

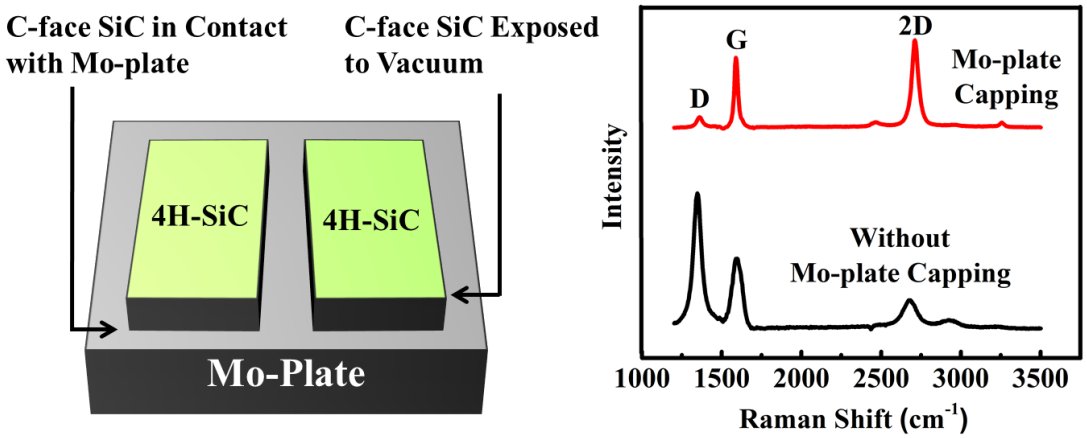

Fig. 1. (Left) The experimental configuration to confirm the effect of Mo-plate capping on the growth of EG layers on SiC surface during vacuum annealing, (Right) Measured Raman spectra

[1] C. Çelebi, C. Yanik, A. G. Demirkol, and I. I. Kaya, Carbon 50, 3026 (2012)
[2] H. Go, J. Kwak, Y. Jeon, S.-D. Kim, B. C. Lee, H. S. Kang, J.-H. Ko, N. Kim, B.-K Kim, J.-W. Yoo, S. Y. Kim, Y.-W. Kim, S.-Y. Kwon, and K. Park, Appl. Phys. Lett. 101, 092105 (2012)

Role of oxygen-doped Ta spacer on the enhanced perpendicular magnetic anisotropy features of CoFeB/MgO interface for the STT-MRAM applications.

SeungMo Yang, JaBin Lee, GwangGuk An, JaeHong Kim, and JinPyo Hong*
The Research Institute for Natural Science, Novel Functional Materials and Device Laboratory, Department of Physics, Hanyang University, Seoul, 133-791, South Korea
E-mail : jphong@hanyang.ac.kr

Perpendicular magnetic anisotropy (PMA) has become one of the key factors in future spintronics. The PMA materials including Co/Pt multilayer and FM/RE alloys were widely tested due to their high perpendicular magnetic anisotropy values. However, recent works reported that the direct contact between these materials and MgO barrier provided a low tunneling magnetoresistance (TMR) ratio that might originate from a discrepancy in their structures. Ikeda *et al*.[1] proposed the significant enhanced PMA features at the interfaces between CoFeB and MgO, resulting in a high TMR ratio with MgO barrier. As the CoFeB thickness is decreased under 1.4nm, the out-of-plane direction becomes the magnetic easy axis due to the large anisotropy at the CoFeB/MgO interface. Recent research suggested that this anisotropy has its origins in charge transfer between 3d orbitals in Co, Fe and 2p orbitals in oxygen. Therefore, this work reports the influence of oxygen doped Ta spacer on the enhancement of the PMA characteristics. The possible nature is described by adapting the effect of oxygen-ferromagnetic interface and by performing various structural analyses.

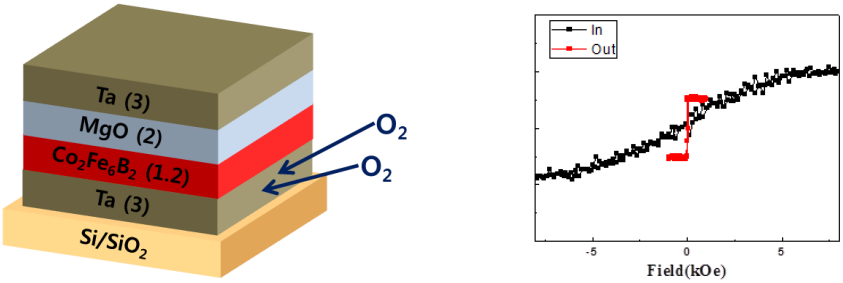

Fig 1. Schematic illustration of CoFeB/MgO with Ta spacer and typical magnetic hysteresis curves.

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Investigation of leakage current mechanisms for different cap layer on AlGaN/GaN Schottky diodes

Minjun Kim[1], Yoonhyung Kim[1], and Jinsub Park[1,2]

[1]*Department of Electronics and computer Engineering, Hanyang University, Seoul 133-791, Korea*

[2]*Department of Electronic Engineering, Hanyang University, Seoul 133-791, Korea*

E-mail : jinsubpark@hanyang.ac.kr

AlGaN based power devices have demonstrated high power and high frequency operation due to the excellent transport properties and larege sheet carrier concentration at the interface of AlGaN and GaN heterojuction [1]. We investigated the effects of various capping layers such as n-GaN and u-GaN formed on AlGaN/GaN Schottky barrier diodes (SBDs) on the device performances. In order to compare the leakage current characteristics in SBDs, the AlGaN/GaN SBDs without any GaN cap layers are fabricated and the electrical characteristics of fabricated AlGaN/GaN SBDs with different capping layer are analyzed. The current-voltage (I-V) measurements and the atomic force microscope (AFM) analysis were conducted to observe the electrical characteristics and dislocation density, respectively. The current-voltage (I-V) characteristics of AlGaN/GaN SBD with n-GaN cap layer shows the dramatic increase of reverse leakage currents compared to the those with u-GaN cap and without cap layer. These phenomena can be explained by the barrier height or the dislocation density observed by the atomic force microscopy.

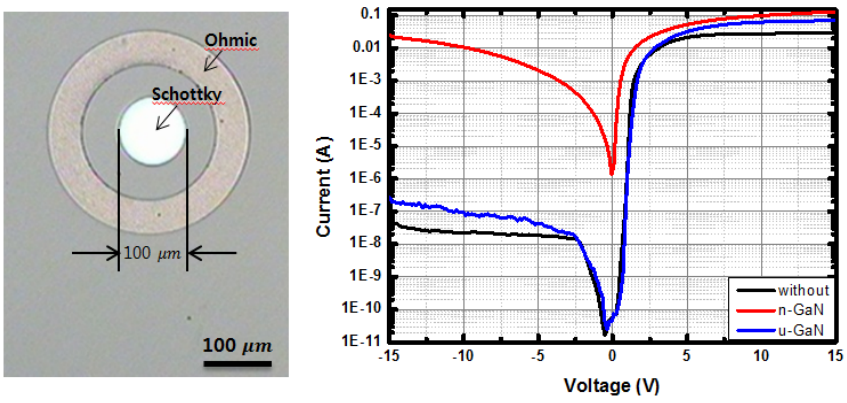

Fig 1. AlGaN/GaN Schottky diode and I-V characteristics of SDBs with different cap

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GaN 열분해 특성을 이용한 자립형 GaN 기판 제작에 관한 연구

김시내 [1)], 이현재 [2)], 김시영 [2)], 구지은 [1)], 장지호 [1)*]
[1)] *한국해양대학교 응용과학과 반도체물리전공, 부산시 영도구 동삼동*
[2)] *㈜판크리스탈, 경기도 수원시 영통구 원천동*
E-mail : jiho_chang@kmou.ac.kr

최근 질화물 반도체의 응용범위가 발광소자 뿐만 아니라 전력 반도체 분야로 확대됨에 따라 고품질 GaN 기판의 수요가 증가하고 있다. 본 연구에서는 GaN 의 열분해(thermal decomposition)특성을[1] 이용한 새로운 완충층(decomposable buffer layer; DBL)을 적용하여, 고온 성장 중에 자발적으로 기판에서 분리되어 자립형 GaN 기판을 제작할 수 있는 기술을 제안한다. 그림 1(a)와 (b)는 DBL 의 열분해 반응에 의한 공극형성 및 분리 형태를 모식도로 나타내었고, 모식도에 따른 시료의 SEM 단면 사진을 그림 1(c)와 (d)에 나타내었다. 이러한 기술의 효과는 공정과정의 단순화 및 이종기판에서 발생하는 계면스트레스로부터 자유로워지므로 고품질의 자립형 GaN 이 성장될 수 있다. GaN 의 열분해 특성을 적용하여 성장된 자립형 GaN 는 (두께 250 μm), (0002)면에서 omega rocking curve 의 좁은 반치폭(67 acrsec)과 낮은 EPD(6×10^{6} cm^{-2})를 얻어 양질의 GaN 기판 제작이 가능함을 입증하였다.

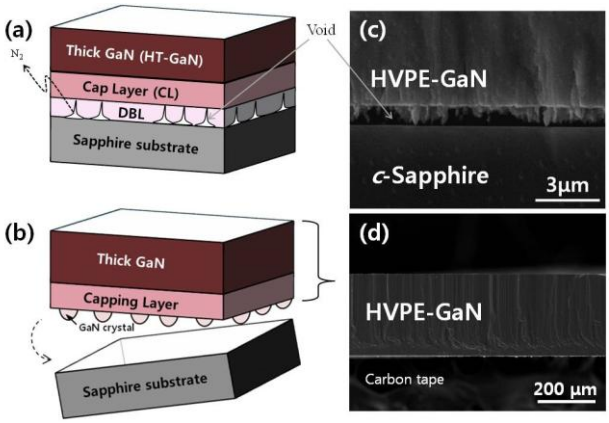

그림 1. (a)와(b) DBL 의 열분해 반응에 의한 공극 형성 및 분리 형태의 모식도, (c)와 (d) 모식도에 따른 시료의 SEM 단면사진.

[1] Ambacher O, Brandt M S, Dimitrov R, Metzger T, Stutzmann M, Fischer R A, Mieher A, Bergmaier A and Dollinger G J. Vac. Sci. Technol. B 14 3532 (1996).

(Grant No.; NIPA-2013-H0301-13-2009)

Enhancement of light extraction by nanostructure arrays on GaN-based vertical light-emitting diode

Taejoon Son, Seunghwan Yeon, Jinsub Park
Department of Electronics & Computer Engineering, Hanyang University, Seoul 133-791, Republic of Korea
E-mail : jinsubpark@hanyang.ac.kr

The GaN-based light emitting diodes (LEDs) have developed to replace the traditional fluorescent light source due to the high performance, long lifetime, and low power consumption[1]. However the improvemetns of light extraction efficiency(LEE) as well as internal quantum efficiency (IQE) of LEDs are still required. Until now, many methods have been suggested to achieve high efficiency LEDs such as surface roughness, photonic crystal, and various nano hybrid structures. Recently, vertical LEDs attract considerable attentions to good current injection, excellent thermal heat dissipation[2]. In this study, we reported the formation of ZnO nanorods on vertical LEDs with different lift-off methods such as laser lift-off (LLO) and chemical lift-off (CLO). The surface morphology has strong relationship with the formation of nanostructures. The surface damage layer is harmful effects on the post formation of ZnO nanostructures on LED surface formed by CLO compared to LED made by CLO. In addition, the integration effects of silica nanospheres with ZnO nanorods on light extraction efficiency of vertical LEDs are investigated. The simulation results using finite-difference-time-domain (FDTD) indicate the integration of nanostructures is the promising technique to improve the extraction efficiency of vertical LEDs as shown in Fig1.

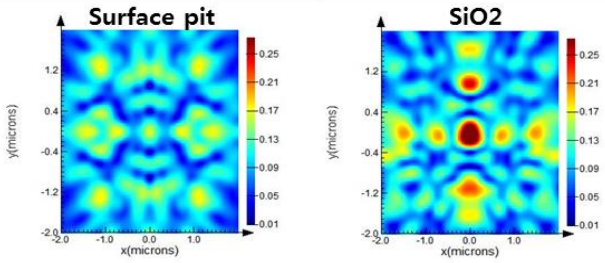

Fig 1. The distribution light intensity when vertical LEDs result in FDTD simulation. Surface factor (left) and SiO2 sphere (right).

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Polar and Non-polar single InGaN/GaN MQW nanowire LED

Yong-Ho Ra, San Kang, Hee-Il Yoo, Seung-Kyu Lee, Il-Seok Song and Cheul-Ro Lee
School of Advanced Materials Engineering, Chonbuk National University, Jeon-Ju 561-756, Korea
E-mail : crlee7@jbnu.ac.kr

We fabricated the controlled synthesis of *c*-plane and *m*-plane InGaN/GaN MQW nanowire(NW) heterostructures by metalorganic chemical vapor deposition. The surface morphology, optical, and electrical characterization of the fabricated *c*-plane and *m*-plane *p*-GaN/InGaN/GaN MQW/*n*-GaN NW LEDs heterostructures are studied by FE-SEM, HR-TEM, CL, I–V, and EL measurements. HR-TEM images reveal high-quality NW structures with sharp InGaN and GaN interfaces. The measured I-V characteristics at room temperature show a sharp onset voltage at 2.6 and 2.2 V for the *c*-plane and *m*-plane MQW NW LEDs, respectively. The electrical properties of *m*-plane NWs exhibit superior characteristics to that of *c*-plane NWs owing to the absence of piezoelectric polarization. The electroluminescence emission intensity of the *m*-plane LEDs shows improved results over about 15% compared to the *c*-plane LEDs. These kinds of *c*-plane and *m*-plane NWs may allow flat band quantum structures that can improve the efficiency of LEDs. Based on our studies, these InGaN/GaN NWs-based heterostructures are promising structures for developing high performance LEDs [1-2].

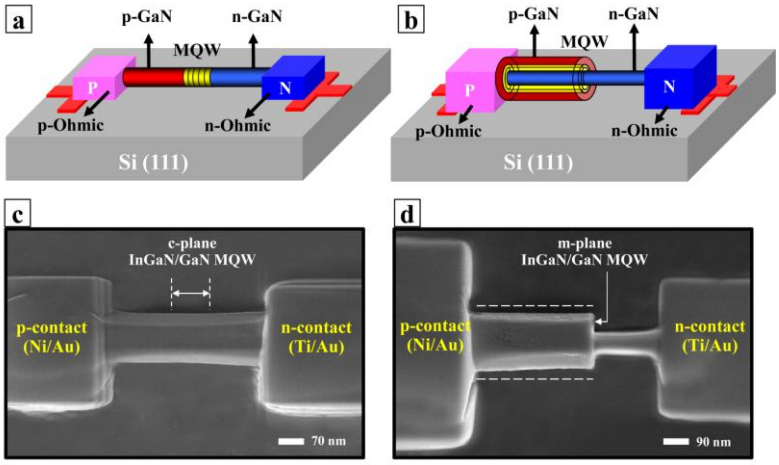

Fig 1. FE-SEM data of *c*-plane and *m*-plane InGaN/GaN MQW nanowires.

[1] Y. Dong, B. Tian, T. J. Kempa, C. M. Lieber, Nano Lett, 9, 2183, (2009).
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The Growth of GaSb on Silicon (100) with AlGaSb/GaSb SPS buffer layers

Kyu-Hyoek Yoen[1, 2], Eun-Hye Lee[2], Min-Han Bae[2], Jun-Young Kim[2], Hye-Joung Jang[3], and Jin-Dong Song[1, 2*]

1Nano-electronic Engineering, University of Science & Technology, Daejeon, 305-350, South Korea
2Center for Opto-Electronic Convergence Systems, Korea Institute of Science and Technology, Seoul 136-791, South Korea
3Advanced Analysis Center, Korea Institute of Science and Technology, Seoul 136-791, South Korea

*Corresponding author e-mail: jdsong@kist.re.kr

Sb-based material semiconductors have attracted for high-speed and low power electric devices. Silicon substrate has a lot of advantages including growth of large area and cost effectiveness comparing to GaSb substrate. However, the lattice mismatch of silicon and GaSb is ~13%. Thermal expansion effect and the growth of polar compound on a non-polar substrate are also obstacles [1]. The large lattice mismatch could make threading dislocations (TDs) and exacerbate GaSb crystal quality on silicon (100) substrate. Therefore, it is important to minimize threading dislocation in AlSb buffer layer [2]. AlGaSb/GaSb shore-period lattice (SPS) layer is used to overcome problem of large lattice mismatch. TDs would be bent to misfit dislocations (MDs) at the interface of SPS layer for strain release [3]. MDs could not affect to upper GaSb layer and would be dissipated at the interface of SPS layer. The surface of AlSb buffer layer was measured by AFM measurement. The root mean square (RMS) value of SPS layer is about 2nm. In addition, AlSb buffer layer will be measured by dark-field (DF) XTEM. GaSb/AlGaSb MQW PL spectra were obtained at room temperature and 10K with a fixed excitation power of 100mW. Emission peaks showed at 1761nm and 1623nm, respectively.

[1] Y.H. Kim, “Transmission electron microscopy study of the initial growth stage of GaSb grown on Si (001) substrate by molecular beam epitaxy method”, Thin Solid Films, 518, pp 2280-2284, (2010)

[2] Y. K. Noh, “Structural and Optical Properties of GaSb Films Grown on AlSb/Si (100) by Insertion of a Thin GaSb Interlayer Grown at a Low Temperature”, Journal of the Korean Physical Society, Vol. 57, No. 1, pp 173~177, (2010)

[3] T. D. Mishima, “Dislocation filtering by AlxIn1−xSb/AlyIn1−ySb interfaces for InSb-based devices grown on GaAs (001) substrates”, Applied Physics Letters 88, 191908, (2006)

Single nanowire diode fabricated by *p-n* junction GaN nanowire

Ji Hyeon Park, Jae Kwan Sim, Yong Hyun Choi, Eun A Cho, Dae Yong Um and Cheul-Ro Lee
School of Advanced Materials Engineering, Chonbuk National University, Jeon-Ju 561-756, Korea
E-mail : crlee7@jbnu.ac.kr

Uniaxially *p-n* junction gallium nitride nanowires have been synthesized via metal-organic chemical vapor deposition method. Nanowires prepared on Si (111) substrates were found to grow perpendicular to the substrate, and the transmission electron microscopy studies demonstrated that the nanowires had single-crystal structures with a <0001> growth axis. The parallel assembly of the p-n junction nanowire was prepared on a Si substrate with a thermally grown SiO_2 layer. The transport studies of horizontal gallium nitride nanowire structures assembled from *p*- and *n*-type materials show that these junctions correspond to well-defined *p-n* junction diodes. The *p-n* junction devices based on GaN nanowires suspended over the electrodes were fabricated and their electrical properties were investigated. The horizontally assembled gallium nitride nanowire diodes suspended over the electrodes were exhibited a substantial increase in conductance under UV light exposure. Apart from the selectivity to different light wavelengths, high responsivity and extremely short response time have also been obtained. [1-2]

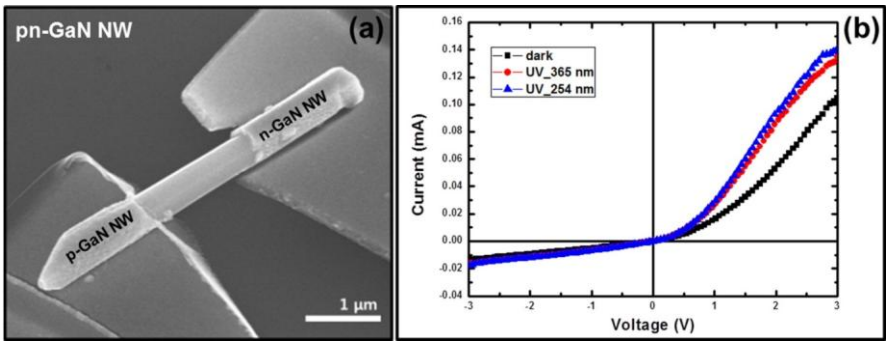


Fig 1. FE-SEM image of (a) horizontally assembled *p-n* junction diode by single GaN nanowire, (b) The I-V measurements of GaN nanowire device in the dark and under UV illumination (wavelength λ = 365 and 254 nm).

[1] Ponce, F. A.; Bour, D. P. *Nature* 386 351-359 **(**1997) .

[2] Xiang, J.; Lu, W.; Hu, Y.; Yan, H.; Lieber, C. M. *Nature* 441 489-493 (2005).

Defects states and dark currents in InAs/GaAs Quantum dot solar cell grown by molecular beam epitaxy

Kyoung Su Lee[1], Dong Uk Lee[1], Eun Kyu Kim[1*], and Won Jun Choi[2]

[1]Quantum-Function Research Laboratory and Department of Physics, Hanyang University, Seoul 133-791, Republic of Korea

[2] Opto-Electronic Convergence System, Korea Institute of Science and Technology, Seoul 136-791, Korea

Email: ek-kim@hanyang.ac.kr*

For the past few years, self-organized quantum dots (QDs) have been investigated in photovoltaic devices to increase the sub-band-gap photon absorption and hence the energy efficiency. The QD absorption cross section can be increased by stacking the QD layers. But the addition of multiple QD layers leads to defect formation. These defects act as carrier traps in QD solar cells reduce photoelectric-conversion-efficiency (PCE) of them and influence on current mechanism of them. To characterize the currents mechanisms that are present in the device, a number of measurements were performed, most importantly of which is the dark current voltage (I-V) and defect states measurements. In this experiment, the efficiency of QD solar cell was analyzed with dark current values and defect states. InAs/GaAs quantum dot solar cells structured with p-GaAs / undoped GaAs (active) inserted by 20 layered QDs with or without delta doping / n-GaAs was fabricated on n-type substrate by molecular beam epitaxy. The thicknesses of active region were controlled about 3.5 μm and the delta doping was controlled about 1×10^{18}. Finally, the p-type GaAs doped with Be ($5x10^{18}cm^{-3}$) was grown to 200-nm-thickness. The defect states of the samples were measured by using deep level transient spectroscopy. From the temperature dependent dark currents, the electrical parameters of QD solar cell such as ideality factor, reverse saturation current, series resistance, and shunt resistance were extracted also. From their electrical characteristics, we will discuss relation between PCE of QD solar cells and their current mechanism.

Optical characteristics of indium tin oxide thin films co-evaporated with magnesium fluoride

Gyujin Oh and Eun Kyu Kim*
Department of Physics, Hanyang University, Seoul 133-791, Korea
*E-mail: ek-kim@hanyang.ac.kr

Transparent conductive oxide (TCO) is one of the powerful materials utilized in fabricating optical devices such as light emitting diode (LED), solar cells, and photo detector. Indium tin oxide (ITO) is one of the TCO materials. This material has over 80% of transparency in visible light region, and its resistivity is less than 10^{-3} Ω·cm. In terms of usage to anti-reflection coatings, because refractive index of ITO is fairly high (approximately 2) compared with other transparent materials, it is a promising candidate for an electrode and an anti-reflection coating of photovoltaic devices such as solar cells.

Glancing angle deposition (GLAD) technique is widely studied for constructing anti-reflection coatings on photovoltaic devices. As deposition angle varies, volume fraction of air in the films becomes greater, and it causes the dielectric constant of materials to get bigger. Dielectric constant is physically equivalent to refractive index. Therefore, GLAD technique can be utilized to make the anti-reflection coatings. However, this fabrication method has one limitation applying to the photovoltaic devices. In GLAD technique, geometrical position between source materials and sample has great importance. As a result, GLAD technique cannot be commonly used on the unpolished substrate. In the micro-scale, unpolished substrate has randomly oriented surface, so the grown thin films by GLAD technique have randomly oriented columnar structure, and it is true to refractive index as well.

In this study, we tried to solve the substrate selectivity during ITO deposition by co-evaporation with magnesium fluoride, which has very low refractive index. The reason why we didn’t use other transparent oxide materials is that indium tin oxide has also oxygen, and other oxide material can influence stoichiometry of indium tin oxide. The thickness of ITO films co-evaporated with magnesium fluoride was determined by scanning electron microscopy (SEM) measurement, and the optical properties of the samples were investigated by scanning ellipsometry.

Design and Analysis of Sub-10nm Junctionless Fin-type Field-Effect Transistors

Sung Yoon Kim[1)], Jae Hwa Seo[1)], Gwan Min Yoo[1)], Young Jae Kim[1)], Hye Rim Eun[1)], Hye Su Kang[1)], Young-Woo Jo[1)], Seongjae Cho[2)], Jung-Hee Lee[1)] and In Man Kang[1), *]

[1)] School of Electronics Engineering, Kyungpook National University, Daegu 702-701, Republic of Korea

[2)] Department of Electronics Engineering, Gachon University, Seongnam, Kyunggi 461-701, Republic of Korea

[*] E-mail : imkang@ee.knu.ac.kr

In this paper, we design the n-channel junctionless fin-type FET (JL FinFET) with 10nm gate length and compare the performances to that of the fin-type bulk MOSFET by 3D Silvaco ATLAS [1]. Recently, the junctionless transistor (JLT) without any metallurgical junction has been proposed. In comparison with conventional MOSFET, the JLT features a single-doping species at the same level in its source, drain, and channel. This novel feature can achieve simple process flow as no need for ultrashallow source/drain junction and low thermal budgets. Also, it reduce the impact of oxide/semiconductor interfaces as current flows not in the surface region but in the bulk of the semiconductor. In addition, it also had advantage of gate controllability and wide channel width as we adopted fin-type structure. V_{DD} is applied as 0.65 V which satisfies the LSTP operation in ITRS roadmap [2]. Fig.1 is the structure of the n-channel JL FinFET with 10nm gate length. The gate oxide material is HfO_2 of 2 nm. First, we optimized fin width (W_{fin}) and height (H_{fin}) considering V_{th}, subthreshold swing (*SS*), and I_{on}-I_{off} ratio. And channel doping concentration (D_{ch}) is determined on the same criteria. When the W_{fin} increases, I_{on}, I_{off} and *SS* increase and V_{th} becomes lower. But when the H_{fin} increases, *SS* decreases and H_{fin} has optimum point in view of I_{on}-I_{off} ratio. Higher D_{ch} improves I_{on} but I_{off} also increases and V_{th} significantly decreases. The optimized values were obtained as W_{fin} = 10 nm, H_{fin} = 15 nm, and $D_{ch} = 1.0 \times 10^{19}\ cm^{-3}$. After the optimized process is completed, fin-type MOSFET with same structure and V_{th} is designed in order to compare in terms of DC and RF characteristics.

Fig.2 is I_D-V_{GS} curves for the two different devices with detailed characteristic values. The JL FinFET has an I_{on} of 129.5 μA/μm (at V_{GS}=0.65 V) and an I_{off} of 59.6 pA/μm (at V_{GS}=0 V). Also, it has V_{th} of 0.22 V. The *SS* is 67.28 mV/dec, and drain-induced barrier lowering (DIBL) is 62.3 mV/V. Also, the f_T was obtained 332.4 GHz and the f_{max} was obtained 1556.4 GHz in JL FinFET.

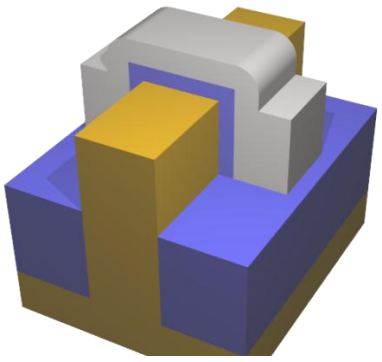


Fig. 4 Structure of the JL FinFET

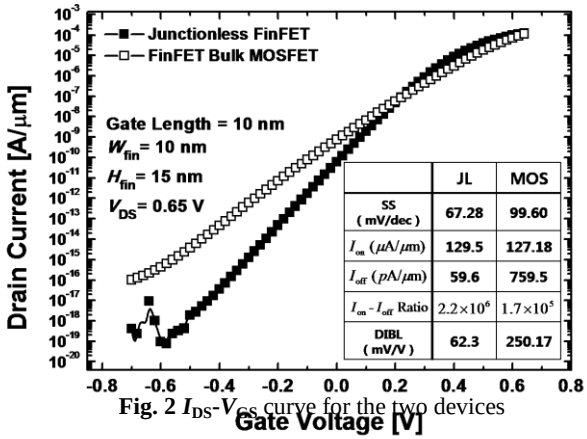


Fig. 2 I_{DS}-V_{GS} curve for the two devices

[1] SILVACO International, ATLAS User's Manual, 2012.

[2] Low Standby Power Technology Requirements, International Technology Roadmap for Semiconductor, 2012.

GOI Improvement of Novel Buried N-Type Capacitor

Kyungmin Kim[1,2], Ilseok Han[1], Jeongho Cho[1], Junggoo Park[1], Sewoon Kim[1], Jiyoung Huh[1], Sungyoun Kim[1], InWha Choi[1], Sibum Kim[1], and Hi-Deok Lee[2]

[1]*SMS Product Engineering, Magnachip Semiconductor, Cheongju-si 361-728, Korea*

[2]*Department of Electronics Engineering, Chungnam National University, Daejeon 305-764, Korea*

E-mail : hdlee@cnu.ac.kr

We investigated the Gate Oxide Integrity (GOI) failure of a novel buried N-type capacitor and found out that the cause of the failure is mainly due to the high dose implantation process. It was confirmed that Si pit phenomenon appears because of the impact of high dose implantation. This is because that insufficient PR treatement can cause the ion implanted photoresist (PR) popping during the high temperature dry strip process.[1] Si pit can also be explained in terms of PR adhesion. Outgassing during the high does implanation weakens PR adhesion and the weakened adhesion of PR is another cause of Si pit.

A new and effective test pattern is used for the GOI test. The test pattern for the novel buried N-type capacitor is consisted of both the active edge and the field edge in the form of array as shown in Fig. 1. The experiment result using Di/O_3 post cleaning process shows the great improvement of the GOI performance than the conventional plasma post cleaning process as shown in Fig. 2. During the plasma post cleaning process, Si pit is generated by the direct reaction between the undercut portion of the oxidized photoresist and the wafer surface. Besides, Si pit can be formed by the photoresist popping. In case of applying Di/O_3 cleaning process, the surface of the wafer is directly oxidized by the PR during the cleaning process, accordingly removing the volatile components, which supress the formation of Si pit.

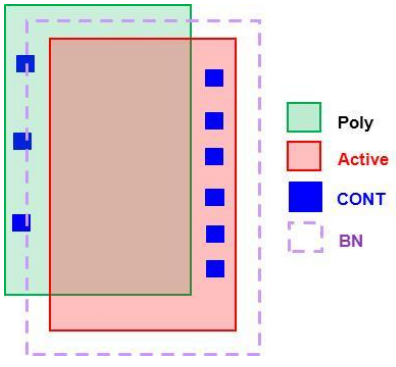


Figure 1. New test pattern for BN capacitor

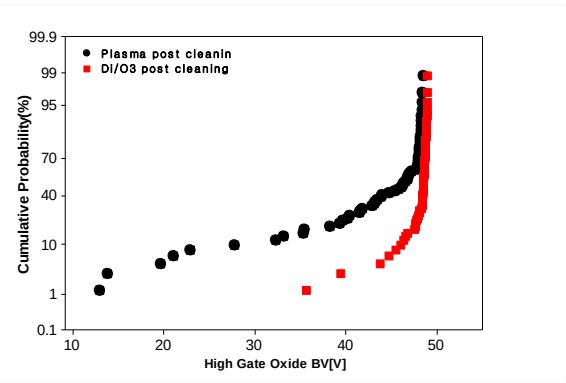


Figure 2. The cumulative distributions of breakdown votlage using the test pattern.

[1] C. Jasper, A. Hoover, K.S. Jones, Applied Physics Letter, Vol.75, No.17, 147 (1999).

Analysis of 90nm RF CMOS characteristics by Gate Layout Optimization

Jong Keun Kim, Bong Woo Han, Hee Kyeong Yang, Myoung Jun Jang, In Wook Cho, and Kyung Dong Yoo

Technology Development in Image Development Group, SK hynix,

Gyeongchung-dearo, Ami-ri, Bubal-eup,Icheon-si, Gyeonggi-do 467-734, Korea

E-mail : jongkeun.kim@sk.com

For several years, considerable research attention has focused on the high performance of RF CMOS due to the advantage of low power consumption and low cost [1]. In this article, we suggest advanced RF CMOS device by improving the cut-off frequency (f_T) and the maximum oscillation frequency(f_{max}) with gate layout optimization. Three types of gate geometry were adopted with 90nm n-MOSFET process; meander type, comb type and window type (Fig 1). First on, number of gate fingers had influence on RF performance in RF CMOS device. In addition, we observed that different gate layout caused the value shift of cut-off frequency and maximum oscillation frequency. This phenomena is caused by parasitic capacitances with several types of gate design [2].
According this result, the optimized gate layout and number of gate fingers to maximize the cut-off frequency and the maximum oscillation frequency have been found.

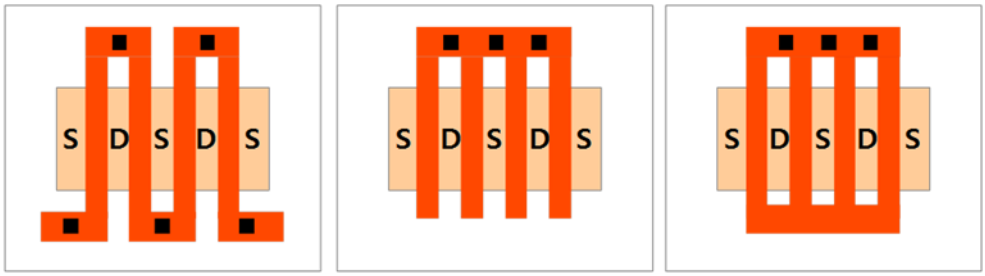


Fig 1. The 90nm Layout of n-MOSFET (a) Case 1(Meander type ; Reference) (b) Case 2(Comb type) (c) Case 3(Window type)

[1] Pierre H. Woerlee,"RF-CMOS Performance Trends," IEEE Transactions On Electron Devices, vol.48, No.8, pp.1776-1782, (2001)
[2] Kwangseok Han, Jeong-hu Han,"RF characteristics of 0.18um CMOS Transistor," Journal of the Korean Physical Society, Vol. 40, No.1, pp45-48, (2002)

Transfer-Printing the micro-structure devices on flexible substrates

Kyu-Bong Choi, and Jong-Ho Lee
Department of ECE and ISRC, Seoul National University, Seoul 151-747, Korea
E-mail : jhl@snu.ac.kr

Recently, flexible devices is impotant to use semiconductor devices on very small or irregular space. But most of the flexible substrate are very vulnerable to high temperature during fabricating Si-based devices. To overcome this issue, transfer-printing method that is transfering the device which is fabricated on si substrates on flexible substrates has been used. [1] To transfer print, the device fabricated on Si substrate must have a structure to be separated easily from Si substrate. So the device should be floated with anchor by means of lateral isotropic etching materials (Si) under the device. In this paper, we deposited a 100 nm SiO_2 and 100 nm Al on bulk Si. This Al was patterned with lines and pads that sizes are 5 μm width, 1000 μm length and 150 μm by 150 μm respectively. After etching the Al, we formed the lateral anchor which supports the device. We etched the SiO2 by reactive ion etching process. The remaining parts of SiO_2 function as lateral anchors. To float the device, Si under the device was etched isotropically by high-density F-based plasma process. Fig. 1(a) shows the device fabricated on Si substrates. After fabricate the floated devices, we lifted-off the devices using the poly-dimethyl-siloxane (PDMS) and transferred the device from PDMS to flexible substrate (PET), as shown in Fig. 1(b). Fig. 1(c) shows measured I-V curve of the device on PET.

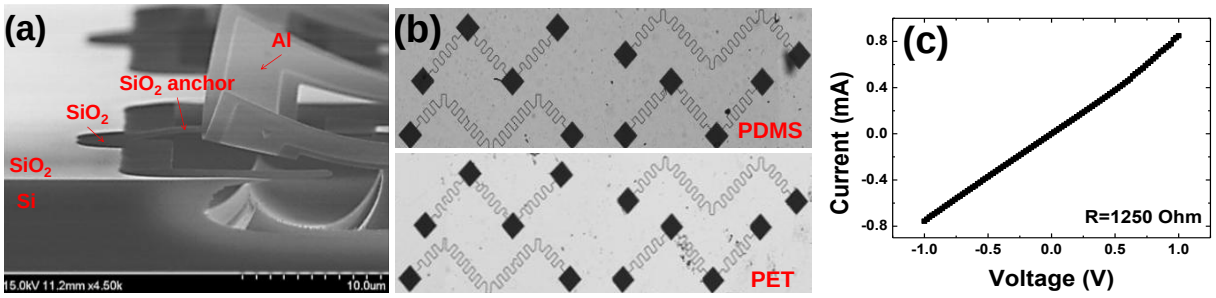


Fig 1. (a) SEM image of fabricated devices. (b) Devices on PDMS and PET.
(c) measured I-V curve of the device on PET

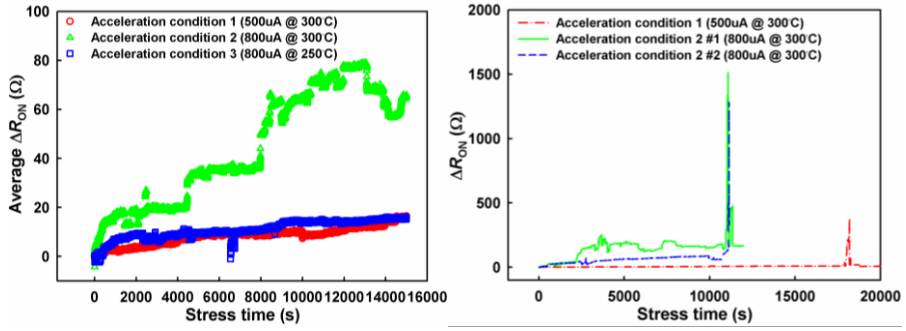
[1] K. J. Lee et al., “Fabrication of microstructured silicon(um-Si) from a bulk Si wafer and its use in the printin of high-performance thin-film transistors on plastic substrates,” in J. Micromech. Microeng., vol. 20, 2010, pp. 075018(8).

On-State Resistance Instability of Antifuses during Read Operation

Jae Hwan Han[1*], Hyunjin Lee[2], Wansoo Kim[2], Gyuhan Yoon[1], and Woo Young Choi[1]
[1]Department of Electronic Engineering, Sogang University, Seoul, 121-742, Korea
[2]SK Hynix, Icheon-si Gyeonggi-do, Korea
E-mail : runblack@naver.com

An antifuse (AF), one of the most promising one-time programmable (OTP) memory technology, is widely used in various applications such as field programmable gate array (FPGA), dynamic random access memory (DRAM) and static RAM (SRAM). Among various AFs, the standard complementary metal-oxide-semiconductor (CMOS) AF using poly-Si gates with SiO_2 gate insulator is cost-effective because it is fully compatible with CMOS process [1]. Although the on-state resistance (R_{ON}) instability (*RI*) of programmed AF occurs during read operation, which means that R_{ON} is increased by read current, there have been few studies on standard CMOS AFs. It is because thermal hard breakdown (HBD) in a SiO_2 film is not recovered. However, if the stress current is limited during breakdown, quantum point contact HBD (QPC HBD) occurs [2]. The reversibility of QPC HBD in an ultra-thin SiO_2 film has already been reported: it is induced by the rearrangement of defects forming conductive filaments (CFs) driven by electron wind force (i.e. electro-migration effects) [3]. Because the program current of an on-chip AF is limited, the CFs of programmed AFs can be formed by QPC-HBD. Thus, it is necessary to investigate the *RI* of standard CMOS AFs. In this paper, we have observed the *RI* of programmed AFs for the first time by using two acceleration factors: stress current and ambient temperature. First, all AF cells are programmed with a compliance current 1 mA at room temperature. Next, the *RI* of programmed AFs has been measured under the constant current stress condition at high temperature.

Fig. 1 shows that the *RI* consists of three phases: soft *RI*, hard *RI* and R_{ON} recovery. R_{ON} increases steadily and slightly in the soft *RI* phase. Then, it increases abruptly due to the electro-migration effects in the hard *RI* phase. Following the hard *RI* phase, R_{ON} is recovered to the initial R_{ON} level in the R_{ON} recovery phase. Fig. 1a shows the average R_{ON} variation ($\Delta R_{ON}(t) \equiv R_{ON}(t) - R_{ON}(0)$) in the soft *RI* phase measured under different acceleration conditions. Fig. 1a shows that high stress current and temperature accelerate soft *RI*. Fig. 1b shows the $\Delta R_{ON}(t)$ of some measured AF cells showing hard *RI* events. These cells show the soft *RI* phase before the hard *RI* occurs. It means that the hard *RI* randomly occurs depending on atomic topology. After the hard *RI* phase, R_{ON} is recovered to the initial R_{ON} level: R_{ON} recovery phase. It is because new defects are easily generated by the high electric field applied across the unoccupied spots of CFs by electro-migration effects. Fig. 1b shows that the hard *RI* has the same acceleration trends as the soft hard *RI*. When higher stress current is applied, the hard *RI* occurs earlier, more frequently and more rapidly. Also, it should be noted that no hard *RI* has been observed at low temperature.



(a) (b)

Fig. 1. (a) Average $\Delta R_{ON}(t)$ in the soft *RI* phase under each acceleration condition. (b) $\Delta R_{ON}(t)$ of some samples showing hard *RI* events.

ACKNOWLEDGMENTS: This work was supported in part by SK Hynix, in part by the NRF of Korea funded by the MSIP under Grant 2013-027714 (Mid-Career Researcher Program), in part by the NIPA funded by the MSIP under Grant NIPA-2013-H0301-13-1007 (University ITRC Support Program) and in part by the KEIT funded by the MOTIE under Grant 10039174 (IT R&D Program).

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[3] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, and X. Aymerich, *Solid-State Electron.*,45 (2001).

In-situ Hafnium capping process for 0.6 nm EOT on Ge wafer

정원일 [1], 신윤상 [1], 이충호 [2], 손동균 [2], 조병진 [1*]
[1]KAIST 전기전자공학과, Phone: 042-350-3485, email: bjcho@kaist.edu
[2]삼성전자 S.LSI 사업부

높은 hole mobility 를 가지는 Ge 은 열과 습기에 취약한 GeO_2 의 특성을 극복할 수 있는 안정적인 gate dielectric 공정이 중요하다. 본 연구에서는 vacuum chamber 내에서 GeO_x native oxide 를 제거하고 곧바로 초박막 (0.5 nm) Hf metal 을 in-situ 로 증착하여 Ge surface 를 capping 하는 새로운 공정을 개발하였다. 이를 통하여 native oxide 의 재생성을 억제하고, 이후 ALD 공정으로 HfO_2 를 gate dielectric 으로 증착하였을 때, 0.7 nm 이하의 EOT 에서 10^{-4} A/cm^2 이하의 낮은 게이트 누설전류 (at $V_G=V_{FB}+1V$), 그리고 낮은 hysteresis 전압 ($\Delta V_{FB} < 80$ mV)을 달성할 수 있었다. 이 공정방법은 HfO_2 유전막내로의 Ge 확산을 효과적으로 억제함을 SIMS 분석을 통하여 확인하였다 (Fig.1(d)). 또한 XPS 분석과 TEM 이미지(Fig.1(b))를 통하여 HfO_2 유전막의 상부에 낮은 κ 값 (~11)을 가지는 Hf-Ge-O 층 (~2 nm)의 생성도 억제 (Fig.1(c))됨으로써 매우 낮은 EOT 를 유지하면서도 효과적으로 전기적 특성을 개선 할 수 있음을 확인하였다. 현재까지 발표된 Ge 위에서의 high-κ gate dielectric (ALD-HfO_2) 과의 benchmark data (Fig. 1(a)) 비교에서, 이 공정은 기존의 방법에 비하여 EOT 를 크게 낮추면서도 낮은 누설전류를 가짐을 알 수 있다.

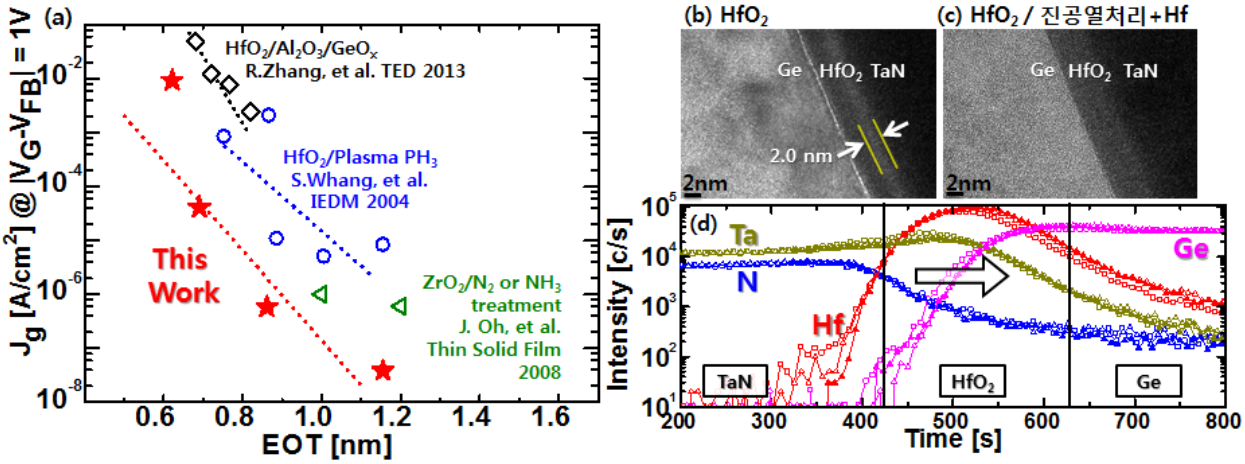

Fig. 1. (a) In-situ Hf capping 공정을 적용한 high-κ on Ge 의 EOT 와 누설전류 비교. (b) 표면처리없이 HfO_2 로만 이루어진 소자의 TEM 이미지와 (c) 진공열처리와 in-situ Hf 초박막처리한 소자의 TEM 이미지. (d) (b)와 (c)구조에서의 SIMS 분석 결과.

Voltage scaling of 3-D stacked NAND Flash string with vertical single-crystal Si channel epitaxially grown on (100) Si-substrate

Wan-Gyu Lee, Ho Seong Jeon, Seung-Dong Yang*, Ga-Won Lee*, and Jeoung Woo Kim
Nano- materials and devices, National NanoFab Center, Daejeon 305-806, Korea,
**Department of Electronics Engineering, Chungnam National University, Daejeon 305-764, Korea*
E-mail : wangyulee@nnfc.re.kr

Recently, 3-D memories have been attracted increasing attention due to their capabilities of continuous integration in bit density and reducing a bit cost[1]. We investigated the vertical NAND Flash with single crystal silicon channel to solve limitations of poly-silicon[2]. The device shows on/off ratio of $>10^8$ and S.S of ~190. The higher on current and on/off ratio may facilitate easy extending 3-D stacking further. The enhancement in channel characteristics can be significantly influenced by channel diameter size, dopant redistribution during the Si channel growth, source and drain (S/D) structure, and S/D extension junction. These phenomena can be well explained by the electrical field focusing due to the rounded gate and/or auto-doping during the epitaxial growth of Si channel. In this study we focused on the channel diameter scaling effects of 3-D NAND flash string. This study enables viable routes toward the further integration and extension to higher stacking of nonvolatile 3-D NAND Flash memory technology.

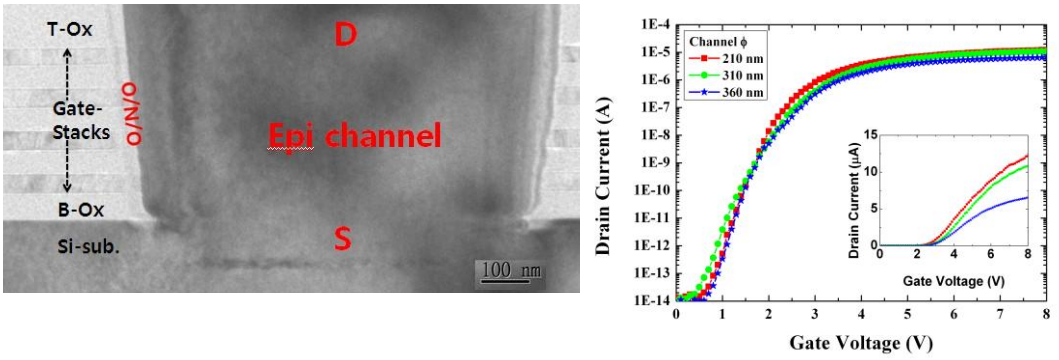

Fig 1. TEM image (left) and I_D-V_{GS} curves (right) of the vertical Flash device.

[1] H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata,Y. Matsuoka, Y. Iwata, H. Aochi and A. Nitayama, VLSI 2007, 14.
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Characterization of dielectric relaxation and reliability of high-k MIM capacitor

Ho-Young Kwak[1], Seung-Yong Sung[1], Hyuk-Min Kwon[1], Sung-Kyu Kwon[1], Jong-Kwan Shin[1], Seong-Yong Jang[1], Sun-Man Hwang[1], Su Lim[2], and Hi-Deok Lee[1,*]

[1]*Department of Electronics Engineering, Chungnam National University, Daejeon 305-764, Korea*

[2]*Dongbu HiTek Semiconductor Inc., Bucheon, Gyeonggi 420-712, Korea*

[*]E-mail : hdlee@cnu.ac.kr

Recently, MIM capacitors have generated great attention in silicon integrated circuit applications as passive component. As the total area of passive devices, capacitor especially, usually consumes a large portion of the whole chip size, MIM capacitors with a high capacitance density have been required to increase the circuit density and reduce the system cost [1]. Due to the outstanding properties, such as high capacitance density, good thermal stability, and high bank gap, hafnium-oxide-based MIM capacitors are widely used for the next generation capacitor [2]. However, the single layer of high-k dielectric shows high leakage current. Therefore, laminate or sandwiched structures of MIM capacitor adding Al_2O_3 or SiO_2 layers have been studied for advanced leakage current. In this paper, the reliability and dielectric relaxation of advanced capacitors with Al_2O_3-HfO_2-Al2O_3 (AHA) and SiO_2-HfO_2-SiO_2 (SHS) sandwiched structure are analyzed under constant voltage stress. Figure 1 shows the general voltage shape across the MiM capacitor. It is shown that the dielectric relaxation of AHA is much greater than that of SHS as shown in Fig. 2.

This work is financially supported in part by the Ministry of Knowledge Economy (MKE) and Korea Institute for Advancement of Technology (KIAT) through the Workforce Development Program in Strategic Technology.

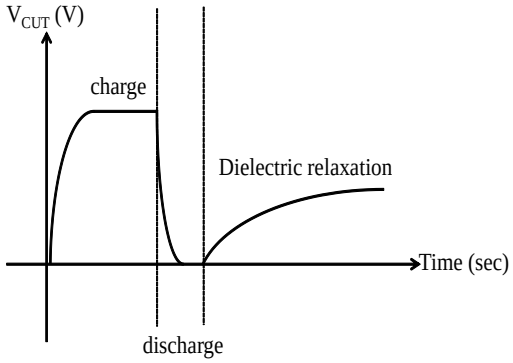


Fig. 1. Voltage shape across the MIM capacitor during the measurement of dielectric relaxation.

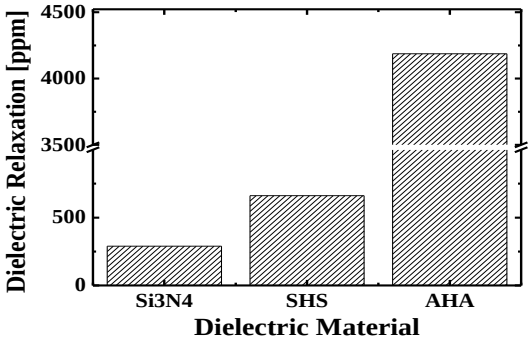


Fig. 2. Dielectric relaxation characteristic of the MIM capacitors with different dielectric materials.

[1] H. Hu, C. Zhu, Y. F. Lu, Y. H. Wu, T. Liew, M. F. Li, B. J. Cho, W. K. Choi, and N. Yakovlev, J. Appl. Phys, Vol.94, No.1, pp.551-557, Jul. 2003.

[2] X. Yu, C. Zhu, H. Hu, A. Chin, M. F. Li, B. J. Cho, D. L. Kwong, P. D. Foo, and M. B. Yu, IEEE Electron Device Lett., Vol.24, No.2, pp.63-65, Feb, 2003.

An experimental verification of a scaled RC-dominant interconnect line model for High-speed wireline

Jiwon Kim, Taehee Kim, Byungsub Kim, Jeong-soo Lee
Department of Electrical Engineering, Pohang University of Technology and Science, Pohang, Korea
E-mail : jiwon104@postech.ac.kr

Computers use many cores to increase throughput in modern computing system. To synchronize distributed cores, systems require energy-efficient high-speed interconnects. The most promising solution is scaled interconnect lines, which have a unique RC-dominant characteristics due to narrow and tightly packed lines and require simple and accurate channel model Choi *et al*. proposed simple and accurate chanel model, but is not experimentally verified [1]. In this work, we verify the previous channel model by experiment.

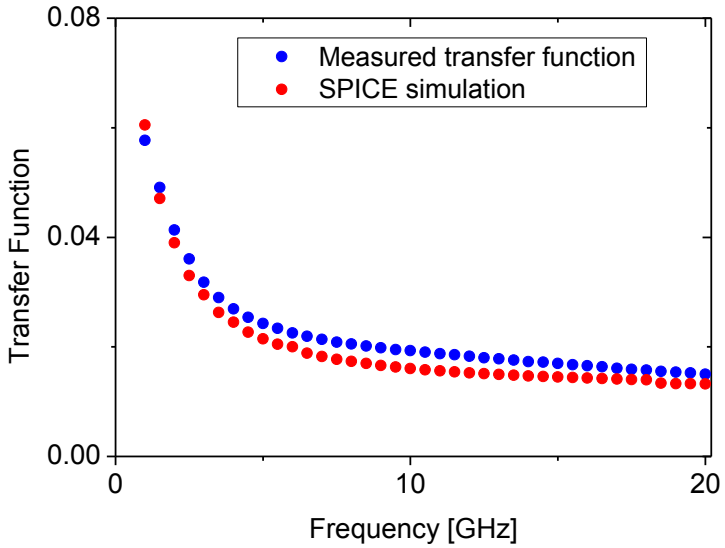


Fig 1. Comparison between the measured voltage transfer function and SPICE simulation.

[1] M. Choi, J.-Y. Sim, H.-J. Park, B. Kim, Journal of Semiconductor Technology and Science, vol. 13, no. 5, oct., 2013.

High Performance of Graphene Ion-sensitive Field-Effect Transistors using a Solution-Processed Al_2O_3 Sensing Membrane

Tae-Eon Bae[1], Jongwan Jung[2] and Won-Ju Cho[1]*
Department of Electronic Materials Engineering, Kwangwoon University, Korea
Institute of Nano and Advanced Materials Engineering, Sejong University, Korea
E-mail : taeunlove1220@nate.com

Graphene is a two-dimensional sheet of carbon atoms forming a single atomic layer. It exhibits excellent electrical, mechanical and chemical properties, such as extraordinary high carrier mobility, high flexibility and high transparency.[1] For these reason, graphene FETs based on the CVD-synthesized technique have recently been a growing interest as chemical and biological sensor. Meanwhile, the sensing characteristics of FET based sensors are mainly determined by the inherent properties of the sensing membrane which is in direct contact with the electrolyte. In this experiment, we fabricated the graphene ISFETs with Al_2O_3 sensing membrane by utilizing a solution-processed deposition technique to overcome the hindrances inherent in a vacuum process. It offers great advantages in terms of low cost, simplicity, high throughput, and large-area devices unlike vacuum-process methods.[2] Most importantly, it can be easily applied to the graphene FETs because the plasma process for deposition of membrane is unnecessary. Particularly, the Al_2O_3 sensing membrane used in this experiment exhibits better chemical stability and performance in comparison with other materials. As a result, the graphene ISFETs with solution-deposited Al_2O_3 sensing membrane exhibited excellent characteristics, which is very promising to biological sensors application.

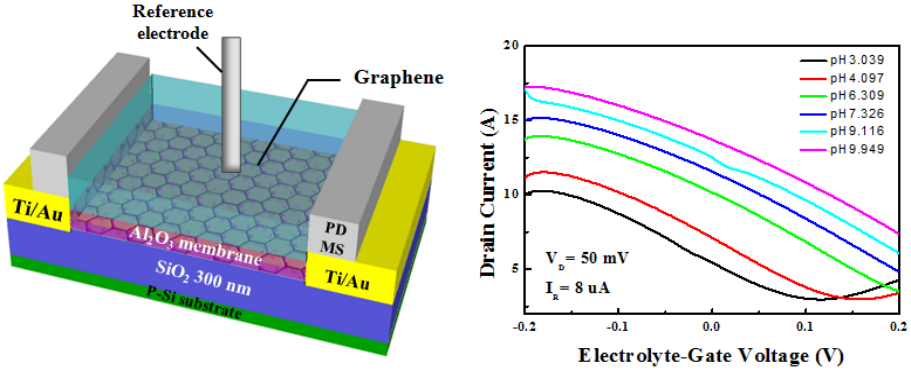


Fig 1. Fabricated graphene ISFETs and its sensing property.

[1] A. K. Geim and K. S. Novoselov, Nature. 6, 183 (2007).
[2] C. G. Lee and A. Dodabalapur, Appl. Phys. Lett. 96, 243501 (2010).

This research was supported by the Converging Research Center Program through the Ministry of Science, ICT and Future Planning, Korea (No. 2013K000372) and the research grant from Kwangwoon University in 2013.

The stability of plug and play quantum cryptography system with double phase modulation method

Osung Kwon, Min Ki Woo, Min-Soo Lee, Byung Kwon Park, Il Young Kim, Yong-Su Kim, Sang-Wook Han, and, Sung Moon

Center for Nano & Quantum Information research, Korea Institute of Science and Technology (KIST), Seoul, 136-791, Korea

E-mail : *oskwon12@kist.re.kr*

We introduce a simple and robust polarization-insensitive phase modulation method that is suitable for a plug and play quantum key distribution system [1], with a polarization sensitive phase modulator. The pulse arrived at Alice is modulated twice before and after it is reflected by a Faraday mirror that is located at the end of Alice. We realize the phase modulation method and verify it by observing a single-photon interference with high visibility (>95%) regardless of the polarization of the signal. The phase modulation method is successfully applied to a plug and play quantum key distribution system and consistently provides less than 5% of quantum bit error rate under changing environmental condition.

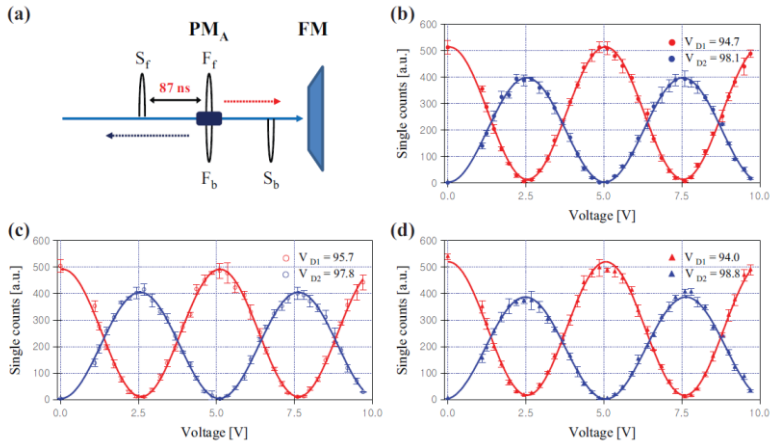


Fig 1. (a) The scheme of double-phase modulation. (b) ~ (d) The single photon interference had been measured by three polarization of pulse.

[1] N. Gisin, G. Ribordy,W. Tittel, and H. Zbinden, Rev. Mod. Phys. 74, 145–195 (2002).

ACKNOWLEDGMENTS

The work was supported by the IT R&D program of MSIP/KEIT. [10044559, Development of key technologies for quantum cryptography network]

Low voltage operation of an electrostatically driven peristaltic pump

Pyohwan Hong[1], Deaseung Pyo[1], Jonghyun Lee[1], Chanseob Cho[1], Bonghwan Kim[2].
[1]*Kyungpook National University, School of Electronics Engineering, Daegu, Korea.*
[2]*Catholic University of Daegu, Department of Electronics Engineering, Gyeonbuk, Korea.*
E-mail : bhkim@cu.ac.kr

Recently, microfluidic systems that enable functions such as electrophoretic separations and fluidic manipulations(mixing, reacting, piping, and valving) have been developed to driving system to move fluids through a micropump. Micropumps can be divided under driving method. There have been several designs for micropumps based on different driving forces including piezo-electric, electrostatic, thermopneumatic, and pneumatic, etc. In general, the advantages of electrostatically driven methode is rapid respons time and high stroke volume. However, electrostatically driven designs are required high operating voltage[1, 2]. This paper describes an electrostatically driven peristaltic micropump which was fabricated using a thin membrane. We reduced to half the thickness of the membrane through dry etching process. The thin membrane of micropump can lead to low driving voltage. To fabricate the thin membrane, the reactive ion etching system(RIE) are used with metal shadow mask which was opened in the marked area in Fig. 1. After shadow mask was aligned to micropump, membrane was etched by RIE. Through this process, the membrane thickness and driving voltage were reduced from 2um to 1um and about 40V, respectively.

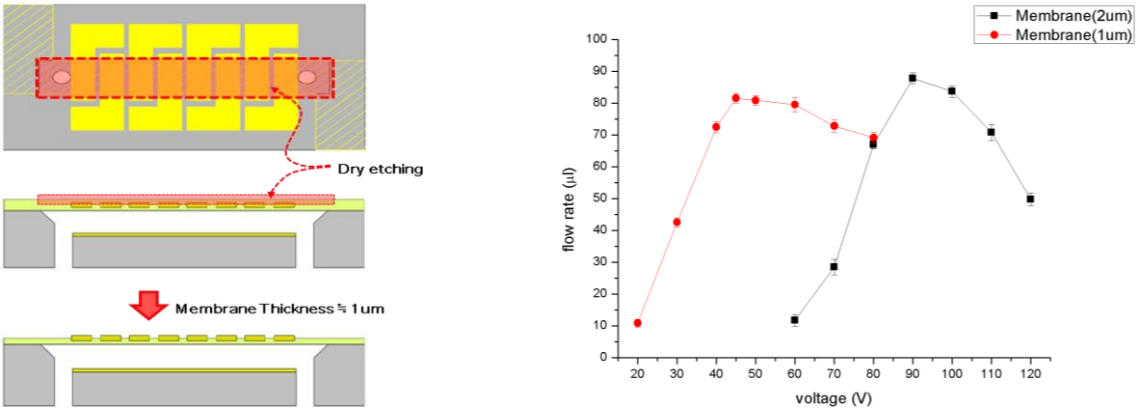


Fig 1. Process flow (left) and the flow rate under operating voltage (right).

[1] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis, Nat. Nanotechnol. 6, 147 (2011).
[2] K. Cho, W. Park, J. Park, H. Jeong, J. Jang, T.-Y. Kim, W.-K. Hong, S. Hong, and T. Lee, ACS Nano, in press (2013).

Effect of microwave annealing for stability improvement of amorphous InGaZnO thin-film-transistor based SnO_2 extended-gate field-effect-transistor

In-Kyu Lee, and Won-Ju Cho
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail : 2002mrlee@hanmail.net

EGFET 는 전해질 속의 각종 이온 농도를 전기적으로 측정하는 바이오 센서로, 감지부와 측정부로 분리된 구조를 가지고 있다. 현재, EGFET 감지부의 감지막으로는 Al_2O_3, HfO_2, TiO_2, SnO_2 와 같은 다양한 물질들이 사용되고 있으며, 그 중 SnO_2 는 고감도와 우수한 안정성을 가지고 있는 물질로 추가적인 열처리 공정이 없어도 우수한 감지 특성을 나타내기 때문에 본 연구에서 감지막으로 사용되었다. 한편, EGFET 의 측정부로는 기존의 비정질 실리콘 TFT 에 비해 10 배 이상의 높은 이동도와 온/오프 전류비를 갖는 InGaZnO 를 채널층으로 사용한 TFT 를 사용하였다. IGZO 는 넓은 밴드 갭으로 인해 가시광 영역에서 투명하며, 향후 이를 이용하여 투명 바이오 센서 제작 시, 물질들 사이의 반응을 전기적 신호뿐만 아니라 광학적인 분석 방법으로도 검출이 가능하기 때문에 고 신뢰성을 갖는 센서의 제작이 가능할 것으로 기대된다. 한편, IGZO-TFT 는 우수한 전기적 특성을 나타냄에도 불구하고 소자 동작 시 문턱 전압이 불안정하다는 단점이 있으며 [1], 이러한 문제의 개선과 향후 투명 기판 위에서의 제작을 위해서는 저온 열처리 공정이 필수적이다. 이때, 열처리 공정에 있어서 기존의 furnace 열처리의 경우, 간접적 열 전달 방식으로 인해 에너지 효율이 떨어지고 공정 시간 및 비용이 많이 든다는 단점이 있으며, 이를 대체하기 위해 본 연구에서는 microwave 열처리를 이용하였다. Microwave 열처리는 타겟에 에너지를 직접적으로 전달하여 에너지 효율이 높고 공정 시간 및 비용 또한 적게 들며, 저온 공정임에도 소자 특성 개선이 우수하다는 장점을 가지고 있다. 결과적으로, 본 연구에서는 microwave 열처리를 통하여 IGZO-TFT 의 전기적 특성 및 안정성을 향상시켰으며, 9.51 [cm^2/V·s]의 이동도와 135 [mV/dec] 의 SS 값, 0.99 [V]의 문턱 전압, 1.18E+08 의 온/오프 전류 비를 갖는 고성능 스위칭 TFT 를 제작하였다. 최종적으로, microwave 열처리된 IGZO-TFT 를 SnO_2 감지막을 갖는 EG 에 적용함으로써 안정성이 향상된 고성능, 고감도의 바이오 센서를 제작하였다.

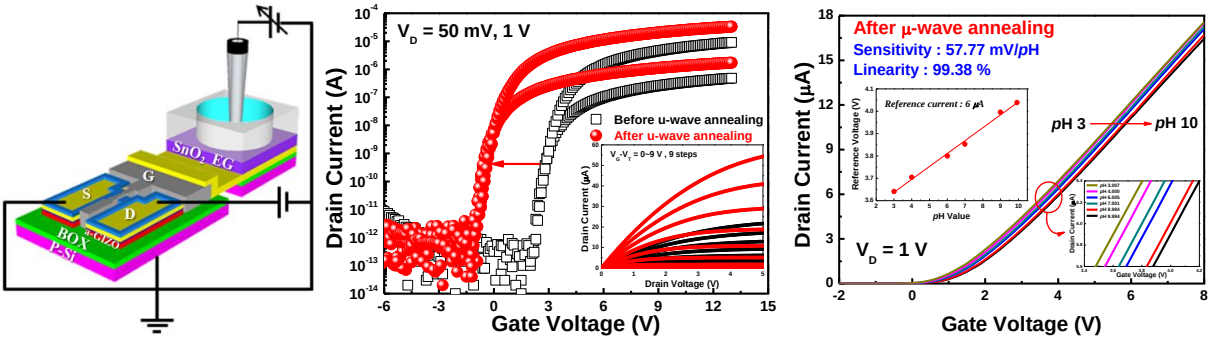


Fig 1. GIZO-TFT based SnO_2 EGFET device and its electrical and sensing characteristics

[1] W. T. Chen, S. Y. Lo, S. C. Kao, H. W. Zan, C. C. Tsai, J, H. Lin, C. H. Fang, and C. C. Lee, IEEE Electron Device Lett. 32, 1552 (2011).

The comparison of noise characteristics between Si and Pyrex substrate in solid-state nanopore

Kyeong Beom Park[1], *Ashvani Kumar*[1], *Hyun-Mi Kim*[1] *and Ki-Bum Kim*[1*]

[1] Department of Materials Science and Engineering, Seoul National University, Seoul 151-742, Korea

[*] To whom correspondence should be addressed. E-mail: kibum@snu.ac.kr, Telephone: 82-2-880-7095, Fax: 82-2-885-5820

DNA sequencing has been known as the key technology to provide human information such as disease, inheritance and individuality. Since the idea was proposed that it might be possible to detect each nucleotides of DNA by using nano-scale pores in 1996[1], the nanopore detection method has widely researched as a new solution of DNA sensing method as well as a single molecule sensing. Among several nanopores, it is indicated that solid-state nanopore has lower noise characteristics than biological nanopore. Generally, solid-state nanopore is fabricated by Si-compatible process and Si substrate is reported to cause a high noise.

So, we investigated the Pyrex glass-compatible process to decrease high noise in solid-state nanopore. Unlike Si-substrate, pyrex-based nanopore shows lower dielectric noise than Si-based nanopore because Pyrex has good dielectric properties. Also, we fabricated the different types nanopore; Graphene, Boron nitride and SiNx membrane. And these nanopores shows similar noise characterics. This fact means that the dielectric noise is dominantly influenced by substrate, not membrane.

This work will offer new fabrication platform in solid-state nanopore replacing Si-based platform and will also widen the possibility of solid-state nanopore into the single molecule detection.

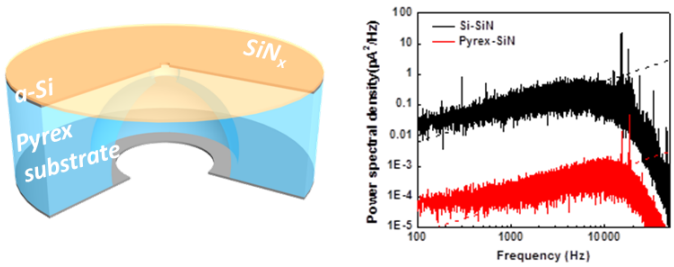


Fig 6. Pyrex-based nanopore and its noise characteristics

[1] J. J. Kasianowicz, E. Brandin, D. Branton, D. W. Deamer,. *PNAS* **93**, 13770 (1996).

Impedance characteristics of GSG electrodes for RLGC modeling of cell-electrode interface

Jongmin Shin, and Jong-Ho Lee*
Department of ECE and ISRC, Seoul National University, Seoul 151-747, Korea
* E-mail : jhl@snu.ac.kr

In the neural engineering, extracellular electrical stimulation and recording has been widely used for decades with microelectrodes[1]. For RLGC modeling of cell-electrode interface, electrode that is suitable for high frequency stimulating and recording neurons must be adopted. In this study, we designed ground-signal-ground(GSG) electrodes for high frequency stimulation and recording of neural network. GSG electrodes were made of platinium (geometric area: 140 ㎛× 90 ㎛) and passivated by 1 ㎛ SiO_2-Si_3N_4-SiO_2(ONO) stack layer. To investigate electrical properties of GSG electrodes, we use elecetrochemical impedance spectroscopy(EIS). The impedance of GSG electrodes was measured in phosphate buffered saline (PBS) solution. The GSG electrodes-electrolyte interface are modeled by charge transfer resistance and constant phase angle(CPA) element. In order to measure impedance, 10 mVrms AC signal is applied as a function of frequency. GSG electrode impedances are ~ 100 kΩ at 1 kHz. As the frequency increases, capacitance of the total impedance becomes dominant. Finally, since GSG electrode-electrolyte interface act as a high pass filter.

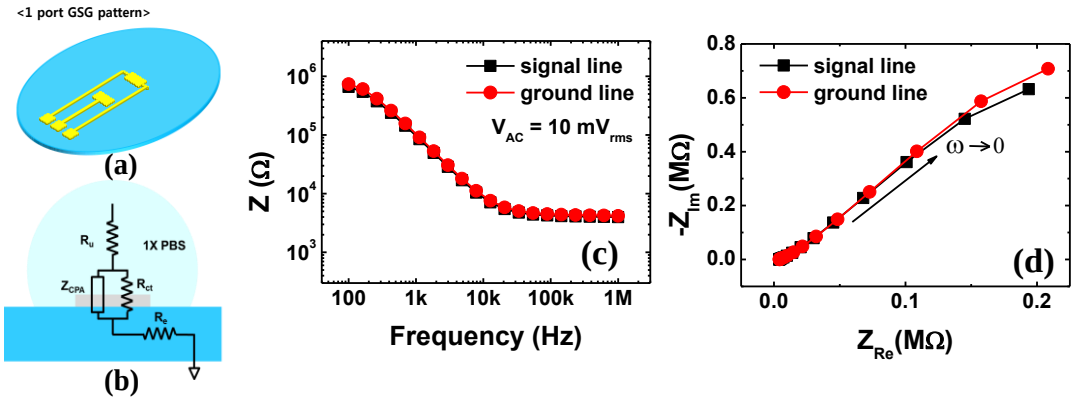


Fig 1. (a) GSG electrodes, (b) equivalent circuit model, (c) measured impedance, and (d) Nyquist plot

[1] Yoonkey. Nam, Bruce C.Wheeler, Marc O. Heuschkel, Journal of Neuroscience Method,. 155, 296-299 (2006).

High sensitive Ge resistance temperature device by adding transition metals

Jiyoun Choi, Jeongyong Choi, Sungyoul Choi, Yooleemi Shin, and Sunglae Cho
Department of Physics, University of Ulsan, Ulsan 680-749, Korea
E-mail : slcho@ulsan.ac.kr

Resistance temperature device (RTD) is a temperature sensor using the temperature dependent electrical resistance variation of materials. The important requirements of RTD for an accurate temperature measurement are good sensitivity, reproducibility, short-term and long-term stability, fast thermal response, and small change at high magnetic field or ionizing radiation, etc. The commercial RTDs are Pt, carbon-glass, Ni, Cu, RuO, NiO, RhFe, Ge, and so on. Among them, the most commonly used cryogenic RTD in the range between 0.05 and 100 K is Ge, which is heavily doped with As, Sb or Ga, because of its high sensitivity, reproducibility, low price, and excellent resistance to ionizing radiation, etc. The electrical resistance variation of a typical Ge RTD was about 10^3 times between 5 and 100 K. We have grown un-doped and transition metal (V, Cr, Mn, Fe, Co, Ni, Cu)-doped Ge bulk single crystals using the vertical gradient solidification method. The electrical resistivities of V, Ni, Co, and Fe-doped Ge crystals significantly increased, $10^4 \sim 10^5$ times, between 5 and 100 K, which were 100 times larger than that of the commercial Ge resistance temperature device(RTD). The large variation of electrical resistance at low temperature arises from decreased carrier density and mobility at low temperature. The mobility reduction at low temperature might be caused by ionized impurity scattering.

An accurate and efficient simulation technique for FET-type biosensors

Bongsik Choi, Jieun Lee, Dong Myong Kim, Dae Hwan Kim, and Sung-Jin Choi*
School of Electrical Engineering, Kookmin University, Seoul 136-702, Korea
E-mail : *sjchoiee@kookmin.ac.kr

There is growing interest in the application of electrolyte-insulator-semiconductor field-effect transistor (EISFET) to the electronic sensing of biomolecules [1]. This study presents a novel simulation method for EISFET in electronic biomolecule sensing application. The proposed method considers the fact that the ionic solution, i.e., the electrolyte, can be defined as an emulated intrinsic semiconductor material for the realization of FET-type biosensors, using a well-established commercial semiconductor 3D TCAD simulator. The proposed simulation method employs the Gouy-Chapman-Stern model [1] of the electrical double layer as well as an effective ionic concentration in a real ionic solution. The simulation results ensure that the Debye length obtained from the simulation corresponds well with the calculated Debye length. Furthermore, the application of the simulation method to pH sensors is successfully demonstrated by incorporating the site-binding model [1-2]. Therefore, the proposed method is able to simulate any type of FET-type biosensor and can be utilized to predict the optimal sensor performance.

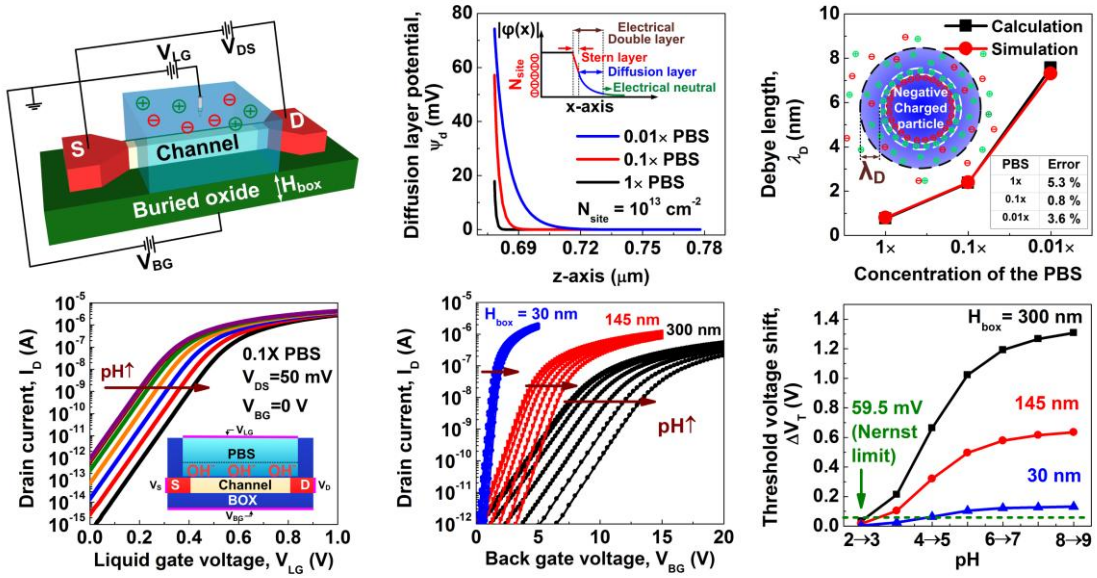


Fig 1. 3D biosensor device and its electrical data under pH and PBS concentrations

[1] M. W. Shinwari, M. J. Deen and D. Landheer, Microelectron. Reliab. 47, 12 (2007).
[2] S. Chen, J. G. Bomer, E. T. Carlen and A. van den Berg, Nano Lett. 11, 6 (2011).

Characteristics of robust infra-red photodiode for harsh environments

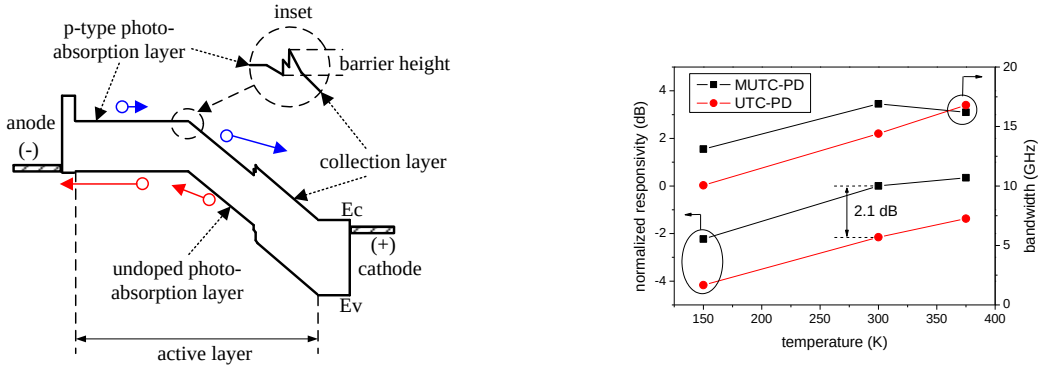
Dong-Hwan Jun[1], Won-Kyu Park[1], Jong-In Song[2]

[1] *Korea Advanced Nano-Fab Center, Suwon, 443-270, Korea*

[2] *School of Information and Communications, Gwangju Institute of Science and Technology*

E-mail : jisong@gist.ac.kr

High sensitivity photodiodes having a wide operating temperature range are advantageous in harsh environments especially for outdoor sensor applications. Semiconductor photodiodes such as p-i-n, avalanche, and uni-traveling carrier photodiodes have exhibited high speed and high efficiency within limited temperature ranges of about one hundred Kelvin[1]. In this paper, a modified uni-traveling carrier photodiode (MUTC-PD) is proposed and compared with a conventional uni-traveling carrier photodiode (UTC-PD) with temperature ranges from 150 K to 375 K. Fig. 1 (a) illustrates a simplified band-diagram of an InP/InGaAs MUTC-PD. The inset also shows the conduction band of an InP/InGaAs UTC-PD at the heterointerface of the p-type photo-absorption layer and the InP collection layer. The major difference between the MUTC-PD and the UTC-PD in terms of electron transport is the location of the potential barrier in the conduction band. In the UTC-PD, electrons are transported in the p-type photo-absorption layer by diffusion mechanism and thus do not have enough energy to overcome the barrier height at low temperatures, leading to reduction in photocurrent. However, in the MUTC-PD, the effect of the potential barrier can be alleviated since it is located away from the edge of the p-type photo-absorption layer within the depletion region, where electrons can get enough energy to overcome the potential barrier even at low temperatures. Fig. 1 (b) shows the comparison of the responsivity and bandwidth of MUTC-PDs and UTC-PDs as a function of the temperature. Further comparisons will be presented.



(a) (b)

Fig. 1. Band-diagram of MUTC-PD and normalized performances of MUTC and UTC-PDs.

[1] H. Ito, S. Kodama, et. al., IEEE J. Sel. Top. Quantum Electron. 10 (2004) 709.

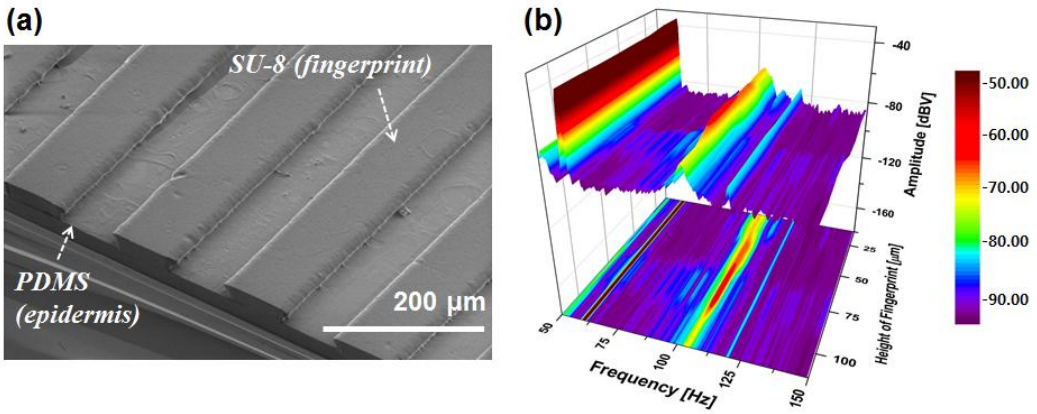
The Shear Force Transfer Characteristics Dependent on the Height of Bio-mimetic Fingerprint Structure for Tactile Sensor

Hyunsuk Chun[1], Eunsuk Choi[1], Soonhyung Hwang[1], Joonhyung Cho[1], Hyungyu Lee[1] and Seung-Beck Lee[1,2*]

*[1] Department of Electronic Engineering [2] Institute of Nano Science and Technology, Hanyang University, Seoul, 133-791, South Korea *E-mail address: sbl22@hanyang.ac.kr*

Humans sense external stimuli such as pressure, temperature, vibration, etc. with tactile corpuscles and perceive the information of contact material. The contact is made at the stratum corneum of the epidermis, where hardened dead skin cells form fingerprint ridge structures with periodicities that match the primary frequency of the texture information transferred down to the mechanoreceptors located at the dermis. The fingerprint amplifies the vibrations which reflect surface texture more than a dozen times compared to flat surfaces. In this study, we have conducted research on the height of bio-mimetic fingerprint structures and the thickness of epidermis for efficiently detecting the periodic textures of the contacted materials.

We controlled the height of bio-mimetic fingerprint (SU-8) and thickness of epidermis (PDMS) from 25 μm to 100 μm each by changing the speed of spin coating. Fabricated fingerprint structures were attached to polyvinylidene fluoride (PVDF) sensor to measure pressure transmission properties of the bottom pressure sensor. As a result, as thickness of PDMS increase, the pressure transfer characteristic increased. However, above ~ 75 μm of thickness, pressure transmission property decrease due to its thickness. The pressure transmission properties increased as the height of fingerprint structure gets higher, but at certain height, mechanical reliability decreased. We have successfully detected the surface properties of diverse materials using our tactile sensor.



(a) The SEM image of bio-mimetic fingerprint and epidermis (b) The periodic pressure transfer characteristics of fingerprint structure with different height

ITO와 금속 격자를 이용한 박막 태양 전지 효율 증대

허형준, 김상인
아주대학교, 전자공학부
E-mail : sangin@ajou.ac.kr

최근에 박막 비정질 실리콘(a-Si) 태양전지의 얇은 흡수 층에서 태양광 흡수효율을 증가시키기 위한 광학 구조에 대한 연구가 많이 진행되어 왔다. 앞서 연구된 여러 광학 구조 중 뒷면에 금속 반사체를 갖는 a-Si 위에 매우 얇은 금속 격자가 놓인 구조[1]는 금속 격자로 인한 surface plasmon polaritions(SPPs) 모드와 누설 모드의 효과를 통해 600~900nm 파장영역의 흡수효율을 크게 증가시켰다. 우리는 이 구조를 기반으로 300~600nm 파장대역의 흡수효율을 증가시키기 위하여 Fig 1.a 와 같이 금속격자 위에 적절한 두께의 Indium Tin Oxide(ITO)를 덮는 구조를 설계하였다. ITO 층의 추가는 바닥 금속과 a-Si 사이에 발생하는 SPPs 모드가 특정 주파수 영역에서 누설 모드로 형성되도록 하는 효과를 줄 수 있다. 따라서 이 누설모드로 인한 흡수효율 증대 효과가 단파장 영역에서 나타나도록 ITO 두께를 설계하여 기존 구조의 흡수율 향상을 기대할 수 있다. Fig 1.b 는 전산모사 결과로 기존 구조의 장파장 대역의 흡수효율의 특성을 상당히 유지하면서 단파장 영역의 흡수효율이 증가됨을 확인할 수 있다. 우리가 설계한 구조는 앞서 유사한 형태의 2D 격자 구조[2]로 소개된 바 있지만 간단한 1D 격자 구조의 모드 분석을 통해서 보다 손쉬운 구조 설계가 가능하다. 또한 이와 같은 구조는 위 부분을 태양전지의 전극으로 이용할 수 있다는 이점도 가지고 있다.

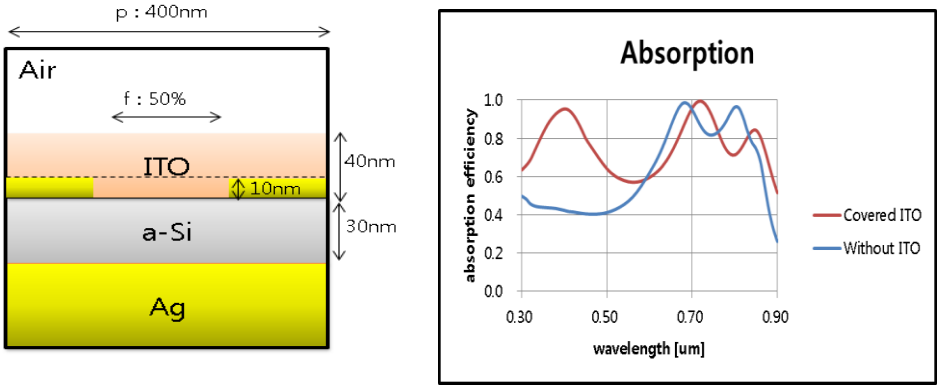


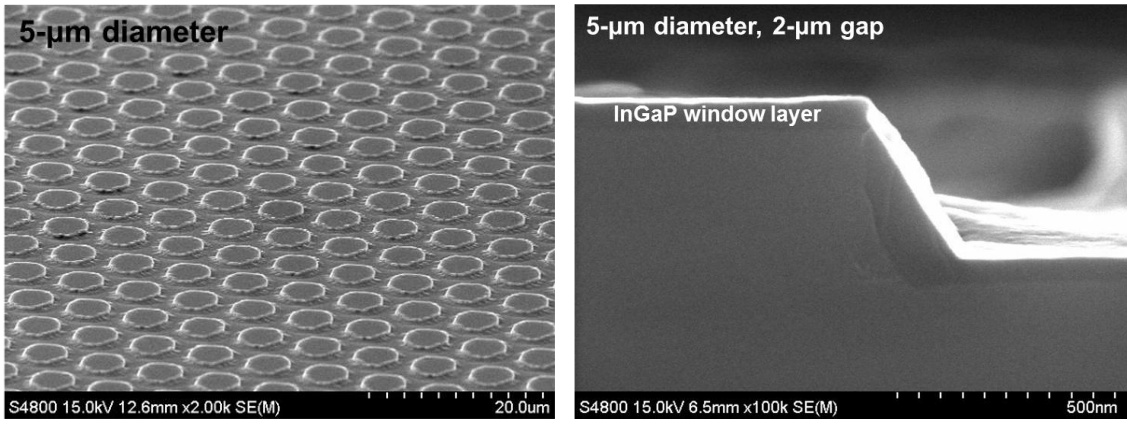
Fig 1. 구조와 흡수 스펙트럼

[1] S. Lee and S. Kim, Photonics Journal, IEEE 5, 5 (2013).
[2] Y. wang, T. Sun, T. Paudel, Y. Zhang, Z. Ren and K. Kempa, Nano Latters 12, 440 (2012).

Influences of cylindrical micro-patterned Ge substrates on the characteristics of the Ge single-junction solar cells

Kangho Kim, Youngjo Kim, Nguyen Dinh Lam, and Jaejin Lee*
Department of Electrical and Computer Engineering, Ajou University, Suwon, 443-749, Korea
E-mail : jaejin@ajou.ac.kr

The Ge single-junction solar cell structures have been grown on micro-patterned Ge substrates using low pressure metalorganic chemical vapor deposition. A height of 300 nm micro-rod arrays are formed on p-Ge substrates using photolithography and dry etching techniques. The micro-rod arrays are disgned with a variation in diameters from 5 to 15 μm and in spaces from 2 to 12 μm. The Ge p-n junction structures are realized by phosphorus atomic diffusion processes on the micro-patterned Ge substrates. A 100 nm thick InGaP window layer and a 300 nm thick GaAs cap layer are grown to reduce the surface recombination and the ohmic contact resistivity, respectively. The GaAs cap layer is removed during the fabrication process. The cross-section and surface of the fabricated solar cells are investigated by a field-emission scanning electron microscopy (FE-SEM). The InGaP window layer can be grown on the micro-patterned Ge substrates as shown in Fig.1. Characteristics of the fabricated solar cells are investigated by a solar simulator under AM1.5 global illuminations. The device performances of the micro-patterned Ge solar cells can be improved compared to a planar cell due to the enhancement of light absoption properties. The highest efficiency of 4.78% can be obtained in the Ge solar cell with 5 μm-diameter, 2 μm-gap, and 300 nm-height micro-rod arrays.



(a) (b)

Fig 1. (a) Tilt- and (b) cross section-view FE-SEM images of the micro-patterned Ge solar cells.

Particle Swarm Optimization of grating enhanced CIGS solar cell

Tran Quyet Thang, Le Duy Khanh, Sangin Kim*
Department of Electrical and Computer Engineering, Ajou University, Suwon 443-749, Korea
**sangin@ajou.ac.kr*

CuInxGa(1-x)Se2 (CIGS) based thin film solar cells has been considered one of the most promising technology due to high efficientcy (as high as 20%) and cost effective [1]. To further enhance performance and reduce the total volume of active material required, a simple 1d dual-grating based light trapping mechanism was proposed and investigated. The structure consists of a bottom silver reflector and grating, and a top CIGS grating. Due to the combined effects of guided mode resonances and light trapping between the two gratings, light can be efficiently trapped and absorbed within a very thin active layer, reducing the recombination rate while keeping absorbtion efficiency high accross the solar spectrum. The structure was numerically studied using the rigoriously coupled wave analysis (RCWA) method. Due to a high number of design parameters, the particle swarm optimization (PSO) method was employed. Normalized net absorption efficiency of the active layer (total absorbtion minus that of non-active material) was used as the evaluating function. The optimized structure showed a net absorbtion efficiency of 86.2% for TM polarization, corresponding to an overall absorbtion efficiency of 95.2%. A non polarized study, however, would be more appropriate at evaluating the performance of solar cells, and would be the objective of our further studies.

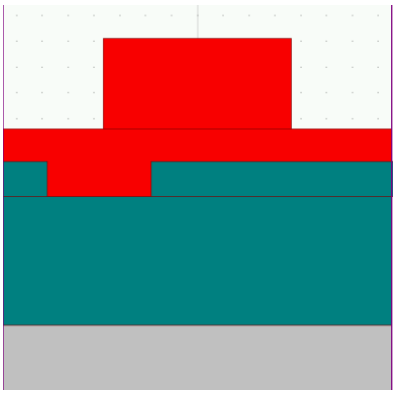


Fig 1. The dual grating unit cell. Overall active layer thickness is 120nm.

[1] W. Wang, S. Wu, R. Knize, K. Reinhardt, Y. Lu, and S. Chen, Opt. Express 20, 3733-3743 (2012).

Abnormal electrical transport properties of ferrocene-alkanethiolate molecular electronic devices on rigid and flexible substrates

Hyunhak Jeong, Dongku Kim, Hanki Lee, Wang-Taek Hwang, and Takhee Lee
Department of Physics and Astronomy, Seoul National University, Seoul 151-747, Korea
E-mail : tlee@snu.ac.kr

Molecular electronics in which individual molecules or molecular layers are utilized as active electronic device components has been widely investigated for a miniaturized device alternative of conventional solid state-based electronics [1]. As an example, it has been recently reported that the molecular junctions based on alkyl molecules with ferrocene moiety exhibited asymmetric electronic properties and were implemented as a half-wave rectifier [2].

Here, we studied the redox-induced electronic transport properties of ferrocene-alkanethiolate molecules using a conducting polymer-interlayer (PEDOT:PSS) device structure [3]. We observed asymmetric electrical transport properties, which arise due to the existence of ferrocene moiety. In particular, we observed abnormal electrical characteristics that the current in the junction decreased with increasing temperature at high temperatures (> ~220 K) and when a large positive bias (> ~0.6 V) was applied to the ferrocene end-group side. This behavior is attributed to the redox process of the ferrocene moiety in the molecular junction. We also fabricated the same molecular junctions on flexible device substrates and demonstrated consistent electrical characteristics under various bending configurations. Our study suggests the importance of consideration of intrinsic molecular reactions especially redox process when we try to organize robust functional molecular devices. And also this work provides a way toward the practical implementation of functional molecular devices with unconventional flexible configurations.

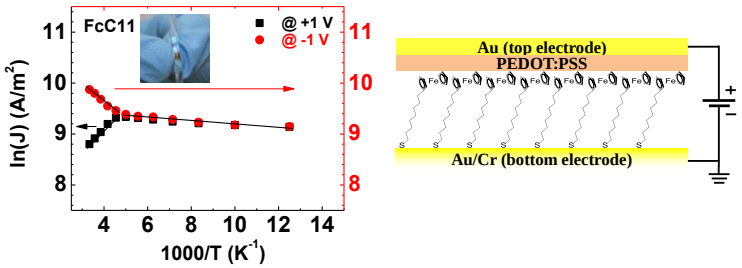


Fig 1. Abnormal electrical characteristics on flexible substrate and device configuration

[1] H. Song, M. A. Reed, and T. Lee, Adv. Mater. 23, 1583 (2011).
[2] C. A. Nijhuis et al., J. Am. Chem. Soc. 133, 15397 (2011).
[3] H. Jeong et al., submitted (2013).

Multi-level Non-volatile Polymer Memory with Solution-blended High *k* Ferroelectric Polymer Insulators for Low Voltage Operation

Sun Kak Hwang, Insung Bae, Kang Lib Kim, Richard Hahnkee Kim, and Cheolmin Park*
Department of Materials Science and Engineering, Yonsei University
Seoul, 120-749, Republic of Korea
E-mail : cmpark@yonsei.ac.kr

Polymer ferroelectric-gate field effect transistors (Fe-FETs) employing ferroelectric polymer thin films as gate insulators are highly attractive as a next-generation non-volatile memory. Furthermore, polymer Fe-FETs have been recently of interest owing to their capability of storing data in more than 2 states in a single device, that is, they have multi-level cell (MLC) operation potential for high density data storage [1,2]. However, among a variety of technological issues of MLC polymer Fe-FETs, the requirement of high voltage for cell operation is one of the most urgent problems. Here, we present a low voltage operating MLC polymer Fe-FET memory with a high k ferroelectric polymer insulator. Effective enhancement of capacitance of the ferroelectric gate insulator layer was achieved by a simple binary solution-blend of a ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) (k~8) with a relaxer high-k poly(vinylidene-fluoride–trifluoroethylene–chlorotrifluoroethylene) (PVDF-TrFE-CTFE) (k~18). At optimized conditions, a ferroelectric insulator with a PVDF-TrFE/PVDF-TrFE-CTFE (10/5) blend composition enabled the discrete six-level multi-state operation of a MLC Fe-FET at a gate voltage sweep of 18 V with excellent data retention and endurance of each state of more than 10^4 seconds and 120 cycles, respectively.

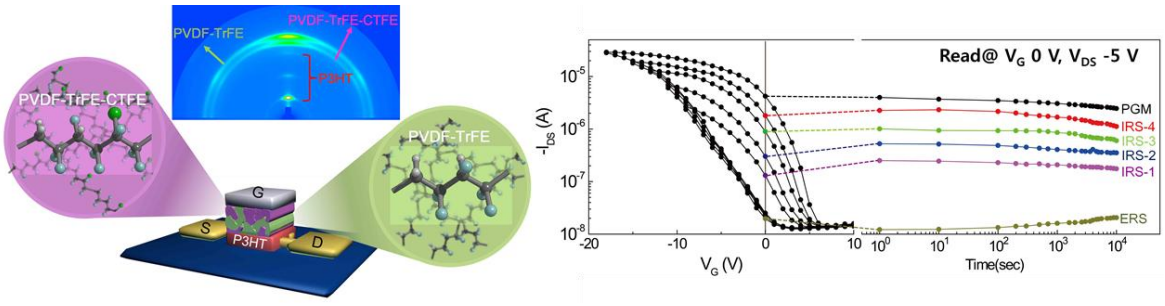


Fig 1. Polymer Fe-FET device and its I-V characteristics

[1] A. K. Tripathi, A. J. J. M. Van Brremen, J. Shen, Q. Gao, M. G. Lvan, K. Reimann, E. R. Meinders, G. H. Gelinck, Adv. Mater. 23, 4146 (2011).
[2] S. K. Hwang , I. Bae , R. H. Kim, C. Park , Adv. Mater. 24, 5910 (2012).

Optical and electrochemical properties of metallic nanostructured materials

Mi Jung, Chulki Kim, Taikjin Lee, Jae Hun Kim, Seok Lee, Deokha Woo
Sensor System Research Center, KIST, Seoul 136-791, Korea
E-mail : jmnano@kist.re.kr

Recently, metallic nanostructured materials has received intensive attention because of their potential applications for biological and chemical sensing[1]. The unique optical property of the metal nanostructure is originated from localized surface plasmon resonance (LSPR), which is a collective oscillation of the conduction electrons that occurs at a specific wavelength when light impinges on metal nanostructure [1]. Surface enhanced Raman scattering (SERS) is an analytical spectroscopy technique based on the enhancement of vibrational signals of molecules adsorbed on rough metal surfaces through the LSPR [2]. Metallic nanostructured materials can be utilized as a SERS platform for sensitive sensing of chemical materials [3].

In this work, we investigated optical and electrochemical properties of metallic nanostructured materials fabricated using nanoporous alumina mask with through-holes as an evaporation mask. The optical property of Au nanodot array and Au film were measured by ultraviolet-visible spectrometer. Electrochemical property of Au nanodot array was studied by Cyclic Voltammetry.

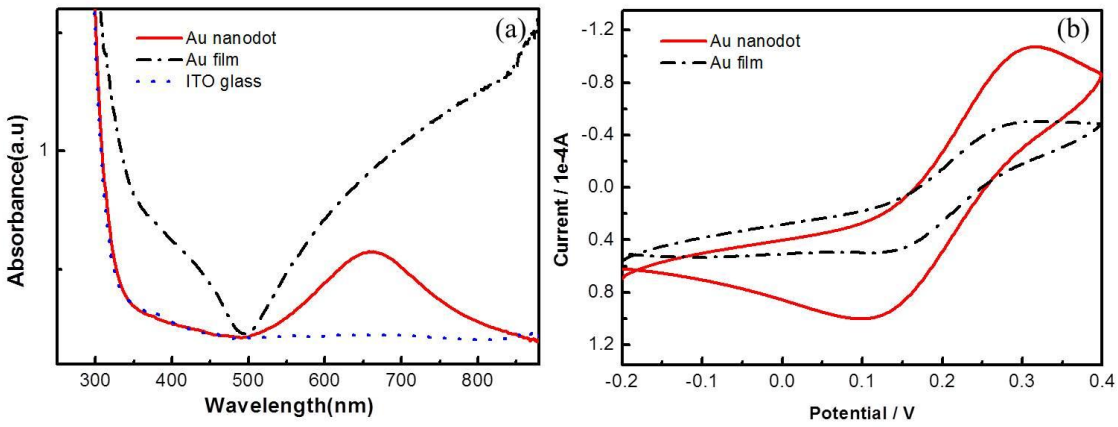


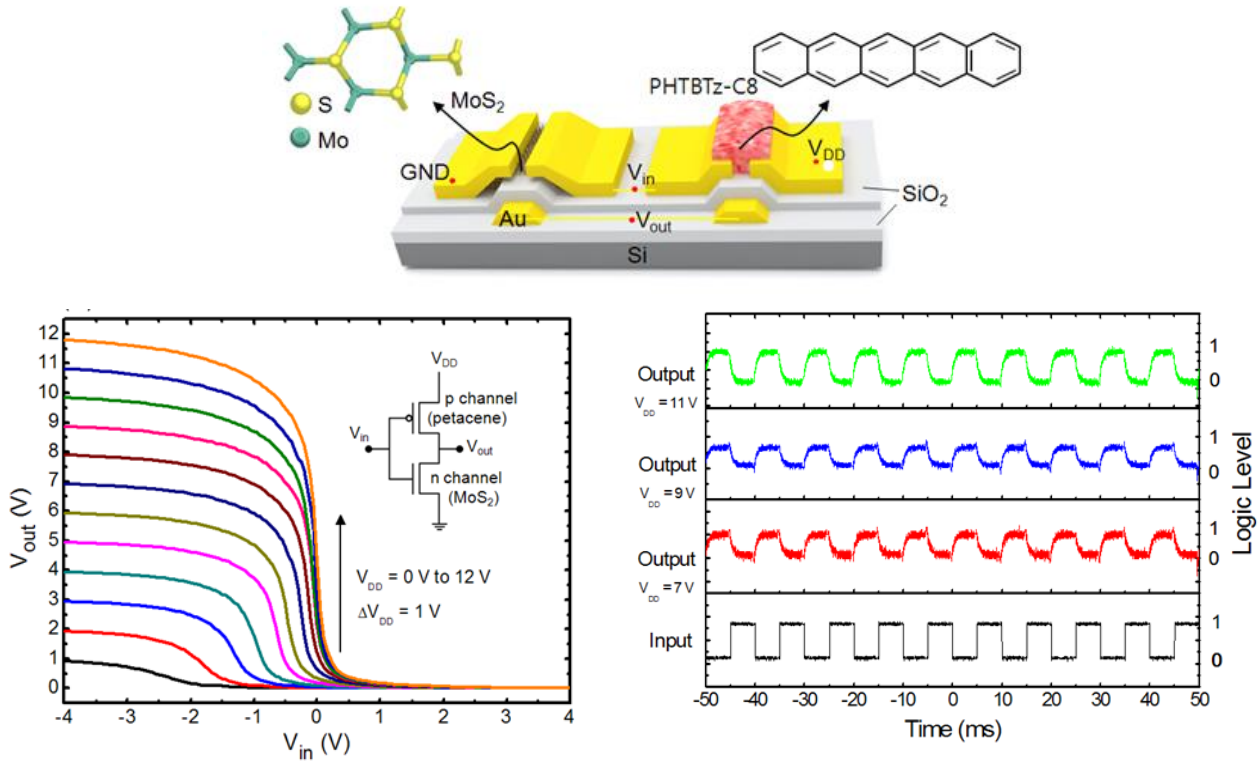
Fig 1. (a) Optical and (b) electrochemical properties of Au nanodot array

[1] K.A. Willets and R.P. Van Duyne, Annu. Rev. phys. Chem. 58, 267(2007).
[2] P L. Stiles, J.A. Dieringer, N.C. Shah and R.P. Van Duyne, Annu. Rev. Anal. Chem.1, 601(2008).
[3] M. Jung, S.K. Kim, S. Lee, J.H. Kim and D. Woo, Journal of Nanophotonics 7(1), 073798(2013).

Hybrid Complementary Invertor Based on Organic / 2D Layered MoS2 Thin Film Transistors

Chulseung Jung, Yeonsung Lee, Junyeon Kwon, Yongbok Lee, and Sunkook Kim
Department of Electronics and Radio Engineering, Kyung Hee University, South Korea
E-mail : seonkuk@khu.ac.kr

The growing demands for low-power human augmented electronics have been widely the driving force for development in flexible/stretchable thin-film transistors and novel process strategies. Various flexible thin-film materials and devices have been designed to integrate them into the basic building blocks of digital circuits, such as invertors, logic gates, and rign oscillators. However, thin film materials are inheretly difficult to dope them into an extrinsic p-type or n-type semiconductor, thus the alternative methods are proposed to exploit pseudo-invertor, consisting of an unipolar transistors and an enhancement load using different work-function gate electrodes. For the realization of high performance, low power building block of digital circuits on the flexible substrate, we report a novel hybrid complementary invertor based on inkjet printed polymer PMOS and 2D layered MoS_2 NMOS on flexible substrate.



[Figure] The schematic structure of hybrid complementary invertor and its dynamic behavior.

Bistable switching of self-assembled photonic crystal devices

Taejoon Park, Sunkak Hwang, Insung Bae, and Cheolmin Park*
Department of Materials Science and Engineering, Yonsei University
Seoul, 120-749, Republic of Korea
E-mail : cmpark@yonsei.ac.kr

Photonic crystals(PCs) are dielectrically periodic structure where forbidden frequency bands can exist for incident light. By proper choice of materials and structural geometry, one can create gaps in the density of states for photons as well as tailor the detailed dispersion relationship for waves propagating in the structure. PCs based on block copolymers have been of interest due to the ability to form a variety of structures, facile tunability of structures by changing molecular weight and more importantly their fabrication cost effectiveness based on solution processes. Especially bistable operation of switching photonic crystals, which allows for preservation of either transparent state or reflective state after state switching in the absence of power, is of prime importance because it significantly reduces power consumption of the device. In the most of current switching photonic crystals, [1] either mirror or transparent state gradually changes with time when the power is off. The retention properties of self assembled PCs without power have rarely been addressed. The bistable operation of self assembled PCs is hardly demonstrated due to the difficulty in fixation of ionic salt molecules preferentially absorbed in the domains in the absence of electric field. In this research, we propose innovative approaches to realize bistable operation of our tandem PC: ferroelectric switching. [2]

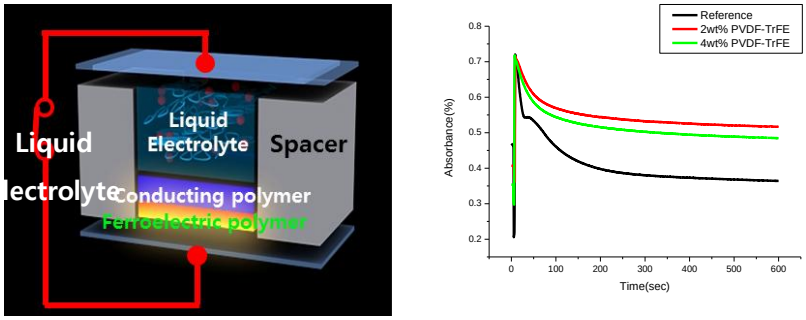


Fig 1. Schematic of switching photonic crystals and retention properties

[1] Yijie Lu,a Cong Meng,a Hongwei Xia,a Guangzhao Zhang*a and Chi Wuab, Journal of Materials Chemistry C., 2013, 1, 6107-6111
[2] Sun Kak Hwang , Insung Bae , Richard Hahnkee Kim , and Cheolmin Park *, Advanced materials., 2012, 24, 5910–5914

Gas sensing properties of Pt nanoparticles decorated ZnO-branched nanowires

Hyoun Woo Kim, Yong Jung Kwon, Hong Yeon Cho
Division of Materials Science and Engineering, Hanayng University, Seoul 133-791, Republic of Korea
E-mail : hyounwoo@hanyang.ac.kr

We have coated zinc-oxide (ZnO)-branched tin oxide (SnO_2) nanowires with a Pt shell layer via a sputtering method and subsequently investigated the effects of thermal annealing. By the thermal annealing, the Pt shell layers were agglomerated to form the nanoparticles, being comprised of the Pt phase. Sensing measurement in terms of NO_2 gas revealed that the morphology of the Pt nanoparticles affected the sensing capability, in that the abundant and dense Pt nanoparticles obtained at certain temperatures enhanced the sensitivity to NO_2 gas. We suggest that the spillover effect of Pt nanoparticles played a significant role in enhancing the response.

Scanning electron micrograph (SEMs) images were obtained by using a Hitachi S-4200 scanning electron microscope. X-ray diffraction (XRD) spectra were taken with a Philips X'pert MRD X-ray diffractometer at the Korean Basic Science Institute (KBSI). Transmission electron micrographs (TEMs) were obtained by using a Philips CM-200 (200 kV) transmission electron microscope operating at 200 kV.

Graphene nano-array fabrication by mussel-inspired directed block copolymer self-assembly

Seokhan Park, and Sang Ouk Kim
Center for Nanomaterials and Chemical Reactions, Institute for Basic Science (IBS), Materials Science & Engineering, KAIST, Daejeon, 305-701, Republic of Korea
E-mail : sangouk.kim@kaist.ac.kr

Directed self-assembly (DSA) of block copolymers (BCPs) is an emerging bottom-up technology for sub-10-nm scale nanopatterning.We have demonstrated that directed self-assembly of block copolymers in conjunction with mussel-inspired polydopamine universal adhesive accomplished highly effective fabrication process for graphene nanostructures, including graphene nanoribbon array and graphene nanomesh. Polydopamine adhesive was utilized for facile and damage-free surface treatment to complement the low surface energy of pristine graphene[1]. Significantly, our mussel-inspired nanopatterning does not require complicated process steps for inorganic sacrificial layer. Multi-channel graphene nanoribbon arrays and graphene nanomesh are successfully fabricated between metal electrodes.

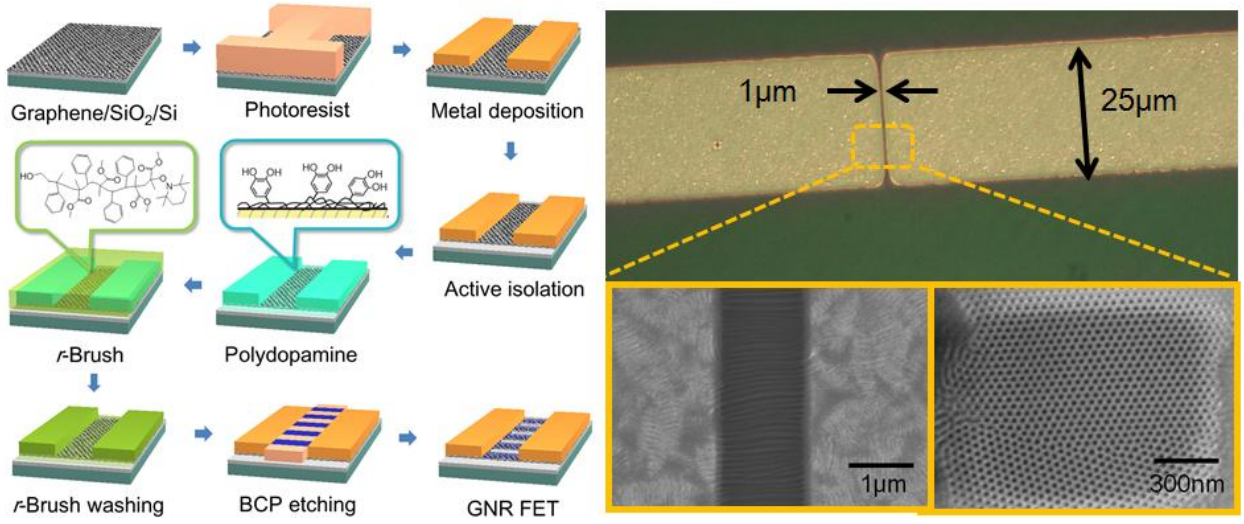


Fig 1. Fabrication procedure of Graphene nano-array

[1] Kim B H, Lee D H, Kim J Y, Shin D O, Jeong H Y, Hong S, Yun J M, Koo C M, Lee H and Kim S O 2011 Adv. Mater. 23 5618-22

Layer-by-layer growth of Bi_2Te_3-Sb_2Te_3 on h-BN via van der Waals heteroepitaxy

Hoseok Heo[1,2], Kibum Kang[1], Inchan Hwang[1,3] and Moon-Ho Jo[1,3,*]

[1]*Center for Artificial Low Dimensional Electronic Systems, Institute for Basic Science (IBS), Pohang University of Science and Technology (POSTECH), 77 Cheongam-Ro, Pohang 790-784, Korea.*

[2] *Division of Advanced Materials Science,* [3]*Department of Materials Science and Engineering Pohang University of Science and Technology(POSTECH), 77 Cheongam-Ro, Pohang 790-784, Korea*

(*The Corresponding Author : E-Mail : mhjo@postech.ac.kr)

Epitaxial growth between graphene, hexagonal boron nitride (h-BN) and chalcogenide compounds can be achieved in terms of van der Waals hetero-epitaxy due to their layered nature in crystal structure. Van der Waals hetero-epitaxy enable abrupt heterojunction with minimized defects or dislocations, because it can allows efficient stress relaxation which originated from its lattice mismatch by weakly bound by unoccupied dangling bonds. Here, we report on van Der Waals epitaxy of layer-by-layer growth of Bi_2Te_3-Sb_2Te_3 on h-BN using a two-step non-catalytic vapor deposition. Atomic force microscopy shows that as-grown Bi_2Te_3-Sb_2Te_3 2-D vertical heterostructure confirms that its growth proceeded by quintuple atomic layers as a unit. Then we found that the formation of Bi_2Te_3-Sb_2Te_3 on h-BN flake is spatially confirmed by confocal Raman spectroscopy. Furthermore, cross-sectional transmission electron microscopy shows that Bi_2Te_3-Sb_2Te_3 plates are epitaxially grown on h-BN by forming abrupt interface in spite of its lattice mismatch. Our epitaxial heterostructure of few-layer topological insulator heterostructure and insulating h-BN can be the essential basis for exotic topological insulator physics and provide practical implication for new electronics and photonics.

Electrical and Optical Properties of 2D layered MoS_2 Thin Film Transistor

Junyeon Kwon[1], Yeonsung Lee[1], Minjung Kim[1], Hyunsung Moon[1], Woong Choi[2], and Sunkook Kim[1]
[1]Department of Electronics and Radio Engineering, Kyung Hee University, South Korea
E-mail: seonkuk@khu.ac.kr
[2]School of Advanced Materials Engineering, Kookmin University, South Korea

2-dimensional crystals offer unique and compelling possibilities for nanotransistor application. The lack of bandgap in 2D graphene is overcome in series of tranisiton metal dichalcogenides: MX_2 M =W, Mo, Ta; X=S, Se, Te. The existence of a large bandgap (E_g > 1.2 eV) makes them highly attractive for electronic switching/driving devices, which are transparent, flexible, and integrable in large-scale circuit. Recently, 2D MoS_2 materials can be expected as next generation high-mobility thin film transistor for OLED and LCD backplane. In this paper, we investigate in detail the electrical and optical characteristics of 2D layered MoS_2 local bottom-gated transistor with the same device structure of the conventional thin film transistor, and expect the feasibility of display application.

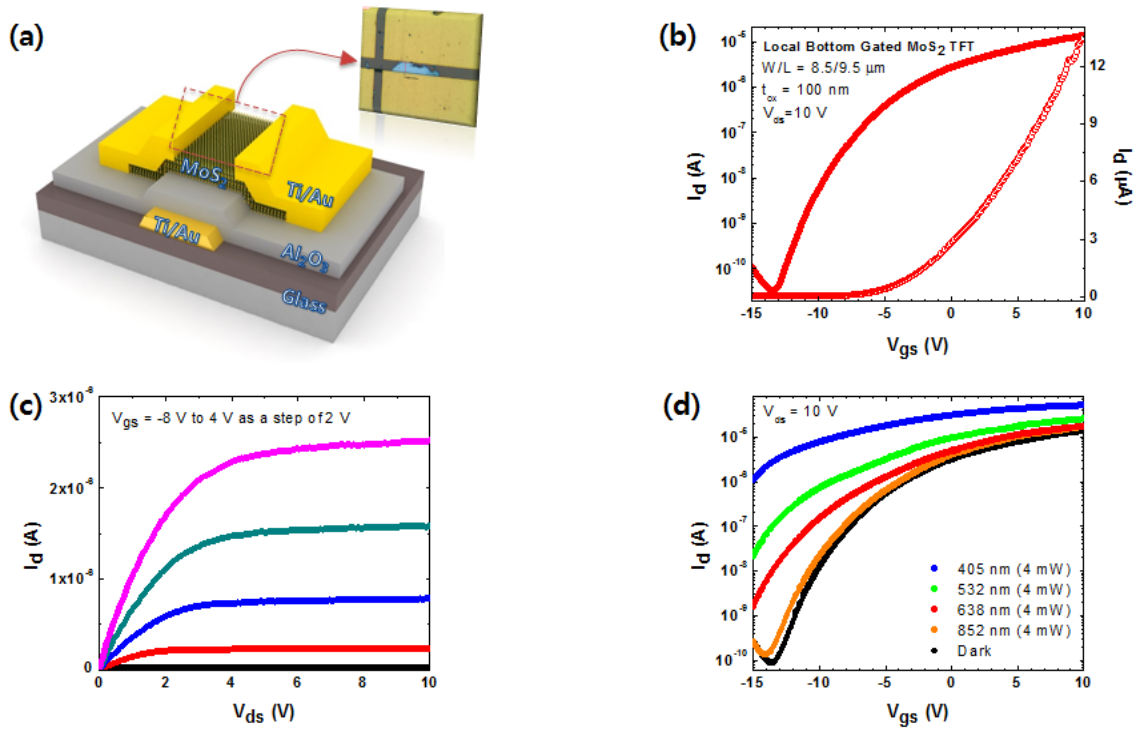


Figure (a) Schematic view of a multilayer MoS_2 transistor including ALD Al_2O_3 dielectric (100 nm), Ti / Au (15 nm / 300 nm) source/drain electrodes with local back-gated structure. Inset shows its optical image. (b) Transfer characteristics of MoS_2 transistor. Device mobility is extracted as 21 $cm^2/V \cdot sec$. (c) Output characteristics of the MoS_2 transistor. The curves recorded for various back-gated voltages with a step of 2 V. (d) Transfer curves of the MoS_2 phototransistor at various wavelengths.

Ultra-thin silicon nanomembrane for transparent and flexible transistor

Houk Jang[1,2], Wonho Lee[2] and Jong-hyun Ahn[2,*]

[1]*SKKU Advanced Institude of Nano Technology(SAINT), Sungkyunkwan University, Suwon, Kyunggi-do 440-746, South Korea*

[2]*School of Electrical and Electronic Engineering, Yonsei University, Seoul, 120-749, Republic of Korea*

E-mail : ahnj@yonsei.ac.kr

For an advanced electronic system, such as transparent and flexible electronics, organic based, oxide based and carbon-based materials, have been studied [1]. However, relatively bad stability and worse electrical properties compared to those of the conventional silicon integrated circuites are still significant challenge to be overcome. Recently, two-dimensional semiconductor material, such as MoS_2, has been studied for the electrical system [2], basic synthesis process such as impurity control and doping density control, has not been established. Here, we report ultra-thin single-crystal silicon nanomembranes (NMs), of which thickness is less than 10 nm through conventional and advanced top-down thinning process. The NMs shows good optical transmittance around 70 % and six-order lower stiffness than that of silicon with a thickness of 1.5 μm. We have successfully fabricated transistor, by combining the NMs with self-assembled monolayer (SAM) dielectric and graphene electrode, which shows good optical transmittance and good electrical properties (transmittance of > 60 %, mobility of > 100 cm^2/Vs, on/off ratio of > 10^6, subthreashold voltage of < 140 mV). The demonstration of the transparent and flexible transistor by integration of ultra-thin materials, including ultra-thin silicon NMs, provides novel routes to the human-friendly computing system.

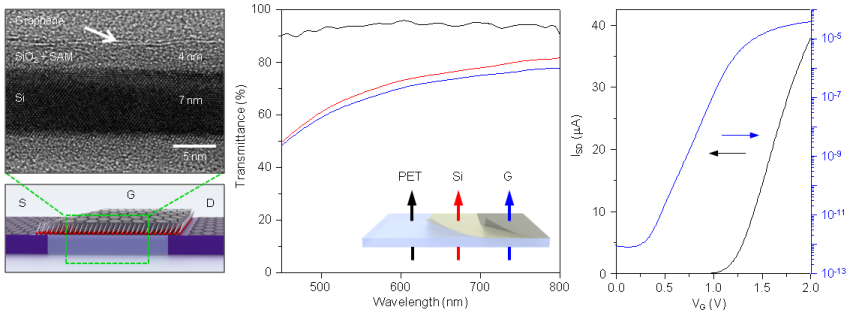


Fig 1. TEM image and schematic illustration of ultra-thin transistor (left), optical transmittance of the transistor (middle), transfer characteristic of the transistor (right)

[1] T. Sekitani, U. Zschieschang, H. Klauk and T. Someya Nat. Mater. 9, 1015 (2010).

[2] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti and A. Kis Nat. Nanotechnol. 6, 147 (2011).

High sensitive and flexible tactile sensors with a driving circuit for robotics application

Min Hoon Park[1], Houk Jang[1], Han Wook Song[3*], Min Seok Kim[3*] and Jong-Hyun Ahn[2*]

[1]*School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 440-746, Korea*

[2]*School of Electrical & Electronic Engineering, Yonsei University, Seoul,* 120-749, *Korea*

[3]*Korea Research Institute of Standards and Science (KRISS)*

Flexible tactile sensors are promising devices for future medical instruments, various electronic components and robot mechatronics. We describe the fabrication and properties of flexible piezoresistive strain sensors consisting of thin single-crystalline silicon ribbons on polymer substrate for high sensitive, conformable and flexible devices [1]. The first step in the fabrication involves heavy p-type and n-type doping using ion implantation method in each part, silicon ribbons and isolated TFT region for defining source, drain with a thickness of 260 nm. Strain gauge and TFT which are simultaneously fabricated in the doping concentration of ~1.5 x 10^{19} /cm^3 with boron and 7 x 10^{19} with phosphorus each, were transferred onto polyimide substrate by using polydimethylsiloxane (PDMS) stamp. We have successfully fabricated a high sensitive and flexible tactile sensor with 8 x 8 arrays by forming electrodes and encapsulating the device. Finally, we have integrated it with driving circuits, and characterized in terms of gauge factor, output performance and hysteresis [2].
Silicon strain gauges show stable operation while it is bent with a bending radius of 2.5 mm, gauge factors of 56, uniformity with a standard variation of 0.28, linearity of < 0.1 %, and hysteresis of < 0.2 %. Furthermore, 64 switching TFTs to block out current interfering accurate signal of each voltage among strain gauge show outstanding uniformity and high mobility of 537 cm^2 / V · s. These properties are comparable to those of conventional strain gauge, and the flexibility of device makes it as a good strain sensor for various applications such as smart gloves and E-skin for robotics.

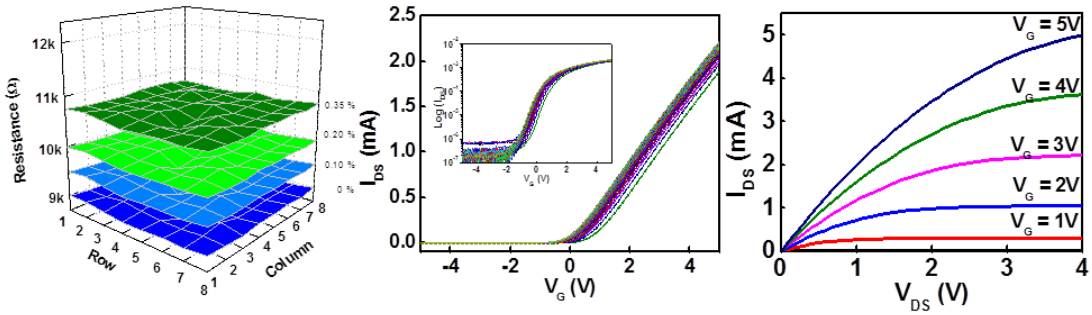


Fig 1. Gauge factor of strain gauges and switching TFT's electrical properties

[1] E. S. Hwang and Y. J. Kim, "Flexible polysilicon strain gauge array," *Jpn. J. Appl. Phys.*, vol. 42, no. 7B, pp. 810–813, Jul. 2003.

[2] J.-H. Ahn, H.-S. Kim, E. Menard, K. J. Lee, Z. Zhu, D.-H. Kim, R. G. Nuzzo, and J. A. Rogers, "Bendable integrated circuits on plastic substrates by use of printed ribbons of single-crystalline silicon," *Appl.Phys. Lett.*, vol. 90, no. 21, pp. 213501-1–213501-3, May 2007.

Superhydrophobic structures fabricated by texturing and PTFE coating

Deaseung Pyo[1], Pyohwan Hong[1], Jonghyun Lee[1], Bonghwan Kim[2], Chanseob Cho[1]
[1]*Kyungpook National University, School of Electronics Engineering, Daegu, Korea.*
[2]*Catholic University of Daegu, Department of Electronics Engineering, Gyeonbuk, Korea.*
E-mail : chocs@knu.ac.kr

Wettability of solid surface in terms of the size of the micro-nano structures has been examined. Hydrophobic experiment has studied great interests in recent years, because Technology has been used in a various field of sensor, auto glass, solar cell, building wall. The structures can be fabricated of the surface roughness and a layer of low surface energy chemical coating. However, the chemical coating is difficult is to obtain a high contact angle. The surface roughness of the high contact angle is expensive, complex, long time process. Therefore, we have developed a surface texturing RIE process with needle structures on micro pyramid structures. This process method has the advantage of low cost, simple process. We have performed p-ytpe(100) single-crystalline Si wafer(area : 156 x 156 ㎟, thickness : 200 ㎛, resistivity : 0.5-3 Ω•cm). First, all the sample were etched in KOH solution. And then needle structures were produced by RIE system(reactive ion etching). After the RIE process, PTFE coating process was conducted. The contact angle of bare wafer was 90.1°, KOH solution was 98.6°, RIE process 20min was 137.3°, PTFE coating was 163°.

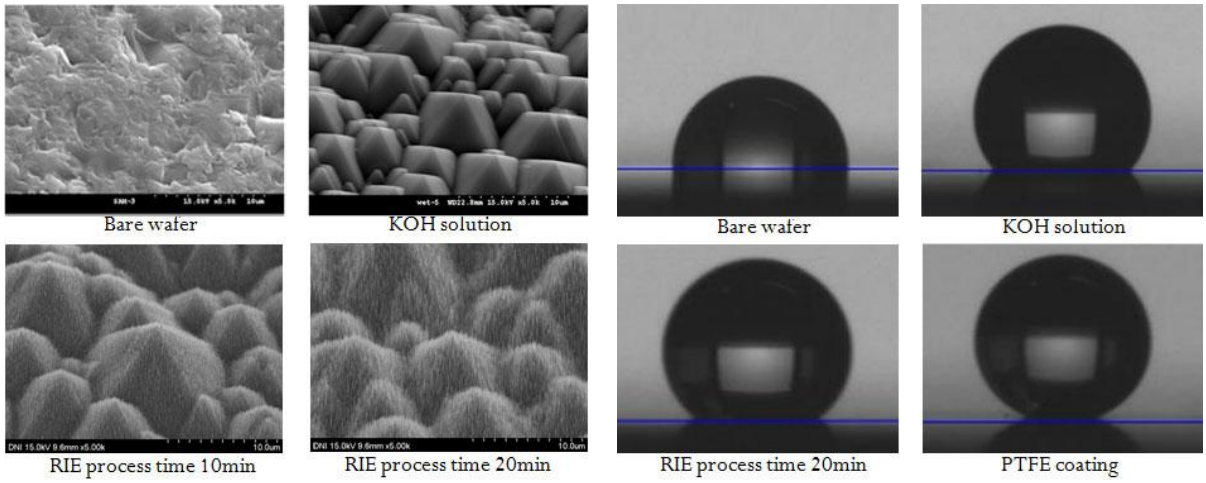


Fig 1. SEM image and Contact angle of RIE process and PTFE coating

[1] M. MORENO, SOLAR ENERGY MATERIALS & SOLAR CELLS 94 (2010)733-737.
[2] UANG HE, Applied Surface Science 257 (2011) 7689-7692.

Flexible Non-volatile Ferroelectric Memory on Metal Wire Substrate

Richard Hahnkee Kim, Sunkak Hwamg, and Cheolmin Park*
Department of Materials Science and Engineering, Yonsei University, Seoul, Korea
E-mail : cmpark@yonsei.ac.kr

The realization of elctronic devices that operate at various mechanical deformation is essential for the next generation of smart wearable and flexible electronic applications[1]. In particular, Ferroelectric-gate field effect transistors (Fe-FETs) with ferroelectric polymer layers as gate insulators have received specific attention due to their nondestructive readout capabilities[2]. We investigated the Fe-FETs on the wire type substrate such as gold wire, copper wire to break through the limit of shape of existing flexible substrates. This round type metal wire substrate has benefit to endure the high annealing temperature and degradation by using organic solvent during making the films of Fe-FETs. We fabricated the films on metal wire by dip-coating method to make the homogenous films all over area uniformly. This study will be helpful in flexible devices that can be easily rolled in various curvature environments for electronics applications.

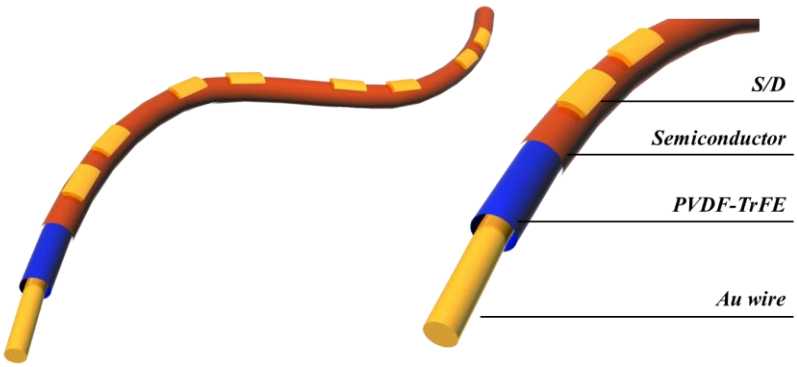


Fig 1. Wire type FeFET device structure

[1] Nomura, K. *et al.* Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432,** 488-492 (2004).
[2] Naber, R. C. G. *et al.* High-performance solution-processed polymer ferroelectric field-effect transistors. *Nature Mater.* **4,** 243-248 (2005).

Enhancing the electrical contacts of MoS_2 Field Effect Transistor via Microwave Assisted Ag Nanoparticle

Sang Jin Lee, Jong Mok Shin, Jae Sung Kim, and Gyu Tae Kim

School of Electrical Engineering, Korea University

• 초록

본 논문에서는 Ag nanoparticle 을 2D material MoS_2 field effect transistors (FET)에 scattering 하여 growth 하여 channel material 에서 metal electrode 의 contact 특성변화를 살펴보았다. 2D 소자 MOS_2 에 Ag nanoparticle 을 도포하여 seeding growth 를 위해 Microwave 를 활용하였다. Microwave 에서 Ag nanoparticle 과 MoS_2 channel material 은 반응하게 된다. Ag nanoparticle scattering 을 진행 single MoS2 FET 대비 electrical characteristic 이
개선효과가 있는지 살펴보았고, 실험을 위해 MoS_2 material SiO_2/p++ Si substrate 기판을 제작하였다. Photolithography 를 통하여 pattern drain and source electrodes 를 제작하였고, p++ Si substrate 는 bottom gate electrode 로 사용하였다. 제작된 소자의 Electrical characteristics 는 Keithley 4200 으로 측정하였다. Ag nanoparticle 은 분산하여 2 분간 microwave 에 넣어 seeding growth 를 진행하였다. Ag nanoparticle 처리 시 I-V 특성을 측정 on-off ratio, mobility, transonductance gm 값이 일부 향상되는 것을 확인 할 수 있었다. 한편 PI 기판에서 테스트 한 I-V peak 일부에서는 scattering 과 trap 으로 인하여 I-V Curve 상의 일부 불연속점이 나타나는 것을 확인 할 수 있었다. Ag nanoparticle 을 도포하여 Microwave 처리한 실험은 flexible polyimide 기판에서도 유사하게 특성이 개선된 것을 확인할 수 있었고, 향후에도 nanoparticle 을 microwave 를 활용하여 growth 처리하는 것은 테스트 및 제작이 용이하여 다양한 hybrid 소자 제작에 활용 가능성이 높다.

• 본문

본 논문의 실험을 간단하게 구성해 보면 아래과 같다.

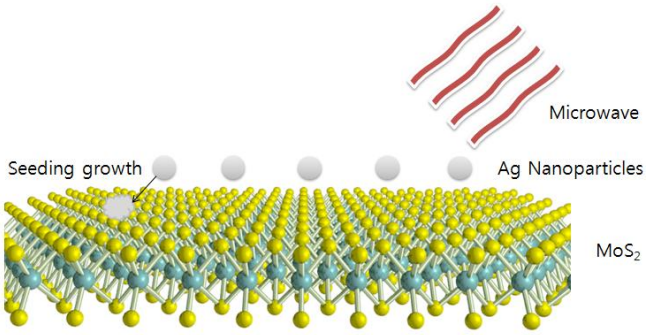


그림 1. Ag nanoparticle on MoS_2 구조

그림 1 은 Ag nanoparticle 을 MoS_2 소자 표면에 microwave 로 처리한 구조를 표현한 그림이다. Ag nanoparticle 은 IPA 를 solvent 로 용해시켜 도포 후 baking 하고 나서 microwave 에 넣었다.

SEM Image 를 통해 MoS_2 위에 Ag Nanoparticle scattering 하여 Microwave 처리한 결과를 확인할 수 있었다. Ag Nanoparticle Size 는 약 50~100 nm 수준의 nanoparticle 을 사용하였다.

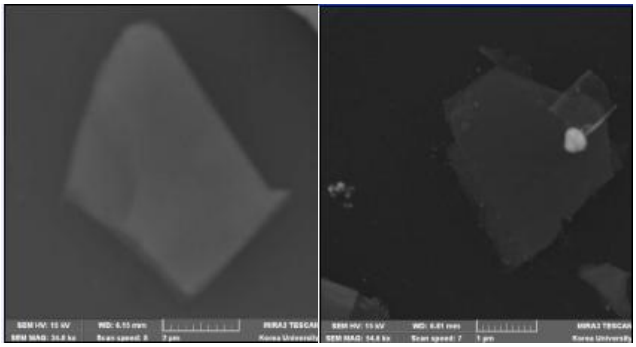


그림 2. (a) MoS_2 SEM Image
(b) Ag nanoparticle on MoS_2 SEM Image

SEM Image 에서 보면 Thin layer MoS_2 위에 Ag nanoparticle 이 growth 되어 있는 것을 알 수 있다. Ag 와 MoS_2 Material 은 Workfuction 이 4.3~4.5 eV 로 큰 차이가 없어 Contact 저항을 최소화 할 수 있다.

Electrical Characteristic

Ag nanoparticle 이 분사되어 있는 MoS_2 를 선정하여 Seeding Growth 전후의 I-V 를 측정하여 소자의 전기적인 특성 변화를 직접 확인해 보았다.

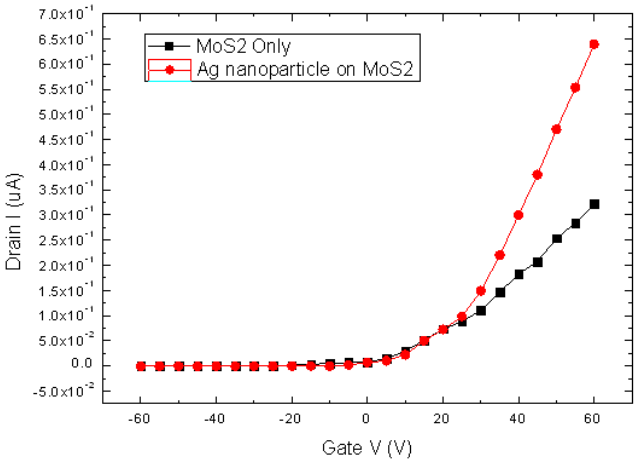


그림 3. Si MOSFET 기판에서 MoS_2 소자의 Ag Nanoparticle 도포 전후 I-V Curve

위 그림은 Drain bias +1.0 V 조건에서 I-V Curve 측정결과 MoS_2 에 Ag nanoparticle 을 Microwave 처리한 case 의 Drain 전류의 peak 값이 커지는 것을 확인 할 수 있었다. 또한 측정된 결과로부터 on-off ratio 의

값은 도 약 2 배정도 커지게 되었다. Transconductance 값 $g_m = \delta I_{ds} / \delta V_{gs}$ Ag Nanoparticle 처리한 시료가 $1.7x10^{-8}$ 로 $7.5x10^{-9}$ 에 비해 2 배정도 크다. Threshold Voltage 또한 -25V 에서 -15V 로 증가한 것을 확인할 수 있었다. Transconductance 값을 기반으로 두 종류 시료의 mobility 를 물질 특성 값을 넣고 비교해보았다.

mobility 수식은 다음과 같다. $\mu = g_m \bullet L / C_{ox} \bullet W \bullet V_{ds}$

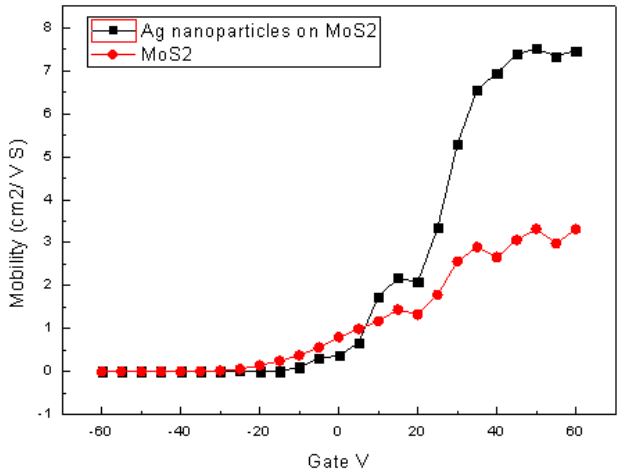


그림 4. Ag nanoparticle 처리 전후의 Mobility 비교

그림을 통해 Mobility 또한 Ag nanoparticle 처리한 시료가 기존시료 대비 다소 높은 값이 나온 것을 알 수 있다.

다음으로는 Flexible PI 기판에서도 비슷한 방식으로 MoS_2 소자에 Ag nanoparticle 을 도포하여 Microwave 로 Seeding growth 시켜 I-V Curve 측정하였다. 다만 PI 기판에서는 back gate voltage 를 인가하지는 못하여 2 단자 측정을 진행하였다.

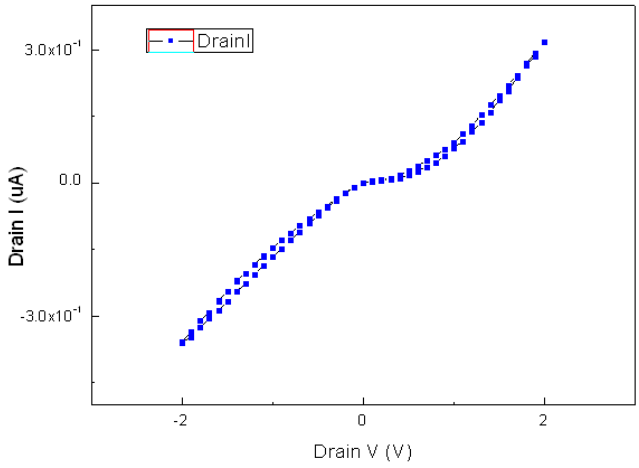


그림 5-1. I-V Curve MoS_2 on Flexible PI Substrate

그림 5-1, 5-2 를 보면 Flexible PI 기판 MoS_2 소자 측정결과 I-V Curve 에서 Ag Nanoparticle Microwave

seeding growth 처리 후에 current level 이 향상된 것을 확인 할 수 있었다. Nanoparticle 처리 후에 일부 전류 level 에 불연속점이 일부 있는 것은 일부 전류가 흐르면서 전자와 Ag nanoparticle 사이에 scattering, trap 현상이 생겼다고 추론해 볼 수 있다.

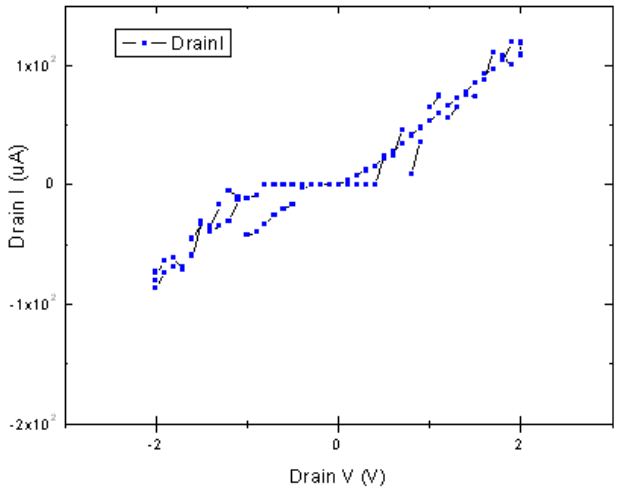


그림 5-2 I-V Curve after microwave seeding growth Ag Nanoparticle on MoS_2 Flexible PI Substrate

• 결론

Ag nanoparticle 입자를 MoS_2 MOSFET 소자에 scattering 하여 microwave 로 growth 한 실험으로 SEM 및 Electrical Characteristic 으로 확인한 결과 일정부분 효과를 보였다. 이러한 특성은 SI 과 Flexible 기판 모두에서 확인 할 수 있었다. 이것은 Workfunction 이 유사한 2D material 인 MoS_2 와 Ag nanoparticle 이 Seeding growth 효과를 일으켜 반응한 것으로 판단 할 수 있다. 본 실험에서 활용한 microwave 를 활용한 기법은 hybrid 소자 제작 및 핸들링이 용이하여 다양하게 응용 가능하며, 물질 고유의 Workfunction 을 고려한 다른 Nanoparticle Application 에도 적용 가능할 것으로 예측할 수 있어 더욱 주목할 만 하다고 할 수 있다.

• 향후 계획

Ag nanoparticle growth on MoS_2 소자의 결합구조를 확인하기 위하여 XPS, XRD, Raman spectroscopy 등을 추가로 진행하여 Morphology 및 결합으로 발생하게 되는 효과를 추가적으로 확인할 것이다.

• 참고문헌

[1] T. S. Sreeprasad," Controlled, Defect-Guided, Metal-Nanoparticle Incorporation onto MoS2 via Chemical and Microwave Routes: Electrical, Thermal, and Structural Properties," Nano Lett., 2013, 13 (9), pp 4434–4441

Publication Date (Web): August 8, 2013.

[2] Makala S. Raghuveer," Microwave-Assisted Single-Step Functionalization and in Situ Derivatization of

Carbon Nanotubes with Gold Nanoparticles " Chem. Mater., 2006, 18 (6), pp 1390–1393 Publication Date (Web): March 02, 2006.
[3] S.M. Aouadi," Tribological investigation of adaptive Mo2N/MoS2/Ag coatings with high sulfur content," Surface and Coatings Technology., Volume 203, Issues 10–11, 25 February 2009, Pages 1304–1309.

Transfer of Graphene Using Au and PMMA and Its Performance

Jinwoo Choi, Jaehyun Park, Hyeji Kim, Won-jun Lee and Jongwan Jung*
Graphene Research Institute, Department of Nanotechnology and Advanced Materials Engineering, Sejong University, Seoul 143-747, Korea
E-mail : jwjung@sejong.ac.kr

그래핀은 이차원 구조의 흑연 덩어리 한층이며, 그 두께는 하나의 원자(0.34 nm) 이다. 그래핀은 화학적, 기계적, 전기적으로 매우 뛰어난 특성을 가지고 있으며, 이때문에 다양한 분야에 적용 하기위해서 많은 연구가 진행되고 있다. 그래핀을 사용하기 위해서는 촉매금속에서 성장시킨 그래핀을 기판으로 옮기는 전사공정이 필요하며, 그리고 이 전사공정에는 PMMA 가 지지층으로 많이 사용된다. 전사공정에서 PMMA 는 그래핀의 찢어짐, 접힘, 표면 오염등을 야기시킨다. 그래서 우리는 PMMA 대신에 금박막을 그래핀의 지지층으로 사용하였다. 지지층으로 사용할 금박막은 thermal evaporator 를 사용하여 촉매금속 위에 성장된 그래핀에 증착하였다. PMMA 와 금으로 동시에 전사공정을 진행하여 비교하였을때 그래핀의 찢어짐, 접힘, 표면 잔여물 등에서 PMMA 보다 금을 사용한 전사공정의 그래핀의 특성이 좋게 측정되었다. 또한 그래핀 소자를 만들때 사진공정에서 쓰이는 PR 도 그래핀의 오염을 야기시키기 때문에 사진공정도 마찬가지로 PR 과 그래핀사이에 금을 증착하고 공정을 진행하였다. 이역시 PR 만 사용한 그래핀보다 금을 사용한 그래핀의 특성이 높게 측정되었다. 고분자 유기물인 PMMA 를 대신해 금을 이용하고, 그래핀과 PR 사이에 금을 증착하여 사진공정을 진행하여 그래핀의 면저항, 그래핀 트랜지스터의 컨택저항과 이동도를 향상시켰다.

[1] Zengguang et. Al. Nano Lett. 11, 767 (2011)
[2] Wei Li et. Al. Applied Physics Letters 102, 183110 (2013)

Controlled growth of Ge/$Si_{1-x}Ge_x$ core/shell nanowires

Byongju Kim, Sun-Wook Kim, Hyunchul Jang, Jeong-Hoon Kim, and Dae-Hong Ko*
Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea
*E-mail : dhko@yonsei.ac.kr

Semiconductor nanowires (NWs) have been proposed to enhance the gate controllability over a channel in transistors. In particular, in Ge/$Si_{1-x}Ge_x$ core/shell structures the Ge core acts as a channel layer where the electrons or holes are transported with high carrier mobility. On the other hand the shell layer of $Si_{1-x}Ge_x$ could be doped with dopant atoms, donating the carriers to the Ge core with a smaller band gap [1]. In this study we fabricated the Ge/$Si_{1-x}Ge_x$ core/shell NWs as a building block for next-generation high speed logic devices. Ge NWs were grown by introducing GeH_4 gas into low pressure chemical vapor deposition chamber via a vapor-liquid-solid mechanism as shown in Fig. 1(a). After removing Au droplets by KI + I_2 solution we deposited the $Si_{1-x}Ge_x$ shells with different compositions as shown in Figs. 1(b) to 1(d). The compositions of the shell layers were controlled by changing a gas flow ratio of SiH_4/GeH_4 and were monitored by grazing incidence x-ray diffraction (GI-XRD). Fig. 1(e) shows GI-XRD results of pure Ge NWs and Ge/$Si_{1-x}Ge_x$ core/shell structures, revealing peaks of (111), (220), and (311) planes. Assuming that the $Si_{1-x}Ge_x$ layers were in fully relaxed state, the compositions of them are calculated from peak positions using Vegard's law. While the $Si_{1-x}Ge_x$ shells with higher Ge concentrations (Figs. 1(b) and 1(c)) revealed rather smooth surfaces, $Si_{0.7}Ge_{0.3}$ shells (Fig. 1(d)) had a rough surface. The origin of the surface roughness will be thermodynamically dicussed at a conference.

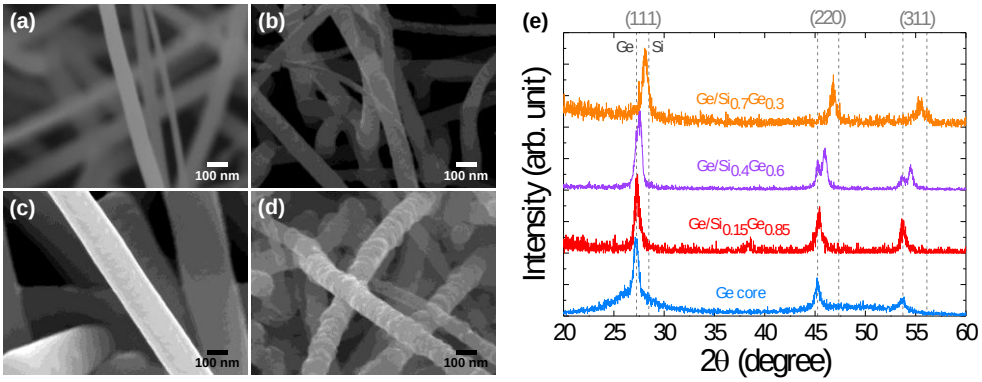


Fig 1. Scanning electron microscopy images of (a) Ge core NWs, (b) Ge/$Si_{0.15}Ge_{0.85}$, (c) Ge/$Si_{0.4}Ge_{0.6}$, and (d) Ge/$Si_{0.7}Ge_{0.3}$ core/shell NWs. (e) GI-XRD data of Ge and core/shell NWs.

[1] Irene A. Goldthorpe, Ann F. Marshall, and Paul C. McIntyre, Nano Lett. **8**, 4081 (2008).

Interfacial charge density measurement for graphene transistor using discharge current analysis (DCA) method

이재은 [1], 정욱진 [2], 이병훈 [2*]

[1]*GIST College,* [2]*School of Materials Science and Engineering*

Gwangju Institute of Science and Technology, 1 Oryong-dong, Buk-gu, Gwangju 500-712, Korea

E-mail : bhl@gist.ac.kr

TEM, STM, Raman spectroscopy 등은 그래핀의 초기 결함 정도를 물리적으로 분석하는 방법으로 주로 이용되고 있다.[1] 하지만, 그래핀 소자 제작 후에는 이 방법들을 적용하기 어렵기 때문에 그래핀 소자의 특성을 전기적으로 분석함으로써 간접적으로 그래핀의 상태를 분석해왔다. 예를 들면, I-V, C-V 특성이 주로 활용되는 데, 이 방법은 그래핀 소자가 주변온도, 분위기, dielectric layer, contact resistance 등 환경에 의한 영향을 포함하고 있어 소자제작과정에서 변형된 그래핀 고유의 특성을 분석하는 데에는 한계가 있다. 따라서, 그래핀 FET 제작 후 관찰되는 그래핀 고유의 특성 변화를 분석할 수 있는 방법이 필요하다.

이 논문에서는 본 연구실에서 개발한 discharge current analysis (DCA) 방법을 Top gate 그래핀 FET 에 적용하여 그래핀과 계면 사이에서 발생하는 charging site 의 밀도를 분석했다.[2] (Fig.1(a)) Fig.1 (b)와 같은 I_d-V_g 특성을 나타내는 소자에 Dirac point 로부터 일정 전압 이상 떨어진 부분에서 측정 주파수를 변경하면서 DCA method 를 적용했다. 또한 Fig.1(c)에 보인 discharge 전류의 주파수 의존성으로부터, 동일한 그래핀에서 공정을 시작했음에도 불구하고, top gate 와 bottom gate 그래핀 FET 에서 관찰되는 discharge 전류 밀도 및 주파수의존 특성이 매우 다른 것을 관찰했다. 이는 그래핀과 접촉하고 있는 계면의 특성에 따른 현상으로 추정되는 데, 이러한 분명한 차이점은 DCA 방법으로 그래핀 소자의 계면 특성을 분석할 수 있음을 입증하는 결과이기도 하다.

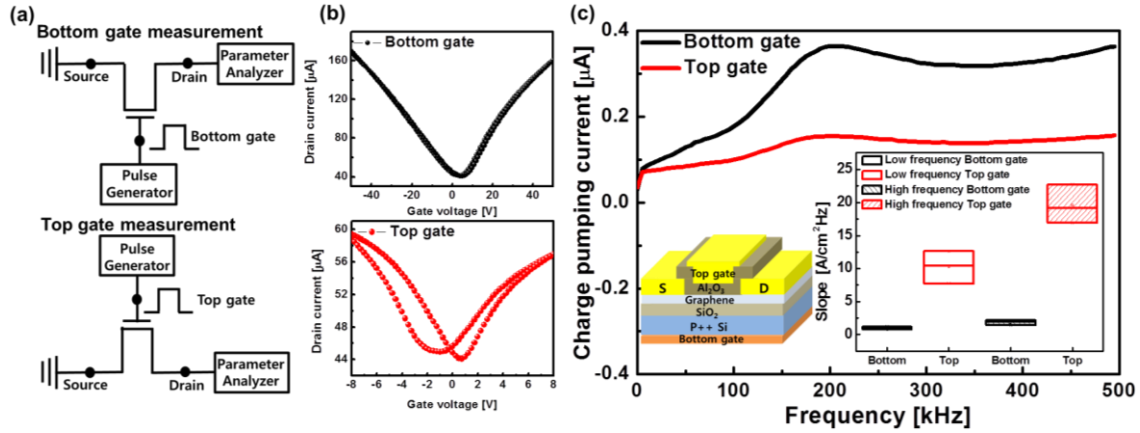


Figure 17 (a)Bottom/Top gate transistor 측정방법 모식도 (b)Bottom/Top gate I_d-V_g 특성 (c)Bottom/Top gate discharging current 특성(Channel L= 2㎛, W=4㎛, Pulse offset= -4V, Pulse amplitude= -5V).

[1] J. C. Meyer et al., Nature, vol. 454, no. 7202, pp. 319–322(2008).

[2] U. Jung et al., submitted for publication (2013).

High-index contrast grating and its applications

Jun Young Kim[1,2], Kyu Hyoek Yoen[1], Jihoon Kyhm[1], Woon Cho Cho[1], Hang Kyu Kang[1], Soo Seok Kang[1], Young Dong Kim[1,2], and Jin Dong Song[1]

[1]*Center for Opto-electronic Convergence, Korea Institute of Science and Technology, Seoul 136-791, Korea*
[2]*Nano-optical Properties Laboratory and Department of Physics, Kyung Hee University,Seoul 130-701, Korea*
E-mail : jdsong72@gmail.com

High-index contrast grating (HCG) is a promising structure for the photonic devices and opto-electronic applications. Especially, HCG has advantages including a high reflectivity over a broad bandwidth and tunable wavelength [1, 2]. In this research, we report the waveguide characteristics of the HCG structure that consists of Si/ITO on GaAs. The waveguide behavior was simulated using rigorous coupled-wave analysis (RCWA) and finite elements method (FEM). Beam steering and focusing are shown in Fig. 1 (a), (b). Transmitted beam from HCG has the steering angle of 8^{o} and the focal length of 15 μm. Also, applications in single photon source (SPS) are shown in Fig. 1 (c). The emission efficiency of SPS with the HCG structure increased comparing only SPS without any structure. We also realized the HCG structure with dry reactive ion etching and e-beam lithography, and performed the optical measurement to demonstrate of the feasibility of the structures.

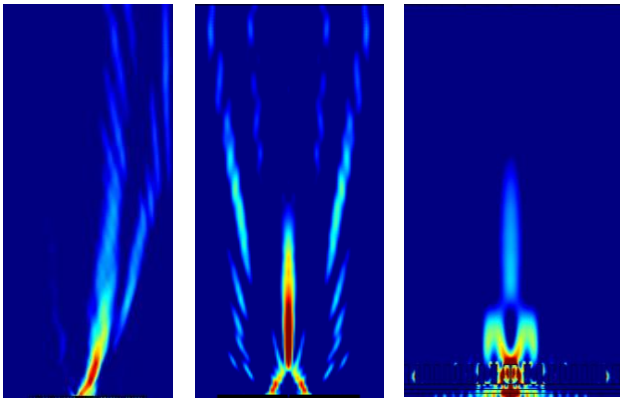


Fig 1. The results of beam steering (a), beam focusing (b), application in SPS (c).

[1] C. F. R. Mateus et al., "Broad-band mirror (1.12-1.62 μm) using a subwavelength grating", IEEE Photon. Tech. Lett. 16, 1676 (2004).
[2] I.-S. Chung, et al., "Broadband MEMS-tunable high-index-contrast subwavelength grating long-wavelength VCSEL", IEEE J. Quant.Electron. 46, 1245 (2010).

Polishing characteristics of supercritical ceria abrasive for STI CMP.

Jihoon Seo,[a] Jinok Moon,[a] Kijung Kim,[b] and Ungyu Paik[a,b,*]

[a]*WCU Department of Energy Engineering, Hanyang University, Seoul 133-791, South Korea*

[b]*Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, South Korea*

E-mail : upaik@hanyang.ac.kr

The shallow trench isolation (STI) process for NAND flash is essential for ultra large scale integration (ULSI) fabrication in chemical mechanical planarization (CMP) for enabling the line width below 250 nm.[1] As pattern sizes of transistors reduced from 50 to 30nm in NAND flash memory, the removal selectivity between SiO_2 and poly-Si in STI CMP process become a critical parameter for CMP performance. Numerous researches have studied ceria for abrasive in CMP due to high removal rate of SiO_2.[2] However, these studies reported in the literature still are difficult to meet the standard as lowering the defect level. Here, we report that ceria synthesized by supercritical technology to improve the characteristics of defect in CMP process. Supercritical synthesis method has an advantage for highly crystalline, an elaborate control of the size and morphology, and a possibility for commercialization. [3] In this study, we synthesized ceria in both acidic and alkaline medium to evaluate the effect of pH on the characteristics of ceria by using supercritical technology. The ceria synthesized in alkaline medium produces higher concentration of Ce^{3+} ions on the surface than the ones synthesized in acidic medium, which lead to 1.4 times higher removal rate of SiO_2 film and higher removal selectivity between SiO_2 and Poly-Si due to high concentration of Ce^{3+} ions on the surface than the ones synthesized in acidic medium.

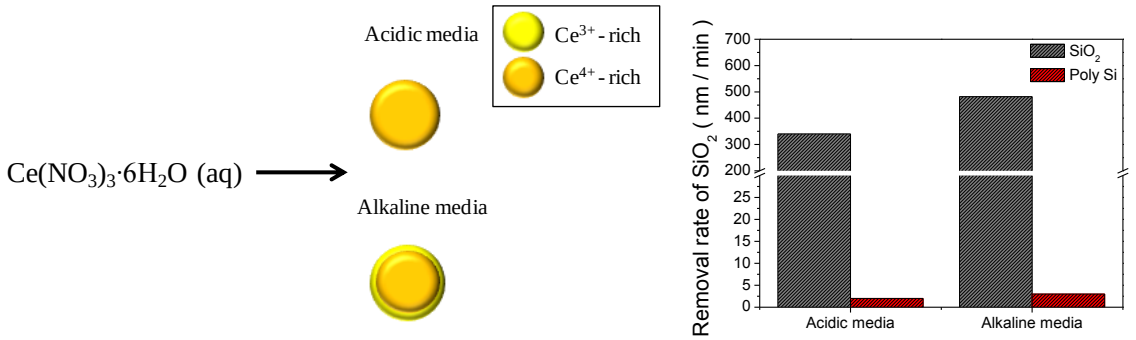


Fig 1. Ceria nanoparticle synthesized in acidic and alkaline medium and its CMP data

[1] T. Katoh, H. G. Kang, U. Paik, and J. G. Park, Jpn. J. Appl. Phys. 142, 1150 (2003)

[2]J. Kim, W. Myeong, and S. Ihm, Appl. Catal., B. 71, 57-63 (2007)

[3] L. M. Cook, J. Non-Cryst. Solids 120, 152 (1990)

Printed Indium-Tin-Oxide Films for Various Sensor Applications

Jieun Koo[1], Youngji Cho[1], Sangtae Lee[2], Jung-Yeul Jung[3] and Jiho Chang[1*]

[1]*Department of Applied Science, Korea Maritime and Ocean University Busan, Republic of Korea*
[2]*Department of Mechatronics Engineering, Korea Maritime and Ocean University, Busan, Republic of Korea*
[3]*Ocean Science and Technology School, Korea Maritime and Ocean University, Busan, Republic of Korea*
* E-mail : jiho_chang@kmou.ac.kr

Printed electronic devices using various materials such as metal, metal oxide, polymer and organics have been actively researched. [1, 2] Among them, printed metal oxide sensors have a lot of advantages such as simplicity, inexpensiveness, easy fabrication and scale-up possibility. In particular, indium-tin-oxide (ITO) has been regarded as a potential candidate, because it has various advantages such as high conductivity, optical properties (wide band gap ~ 4 eV), and chemical stability.

In this work, we demonstrated an ultraviolet (UV) sensor, gas sensor, and oil sensors by printing ITO nanocrystals (NCs) on glass substrates. We have fabricated a coil-shaped ITO sensor by screen printing method. Printed ITO sensors revealed relatively low resistivity 1.56 Ω·cm after annealing under proper conditions. And the high performance of gas sensing, UV sensing, and oils sensing properties were obtained as shown in Fig.1. In summary, we proposed the high performance of sensor devices based on printed ITO NCs, and confirmed its feasibility. (Grant No; NIPA-2012- H0401-12-1007)

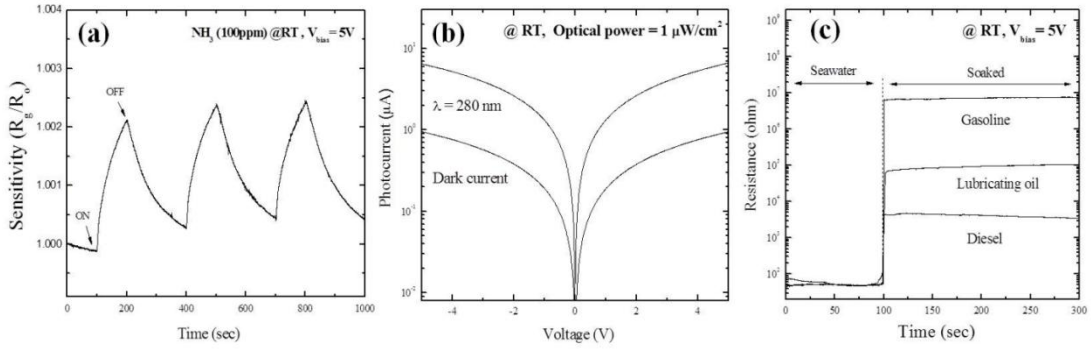


Fig.1 (a) Methane gas sensing response, (b) I-V characteristics of UV sensing, and (c) oils sensing response of ITO NCs sensors in saltwater (NaCl 3.4%) at room temperature.

[1] M.G. Kim, M. G. Kanatzidis, A. Facchetti and T. J. Marks, Nature Mater. **10**, 382 (2011).
[2] S. Capone, M. Zuppa, D. S. Presicce, L. Francioso, F. Casino, P. Siciliano Sen. Actuators B 131, 125 (2008).

Effect of Surface Morphology on Nano Embossing ceria for CMP performance

Young-Hye Son, Hyun-Min Seung and Jea-Gun Park*

Department of Electronics Computer Engineering,
Hanyang University, Seoul 133-791, Republic of Korea
E-mail : Parkjgl@hanyang.ac.kr

Wet ceria has been using widely for CMP process of NAND flash fabrication. As the design rule of semiconductor device scale down below 20nm, generating a scratch caused by wet ceria slurry has been critical issue in CMP process. In particular, conventional wet ceria slurry is facing on the limitation in reducing a scratch generation resulting from its polyhedral shape and sharp edge. We studied how surface morphology of nano ceria effects scratch generation. By considering that the conventional wet ceria abrasive has cubic crystal structure, polyhedral shape and sharp edge. We synthesized a nano embossing ceria abrasive which was synthesized by continuous chemical precipitation method to suppress scratch formation. It was demonstrated that the nano embossing ceria abrasive, secondary growth of small spherical ceria particle on the primary polyhedral ceria seed particle, reduced scratches and the probability of scratch generation without deteriorating crystallinity. In particular, the nano embossing ceria abrasive showed a reasonable removal rate of SiO_2 film and reduced scratch generation on poly-Si film. In the presentation, we report the effect of surface morphology on nano embossing ceria for CMP performance, how to reduce scratch generation by our novel wet ceria slurry.

* This investigation was financially supported by UB materials Inc. and the Brain Korea 21 Plus Project in 2013, Republic of Korea. We also thank Sumco Corp. for helping us with the experiments.

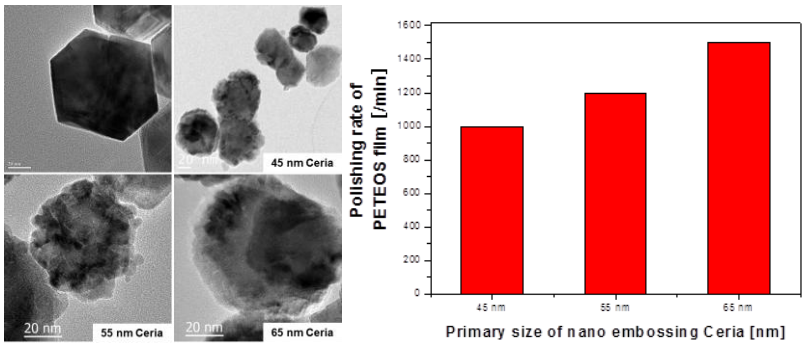


Fig 1. TEM image of nano ceria and nano embossing ceria with various primary sizes and its polishing rate of SiO_2 film.

[1] J. Y. Bae, J. H. Seo, K. W. Park, J. O. Moon, H. B. Park, U. Park, ICPT, #2503, (2012).

Nucleation-controlled growth of monolayer MoS_2 by vapor phase transport

SooHo Choi, and Woochul Yang
Department of Physics, Dongguk University, Seoul 100-715, Korea
E-mail : wyang@dongguk.edu

Layered transition metal dichalcogenide (TMD) materials have attracted significant research interests owing to their exceptional thermal, mechanical, electronic and optical properties. Among them, mono-layer molybdenum disulphide (MoS_2) with a direct energy bandgap is a promising two-dimensional material which can overcome the disadvantage of bandgap free graphene for the next generation nanodevice applications. However, growth of atomic layer MoS_2 with large area and high quality remains a challenge. Here we report vapor phase transport growth of MoS_2 atomic layers. In particular, an initial stage of the atomic layer formation was explored by controlling growth temperatures and rates. MoS_2 powder source and Ar carrier gas was used to grow the atomic layers on SiO_2 substrates and the growth temperatures were 600-700^oC. The shape and dimension of the grown layers were examined by atomic force microscopy. Also, the structural and electronic properties of the layers were investigated by Raman spectroscopy and Kelvin probe force microscopy. Growth processes of nucleation, lateral growth, and grain boundary formation in the monolayer MoS_2 are discussed in terms of kinetics and energetics of surface adatoms in the growth processes. On the basis of our results, we suggest a nucleation- controlled growth mechanism for the high quality and scalable synthesis of atomic layer MoS_2.

High performance Transparent Flexible and Robust Graphene & h-BN stacked Micro-Heater

Tae-ho Kim[1,] Kang Hyuck Lee[1)], and Sang-Woo Kim[1)]

[1)] School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 440-746, Korea

E-mail : kimsw1@skku.edu

There are considerable interests in decreasing the power consumption of available semiconductor metal oxide gas sensors and thermal actuating applications. The low voltage and low power consumption metal oxide gas sensors can be easily produced by combining micro-machining and thin-film technologies. The concept of micro-heater is one of the possible solutions. Many types of micro-heater materials have been investigated to realise micro-heaters for gas sensing and thermal actuating applications; however, the device integration with such materials is quite difficult and time consuming. Herein, we report the fabrication of hetero-stacked device by using 2D materials for simple micro-fabricating applications. We have recently investigated transparent felxible and robust micro-heater based on on CVD-grown graphene and h-BN stacked structure on PEN film. Both measured output power consumption and detected temperature distribution by infrared camera were consistent with FEM simulation results. The maximum temperature achieved by the micro-heater is around 220 ℃ indicating the better performance which can replace traditional low-temperature micro-hot-plates.

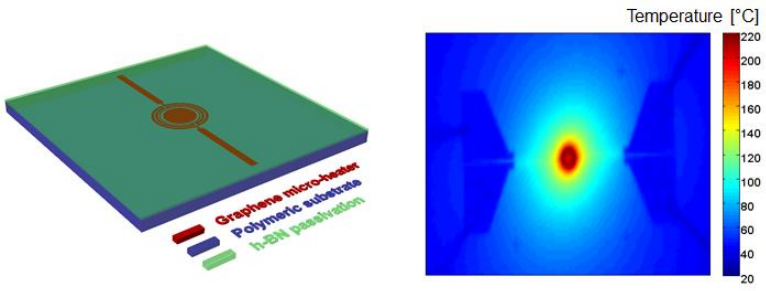


Fig 1. The structure of a micro-heater and its temperature distribution detected by IR camera

[1] S. Semancik and D.L. DeVoeActuators B, 77, 579-591 (2001).

[2] Junmo Kang and Byung Hee Hong, Nano Lett., 11, 5154-5158 (2011)

Correlation between structural and electronic properties of grapheme depending on substrate roughness

Min Baik, DeukGong Yoon, PooReum Choi, SooHo Choi, Shaolin Zhang, and Woochul Yang*

Department of Physics, Dongguk University, Seoul 100-715, Korea

* Corresponding author: wyang@dongguk.edu

Graphene has raised extensive interest in a wide scientific community for its exceptional properties, such as ambipolar electric field effect, high mobility of charge carriers, anomalous quantum Hall effect, and massless relativistic carries, making itself appropriate for various potential applications, such as supercapacitors, transparent conducting electrodes, and single molecule gas sensor. As a hexagonal two dimensional network of carbon atoms, it is known that every carbon atom in graphene is a surface atom. Thus, substrate-induced structural distortion, adsorbates, local charge disorder, atomic structure at the edges, and even atomic scale defects play a great role in electronic properties of graphene. Specifically, the surface roughness of substrate is critically important for thin and flexible graphene. The morphology of graphene is partly determined by the supported substrate, which means the surface roughness of substrate can lead to structure distortion of graphene and vary its properties. Moreover, the rough surface of the substrate also induces the strain between the graphene and substrate, leading to a great variation on the properties.

In this study, we report the electronic properties of mono-layer graphene depending on the roughness of SiO_2 substrate. The roughness of SiO_2 substrate was controlled by spin-coated SiO_2 nanoparticles. The roughness of spin-coated SiO_2 substrate was measured by Scanning Probe Microscopy (SPM). Then CVD grown graphene sheets were transferred on the substrates with different roughness. The electronic properties, such as work-function and conductivity were measured by Scanning Kelvin Probe Force Microscopy (SKPM) and Conductivity Atomic Force Microscopy (C-AFM).

기계식 박리법으로 분리된 Multilayer MoS 2의 물리적 및 광학적 특성

추동일, 이동욱, 김은규* 한양대학교 물리학과,133-791 E-mail: ek-kim@hanyang.ac.kr

그래핀은 높은 캐리어 이동도를 갖는 2차원 물질로서 밴드갭이 없는 단점으로 전기장 효과 트랜지스터에 대한 응용이 제한되었다. 최근에는 그래핀 대신 물리적 특성이 우수한 TMD (transition metal dichalcogenide)족 반도체인 Molybdeum disulphide (MoS 2)가 나노전자소자 및 광학적 응용에 훌륭한 전망이 보여 많은 주목을 받고 있다. MoS_2의 S-Mo-S층간 약한 van der Waals interaction으로 인해 기계식 박리법으로 쉽게 단층 또는 다층의 2차원 물질을 제작할 수 있다.[1] 스카치 테잎을 이용한 박리법 뿐만 아니라 chemical vapour deposition, liquid phase exfoliation 등의 방법으로도 MoS_2의 monolayer을 제작할 수 있다.[2] 그래핀과 마찬가지로 2차원 물질은 특정한 두께의 실리콘 산화막 위에 놓여 있을 때 광학현미경을 통해서도 쉽게 관찰할 수 있다.[3] 본 연구에서는 두께가 270nm인 실리콘 산화막 기판위에 기계적 박리법으로 분리된 MOS_2를 광학현미경을 통해 관찰하였다(그림 1(a)). 여기서 형성된 MoS_2 조각에 대한 표면형상을 AFM(atomic force microscopy)으로 측정하였으며(그림1(b)), 또한, 그림1(c)와 같이 각 부분에 대한 층상구조를 파장 532nm의 레이저를 이용하여 Raman spectroscopy 분석을 하였다. 본 연구에서는 단층 또는 다층의 결정구조를 얻기 위한 최적 조건과 물리적 광학적 특성에 대해 논의할 것이다.

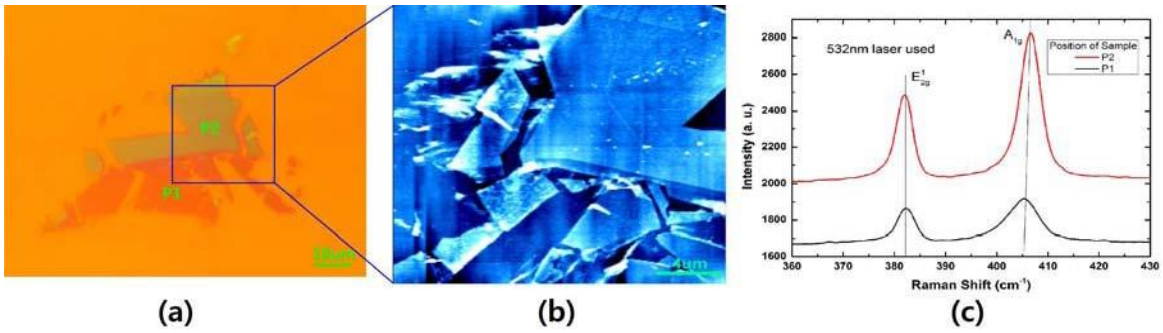


그림 1 (a) 광학현미경으로 본 270nm SiO_2위의 다층 MoS_2의 사진, (b) AFM 이미지 및 (c) 위치에 따른 다층 MoS 2의 Raman 스펙트럼.

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[2] B. Radisavljevic and A. Kis, Nature Materials 12 (2013) 815.

[3] M.M. Benameur, B. Radisavljevic, J.S. Heron, S. Sahoo, H. Berger, and A. Kis, Nanotechnology 22 (2011) 125706.

Improvement in photoluminescence of thin-film phosphor

using double-side patterning

Chul-Kyun Park[1], Ki-Kang Kim [1], Ki-Young Ko[2], and Jinho Ahn[1*]
[1]*Department of Materials Science and Engineering, Hanyang University, Seoul 133-791, Korea*
[2]*Korea Institute of Patent Information, Seoul 121-816, Korea*
E-mail : jhahn@hanyang.ac.kr

Over the past few decades, the excellent luminescence of Eu-doped yttrium oxide (Y_2O_3:Eu^{3+}) powder phosphors has lead to their widespread use as red components in plasma display panel and fluorescent light [1]. Two-dimensional (2D) photonic crystal layers (PCLs) have been applied to various light emitting devices incorporating luminescent film materials in an attempt to enhance their extraction efficiency [2]. This method can enhance the extraction efficiency, which is limited to approximately 7.0% in Y_2O_3:Eu^{3+} thin film phosphors (THFs) by the total internal reflection (TIR). In this study, we examined the structural effects of 2D ZrO_2 nanoparticle PCLs on the photoluminescence properties of annealed Y_2O_3:Eu^{3+} THFs fabricated by sol-gel method [3]. The 2D hexagonal-type hole patterns of ZrO_2 nanoparticle PCLs were generated on the Y_2O_3:Eu^{3+} TFPs or quartz substrates by reverse nano-imprint lithography. This simple process results in a double-side 2D ZrO_2 nanoparticle PCLs, where the extraction efficiency was improved by 6.68 times compared to the conventional Y_2O_3:Eu^{3+} TFPs.

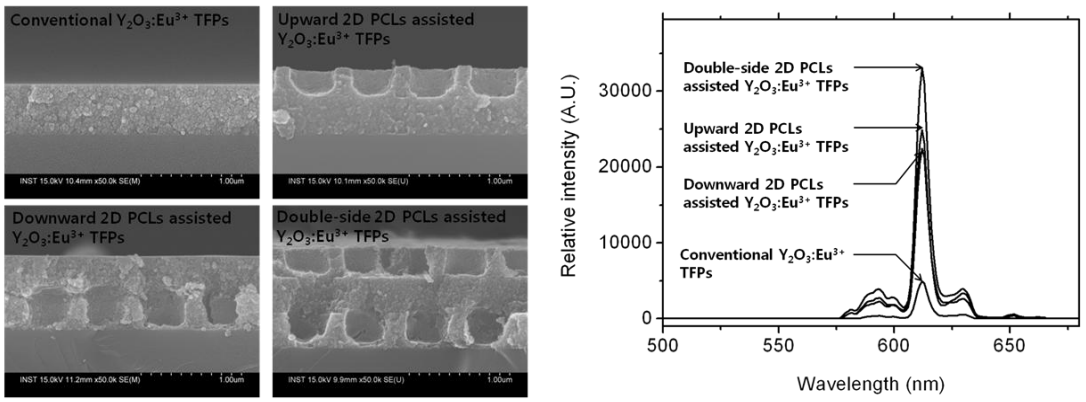

Fig 1. SEM images of Y_2O_3:Eu^{3+} TFPs (conventional, downward 2D PCLs assisted, upward 2D PCLs assisted and double-side 2D PCLs assisted TFPs) and its photoluminescence spectra

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Influence of Gate Dielectrics on Electrical Characteristics of Solution-Processed ZnO Transistors

Xue Zhang[1], Jaehoon Park[1], Hyunji Shin[2], Dong Wook Kim[2], Jong Sun Choi[2], Jae Eun Hwang[3], and Hong Doo Kim[3]

[1]*Department of Electronic Engineering, Hallym University, Chuncheon 200-702, Korea*

[2]*Department of Electrical, Information and Control Engineering, Hongik University, Seoul 121-791, Korea*

[3]*Deparment of Display Materials Engineering, Kyunghee University, Gyeonggi-do 446-701, Korea*

E-mail : jaypark@hallym.ac.kr

In recent years, there has been a great deal of interest in zinc oxide (ZnO) semiconductor materials, as seen from a surge of a relevant number of publications [1]. We investigated the electrical characteristics of solution-processed ZnO transistors fabricated with two types of gate dielectrics; silicon dioxide (SiO_2) and silicon nitride (SiN_x). We compared the threshold voltage and threshold voltage shift in each device according to gate dielectrics. The transistor having the SiNx gate dielectric exhibited lower threshold voltages compared to those for the SiO_2 case, which can be explained by relatively higher dielectric constant of the SiNx film. In particular, it was found that the dielectric surface treatment using O_2 plasma contributed to more stable operation for both types of devices such as less shift in the threshold voltage upon reversal sweep of the gate voltage. These are intimately compared in Figure 1. We will explain the results with respect to interfacial characteristics between the ZnO film and gate dielectric layer. This study will be helpful to understand the significant role of gate dielectric and interface properties in solution-processed oxide transistors.

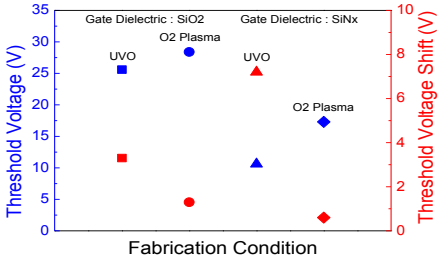

Fig 1. Comparison of extracted threshold voltages and threshold voltage shifts in the fabricated ZnO transistors.

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Purge-time-induced changes in preferred orientation of zinc oxide thin films grown by atomic layer deposition

Hui Kyung Park and Jaeyeong Heo
Department of Materials Science and Engineering, Chonnam National University, Gwangju 500-757, Korea
E-mail : jheo@jnu.ac.kr

Transparent conducting oxides (TCOs) have been actively researched with the increasing demand on various applications, including photovoltaic devices and flat panel displays, and zinc oxide (ZnO) is one of the representative TCO materials [1]. For forming extremely conformal and ultrathin films in various nanostructured devices, atomic layer deposition (ALD) has been highlighted as an ideal method [2]. There has been numerous reports on the formation of ZnO thin films by ALD. However, less attention has been paid on the effect of extremely long purge time for both Zn precursor and oxidant (H_2O) on the grown films' overall properties. In this study, we varied diethylzinc and water purge time from 20 to 120s, which in general is regarded as excessively long purge time in ZnO ALD. The preferred orientation changed from (002) to (101) and (100) as H_2O purge time increased from 20 to 120s [3]. Related growth behaviors, electrical, optical, and structural properties will be presented in detail. This work will provide insights on the growth of ZnO especially on nanostructures, which requires extremely long purge time to acheive ideal ZnO ALD growth.

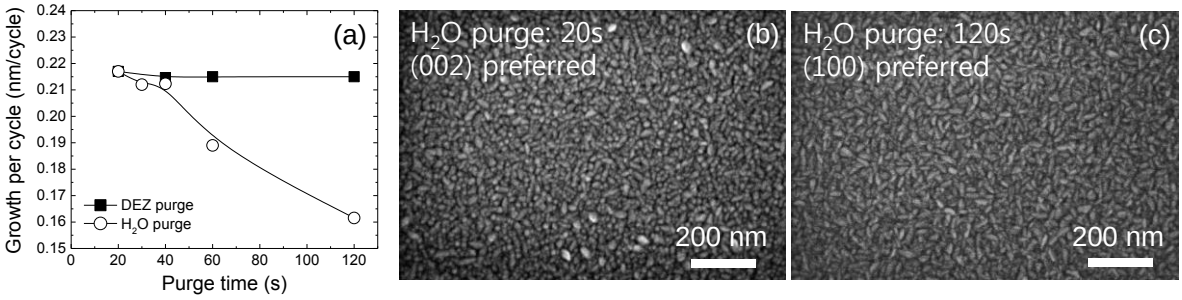

Fig 1. (a) Growth rate *vs*. purge time, (b-c) surface morphologies observed by SEM for 20 and 120s H_2O purge.

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Flexible micro-scale organic field effect transistors fabricated achieved via orthogonal photolithography

Jingon Jang[1], Younggul Song[1], Hyuntaek Oh[2], Daekyoung Yoo[1], Jin-Kyun Lee[2], and Takhee Lee[1,*]
[1]Department of Physics and Astronomy, Seoul National University, Seoul 151-747, Korea
[2]Department of Polymer Science and Engineering, Inha University, Incheon 402-751, Korea
*E-mail : tlee@snu.ac.kr

Organic electronic devices have been intensively researched in recent years due to their outstanding advantages such as simple device structure, low cost, ease of fabrication, flexibility, printability, limitless material variety, and a wide span of potential applications [1]. But it is still difficult to apply a standard photolithographic technology to organic electronic devices because organic solvent required for the lithographic process generally damages underlying organic layers. By applying highly fluorinated solvents and its comparable photoresists which exhibit the orthogonal properties with organic materials to the photolithographic fabrication process, it became possible to make the micro-scale patterning for organic devices without damaging the underlying polymer layers [2]. In this method, we successfully fabricated 3 μm-channel pentacene organic field effect transistor (OFET) devices on flexible PET substrate. The fabricated OFET devices showed stable electrical characteristics in flat and bending conditions and also exhibited excellent reliability even after repeated bending cycles (up to 10^3 times).

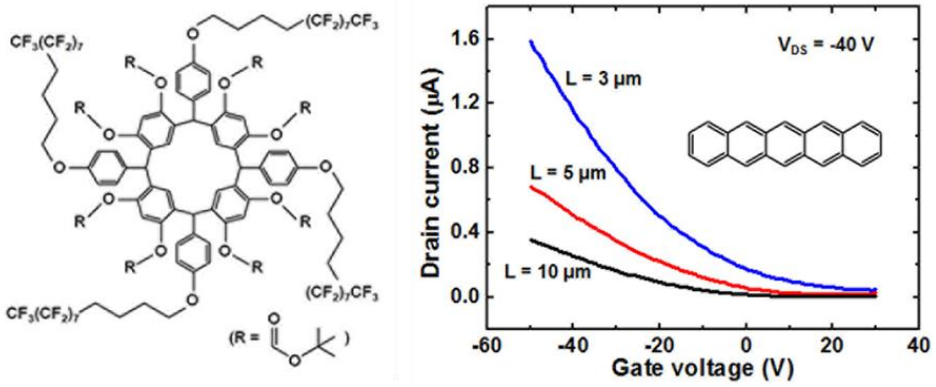

Fig 1. (Left) Semi-perfluoroalkyl resorcinarene photoresist. (Right) Transfer curves of 3 μm-channel length pentacene OFET.

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Gate Dielectric Effects on Electrical Characteristics of 6,13-Bis(triisopropylsilylethynyl)-Pentacene Transistors

Hyunji Shin[1], Dongwook Kim[1], Jaehoon Park[2], and Jong sun Choi[1]

[1] *Department of Electrical, Information and Control Engineering, Hongik University, Seoul 121-791, Korea*

[2] *Department of Electronic Engineering, Hallym University, Chuncheon 200-702, Korea*

E-mail: jschoi@wow.hongik.ac.kr

Recently, organic thin film transistors (TFTs) are under the spotlight due to their potential in low-cost production and high mechanical flexibility [1~2]. In this study, we examined the electrical reliability of 6,13-bis(triisopropyl-silylethynyl)pentacene (TIPS-pentacene) according to gate dielectric materials, i.e. aluminium oxide (Al_2O_3) and cross-linked poly(vinylphenol) (cPVP). Compared to the electrical characteristics of the OTFT with the Al_2O_3 dielectric, the device with the cPVP dielectric exhibited lower threshold voltage and less shift in the threshold voltage upon reversal sweep of gate voltage, as shown in Fig. 1. This implies the significance of interfacial properties between the TIPS-pentacene layer and gate dielectric film. It is considered that the cPVP dielectric produced more reliable interface in TIPS-pentacene TFTs in comparison to the Al_2O_3 case owing to lower surface energy and smoother morphology of the cPVP film. Further analyses of gate-bias stability of the TFTs and surface properties of the dielectric films will be discussed.

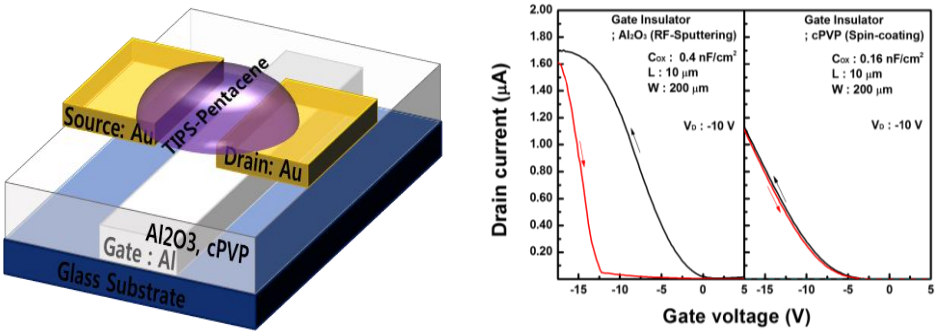

Fig 1. (Left) Schematic of the fabricated TIPS-pentacene TFT. (Right) measured transfer characteristics.

[1] B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, A. LaDuca, R. Sarpeshkar, H. E. Katz, and W. Li, Nature 403, 521 (2000).

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Deposition of thicker ferroelectric (Hf,Zr)O_2 thin films using Al_2O_3 inter-layer

Han Joon Kim, Min Hyuk Park, Yu Jin Kim, Taehwan Moon and Cheol Seong Hwang
WCU Hybrid Materials Program, Department of Material Science & Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea
E-mail : june110@snu.ac.kr

최근 Zr, Si, Y, Al 등의 Dopant 를 활용한 Hf O_2 기반의 강유전체에 대한 연구가 진행되었다. 이는 기존의 perovskite 기반의 고전적인 강유전체에 비해 매우 얇은 두께(~10nm)를 갖기 때문에, 3-D fabrication 등에 적용할 수 있는 많은 이점들이 있다. 이렇게 HfO_2 박막이 강유전성을 나타내는 이유로는 $Pbc2_1$ 이라는 non-centrosymmetric orthorhombic phase 가 나타나기 때문이라고 알려져 있다. [1] 한편, HfO_2 을 piezoresponse force microscope 등으로 domain dynamics 를 측정하면 강유전성의 기원을 이해하는 데 있어 도움이 될 텐데, HfO_2 의 두께가 너무 얇기 때문에 이를 측정하기에는 큰 어려움이 있는 것이 현실이다. 기존 연구에서는 (Hf,Zr)O_2 (HZO)의 두께를 20nm 이상 키우게 되면, 급격하게 강유전성이 사라지는 현상을 발견되었다. 이는 grain size 가 커짐에 따라, monoclinic phase 가 많아지면서 강유전성이 열화되기 때문이다. [2] 따라서 grain size 를 임계 크기 이하로 유지시켜 강유전성을 유지한 채 박막을 성장시킬 방법이 필요하다. 본 연구에서는 DRAM capacitor 에서 주로 사용되고 있는 ZAZ ($ZrO_2/Al_2O_3/ZrO_2$) stack system 을 모방하여 ALD 방법을 이용 하여 전체 20nm 의 두께를 갖는 HZO layer 에 각각 아래, 중간, 위 등 여러 위치에 1nm 두께의 Al_2O_3 layer 를 삽입시켜 보았다. ZAZ 에서는 Al_2O_3 가 중간에 위치하였을 때, ZrO_2 grain 의 연속성장을 방해하기 때문에 grain size 를 조절하는 역할을 할 수 있다고 알려져 있다. [3] 이렇게 제작된 HZAHZ ((Hf,Zr)O_2/Al_2O_3/(Hf,Zr)O_2) 박막은 가장 우수한 잔류 분극 값을 나타내었고 유전 상수 역시 크게 관찰되었다. X-ray diffraction 을 통해 monoclinic phase 가 잘 억제된 것을 확인할 수 있었고, scanning electron microscope 를 통해 grain 의 성장 역시 잘 억제된 것을 확인할 수 있었다. 이를 통해 Al_2O_3 layer 가 두꺼운 HZO 에서도 강유전성을 유지시킬 수 있는데 중요한 역할을 할 수 있다고 생각된다. 하지만 심각한 fatigue 현상을 확인할 수 있었는데, 이는 박막을 증착 할 때 필연적으로 HZO 와 Al_2O_3 계면 사이에 많은 charged trap 이 생성 및 분포하게 되어 이러한 현상이 나타나게 되는 것으로 생각된다.

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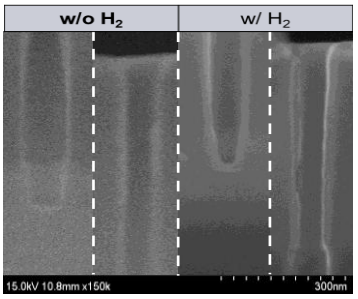
Improving conformality of $SrRuO_3$ film grown by combined ALD SrO and CVD RuO_2 or Ru layers

Cheol Hyun An, Woojin Jeon, Woongkyu Lee, Yeon Woo Yoo, and Cheol Seong Hwang
Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-747, Korea
E-mail : ach510@snu.ac.kr

반도체 소자의 집적화가 이루어지면서, DRAM 커패시터의 소형화를 가능케 하는 재료들에 대한 연구들이 진행되고 있다. 그 중 페로브스카이트 계열 물질인 $SrTiO_3$와 $SrRuO_3$(SRO)는 각각 높은 유전율(k~150) 값을 가지는 유전막과 그에 상응하는 결정 구조를 가지는전극 물질로 각광받고 있다. SRO 는 높은 일함수(~5.1eV)를 가지므로 커패시터의 누설전류를 줄일 수 있고, 무엇보다 $SrTiO_3$ 와의 결정격자 차이가 작아 유전막의 in-situ 결정화에 적용할 수 있어 후열처리 없이도 높은 유전율을 얻을 수 있다[1]. DRAM design-rule 감소에 따라 DRAM 커패시터의 aspect ratio 역시 급격히 증가하게 되는데, SRO 를 DRAM 커패시터의 전극막으로 사용하기 위해서는 이러한 구조 변화에 대응할 수 있는 우수한 step coverage 를 갖는 SRO 박막 증착 공정 확보가 필수적이다.

SRO 박막을 증착하기 위해 SrO 막과 RuO_2 막을 각각 ALD 공정과 pulsed CVD 공정을 이용하는 공정에 대해서는 이미 보고되어 있다.[1] 하지만 RuO_2 막 위에 SrO 를 증착할 경우 하부 RuO_2의 산소와 Sr 전구체가 반응하게 되어, SrO 막의 증착 단계에서 이상적인 ALD 성장거동에서 벗어난 과잉성장 거동을 보인다.[2] 이는 SRO 박막 증착 공정의 step coverage 를 저하시키는 가장 큰 요인이다. 따라서 본 연구에서는, 기존 SRO 증착 공정에 수소 기체 주입 단계를 추가함으로써 SrO 막의 과잉성장을 억제하고자 하였다.

수소 주입 공정으로 증착한 박막을 분석한 결과 기존 공정에서의 SrO 막의 과잉성장이 억제됨을 알 수 있었다. 또한 전기적 특성이나 결정성, 표면 morphology 등이 기존 공정의 박막과 비교하였을 때 열화되지 않음을 확인하였다. 따라서, 수소를 주입한 SRO 박막 증착 공정은 SrO 막의 과잉성장을 효과적으로 제어하면서 step coverage 를 향상시킬 수 있다.



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Microwave-Annealing effects of Solution-processed HfOx Thin Film as a Resistive Switching for ReRAM

Ki-Hyun Jang, Se-Man Oh, Se-Ho Kim and Won-Ju Cho
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail : jayz1226@nate.com

The solution-processed ReRAM, which has attracted considerable interest owing to its simplicity, minimum plasma-damage of large-area device applications, and cost effectiveness, has been reported in some high-k materials such as the TiOx, ZrOx or ZnO. The solution processed film commonly is treated conventional thermal annealing (CTA) in a furnace to control the defects, i.e. oxygen vacancies and organic impurities from organic precursors. However, the CTA is limited by a low efficiency of heating and a high thermal budget and annealing temperature is strictly restricted in case of a glass or flexible substrates. Recently, the MWA has been reported to solve this problem. It can transfer the energy directly to the target materials by absorption of microwave energy throughout the volume of the material [1]. Moreover, it has many advantages such as thermal uniformity, short processing time and selective heating of materials.

In this work, we demonstrated solution-processed HfO_x based ReRAM with MWA below 60 ˚C. The device has low voltage operation and set operation through the forming free. Also, it has similar resistance ratio at read 0.2 V compared to device with CTA. For these results, MWA could be a milestone in low temperature process.

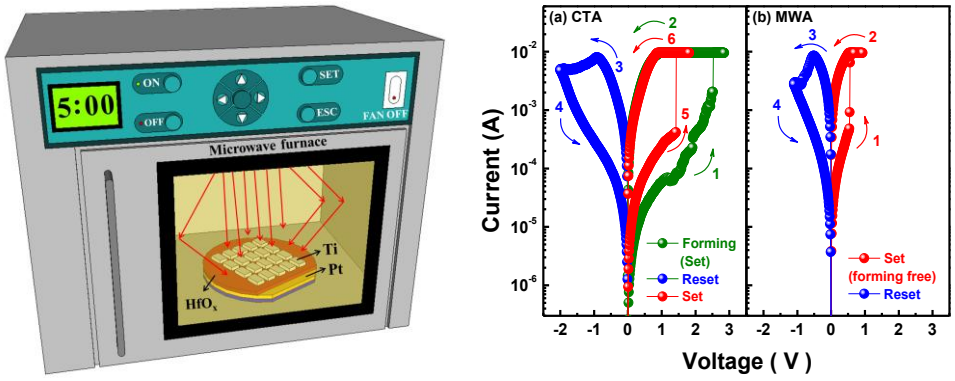

Fig. 1. Schematic diagram of the solution-processed HfO_x thin film based ReRAM device with MWA and I-V curves for set and reset operations.

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Acknowledgment

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Surface Reaction Chemistry during Atomic Layer Deposition of Sc_2O_3 and Gd_2O_3 from Cp-based Metal Precursors

Jeong Hwan Han[a,b]

[a]Present address: *Advanced Materials Division, Korea Research Institute of Chemical Technology, 141 Gajeong-Ro, Yuseong-Gu, Daejeon 305-600, Korea*

[b]*Imec, B-3001 Leuven, Belgium*

E-mail : jhan@krict.re.kr

Sc_2O_3, Gd_2O_3, and $GdScO_3$ thin films have recently attracted strong interest for applications in microelectronic devices (e.g., as gate dielectrics for metal-oxide-semiconductor field-effect transistors or as tunneling or blocking dielectrics in non-volatile flash memory cells) because they possess relatively high dielectric constants, wide band gaps, and excellent thermal stability. Despite a number of experimental[1] and theoretical[2] reports on the ALD of REOs from Cp-based metal precursors and oxidant (H_2O or O_3), there have been so far no in situ studies of the surface reactions during the ALD process. In this presentation, we studied the surface reactions during the steady-state ALD of Sc_2O_3 and Gd_2O_3 by time-resolved *in situ* QMS analysis. Furthermore, we address the transient growth behavior of Gd_2O_3 on Sc_2O_3 and vice versa to understand the effect of the nature of underlying surface on the ALD growth mechanism of ternary $Gd_xSc_{1-x}O_3$. The surface chemistry is then linked to the process behavior as well as the film properties.

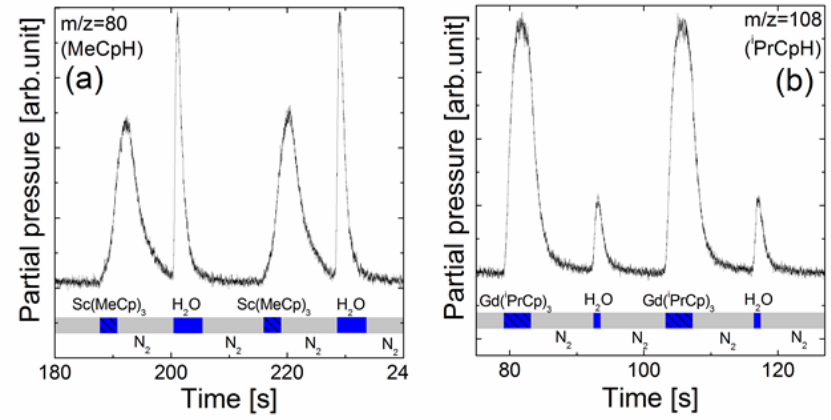

Fig 1 (a). The variation of the partial pressure of MeCpH during 2 $Sc(MeCp)_3/H_2O$ cycles at 300°C. (b) The variation of the partial pressure of ^{i}PrCpH during 2 $Gd(^{i}PrCp)_3/H_2O$ cycles at 300°C.

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Characterization of charge trapping and current conduction mechanism in Hf-aluminate for 3D-stacked NAND flash memory

Jinho Oh, Heedo Na, and Hyunchul Sohn
Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : hyunchul.sohn@yonsei.ac.kr

In order to enhance the performance of charge trapping type 3D-stacked NAND flash memory, the introduction of high-k oxide in blocking oxide has been considered as a promisng strategy.[1] However, high-k materials typically have more defects compared to SiO_2. These defects lead to charge trapping and leakage current and degrade the retention characteristics.[2] In this study, the effect of annealing condition on the dielectric properties of Hf-aluminate with various annealing temperature was investigated in terms of fixed oxide charge, leakge current and conduction mechanism. A 17 nm thick Hf-aluminate film was grown by atomic layer deposition on a p-type Si substrate. The deposited Hf-aluminate film was annealed in O_2 ambient at various temperatures from 750 ^oC to 950 ^oC for 1min. The negative fixed charges and leakge current in Hf-aluminate were increased with increasing annealing temperature. It is known that oxygen intersitial which caused by high temperature annealing in O_2 ambient acts as a negative charge. In order to have a better understanding of the impact of annealing on the leakage current, the conduction mechansim was also investigated. The 950 ^oC film was consistent with the Poole-Frenkel conduction and the activation energy was estimated to be Ea ~ 0.19 eV.

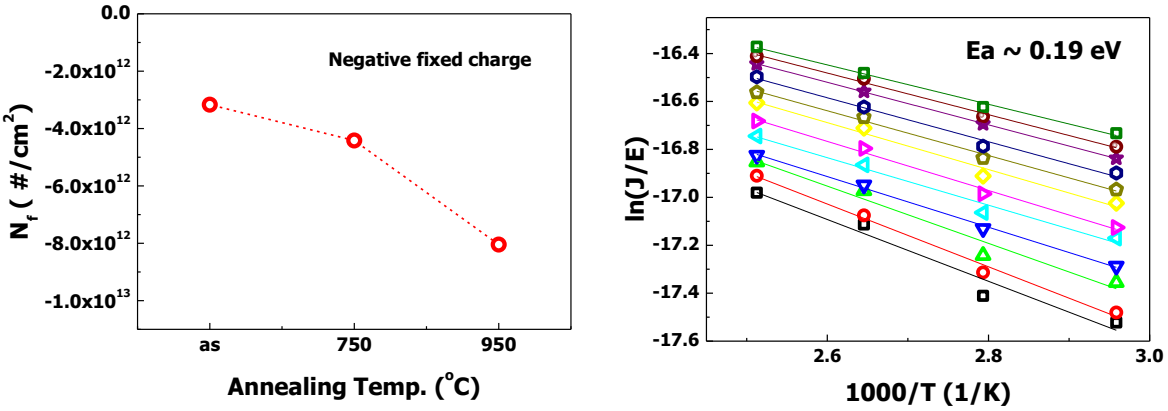

Fig 1. Fixed oxide charges and PF plot of Hf-aluminate films.

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A novel low-temperature treatment on solution-derived amorphous InGaZnO thin-film transistor for flexible display

Yeong-Hyeon Hwang, Sung-Wan Moon, Ja-Kyung Gu, and Won-Ju Cho
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail: chowj@kw.ac.kr

For the inexpensive technologies, the fabrications of solution-derived amorphous InGaZnO thin-film transistors (a-IGZO TFTs) have been intensely studied as of early 2010 [1]. In general, a high melting points and synthesis temperature are required for these TFTs. However, the limit of fabrication is inappropriate condition for flexible display [2]. At present, low-temperature treatments are investigated, such as ultra violet (UV) ozone, exposure of plasma, and microwave irradiation (MWI), etc.

At present, we investigated a low-temperature treatment on solution-derived a-IGZO TFTs by Ar/O_2 plasma with MWI. For a detail research, the plasma ambients were studied as a function of Ar and/or O_2 plasma sources. The MWI is used for a synthesis of solution at low-temperature. Note that, a pristine device is treated only MWI treatment. As a result, the Ar plasma enhanced the mobility of carrier and O_2 plasma improved stability in electrical characteristics of a-IGZO TFTs. These novel treatments led to remarkable results for high electrical performance. Therefore, we demonstrates the feasibility of flexible display with solution-derived a-IGZO TFTs

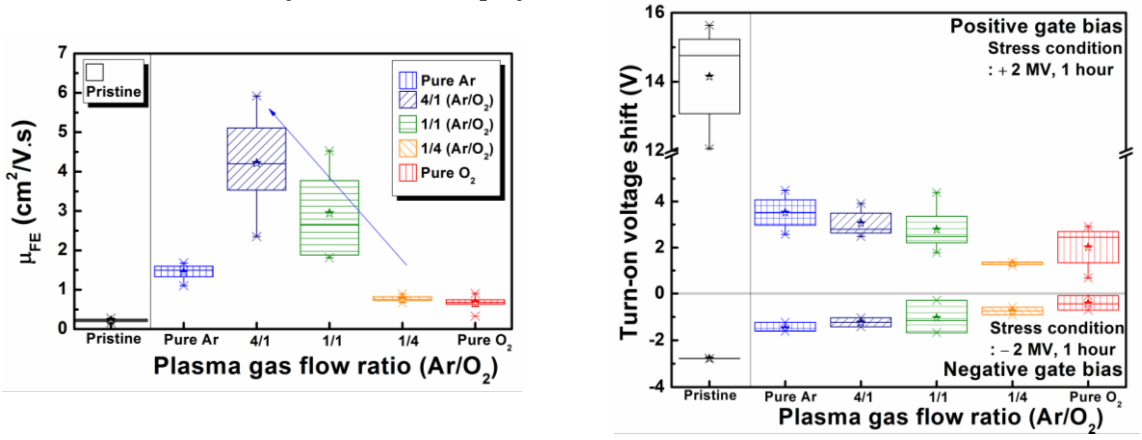

Figure 1. Electrical parameter of solution-derived a-IGZO TFTs

[1] E. Fortunato, P. Barquinha, and R. Martins, Adv. Mater. **24**, 2945 (2012)
[2] T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11**, 044305 (2010)

Acknowledgment

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The speed improvement of In_3SbTe_2 phase change material by doping Bi element

Minho Choi[1], Yong Tae Kim[2], and Jinho Ahn[1]
[1]*Department of Materials science and engineering, Hanyang University, Seoul 133-791, Korea*
[2]Semiconductor Materials and Device Laboratory, Korea Institute of Science and Technology, Seoul, Republic of Korea
E-mail : jhahn@hanyang.ac.kr

Recently, the reversible switching from amorphous phase to crystalline phase and vice versa is attractive for phase change random access memory (PRAM). Particularly, multi-level phase changing properties are strongly required for multi-bit application. In_3SbTe_2 (IST) has high crystallization temperature and activation energy and it seems to be promising candidate for multi-level application. Higher crystallization temperature and activation energy offer thermal stability, however, there is a tradeoff between the crystallization temperature and the crystallization speed. According to the nucleation and growth mechanism, the crystal growth rate of the IST depends on the activation energy for the crystallization as the growth-dominated phase change material. In this work, we have tried to modulate the crystallization temperature by adding Bi atom in the IST alloy. As a result, not only the initial and other multi-level crystallization temperatures but also the activation energy decreases. The Crystallization temperature and the activation energy of Bi-doped IST(3.2-5.5at.%Bi) are higher than those of $Ge_2Sb_2Te_5$, but lower than those of IST. The gap between the initial and the other multi-level crystallization temperatures becomes to widen. Consequently, these effects of Bi doping will be an advantage for controlling multi-phases according to the amount of joule heating. From the fabricated PRAM cell devices, We confirm the resistance difference between each level and compare the Bi doping effects on the multi-level phase change. Multi-level resistances corresponding to several phases are introduced by controlling different pulses and the change of microstructures are thoroughly investigated using Transmission Electron Microscopy (TEM).

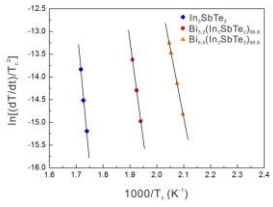


Fig 1. The Kissinger's plots of IST and Bi-doped IST alloys

High Performance Solution-processed MoS_2 Field Effect Transistor by Two-step Annealing

Juyeon Won, Chul-Kyu Lee, Byeong-Geun Son, Hyo Jin Kim, Soyeon Je, and Jae-Kyeong Jeong
Department of Materials Science and Engineering, Inha University, Incheon 402-751, Korea
E-mail : jkjeong@inha.ac.kr

이황화몰리브데늄 (MoS_2) 은 좋은 전기적 특성으로 트랜지스터 재료로서 주목 받고 있다. 같은 이차원 구조를 가지지만 밴드갭이 존재하지 않아 트랜지스터에 사용하기 어려운 그래핀과 달리 MoS_2 는 밴드갭(1.2~1.8eV)을 가지고 있어 Field effect transistor (FET) 의 재료로서 사용될 수 있다 [1]. MoS_2 박막을 만들기 위한 방법은 물리적 박리, 화학적 박리, 열분해 등 여러 가지가 있지만 좋은 전기적 특성을 갖는 양질의 MoS_2 박막을 넓은 범위에 걸쳐 증착 하는 방법은 제한적이다. 대면적 증착 확장성이 우수한 용액 공정의 경우 용매에 의한 탄소 잔여물에 의해 낮은 결정성을 갖는 박막이 형성되게 된다 [2].

본 연구에서는 기존에 많이 사용되고 있는 물리적 박리가 아닌 $(NH_4)_2MoS_4$ 원료를 이용한 용액 공정을 통해 바텀게이트 구조를 갖는 MoS_2 FET 를 제작하였다. 좋은 전기적 특성을 갖는 박막의 형성을 위하여 원료의 열분해 온도에서 열처리를 진행하고 탄소 잔여물을 제거하기 위한 고온 열처리를 2-step 으로 실시했다. 이와 같은 방법으로 450℃ 열처리하고 냉각한 후 850℃ 열처리를 진행한 소자와 450℃ 열처리 후 연속적으로 850 ℃ 열처리를 진행하여 제작한 MoS_2 FET 소자의 전기적 특성을 비교하였다. 최적조건에서 제작된 MoS2 FET 소자는 이동도 26cm^2/V-s, Subthreshold Swing 0.92V/dec, I_{on-off} 10^{-7} 의 우수한 특성을 나타내었다.

[1] B. Radisavlijevic, A. Radenovic, J. Brivio, B. Giacometti, and A. Kis, Nat. Nanotechnology, **6**, 147 (2011).
[2] Keng-Ku Liu, Wenjing Zhang, Yi-Hsien Lee, Yu-Chuan Lin, Mu-Tung Chang, Ching-Yuan Su, Chia-Seng Chang, Hai Li, Yumeng Shi, Hua Zhang, Chao-Sung Lai, and Lain-Jong Li, Nano Lett., **12**, 1538 (2012).

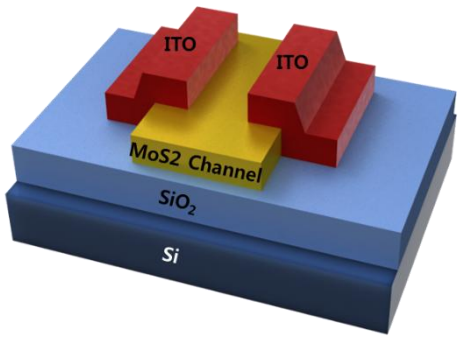


Figure 1. Structure of MoS_2 TFT device

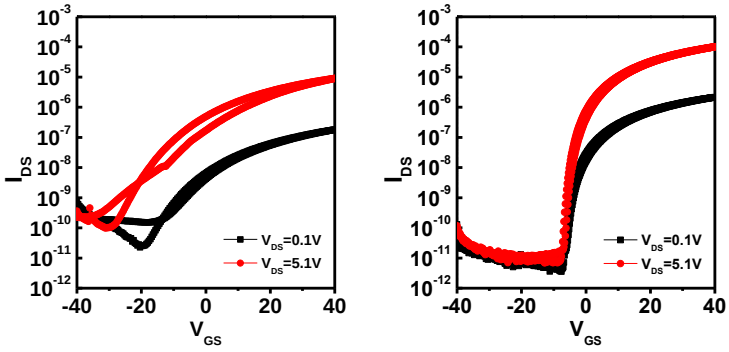


Figure 2. Representative transfer characteristics of (a) annealing at 450℃ to 850℃ (conventional) (b) 2-step annealing at 450℃ to 850℃

Solution processed CuO_x and its transport characteristics

Si-Hong Kim, Myung-Ji Kim, Ji-Su Ahn, Deok-kee Kim*
Department of Electrical Engineering, Sejong University, Seoul, Korea
*E-mail : deokkeekim@sejong.ac.kr

CuO_x has been known as a p-type semiconductor with a monoclinic structure, exhibiting a narrow band gap (1.2 eV) and a number of interesting properties such as Mott transition. The carrier type is ascribed to the presence of Cu vacancies, which make an acceptor level of 0.3 eV above the valence band. CuO_x has been used widely in catalyst, electrochemical cells, gas sensing, field emission devices, storage media, and superconductors.

Both the MIM and back-gated TFT structures were fabricated to study the transport characteristics of CuO_x. Arsenic doped Si wafer ($\rho \sim 5$ mΩ·cm) was used as the gate and 100-nm-thick oxide was thermally grown as the gate dielectric. CuO_x nano-particle dispersed solutions were formed using MIBK solvent with the ratio of 2:8. 100-nm-thick CuOx films were spun-coated as the semiconductor layer using the CuO_x dispersed solution. CuO_x films were annealed at the temperatures of 200 – 600 ˚C for 30 min under forming gas (H_2 5%, N_2 95%) and O_2 atmosphere. 5 nm Ti/100 nm Au electrodes were formed by e-beam evaporator with the varing channel length/width using shadow mask. X-ray diffraction and scanning electron microscopy were used for the microstructure and morphology of the films, and mobility of the CuO_x film was measured by the hall measurement system. Transport characteristics were measured by the Agilent B1500 parameter analyzer .

CuO MIM structure showed resistive switching characteristics since sufficient Cu ions were provided to form the reversible metallic filaments from the electrodes. Cu_2O MIM structure showed bipolar exponential I-V characteristics, which was attributed to mixed ionic and electronic conduction.

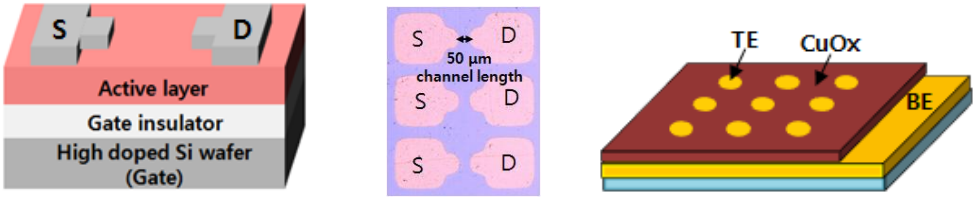


Fig. 1 Schematic and optical microscopy image of CuOx TFT and MIM structures.

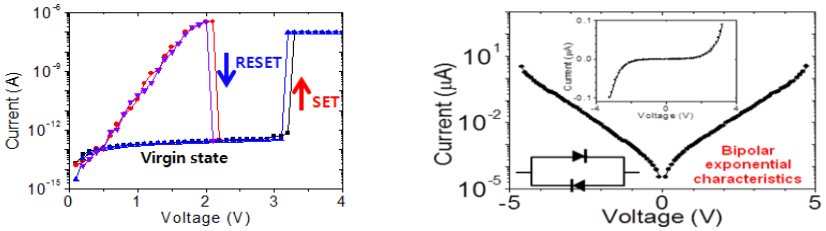


Fig. 2 (left) resistive switching characteristics of CuO, and (right) bipolar exponential characteristics of Cu_2O MIM structure.

[1] J. B. Reitz and E. I. Solomon, J. Am. Chem. Soc. **120**, 11467 (1998)

Improvement in Bias Stability of Amorphous IGZO Thin Film Transistors by High Pressure H_2O_2 Annealing

Ji Hun Song, Chang-Kyu Lee, Ah Young Hwang, and Jae Kyeong Jeong
Department of Materials Science and Engineering, Inha University, Incheon 402-751, Korea
E-mail : jkjeong@inha.ac.kr

훌륭한 전기적 특성을 갖는 ZnO 기반의 산화물 반도체 박막트랜지스터(TFT)는 AMOLEDs 에 적용 될 수 있다. 하지만 이러한 장점에도 불구하고 산화물 반도체 TFT 소자에 전압이 인가되었을 때 문턱전압이 이동하게 되는 안정성 문제를 갖는다. 따라서 이를 해결하기 위한 연구가 널리 진행 되고 있다. 본 연구소에서는 고압 분위기 열처리를 통해 안정성의 원인으로 작용할 수 있는 산소공공(Oxygen vacancy)을 감소시키는 연구를 진행하였다.

산화물 반도체 TFT 소자의 안정성을 향상시키는 대표적인 분위기 열처리로는 산소 고압 열처리(HPA)가 있으며, 또한 H_2O 기체를 사용한 열처리를 통해 TFT 소자의 안정성을 높일 수 있다는 연구 결과가 보고된 바 있다[1,2]. 본 연구에서는 IGZO TFT 소자에 H_2O 보다 더 큰 반응성을 갖는 산화제인 H_2O_2 기체를 사용한 HPA 를 통해 positive bias stress(PBS) 및 negative bias illumination stress(NBIS) 조건에서 안정성이 향상됨을 확인하였고 이를 H_2O 기체를 사용한 경우와 비교하였다. 그 결과 H_2O_2 기체를 산화제로 사용할 때 기존 H_2O 기체에 비해 효과적인 PBS 및 NBIS 신뢰성 개선을 확인하였다.

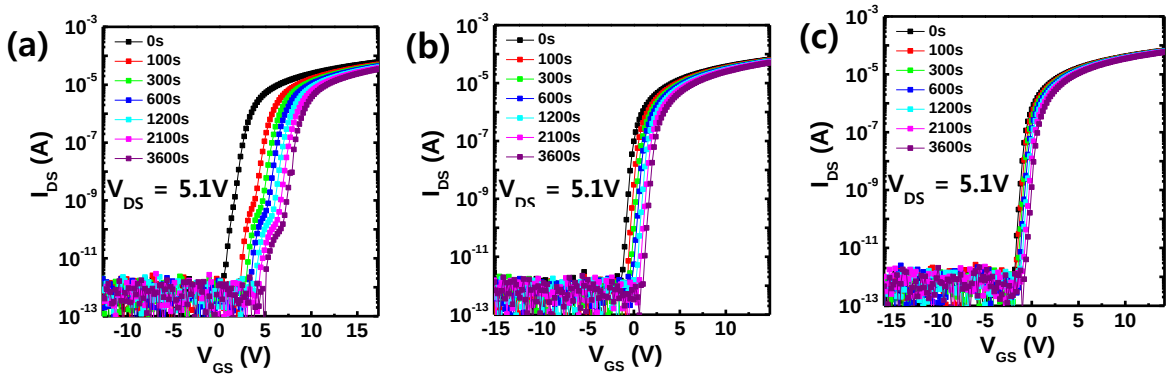


Fig 1. PBS 조건에서 IGZO TFTs 의 (a) Reference, (b) H_2O HPA, (c) H_2O_2 HPA 전기적 특성의 비교

[1] S. Y. Park, J. H. Song, C. –K. Lee, B. G. Son, C. K. Lee, H. J. Kim, R. Choi, Y. J. Choi, U. K. Kim, C. S. Hwang, H. J. Kim, and J. K. Jeong, IEEE Electorn Device Lett., **34**, 894 (2013).
[2] K. Nomura, T. Kamiya, M. Hirano, H. Hosono, Appl. Phys. Lett., **95**, 013502 (2009).

Soluble-Processed Zr-La-O/SiO_2 Gate Dielectrics at 180℃ for flexible metal oxide transistors

Soyeon Je, Byeong-guen Son, Hyojin Kim, Juyeon Won, and Jaekyeong Jeong
Department of Materials Science and Engineering, Inha University, Incheon, Korea
E-mail : jkjeong@inha.ac.kr

차세대 디스플레이인 플렉서블 디스플레이의 구현을 위해서는 플라스틱 기판 사용이 필수적이므로, 저온 공정 개발의 중요성이 대두되고 있다. 그러나 기존의 화학 기상 법(Chemical vapor deposition)이나 스퍼터(Sputter) 장비를 이용한 공정은 우수한 소자 성능을 나타내지만, 공정 온도가 300 도 이상이며 비싼 제조 설비와 긴 공정 시간이 필요한 단점이 있다. 그래서 대안으로 용액 형 소재를 만들어 값싼 제조 공정과 저온에서 소자 제작이 가능한 솔젤(sol-gel)법을 이용한 방법이 대두 되고 있다. [1-2]. 이러한 솔젤법을 이용하여 박막 트렌지스터(TFT) 내에 들어가는 게이트 절연막을 250 도 이하 저온에서 제작함으로써 소자 가공이 간단해지고 경제성을 가질 것으로 기대된다.

본 연구에서는 High-k 물질인 ZrO_2 와 La_2O_3 두 가지 물질로 만든 용액을 Perhydropolysilazane (PHPS) 용액 위에 각각 스핀 코팅하여 Zr-La-O/SiO_2 이중 층 게이트 절연막을 형성 하였다. IZO 를 채널로, ITO 를 소스/드레인으로 하는 바텀 게이트 박막트렌지스터를 180 도에서 제작하였다. High-k 물질인 Zr-La-O 를 산화물 반도체와 접하는 이중 층 구조 상층에 코팅함으로써 채널 물질과의 양질의 계면 형성과 절연효과를 기대할 수 있다. 이중 층 구조 하층의 SiO_2 는, 점도가 낮아 얇게 코팅되는 Zr-La-O 박막이 받는 전계의 크기를 감소시켜 소자의 항복전압을 높여준다.

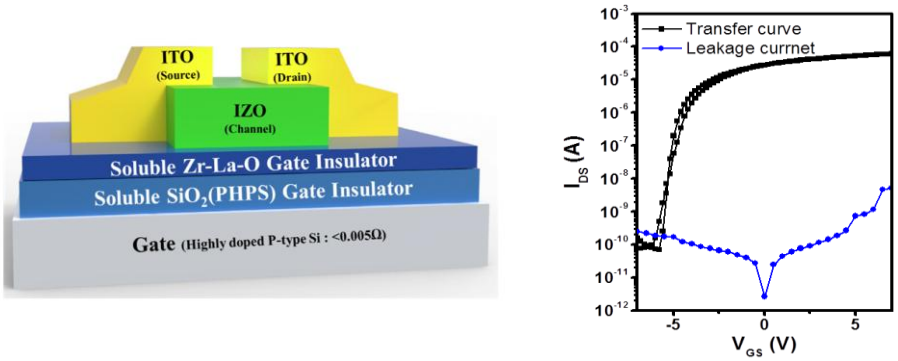


Fig 1. TFT device structure and transfer curve

[1] S. M. Lee, S. M. Hwang, J. H. Choi, K. Park, H. Kim, J. H. Lim, and J. Joo, Jpn. J. Appl. Phys., **51**, 09MF13(2012)

[2] C. G. Lee , A. Dodabalapur, J. of Electronic Materials, **41**, 895(2012)

Atomic Layer Deposition of Ruthenium Thin Film from Ru precursor

Hyo Jun Jung,[a,b] Eun Ae Jung,[a] Jeong Hwan Han,[a] Bo Keun Park,[a] Sun Sook Lee,[a] Jin Ha Hwang,[b] Chang Gyoun Kim,[a] Ki Seok An,[a] and Taek Mo Chung[a]

[a]*Thin Film Materials Research Group, Advanced Materials Division, Korea Research Institute of Chemical Technology, 141 Gajeongro, Yuseong, Daejeon 305-600 Republic of Korea*
[b]*Department of Materials Science and Engineering, Hongik University, Seoul 121-791, Korea*
E-mail : Hyo918@krict.re.kr

Ruthenium (Ru) 박막은 우수한 화학적 · 열적 안정성 및 높은 일함수 (4.7eV) 특성으로 인해 20nm 급 이하의 차세대 DRAM capacitor 의 전극 물질 및 Cu metalization 을 위한 seed layer 로 각광을 받고 있다. Ru 박막의 나노스케일 정보전자소자로의 적용을 위해서는 두께제어가 용이하고 3D 구조에서 우수한 단차 피복특성을 갖는 atomic layer deposition (ALD)을 이용한 박막 형성이 필수적이다. 이에 본 연구에서는 0 가의 Ru 전구체를 이용하여 우수한 초기성장거동을 갖는 Ru 박막을 ALD 방법을 이용하여 증착 하고자 하였다. 그림 1 (a,b)에 나타낸 바와 같이 270 도의 공정 온도에서 Ru 전구체와 반응가스(O_2)의 주입시간에 따라 각각 saturation 거동을 보여 ALD self-limiting 반응을 함을 확인 하였다. 이렇게 증착된 Ru ALD 박막은 0.075nm/cycle 의 증착 속도를 보이고 그림 2 에 나타난 바와 같이 SiO_2 기판 상에서 15 cycles 의 짧은 incubation period 를 나타내어 기존 cyclopentadienyl 기반의 Ru 전구체와 비교하여 우수한 초기성장거동 특성을 가짐을 확인하였다. [1] 또한 본 여러 기판에서의 루테늄 박막의 초기 성장 거동을 확인하였고, 위 같은 self-limiting 반응을 기반한 Ru ALD 박막의 화학적, 물리적 특성을 보고하고자 한다.

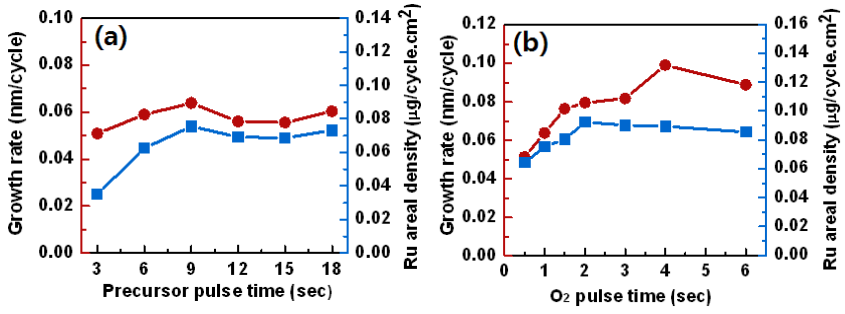


그림 1. (a)Ru 전구체 주입시간에 따른 growth rate 변화 (b) O_2 주입시간에 따른 growth rate 변화

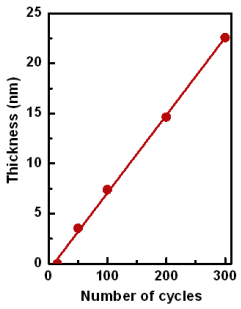


그림 2, ALD cycle 수에 따른 Ru 박막의 두께 변화

[1] Titta Aaltonen, Petra Alen, Mikko Ritala and Markku Leskela, chem. vapor dep. 2003, 9 (1), 45–49.

Anomalous behavior of oxygen gas ratio-dependent field effect mobility in In-Zn-Sn-O thin film transistor

Ah Young Hwang, Chang-Kyu Lee, Ji Hun Song, and Jae Kyeong Jeong
Department of Materials Science and Engineering, Inha University, Incheon 402-751, Korea
E-mail : jkjeong@inha.ac.kr

InGaZnO 박막트랜지스터(TFT)는 기존의 널리 사용되던 비정질 실리콘보다 높은 전하이동도와 $I_{on/off}$, 우수한 균일성과 신뢰성의 장점으로 최근 AMOLED 양산에 적용되기 시작하였다. 그러나 60 인치 이상의 대면적 디스플레이와 초고해상도의 성능을 동시에 만족하기 위해 10 cm^2/Vs 정도의 전하이동도를 가지는 InGaZnO 로는 한계가 있어 30 cm^2/Vs 이상의 전하이동도를 가지는 물질의 연구가 필요하다 [1, 2].

본 연구에서는 높은 전하이동도를 만족하기 위해 InO_2를, 우수한 신뢰성을 가지는 SnO_2를 포함하는 InZnSnO 로 실험을 진행하였다. 스퍼터링 시스템에서 ITO 타겟과 ZTO 타겟을 사용하여 동시증착법으로 채널을 증착하였고, 산소 분압 변화시에 IZTO TFT 소자 특성의 의존성을 평가하였다. Ar : O_2 = 10 : 0 일 때와 Ar : O_2 = 7 : 3 일 때의 이동도가 각각 12.6cm^2/Vs, 19.7cm^2/Vs 로 산소 비율이 증가함에 따라 전하이동도가 증가하였다. 기존 IGZO 산화물 반도체에서는 산소 비율이 증가하면 산소공공(V_O) 농도감소로 인해 전하이동도가 감소한다. 이는 전하농도가 증가하면 전하이동도가 증가하는 percolation 전도기구로 이해할 수 있다. 그러나 본 IZTO 물질에서는 산소비율 증가에 따라 오히려 전하이동도가 증가하였는데, 이는 IZTO 반도체에 함유된 Sn 이온의 가전자상태가 +2/+4 가의 상대적 비율이 산소농도에 따라

의존하기 때문인 것으로 분석되었다.

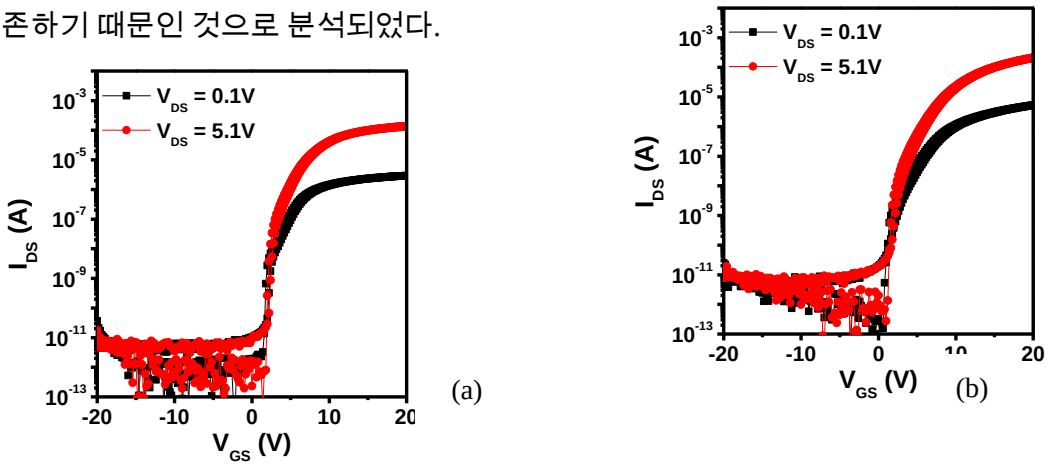


Fig 1. Transfer characteristics of the TFTs (a) Ar : O_2 = 10 : 0, (b) Ar : O_2 = 7 : 3

[1] M. K. Ryu, S. H. Yang, S. H. Ko Park, C. S. Hwang, and J. K. Jeong, Appl. Phys. Lett., **95**, 173508 (2009).

[2] M. K. Ryu, S. H. Yang, S. H. Ko Park, C. S. Hwang, and J. K. Jeong, Appl. Phys. Lett, **95**, 072104 (2009).

Effect of HfO_2 charge trap layer and Al_2O_3 blocking layer thickness on MAHAS structure memory characteristics

Heedo Na, Jinho Oh, Kyumin Lee, and Hyunchul Sohn
Department of Material Science and Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : hyunchul.sohn@yonsei.ac.kr

For development of high density memory applications, charge trap storage devices would be replaced the conventional floating-gate flash memories. However, memory retention degradation due to the tunnel oxide thickness scale down has been big issue of the conventional SONOS memory development. To overcome this limitation, high-k dielectrics have been attempted by replacing the charge trap layer Si_3N_4 (CTL) / blocking layer SiO_2 (BL). Especially, HfO_2 and Al_2O_3 have been mainly developing for CTL and BL, respectively. [1, 2] But, it is still required to investigate the memory dielectrics scale down for good memory performance. In this study, optimized thicknesses of the HfO_2 CTL and the Al_2O_3 BL were investigated in Junctionless MAHAS devices. V_g vs. V_{th} slope in Increase Step Pulse Program (ISPP) characteristic show program efficiency. [2] Under the 4nm of HfO_2 thickness, ISPP slope is decreased by high applied voltage. Al_2O_3 blocking layer show saturated retention characteristics over the 12nm of thickness. It is suggested that leakage current through the memory dielectric is increased by thickness decrease. For these results, we determine optimized high-k dielectric thickness in MAHAS memory device.

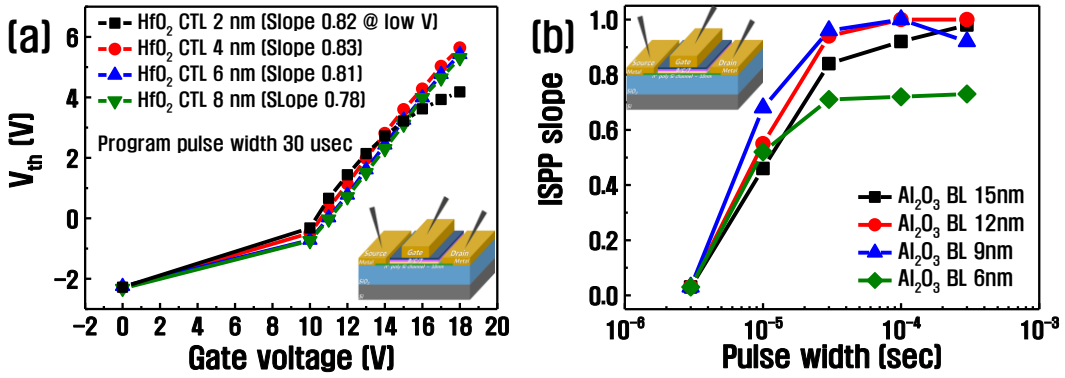


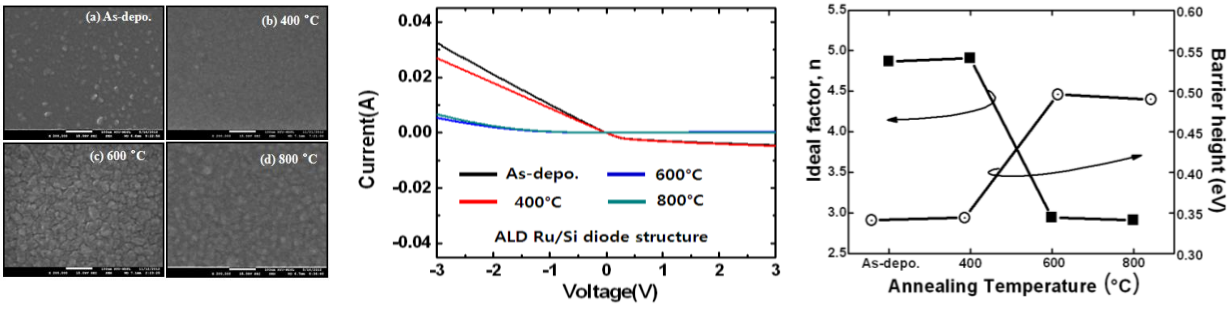
Fig 1. ISPP characteristics in MAHAS a)HfO_2 and b) Al_2O_3 thickness dependence

[1] C. H. Lee, S. H. Hur, Y. C. Shin, J. H. Choi, and K. Kim, Appl. Phys. Lett. **86** (2005) 152908.
[2] J. Buckely, B. D. Salve, G. Ghibaudo, M. Gely, J. F. Damlencourt, F. Martin, G. Nicotra, S. Deleonibus, Solid-State Elect. **49** (2005) 1833
[3] J. Fujiki, T. Haimoto, N. Yasuda, and M. Koyama, J. Jour. Appl. Phys. **50** (2011) 04DD06

The Effects of Post Annealing on the Schottky Behaviors of Atomic Layer Deposited Ruthenium on the Si Substrate

Donghwan Lim[1], Moon-Suk Choi[1], Dohyung Kim[1], Youngil Gil[1], Woosuk Jung[1], Seong Chan Heo[2], and Changhwan Choi[1,*]
[1] Division of Materials Science and Engineering, Hanyang University, Seoul, 133-791, Republic of Korea
[2] SK Hynix Semiconductor, Icheon, 467-701, Republic of Korea
[*]E-mail: cchoi@hanyang.ac.kr

Ruthenium silicide (Ru_2Si_3) is a direct band semiconductor with theoretical value 0.42 eV [1]. However, various band gap ranges were reported with 0.7-1.09 eV as well as 0.86-0.90 eV by the resistivity and optical measurements, respectively. These ones strongly depend on the processes such as (i) Ru implantation into Si, followed by the high temperature recrystallization, (ii) Ru silicide formation on the Si through solid state reaction at high temperature, (iii) reactive co-deposition of Ru and Si on the Si [2]. Since three dimensional devices are of great interest, atomic layer deposition (ALD) becomes more important technique to attain the conformal and uniform films. Many reports on the ALD Ru thin films for the trench memory devices have been shown. However, ALD Ru or Ru_2Si_3 have not been proposed as a metal to semiconductor contact application even though Ru and its silicide are attractive materials. Until now, only PVD-based Ru silicides have been reported. In this study, we have investigated the characteristics of ALD Ru/Si schottky diode under various post annealing temperatures. Deposition method and post annealing affect on the microstructure and lead to the different silicide formation temperature. In this study, Ru-Si (Metal-Semiconductor, MS) diode devices were fabricated. After the native oxide removal with the subsequent cleaning on the p-type Si substrate, 50 nm-thick ALD Ru were deposited with bis (ethylcyclopentadienly) ruthenium, $Ru(EtCp)_2$, precursor. After the photolithography step, ALD Ru thin film was etched by Reactive Ion Etching. 100 μm by 100 μm square patterns were attained. As a reference, PVD Ru/Si diode was also prepared. Finally, in order to study the effects of post annealing on the MS contact, the samples were annealed in the furnace by varying temperatures from 400℃ to 800℃ under vacuum (10^{-3} torr) for 1 hour. Materials properties of the devices were characterized with Atomic Force Microscopy (AFM), X-ray diffraction (XRD), Field Emission Scanning Electron Microscopy (FE-SEM), Auger Electron Spectroscopy (AES) and Current-Voltage. Grain size was increased with higher annealing temperatures. However, relatively finer grains were observed up to 400℃ annealing. Surface morphologies suggest that the ALD Ru thin film is uniform and grains are relatively finer. With increasing temperature, higher n and lower Φ_B were attained. Significant current mode change was observed with over 600℃ annealing. Surface morphologies, crystal structure change and elemental profiles support that current mode change stems from Ru_2Si_3 formation as a result of Ru and Si interdiffusion.



(a) (b) (c)

Fig1. SEM analysis (a), I-V characteristics (b), ideal factor and barrier height (c) as function of annealing temperatures on ALD Ru/Si diode.

[1] W. Henrion et al, *Thin Solid Film*, 313/314, (1998), 218
[2] D. Lenssen et al, *Microelectron. Eng*. 50 (2000), 243

This research was supported by the IT R&D program of MKE/KEIT (10039174, Technology Development of 22 nm level Foundry Device and PDK).

Top-gate oxide thin-film transistors using solution-processed gate stack of PVP/Al-Zn-Sn-O with an Al_2O_3 capping layer for full-patterning process

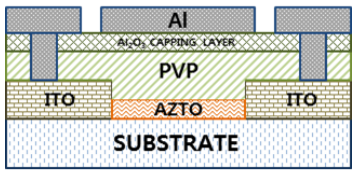
Kyeong-Ah Kim, Jun-Yong Bak, Sung-Min Yoon*

Department of Advanced Materials Engineering for Information & Electronics,

Kyung Hee University, Yongin, Gyeonggi-do 446-701, Korea

E-mail: sungmin@khu.ac.kr

In order to realize the oxide thin-film transistors (TFTs) fabricated by solution process, the gate stack composed of poly-4-vinylphenol (PVP) organic gate insulator (GI) and Al-Zn-Sn-O (AZTO) active channel was proposed. Although the PVP GI layer could be easily prepared by solution process at a temperature lower than 100 ^oC, it was very difficult to form the contact holes through the PVP via conventional patterning process. Actually, the electrical properties including leakage currents and dielectric breakdown fields for the PVP films were seriously degraded by the use of chemicals such as developer and/or resist stripper during the photolithography process. Thus, the first feature of this work is that an atomic-layer-deposited Al_2O_3 thin film was introduced as a capping layer for protecting the PVP GI to fabricate the top-gate oxide TFTs. The choice of the solution-processed AZTO as an active layer composition was the second feature of this work, in which the effects of the Al contents incorporated into ZTO on the TFT behaviors were systematically investigated. The thickness values of each layer of Al_2O_3, PVP, and AZTO were designed to be 12, 300, and 25 nm, respectively. Figure 1 shows the schematic cross-section of the fabricated AZTO TFT. Transfer characteristics and gate leakage currents of the fabricated TFT were evaluated as shown in Fig. 2. Thanks to the introduction of Al_2O_3 capping layer, a large on/off ratio and a high field-effect mobility were successfully obtained. For the TFT using ZTO channel without an Al incorporation, the field-effect mobility, subthreshold swing, and on/off ratio were estimated to be approximately 45.2 $cm^2V^{-1}s^{-1}$, 0.87 V/dec, and 1.03×10^6, respectively. This is the first report on the fabrication of top-gate oxide TFT with organic/inorganic hybrid-type gate-stack by full-patterning process. We confirmed the process feasibility of PVP GI and the potential of AZTO active channel for the oxide TFTs with good performances.



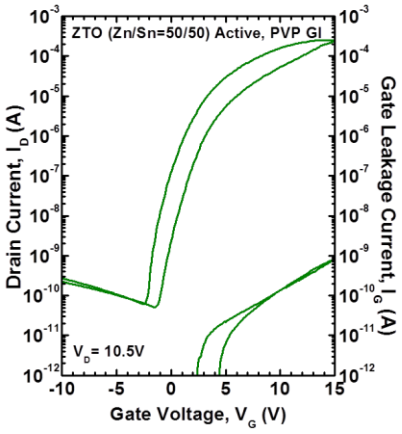


Fig. 1 (Left) Schematic cross-section of the fabricated devices.

Fig. 2 (Right) Drain current-gate voltage transfer characteristics and gate leakage currents.

Improvements in bias-stress stability characteristics of solution-processed Al-In-Zn-O thin-film transistors with optimizing the channel composition

Minji Park, Jun-Yong Bak, Jeong-Seon Choi, Sung-Min Yoon*
Department of Advanced Materials Engineering for Information and Electronics, Kyung Hee University, Yongin, Gyeonggi-do 446-701, Korea
*E-mail: sungmin@khu.ac.kr

There have been enormous studies on the fabrication of oxide thin-film transistors (TFTs) using solution process due to its features of low-cost and simplicity. From the viewpoint of thermal budget for the production, the process temperature lowering has been the main issue for the solution-processed oxide TFTs. However, the improvement of excellent device stabilities are also significantly urgent concerns to realize the oxide TFT backplanes using the solution process. Thus, the main object of this work was to search for suitable compositions of solution-processed oxide channel layers and to clarify the effects of channel composition modification on the TFT bias-stress stabilities. We fabricated top-gate oxide TFTs using solution process, in which an In-Zn-O (IZO) was chosen as an essential composition and an appropriate amount of Al was incorporated into the IZO (AIZO). As a typical composition, the atomic ratio of In/Zn was set to be 3:7 and the incorporated Al content was 5 mol%. Fig. 1(a) shows the drain current-gate voltage (I_{DS}-V_{GS}) characteristics of the fabricated IZO and AIZO TFTs. While an on/off swtiching was not confirmed for the IZO TFT even at the V_{GS} sweep to -40 V, excellent transfer characteristics were obtained for the AIZO TFT. The field-effect mobility, subthreshold swing, and on/off ratio were estimated to be 1.06 $cm^2V^{-1}s^{-1}$, 0.24 V/dec, and 2.1×10^7, respectively. The negative and positive-bias stress stabilities were also examined, in which V_{GS} of -20 V or +20 V was continuously applied for 10,000 s, as shown in Figs. 1(b) and (c), respectively. The shifts in turn-on voltages were as small as 0.5 V. These results suggest that the appropriate control of channel composition could effectively enhance the stability properties as well as TFT operations. It can be concluded that these improvements in the bias-stress stabilities for the solution-processed AIZO TFT were very competitive performance, and that carefully modified AIZO compositions could be very suitable for the future backplane devices. At the presenstation, we will fully discuss on the material properties and device behaviors when the channel compositions of IZO and AIZO were extensively varied.

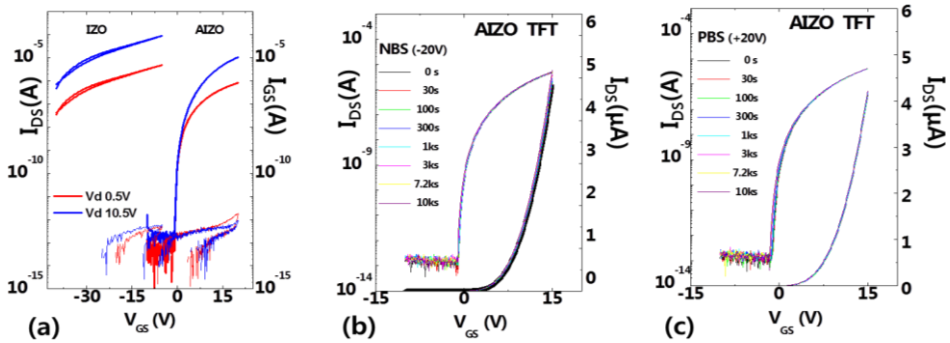


Fig. 1. (a) Transfer characteristics and gate leakage currents of the IZO and AIZO TFTs. The variations in transfer curves of the AIZO TFT under the (b) negative and (c) positive bias-stress conditions.

Thickness and composition effects of Al-doped ZnO channels prepared by atomic layer deposition on the device behaviors of oxide thin-film transistors

Eomji Kim, Jun-Yong Bak, Jeong-Seon Choi, and Sung-Min Yoon*
Department of Advanced Materials Engineering for information and Electronics
Kyung Hee University, Yongin, Gyeonggi-do 446-701, Korea
*E-mail: sungmin@khu.ac.kr

An aluminum-doped zinc oxide (AZO) thin film was proposed as an active channel layer of the thin-film transistors (TFTs) composing the backplane for the next-generation flat-panel displays. In these applications, the film thickness and composition of AZO layer would be remarkably important parameters to determine the electric characteristics of the AZO[1-2]. Atomic-layer deposition (ALD) is the best methods to precisely control these process parameters. Thus, in this work, the AZO films were prepared by ALD as channel layers of the oxide TFTs and the effects of their thickness and composition conditions on the TFT behaviors were investigated.

We fabricated the AZO TFTs with a top-gate bottom-contact structure, in which the AZO film thickness were varied from 20 to 100 nm. The atomic ratio of Al:Zn was controlled to be 1:20, 1:50, and 1:100, which was readily modified by changing the number of process cycles for the precusors of trimethylaluminum and diethylzinc during the ALD.

When the composition was fixed at 1:50, excellent on/off switching of TFT was confirmed for the device employing the AZO channel thickness of 20 nm, as shown in Fig. 1(a). It was found that the carrier concentration of the AZO film drastically increase with incresing the film thickness. On the other hand, higher carrier mobility was obtained when the Al:Zn ratio was reduced to 1:100 for the 20-nm-thick AZO channel, as shown in Fig. 1(b). These investigations strongly suggest that there are optimum conditions with compromising two parameters of film thickness and composition for guaranteeing higher performances of the AZO TFTs. In this work, the feasibility of ALD-AZO channel layer were succesfully confirmed for the TFT applications with controlled characteristics.

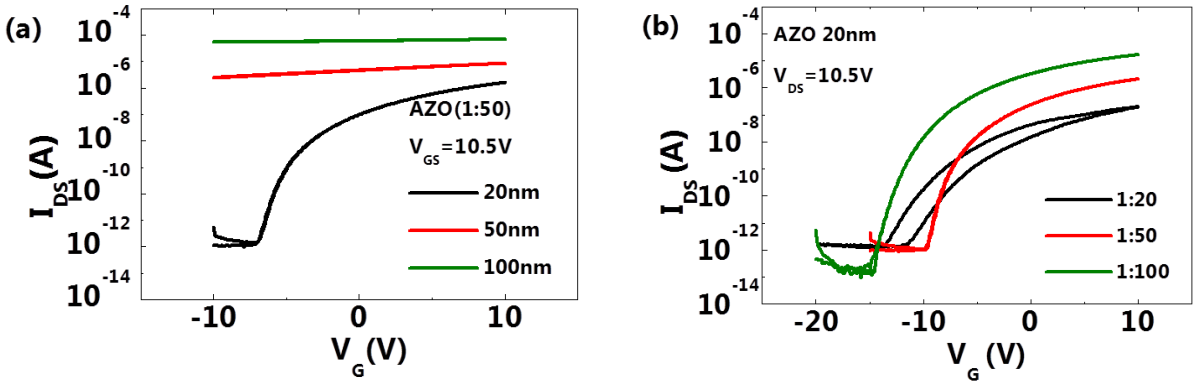


Fig. 1. Variations in drain current-gate voltage characteristics of the fabricated AZO TFTs (a) with changing the active layer thickness and (b) with changing the film composition.

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[2] W.J. Maeng et al., J. Vac. Sci. Technol. B 30, 031210 (2012).

Effect of bottom gate insulator thickness on the threshold-voltage tunability and stress stabilities of the fully-transparent double-gate In-Ga-Zn-O TFTs

Da-Bin Jeon and Sung-Min Yoon*

Department of Advanced Materials Engineering for Information and Electronics,

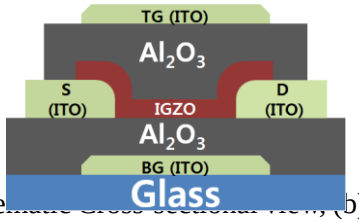
Kyung Hee University, Yongin, Gyeonggi 446-701, Korea

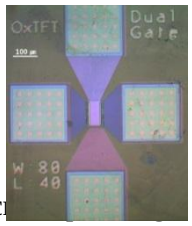
*E-mail: sungmin@khu.ac.kr

Although double-gate (DG) configurations have been developed for improving the current drivability of the field-effect devices, they could also be very useful for the oxide thin-film transistors (TFTs) in controlling the threshold voltage [1, 2]. Typically, the oxide TFTs exhibit depletion-mode behaviors with a negative turn-on voltage. Furthermore, it is very difficult to adjust the threshold voltages to be target values. These features limit the utilization of oxide TFTs for the practical circuit applications. For this purpose, it is very important to optimize the coupling ratio between the top- and bottom-gate capacitances. However, detailed investigations on these viewpoints for the DG oxide TFTs have hardly been reported. Thus, the main object of this work was to systematically examine the threshold-voltage tunability for the DG oxide TFTs.

We fabricated the DG TFTs using an In-Ga-Zn-O (IGZO) channel layer, in which the gate stack structure was designed to be top-gate (TG) ITO/top gate insulator (TGI) Al_2O_3/active IGZO/source and drain (S/D) ITO/bottom gate insulator (BGI) Al_2O_3/bottom-gate (BG) ITO, as schematically shown in Fig. 1(a). The capacitance coupling ratio between TG and BG were modified by changing the film thickness of BGI. While the TGI thickness was fixed at 120 nm, the BGI thickness was varied to 40, 60, and 120 nm. Although a larger electric field applied to a thinner BGI would be expected to enhance the threshold-voltage tunability, the optimum coupling ratio should be determined by considering overall performances of the DG TFTs. Bias-stress stability for the fabricated DG oxide TFT is another important concern to be verified. It can be noticeable that the DG TFT was fabricated to be fully transparent in a visible range, as shown in Fig. 1(c). Thus, the bias-stress stabilities characteristics under illumination conditions, such as negative-bias and positive-bias illumination stresses, will be extensively evaluated and the effects of BGI thickness will be clarified for the fabricated DG TFTs.

(a)





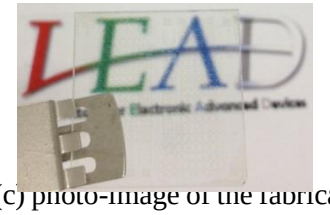


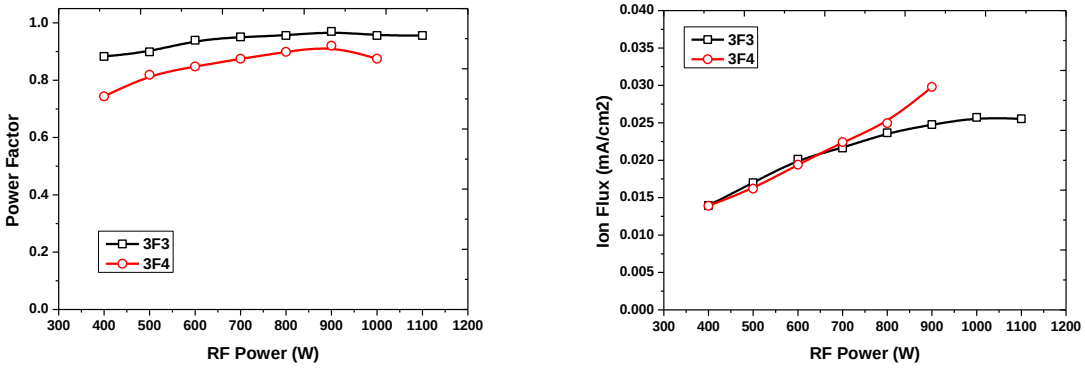
Fig. 1. (a) Schematic cross-sectional view, (b) micr and (c) photo-image of the fabricated transparent DG TFTs.

[1] H. Lim et al, Appl. Phys. Lett., 93, 063505 (2008)
[2] C. H. Park et al, IEEE Electron Device Lett. 30, 30 (2009)

Effects of Ferrite Core Loss and Permeability at 400 kHz Ferrite Inductively Coupled Plasma

Sung-Won Cho[1], June Young Kim[2] and Chin-Wook Chung[1]*
[1]*Department of Electrical Engineering, Hanyang University, Seoul 133-791, Korea*
[2]*Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Korea*
*E-mail : joykang@hanyang.ac.kr

Permeability and loss of ferrite core material are important characteristics at the ferrite enhanced inductively coupled plasma. The hysteresis loss of ferrite depends only on the induced magnetic flux in the ferrite. Also, the eddy current loss is related to the driving frequency of discharges. These kinds of loss strongly affect the plasma characteristics such as the electron temperature and plasma density. Furthermore, the permeability of ferrite can be an important factor of the electrical characteristics of ICP. The loss of ferrite can be regarded the reluctance in the transformer circuit which can estimate the plasma impedance. In this paper, effects of these properties of ferrite core were determined at low frequency (400 kHz) ferrite ICP. The plasma diagnostic which uses the floating harmonic method was performed to achieve the electron temperature and plasma density. By the experimental result, it was founded that the power factor of ICP was strongly related to the permeability of ferrite. Then, the loss of ferrite that contains the hysteresis and eddy current loss significantly affects the growth of plasma density.



(a) (b)

Fig 1. (a)The power factor and (b) ion flux of each ferrite (3F3, 3F4) at 75 mTorr

In-situ measurement method of dielectric-film thickness for processing chamber wall monitoring

Jin-Yong Kim and Chin-Wook Chung*

Department of Electrical Engineering Hanyang University,

17 Haengdang-dong, Seongdong-gu, Seoul, 133-791, Republic of Korea

In-situ measurement method of dielectric film thickness was studied. To measure the thickness of dielectric film, two frequencies of small sinusoidal voltage (~1V) signals are applied to an electrically floated planar type probe, and our system measure amplitude of current signals and voltage‑current phase shift. A sheath circuit model is considered in order to measure the dielectric thickness in varying plasma status. In our experiments, accurate dielectric thickness was obtained regardless of RF power, gas pressure and argon-oxygen mixture ratio. This method may be feasible to monitor the contamination of processing chamber wall and helpful to optimize periodic maintenance in semiconductor manufacturing process, such as chemical vapor deposition (CVD) and etching.

e-mail : joykang@hanyang.ac.kr

Comparison of properties of poly SiGe deposited by disilane and trisilane

Hyunchul Jang, Sangmo Koo, Byongju Kim, Sun-Wook Kim, and Dae-Hong Ko
Department of Materials Science and Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : dhko@yonsei.ac.kr

Recently, three-Dimensional multi-layer-stack memory is proposed to beyond scaling down issue of NAND Flash memory [1]. Polycrystalline SiGe layer is investigated for application of the channel layer of 3D NAND flash memory. Disilane gas and trisilane gas are used as Si source gas respectively in CVD process in order to compare properties of poly layer for different kind of precursors. Germane gas and phosphine gas are used as Ge source gas and dopant. We deposited 100nm thickness poly SiGe layer on oxide Si wafer using CVD process at 575 ℃, 650 ℃, and 700 ℃. At 575 ℃, the growth rate of trisilnae case is higher than disilane case. At 700 ℃, the growth rate of both cases is about 16 nm/min. From Arrhenius equation, activation energies are calculated that disilane case is 0.16 eV higher than trisilane case. Resistivity of poly SiGe increases with temperature. Whereas at 575 ℃ and 650 ℃ resistivity of both cases is same, at 700 ℃ trisilane case is higher than disilane case. SIMS data shows phosphorus concentration decreases with temperature and trisilane case decreases more than disilane case. From TEM images, at 700 ℃ grain size of trisilane case is smaller than disilane case. Consequently, the result that trisilane case is higher resitivity at 700 ℃ is because that disilane case is lager grain size and higher dopant concentration than trisilane case.

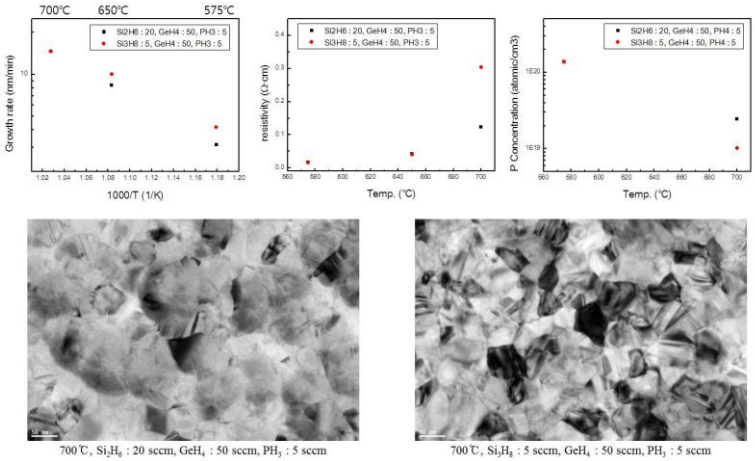


Fig 1. TEM Images, growth rates, resistivity, and P concentrations of poly SiGe layers

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Bipolar Resistive Switching in Amorphous $SrTiO_3$ Films Grown by Atomic Layer Deposition

Woongkyu Lee, Kyung Jean Yoon, Woojin Jeon, Yeon Woo Yoo, Cheol Hyun An, and Cheol Seong Hwang
Department of Materials Science and Engineering and Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-744, Korea
E-mail : hugeant1@snu.ac.kr

저항 변화 메모리는 전극/절연체/전극 구조의 소자에 적절한 외부 전압을 인가하는 방법을 통해 절연체의 저항을 변화시켜, 저저항 상태 (low resistance state, LRS)와 고저항 상태 (high resistance state, HRS)의 저항 차이에 따라 정보를 저장한다. 본 연구에서는 TiO_2, NiO, ZrO_2, HfO_2 등의 전이금속 산화물보다 구조가 더 복잡하며 증착 공정도 어려워서 저항변화 특성이 잘 알려지지 않은 페로브스카이트 구조 산화물인 $SrTiO_3$ 물질을 원자층 증착방법을 통해 성장시키고, (상부)TiN/$SrTiO_3$/Pt(하부) 구조의 소자를 제작하여 저항변화 특성을 알아보았다. 이때 형성된 $SrTiO_3$ 박막의 Sr:Ti 비율은 1:1 을 잘 유지하고 있었으며 비정질의 구조를 가지고 있다. 여러 예비 실험을 거쳐 상부 전극에 음의 전압을 가하여 electroforming 을 시켰을 때 후속 실험 에서 unipolar switching mode 에서 reset 이후 bipolar resistive switching(BRS) 을 잘 유도 할 수 있었다. 이는 전도성 필라멘트가 생성된 이후 이들이 국부적으로 파열되어 나타나는 현상으로 이해 된다. [1] 아래 그림 1 의 왼쪽 그림은 BRS SET 과정에서 compliance current 를 다르게 하여 저항변화 특성을 살펴본 것으로, 여러 크기의 compliance current 에 따라 그래프의 개형이 경향성 있게 바뀌고 있다. 또한 오른쪽 그림과 같이 LRS, HRS 저항에 대한 compliance current 및 RESET voltage 의 영향 역시 타당한 경향성을 보여주었다. 본 발표에서는 $SrTiO_3$ 박막의 morphology 및 불순물 함량 등 물리적 화학적 특성 역시 보고될 예정이다.

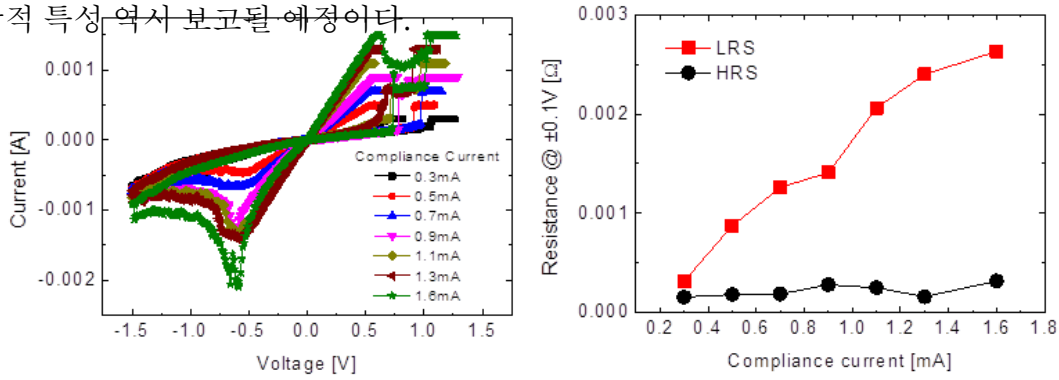

그림 1. (좌) TiN/$SrTiO_3$/Pt 구조의 저항변화 특성
(우) compliance current 에 따른 저항 변화

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Distribution of plasma parameters at wafer level measured by 2D plasma parameter diagnostic method in inductively coupled plasmas

Young-Cheol Kim[1], and Chin-Wook Chung[1*]

[1]*Department of Nanoscale Semiconductor Engineering, Hanyang University, 17 Haengdang-dong, Seongdong-gu, Seoul 133-791, Republic of Korea*

E-mail : saladin072@hanmail.net, joykang@hanyang.ac.kr(coresponding)

Recently, measurement method of two dimensional (2D) spatial distribution of plasma parameters based on the floating harmonic method was developed by Chung and co-workers[1,2]. Because small sinusoidal voltage is applied to wafer-type probe sensor, this method could measure plasma parameters at wafer level in real time without plasma perturbation.

In this study, the 2D plasma density profile and electron temperature were measured in inductively coupled plasma (ICP) with various external parameters such as RF power, processing gas, and mixing ratio in mixture of rare gas and processing gas such as Ar/He and Ar/SF_6. In the argon/helium gas mixture discharge, as a portion of the helium gas increases at a fixed total gas pressure, the uniform 2D plasma density profile was observed, and it is mainly due to the increase in the diffusivity by adding helium gas. Also as mixing ratio of SF_6 was increased, the decrease of plasma density and the incrase of plasma uniformity were observed. It could be understood by addtional partical loss mechanism of SF_6 and change of plasma potential profile by negative ion. These these measurement results can be database for improvnig processing result and characteristic of processing chamber.

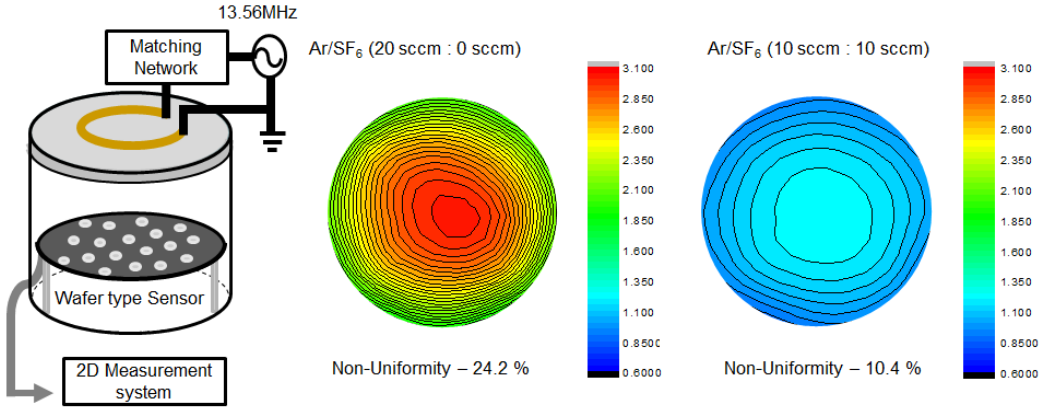

Fig 1. A schematic of experimental setup and 2D ion density profiles of Ar/SF_6 discharge.

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Characteristics of Grain Boundary and Interface Traps in Polysilicon Channel Thin Film Transistors

Yoonseok Jeon, Musarrat Hasan, Cuong Nguyen Manh, Seung-Won You, Duc-Tai Tong, Dong-Hwi Lee, Jae-Kyung Jeong and Rino Choi
Inha University, Incheon, Korea
E-mail : rino.choi@inha.ac.kr

We have investigated thin film transistors (TFTs) with ultra-thin polycrystalline silicon. Characteristics and energy profile of trap states in polysilicon channel TFT are analyzed using charge pumping method. It is found that trap states of small grain size device are higher than lager grain size device from intrinsic energy level to conduction band. On the other hand, trpa states of thick channel device are higher than thin channel device only around midgap energy level. It clearly demonstrates that trap states of grain boundray affect to the midgap and trap states of interface affect to the band edge.

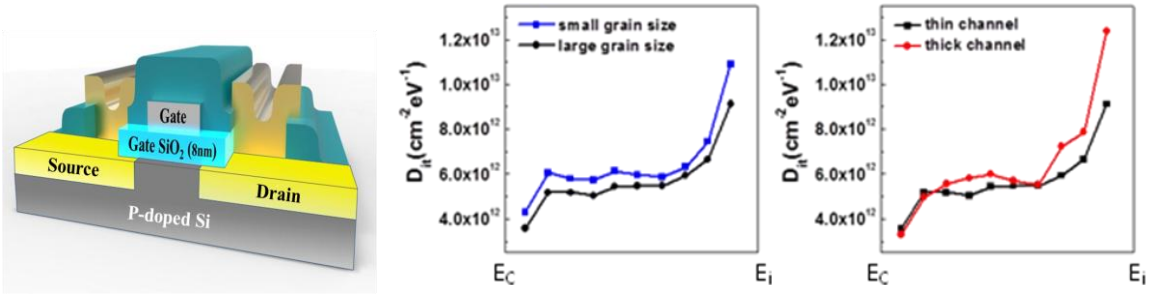

Fig 1. device structure and trap distribution

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Stress induced leakage current characteristic of La-incorporated HfO_2 gate dielectric

Seung-won You, Musarrat Hasan, Manh Cuong Nguyen, Yoon Seok Jeon, Duc-Tai Tong,
Dong-Hwi Lee, Jae Kyoung Jung and Rino Choi
Department of Materials Science and Engineering, Inha University, Incheon 402-751 Rep. of Korea
E-mail : rino.choi@inha.ac.kr

La-incorporated HfO_2 has been attractive candidate for high-k dielectric materials for excellent mobility and ability to modulate threshold voltage [1]. In this work, we have incorporated different thickness of La (4Å to12Å) on top of HfO_2 (20Å). As the gate dielectric is thinner, stress induced gate leakage (SILC) phenomenon is much more enhanced. SILC provides a very sensitive measurement of the defect density. In the stress voltage SILC shows as La thickness increased higher and wider single peak, which indicates that more traps are formed in the dielectric bulk or interface. These traps help electron can move to gate by trap assisted tunneling (TAT). And we also measure time dependent dielectric breakdown (TDDB). As La thickness increased dielectric breakdown time is shorter. It is powerful evidence to conclude that the La incorporation makes electrons can move easily by trap.

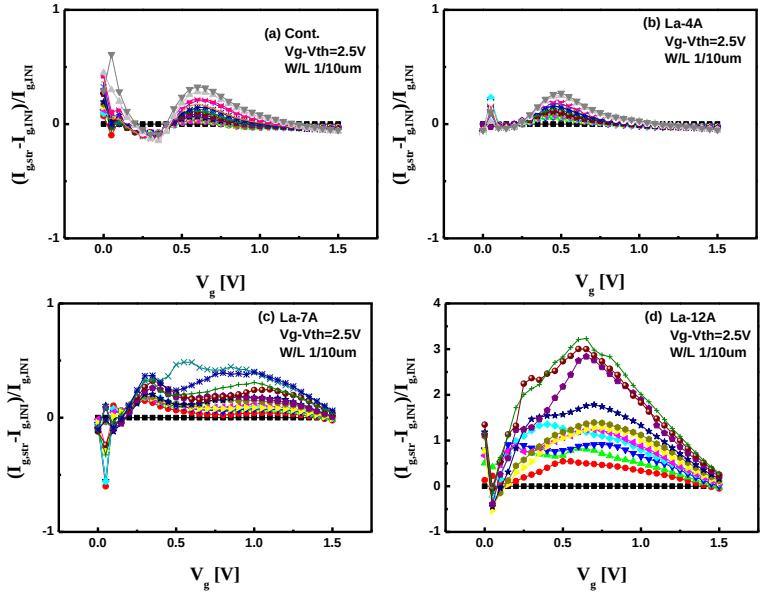

Fig 1. Normalized SILC as a function of V_g for (a) control, (b) La-4Å, (c) La-7Å and (d) La-12Å

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A study on the enlargement of the plasma reactor using a global model

Dong-Hwan Kim[1], Young-Kwang Lee[2], and Chin-Wook Chung[2*]
[1]*Department of Nanoscale Semiconductor Engineering, Hanyang University, Seoul 133-791, Korea*
[2]*Department of Electrical Engineering, Hanyang University, Seoul 133-791, Korea*
[*]E-mail: joykang@hanyang.ac.kr

In various semiconductor manufacturing processes, such as etching and deposition, the electron temperature, the plasma density, and their uniformity are the most important plasma parameters because they influence the discharge properties and the processing results. Due to their importance, studies of the measurement and prediction of the plasma parameters have been a research focus. The global model, developed by Lee and Lieberman [1], is the simplest and most widely used to predict the tendencies of the plasma parameters at various discharge conditions. Recently, many researches and developments concerning the 450mm wafer processing have been done to enhance the throughput in semiconductor manufacturing. To enlarge the wafer size, plasma reactor must be scaled up. However, this change causes variations of the plasma parameters and gas residence time that are directly related to neutral gas composition. To maintain these parameters as the reactor-size increases, accurate control of the external variables, such as the input power, gas pressure, and flow rate, is required. The external variables were calculated through the global model including multistep ionizations. The obtained results from the global model were compared with the experiment for the scale up of the reactor, and they are in good agreement. This can be used as a reference to determine the external variables as the chamber scales up.

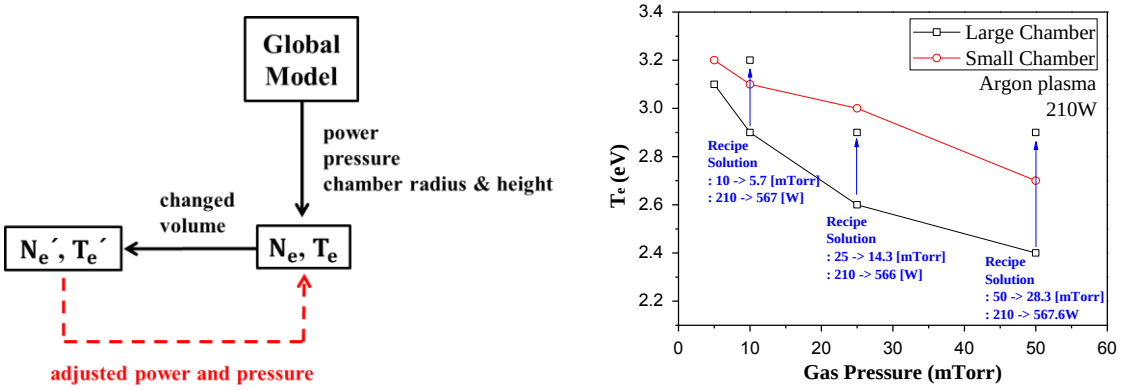

Fig 1. Application of recipe solutions calculated by using a global model

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Conduction mechanism of Metal-Oxide-Semiconductor Field Effect Transistor with La – incorporated Hf based dielectric

Dong-Hwi Lee, Musarrat Hasan, Manh-Cuong Nguyen, Yoon-Seok Jeon, Seung-Won You, Duc-Tai Tong, Jae-Kyoung Jeong, Rino Choi

School of Materials Science and Engineering Inha University, 100 Inharo, Nam-gu, Incheon 402-751, Korea

E-mail : Rino.Choi@inha.ac.kr

Metal-oxide-semiconductor field effect transistors (MOSFETs) with various concentrations of La-incorporated in Hf-based dielectrics were characterized at various temperature range to evaluate the effect of La on device properties. We investigated our experimental data using Poole-Frenkel carrier transport model [1]. From the ln(J/E) vs 1/T plot, we found linear Arrhenius relationship [2]. Generally, the J/E (current density above electric field) values increases with higher concentration of La. It also shows higher values with increasing temperature. To investigate the electrical properties, we used linear equation parameters, the slope for dielectric constant and intercept at y-axis to calculate barrier heights when no electrical field is applied. With La_2O_3 thickness, barrier height increases gradually but dielectric constant decreases rapidly. These parameters can be helpful to understand the dielectric conduction mechanism and electrical properties.

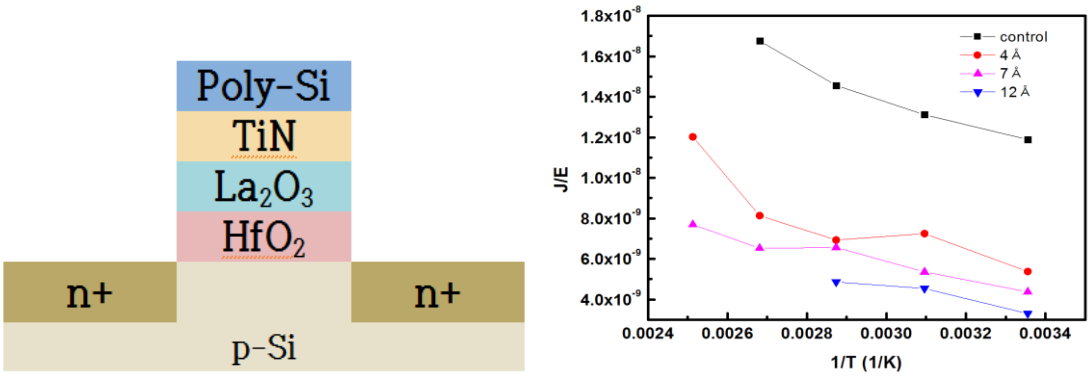

Fig.1 The structure devices and P-F effect data

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Optimization of GZO/Ag/GZO multilayer electrodes obtained by pulsed laser deposition at room temperature

Eunyoung Cheon, Sang Woo Song, Hwan Sun Kim, Dae Hui Cho, Ji Hun Jang, Byung Moo Moon
Department of Electrical Engineering, Korea University,

Transparent Conducting Oxide (TCO) thin film are used as the fabrication of various devices, such as flat panel display, transparent electrodes, solar cell, touch screen, and various optical devices. Recently, ZnO has attracted attention as alternative materials to ITO film due to its abundance in nature, low cost, and excellent transmittance in the visible region. However, ZnO films with high quality could be required either a high substrate temperature during deposition (>300 ° C) [1] or post annealing.[2] To solve this problem, By adding the conductive metal on films can decrease the sheet resistance and increase the mobility of the films at room temperature.[3] In this study, we investigate Ga-doped ZnO/Ag/Ga-doped ZnO (GAG) multilayer structure as a function of the Ag, top and bottom Ga-doped ZnO thickness. Also optimized GAG film is expected to replace ITO film.

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Yong Tae Kim, Ki Hyun Yoon, In-Hoon Choi,
Korea Ceramic Society, Vol 35, No.7, 1998, pp 733-739
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Thin Solid Films, Vol 520, No14, 2012, pp 4666‑4668

Characteristics of Solution Based Oxide TFT with Solution Heating

Sang-A Oh[1], Kyeong Min Yu[1], So-Hyun Jeong[1], Eui-Jung Yun[2], and Byung-Seong Bae[1]
[1]*Department of Display Engineering, Hoseo University, Asan, Chungnam 336-795, Korea*
[2]*College of IT Engineering and System Control Engineering, Hoseo University, Asan, Chungmam 336-795, Korea*
E-mail : bsbae3@hoseo.edu

Recently, research on solution processed oxide thin-film transistors (TFTs) has increased. Solution processed Zinc oxide (ZnO), indium gallium zinc oxide (IGZO) and zinc tin oxide (ZTO) TFTs [1] are most representative. Conventional oxide TFTs have been fabricated by vacuum processes. Vacuum process has disadvantage like high-cost fabrication and complicated process. However solution process has advantage of low-cost fabrication and possible to selective deposition without photolithography. We need outstanding electrical characteristic by solution process similar to vacuum processed oxide TFTs in order to apply the solution processed oxide TFT to the product.

In this paper we fabricated solution at the different heating temperature. We measured characteristics of oxide TFTs and compared properties of solution processed oxide TFTs. Active layer is coated on the top of a 300 nm thick SiO_2 gate dielectric layer thermally-grown on a doped p-type Si wafer. After mixing solute and solvent, precursor solution was heated at different temperature. The prepared solution was filtered through a PTFE syringe filter and spin-coated on prepared wafer. Then prebake was carried out at 100℃ for 1 min 30 sec and annealed at 600℃ for 1 hour. The 100 nm thick Al source/drain electrode was thermally evaporated with a shadow mask.

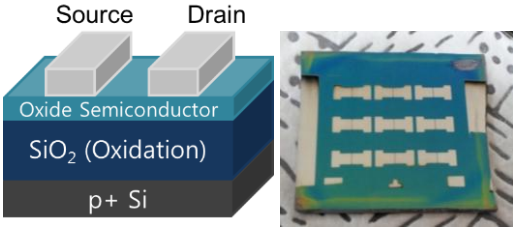

Fig 1. Solution processed oxide TFTs structure.

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A Study of Advanced Al RDL Development

Koeun Cheon, Yonji Park, Yongkuk Kim, Sungwon Yoon, Sangjae Kim, Minki Son, Junhyun Cho, Pilsoon Bae, Jaesung Oh, Jaemyun Kim, Kwangyoo Byun
SK hynix, 2091 Gyeongchung-daero Bubal-eub Icheon-si Gyeonggi-do, Korea
E-mail : koeun.cheon@sk.com

본 논문은 Aluminum(Al) 박막에 대한 기술 연구를 통해 Wire Bondability 와 Reliability 를 만족하는 Al RDL 개발을 목적으로 한다. Al RDL 은 PVD 방식으로 Al 박막을 wafer 전면에 증착하고, PR photo 공정으로 masking 한 뒤 wet-etch 방식으로 각각의 개별 배선으로 isolation 하는 방식으로 제작하였다. 단, PVD 방식으로 RLC 값을 만족하는 1um 이상 두꺼운 두께의 배선을 형성을 위해서는 박막 증착 시 온도에 대한 제어가 중요하며, 이에 대한 평가를 진행하였다. 또한 Al 박막 열처리를 진행함으로서 박막의 접합특성을 개선할 수 있었다. 이를 통해 적합한 wire to pad connectivity 를 확보 뿐 아니라 Moisture sensitivity level 2a 에 상응하는 85ºC/85%R.H, 48hours, T/C -55℃/125℃ 500cycle 및 Hast 168hrs 의 신뢰성 조건을 만족하는 결과를 얻었다

Effect of ALD grown aluminum oxide film on the IGZO TFT

Heeok Kim[1], Jong-Heon Yang, Sung Haeng Cho, Minki Ryu, Jae-Eun Pi, Jong-woo Kim,
Oh Sang Kwon, Eun Suk Park, Chi-Sun Hwang, and Sang-Hee Ko Park*
Oxide TFT Research Section, Electronics and Telecommunications Research Institute, Korea
E-mail : istoo85@etri.re.kr [1] shkp@etri.re.kr *

Recently, Al_2O_3 thin film deposited by ALD has attracted much attendtion as the gate insulator and passivation film of the oxide TFT because of its good quality and high barrier properties, respectively. Alumina deposited using water precursor, however, contains hydrogen which induce carrier increase in the active layer. In addition, rather high mobility of oxide TFT adopting alumina film as the gate insulator needs oxygen supply during high temperature thermal annealing to show well behaved TFT performance.

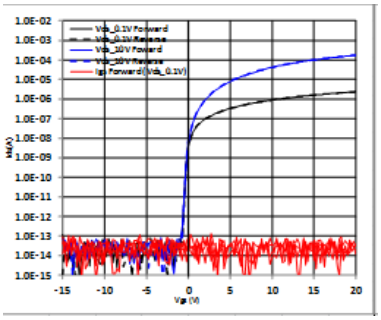
To investigate and confirm the effect of the aluminum oxide film as the passivation layer and gate insulator on the IGZO TFT, we fabricated the IGZO TFT of which structure was coplanar-bottom gate and bottom contact.

150nm thick Indium-Tin-Oxide galss was used for the substrate and gate eletrode. Gate insulator was Al2O3 deposited by Atomic Layer Deposion at 150℃ and ITO was deposited as the source/drain electrode by RF sputter. IGZO was deposited by sputter as active layer. Al2O3 deposited by ALD using water was covered as the passivation layer.

While the nude TFT annealed under vacuum at 300°C has good electriacl properties, that with aluminnum oxide as a passivatin film shows conductive characteristic as shown in fig.1and 2. We suspect hydrogen diffusion from the gate insulator of alumina at elevated temperature, which could not diffuse out due to the high barrier property of the alumina passivation film.

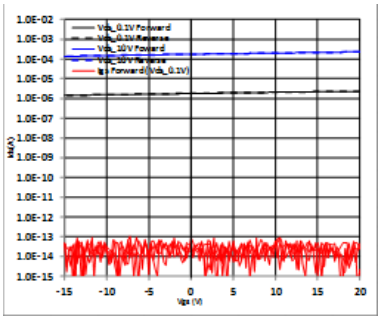
We will present the effect of deposition temperature of Al2O3 by ALD as the gate insulator on the oxide TFT performance to clarify the origin of TFT performance passivated by Al2O3.

<fig. 1>



as fabricated

<fig. 2>



as passivated using Al2O3

Suppression of current collapse effect by insertion of Mo on Ni/Au based schottky contacts in AlGaN/GaN HEMT

Su-Keun Eom, Neung-Hee Lee, Kwang-Seok Seo*
Department of Electrical and Computer Engineering, Inter-university Semiconductor Research Center, Seoul National University, Seoul 151-742, Republic of Korea
E-mail : ksseo@snu.ac.kr

AlGaN/GaN HEMTs have superior properties for high power application. However, current collapse effect prevents its potential by reducing the drain current and increasing the knee voltage. Many studies have been done to solve this problem and they are usually focused on surface passivation or epilayer design and growth. In this research, we propose a new approach to reduce current collapse effect by changing the gate metal stack. Recently, suppression of current collapse by using TiN gate [1] and reliability study by comparing pulse characteristics of Ni/Au and Mo/Au [2] was already observed. We thought modification of the Ni-based schottky metal would also suppress the current collapse effectively without changing the bottom metal unlike ohter studies. Our devices were fabricated in the same steps, only altering the gate metal. Both conventional Ni/Au (40/200 nm) and suggested Ni/Mo/Au (30/10/200 nm) schottky contact were annealed at 400 ℃ using a furnace.

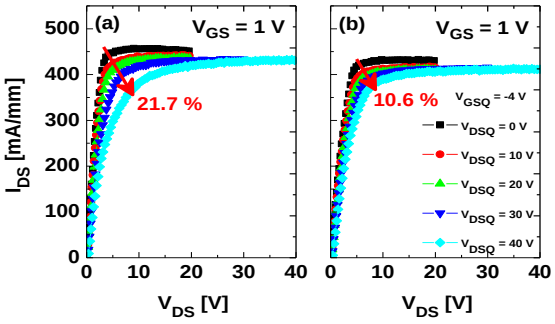
Table I shows the overall results of the measurement. Comparing with the reference, insertion of Mo showed no noticeable effect in DC performance. It resulted in similar transconductance and gate leakage current. On the other hand, significant improvement in pulsed I-V characteristics was measured. Current discrepancy has decreased considerably from 21.7 % to 10.6 %. Figure 1 shows how Mo insertion has effectively reduced the current collapse effect. We could obtain better suppression of current collapse without degradation of other DC characteristics by using the suggested metal stack. This result can be explained in several ways. One explanation is that, through annealing process, the Ni diffusion may eliminate the existing interface states, in the meanwhile, inducing new ones due to thermal stress. Thus, Mo may help reducing the thremal stress leading to better interface. Another explanation is that Ni and Mo may react, and Ni-Mo alloy may create a smoother interface resulting in less interface trap. The exact mechanism needs to be studied further. As a conclusion, through optimization of the ratio of insertion metal with appropriate annealing, current collapse phenomenon can be more reduced.

TABLE I. PROPERTIES OF DIFFERENT GATE METAL STACK

	Ni/Au (40/200 nm)	Ni/Mo/Au (30/10/200 nm)
$G_{m(max)}$ [mS/mm]	112	110
I_G [A/mm] @V_G=-100V	1.37E-07	1.27E-07
Current discrepancy	21.7 %	10.6 %

Current discrepancy was defined between I_{DS} at V_{DS} = 5 V, V_{DSQ} = 0 V and I_D at V_{DS} = 7.5 V, V_{DSQ} = 40 V

Fig. 1. Pulsed I-V characteristics of (a) Ref. (b) Ni/Mo/Au



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Acknowledgements

This work was supported by the IT R&D program of MSIP/KEIT. [10035173, Research on the Class-S base-station power amplifier technology for future mobile communications]

Improvement of Device Characteristic on Solution-Processed InGaZnO Pseudo Metal-Oxide-Semiconductor Field-Effect-Transistor using microwave annealing.

Sung-Wan Moon, Ja-Gyeong Gu, and Won-Ju Cho
Department of Electronic Materials Engineering, Kwangwoon Univ., Seoul, Korea
E-mail : mswkang@naver.com

최근, 비정질 산화물 반도체 thin film transistor (TFT)는 차세대 투명 디스플레이로 큰 관심을 받고 있으며 많은 연구가 진행되고 있다. 이러한 비정질 산화물 반도체 TFT 는 기존의 비정질 실리콘 TFT 에 비하여 높은 이동도와, on/off 전류비 그리고 낮은 subthreshold swing 값을 가지며 차세대 투명 디스플레이 산업에 적용 가능하다는 장점이 있다 [1]. 한편 기존의 고진공 증착 을 이용한 방식은 우수한 막의 특성에도 불구하고 많은 시간과 제작비용이 든다는 단점을 가지고 있다. [2]. 따라서, 최근에는 대면적화에도 유리하다는 장점을 가진 스핀코팅이나 잉크젯 방식을 이용한 용액공정 방식이 개발되고 있다. 하지만, 용액공정을 이용한 증착 방식은 높은 열처리 온도가 필수적이며, 이는 유리 기판과 플라스틱 기판에 적용하는 것이 적합하지 않다. 따라서, 본 연구에서는 전기적 특성 평가가 용이한 pseudo-MOSFET 구조에서 용액공정을 이용한 a-IGZO 채널에 microwave 열처리를 하여 열처리 온도에 따른 전기적 특성을 평가하였다. 열처리 조건으로는 conventional thermal 열처리의 경우, furnace 를 이용하여 500℃ 에서 30 분 동안 N_2 가스 분위기에서 열처리를 실시하였고, microwave 열처리는 microwave irradiation 장비를 이용하여 각각 200℃, 250℃, 300℃, 에서 30 분 동안 N_2 가스 분위기에서 열처리를 실시하였다. 그 결과, furnace 를 이용하여 열처리한 소자와 비교하여 microwave 를 통해 열처리한 소자에서 swing(SS), on/off (Ratio), mobility 등이 개선되는 것을 확인하였다. 따라서, microwave 열처리 공정은 향후 저온 공정을 요구하는 TFT 제작에 있어서 훌륭한 대안으로 기대된다.

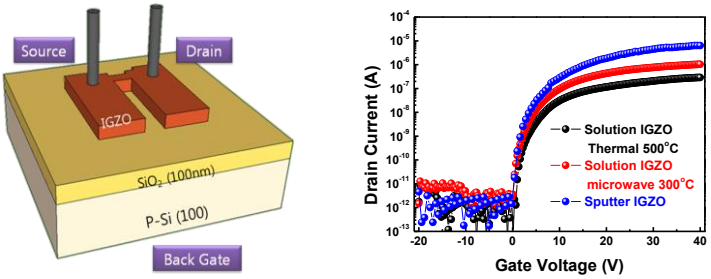

그림 1. Conventional furnace 와 microwave 열처리에 의한 용액공정 기반 IGZO pseudo-MOSFET 의 전달 특성과 sputtering system 을 이용하여 증착한 IGZO pseudo-MOSFET 의 전달 특성 비교.

[1] E. M. C. Fortunato et. all,, Adv. Mater. 17, 590 March (2005).

[2] Seok-Jun Seo et. all, J. Phys. D: Appl. Phys. 42 (2009) 035106 (5pp), December (2008).

Acknowledgment

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Effect of baking temperature on device characteristics in TFT based solution-processed amorphous ZnSnO

Kwang-Won Jo, Young-Hyun Hwang and Won-Ju Cho
Department of Electrical Material Engineering, Kwangwoon University, Seoul 151-747, Korea
E-mail : chowj@kw.ac.kr

최근에 차세대 디스플레이 소자로 각광받고 있는 AM-OLED(active matrix-organic light emitting diode)의 구동회로를 구성하기 위한 소자로서 oxide semiconductor 를 이용한 TFT(thin film transistor)가 큰 주목을 받고 있다. 특히, TFT 의 채널층을 형성하는 방법 중에서 기존의 고진공 장비를 이용한 박막 형성보다는 용액 공정을 이용한 방법이 대면적화, 경제성 측면에서 유리하며 또한 공정과정이 간단하다는 장점을 가지고 있기 때문에 많은 관심이 집중되고 있다. 그러나, 용액 공정으로 형성된 박막에는 프리커서 및 솔벤트에 기인하는 OH 및 탄소 등의 불순물이 다량으로 포함되어 소자의 전기적 특성 열화를 초래하기 때문에 수분 및 탄소결합 불순물들을 효과적으로 제거하기 위한 baking 과정이 필수적이다[1]. 따라서, 본 연구에서는 용액 공정 중의 baking 조건이 용액 기반 ZTO(Zinc-Tin-Oxide) TFT 의 전기적 특성에 미치는 영향에 대하여 연구하였다.

먼저, p-type Si 위에 gate oxide 로 건식산화방식으로 성장한 SiO_2(100 nm)위에 Zn 과 Sn 의 조성비를 1:1 의 비율로 만든 용액 precursor 을 이용하여 spin-coating 방식으로 ZTO 박막을 형성하였다. 그리고, baking 과정으로 180~250 ℃ 의 온도 범위에서 10 분 동안의 열처리를 실시하였다. Furnace 를 이용하여 O_2 기체 분위기에서 600℃ 로 30 분 동안 후속 열처리를 실시하고 S/D 금속전극을 형성하여 전기적인 특성을 평가하였다.

그 결과, 600℃ 의 고온에서 동일한 후속 열처리를 거쳤음에도 불구하고 baking 과정에서의 온도(180~250℃)에 의해 소자의 mobility, hysteresis 등의 전기적 특성에 큰 차이를 발견하였다. ZTO TFT 소자의 전기적 특성은 수분 및 solvent 가 decomposition 되는 baking 온도가 낮을수록 높은 구동 전류와 양호한 hysteresis 특성을 보였으며, 이는 baking 과정에서 발생되는 ZTO 채널 내의 결함과 관련이 있는 것으로 판단된다.

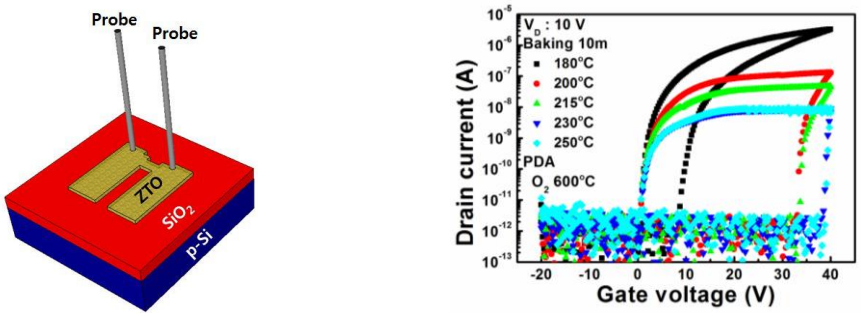

그림 1. 소자의 구조와 baking 과정의 온도변화에 따른 ZTO TFT 의 전달특성.

[1] S. Jeong, Y. Jeong and J. Moon, J. Phys. Chem.Lett. **4**, 11082(2008)

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This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (No. 2013R1A1A2A10011202).

선택적 리세스 게이트 소자의 공정 및 특성 분석

김정진 [1)2)], 박영락 [1)], 고상춘 [1)], 문재경 [1)], 장우진 [1)], 장우영 [1)], 배성범 [1)], 양전욱 [2)]
[1)]한국전자통신연구원, [2)]전북대학교 반도체화학공학부
E-mail : kjj_jin@etri.re.kr

본 연구에서는 AlGaN/GaN HEMT 에서 고 항복 고 전류 전력소자로서 동작하기 위한 필수 조건인 고항복전압, normally-off 특성, 대전력 구동을 만족 하기 위하여 전체 게이트 길이 중 일부만 선택적으로 리세스 식각한 구조의 소자를 제작하였다. 선택적 리세스 식각에 의해 넓은 게이트 면적과 좁은 리세스 영역을 형성함으로써 높은 온-전류와 높은 항복전압 그리고 normally-off 특성을 최대한 동시에 나타날 수 있도록 설계하였다. 또한, 표면 누설전류 및 전류 붕괴 현상을 완화하기 위하여 소스 접촉 필드플레이트를 적용하였다. 제작된 소자는, 1.5V 이상의 문턱전압을 가지며 500 mA/mm 이상의 온 전류를 보였다. 항복 전압은 게이트-드레인 간격이 20 μm 일 때 1100 V 이상으로 나타났다. 소스 접촉 필드플레이트가 적용된 소자에서 필드플레이트가 없는 소자에 비해 3~4 배 더 낮은 게이트 누설전류가 흐르는 것이 확인되었다. 필드플레이트 공정 전의 소자는 게이트 전압 인가 방향에 따라 수백 mA/mm 크기의 전류 붕괴가 발생하였다. 이는 소자 표면의 전기적 trap 들에 의해 가상 게이트가 형성되었기 때문으로 생각된다. 소자의 전류 붕괴 현상은 필드플레이트 공정을 위한 SiN_X 증착 후에 거의 완화되었다.

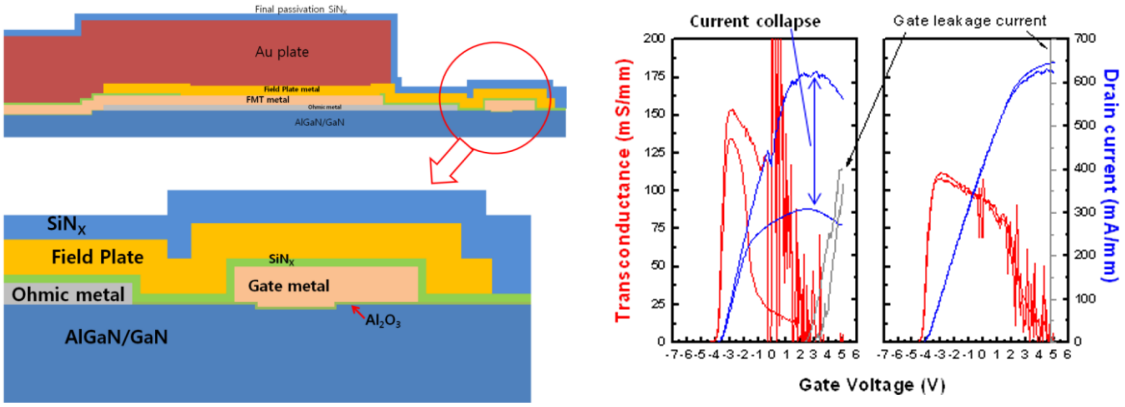

Fig 1. Fabricated HEMT device structure and recovery of current collapse

Electrical Characteristics and Instability of Solution-Derived An-Zn-Sn-O Thin-Film Transistors

Yeong-Hyeon Hwang and Won-Ju Cho
Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
E-mail: chowj@kw.ac.kr

Oxide thin film transistors have attracted the driving device of active-matrix OLED due to its superior characteristics of high mobility, transparency in the visible region, good uniformity, and compatibility with present display industry. Above all, rare elements-free An-Zn-Sn-O (AZTO) material is considered to be the promising candidates for the next generation display technologies [1]. In this study, we have fabricated junctionless type thin-film transistors (TFTs) with the AZTO active layer solution derived at room temperature. The film's composition of Zn:Sn was fixed 1:1 while Al moles were varied by using solution method.[2] When the mole of Al is 0.2, a field effect mobility was faster. Also, we observed instability of the solution AZTO TFTs with double sweep and gate bias stress [3]. The optimized solution AZTO TFT, which is 0.2:1:1 for Al:Zn:Sn, exhibited a mobility of 0.85 $cm^2/V{\cdot}s$, on/off ratio of over 10^6, and subthreshold swing of 0.5 V/decade.

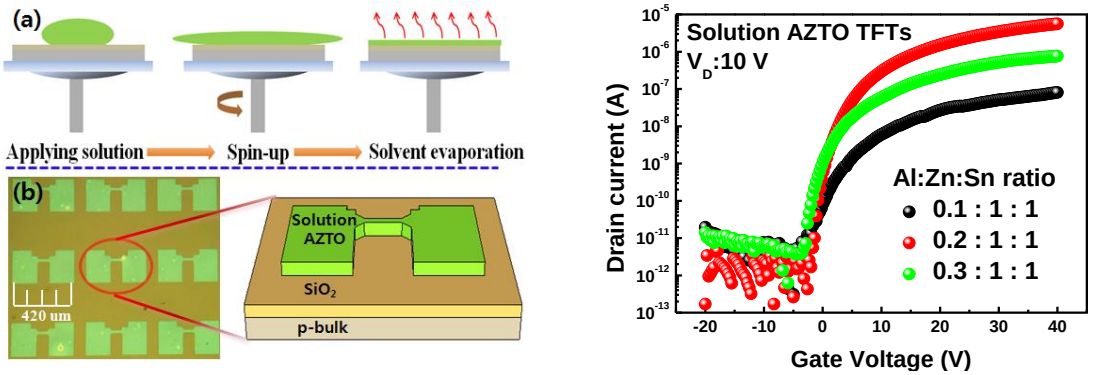

Fig 1. Schematic cross section of (a)spin coating process, (b)device structure with solution process and transfer characteristic of solution AZTO TFTs

[1] D.-H. Cho, S. Yang, C. Byun, J. Shin, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, S. M. Chung, W.-S. Cheong, S. M. Yoon and H.-Y. Chu, Appl. Phys. Lett., **93**, 142111 (2008)

[2] K.-S. Kim, S.-W. Lee, S.-M. Oh, W.-J. Cho: Mater. Sci. Eng. B. **178** (2013) 811

[2] T. Kamiya, K. Nomura, and H. Hosono, Sci. Technol. Adv. Mater. **11**, 044305 (2010)

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Systematic Analysis of Electrical Traps at Surface, AlGaN Barrier, and GaN Buffer of AlGaN/GaN HFET Device

Seung Yup Jang[1], Jong-Hoon Shin[1], Myeong-Kyu Eo[2], Hyo-Seung Choi[2], Hyuck-In Kwon[2], and TaeHoon Jang[1+]

[1]*IGBT part, System IC R&D Laboratory, LG Electronics, Seoul, Korea*

[2]*School of EEE, Chung-Ang University, Seoul, Korea*

[+]E-mail : th.jang@lge.com

AlGaN/GaN heterostructure field effect transistors (HFETs) have recently recognized as an excellent candidates for high power applications due to their superior properties such as high breakdown field and high 2-D electron gas density. However, current collapse effect of AlGaN/GaN HFET on Si is still critical problem which needs to be overcome for successful commercialization [1]. In this presentation, systematic analysis of the electrical traps at surface, AlGaN barrier, and GaN buffer of AlGaN/GaN/Si HFETs will be introduced. Since the traps could be located at the surface and layer of AlGaN/GaN device, it is very important to know their location, density, and finally, effect on the current collapse. To detect the location and density of traps, measurement approach using simple device geometry (Schottky diode, TLM pattern, etc.) has been developed. The effects on current collapse were precisely investigated by dynamic on-resistance analysis. Enhanced-mode (normally-off) AlGaN/GaN HFETs were fabricated and measured with our circuit for dynamic test. Systematic analysis of the trap-measurement results and dynamic performance will be discussed.

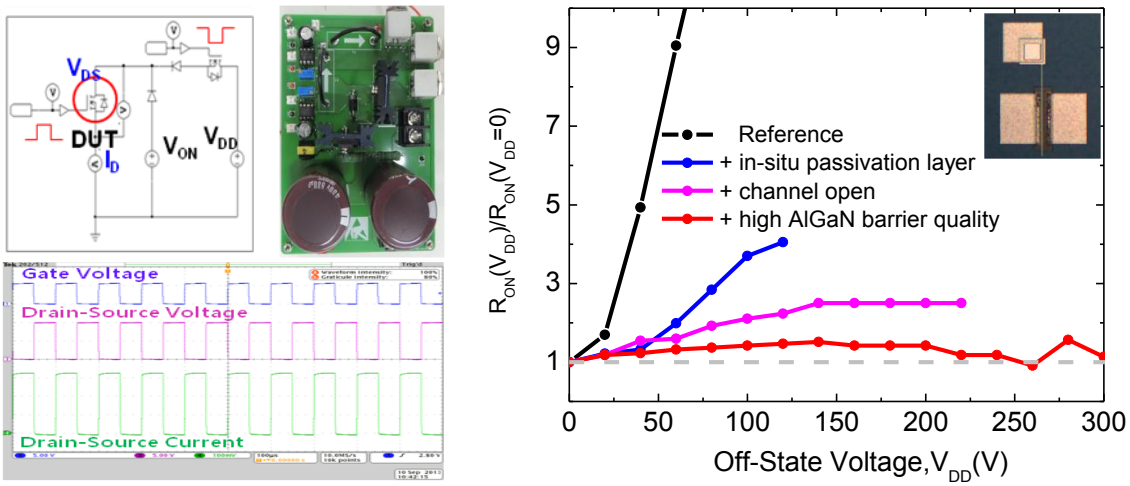


Fig 1. Circuit for dynamic test [2] and measured results for various E-mode AlGaN/GaN HFETs

[1] M. Tajima and T. Hashizume, Jpn. J. Appl. Phys. 50, 061001 (2011).

[2] J.-H. Shin, S. Y. Jang, and T. Jang, poster (PS-6-10) presented at SSDM 2013.

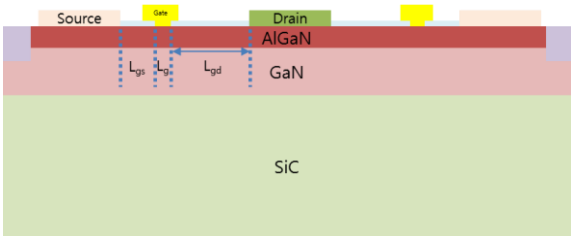
RF characteristics of GaN on SiC for different device topology

Youngrak Park, Woojin Jang, Sangchoon Ko, Jungjin Kim, Wooyoung Jang, Sungbum Bae, Jongwon Lim, Hogyun Ahn, Jaekyung Mun

GaN Power Electronics Research Section, Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea

E-mail : raferer@etri.re.kr

GaN-based high electron mobility transistors (HEMTs) are promising devices for high power and high frequency applications. A lot of research pay much attention to millimiter wave GaN devices [1]. We investigated the feasibility of fabrication of GaN devices for millimeter wave by implementing different types of device layout. After Ti/Al based Ohmic contacts were performed, 100 nm SiN were deposited. 500nm gate length was developed by stepper lithography, and gate length of 250 nm was patterned for high frequency device and by using e-beam lithography. SiN was etched by using CF_4 based gas, followed by Ni/Au (30/350 nm) metal stack deposition. The metals were annealed at 350℃ for 5 min for thermal stabilization and post gate annealing process. Device name S correspond to 0.5um gate length device and X for 0.25um. DG2 means the length between gate and drain is 2um instead of 4um for normal devices. Fig 1 shows the RF performance of above-mentioned devices. For X device has around 20GHz better f_{max} than S device. We improved 10GHz f_{max} by narrowing the length between drain and gate. It does not suffer by comparison with T-gate sharped device shown in Fig 1. This study will be helpful in understanding the RF performance of GaN on SiC device for various device layout and also possibility for using millimeter wave GaN device.



ID	Vg	f_T	f_{max}
SO200	-1.6	17.74	55.16
SO200_DG2	-1.6	18.51	60.23
XO200	-2.6	41.29	78.03
XO200_DG2	-2.6	44.62	85.08
XO200(T-gate)	-2.6	36.3	93

Fig 1. RF performance of different types of device layout

[1] D. Marti, et al., IEEE Electron Device Letters, vol. 33, no. 10, pp. 1372–1374, 2012.

에피텍셜 방법으로 성장된 In-situ SiN 의 surface trap 감소 효과 연구

조성무, 황의진, 김재무, 김준호, 장태훈
LG 전자 System IC 연구소 IGBT part
E-mail : th.jang@lge.com

AlGaN/GaN HFET 에서 AlGaN 표면에 존재하는 surface trap 은 current collapse 를 일으키는 주요한 원인중에 하나이다[1]. 본 연구에서는 MOCVD (Metal Organic Chemical Vapor Deposition) 를 이용하여 HFET 구조위에 in-situ SiN 로 passivation 된 샘플과 외부장비를 이용하여 passivation 된 샘플을 소자로 제작 후에 dynamic Ron 에 미치는 영향을 조사하였다[2]. HFET 구조위에 60nm 두께로 성장된 in-situ SiN 의 Hall 측정을 통해 in-situ SiN 로 passivation 된 샘플의 경우 sheet carrier density 가 SiN 가 없는 샘플에 비해 40% 높아진 것을 확인하였다. 이는 상온으로 냉각시에 AlGaN 층이 아래 GaN 와 격자상수 차에 의해 relaxation 이 발생하는 것을 SiN 가 막아주어 AlGaN 이 가지고 있는 strain 을 유지시켜주기 때문이다. 또한 고온에서 성장된 in-situ SiN 는 다른 SiO2, HfO2 등의 절연막에 비해 절연특성이 ~100 배 정도 낮게 측정되었다. In-situ SiN 를 적용하여 제작한 HFET 의 dynamic Ron 을 측정한 결과 200V 에서 1.5 이하로 in-situ SiN 를 적용하지 않은 샘플에 비해 4 배 이상 개선됨을 확인하였고, 이것은 in-situ SiN 가 공기중의 산소 또는 공정에서의 수분과의 접촉으로 인해서 발생하는 AlGaN 표면의 산화를 차단 함으로서 surface trap 을 감소시켜 current collapse 을 억제시킨 것으로 보인다[3].

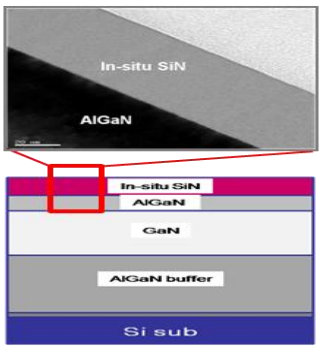


그림 1. HFET 성장 구조 및 TEM 단면사진

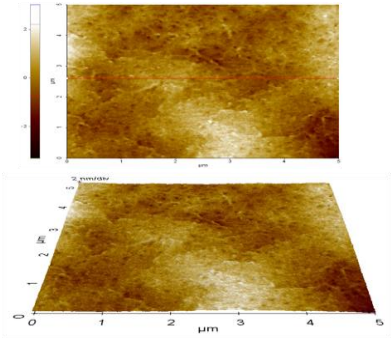


그림 2. AlGaN 위에 성장된 In-situ SiN 의 AFM 표면사진

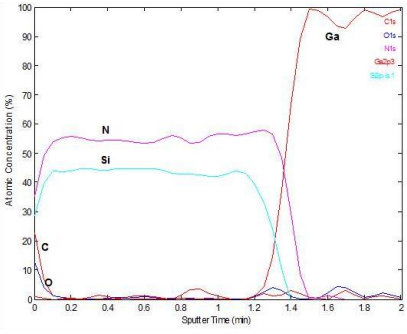


그림 3. In-situ SiN 의 XPS 성분분석 그래프

[1] R. Vetury, N. Zhang, S. Keller, and U. Mishra, IEEE Trans. Electron Devices, Vol. 48, pp. 0018-9383(01) (2001).
[2] HY. Ko, JH. Park, HJ. Lee, YJ Jo, MS. Song, and T. Jang, Solid State Devices and Materials (SSDM) presented (2013).
[3] Miao MS, Weber JR, Van de Walle CG, J. Appl Phys. 107, 123713 (2010).

Structural Optimization of Field-Plated Normally-off AlGaN/GaN-on-Si MOSHFETs

Jae-Gil Lee, Bong-Ryeol Park and Ho-Young Cha*
School of Electronic and Electrical Engineering, Hongik University, Seoul 121-791, Korea
*E-mail : hcha@hongik.ac.kr

Field plate structures are typically employed to further improve the breakdown voltage of AlGaN/GaN HFETs. In this study, we fabricated normally-off AlGaN/GaN-on-Si recessed MOSHFETs for high breakdown voltage where both a gate overhang length and a source field plate length were varied for structural optimization. The breakdown voltage obviously increases, including a source field plate as well as a gate overhang. It was observed in our simulation study using Silvaco ATLAS that the gate overhang was enough to suppress the high electric field at the gate edge and also the source field plate distributed the electric field at the gate overhang edge. In comparison with the optimized gate overhang structure, the breakdown voltage of the device fabricated using the optimized source field plate structure was improved by 19.7%. There is no significant different between two devices in the on-resistance(5.58 mΩ-cm^2). The breakdown voltage of 1015 V was achieved for the gate-to-drain distance of 12 μm in which the gate overhang length and source field plate length were 1 μm and 2 μm, respectively.

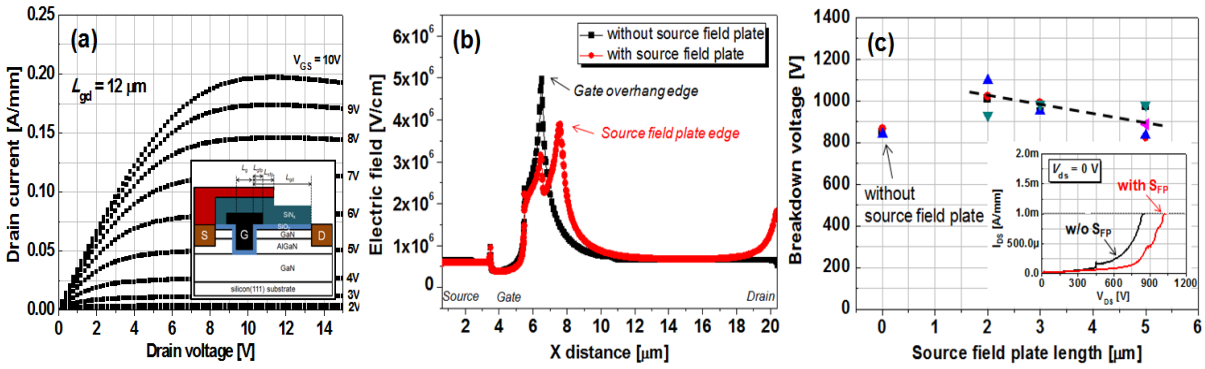


Fig 1. (a) Current-voltage characteristics of the normally-off device with a source field plate, (b) Electric field distribution along the 2DEG channel at high drain bias, (c) Measured breakdown voltage characteristics as a function of source field plate length.

[1] J.-G. Lee, B.-R. Park, H.-J. Lee, M. Lee, K.-S. Seo, and H.-Y. Cha, Appl. Phys. Expr, **5**, 066502 (2012).

Acknowledgements This work was supported by the 'Energy Efficient Power Semiconductor Technology for Next Generation Data Center' IT R&D project (No. 10038766) of MKE/KEIT.

Effect of basal-plane stacking faults on X-ray diffraction of nonpolar *a*-plane GaN films

Ji Hoon Kim[1], Sung-Min Hwang[2], Kwang Hyeon Baik[3], and Jung Ho Park[1]

[1]*School of Electrical Engineering, Korea University, Anam-dong, Seoul 136-713, Korea*

[2]*Photonics Convergence Research Center, Korea Electronics Technology Institute, Seongnam 463-816, Korea*

[3]*Department of Materials Science and Engineering, Hongik University, Jochiwon, Chungnam , 339-701, Korea*

E-mail : jhpark@korea.ac.kr

Over the past decade, nonpolar GaN has been a topic of active interest due to the promise of avoiding the polarization-induced built-in electric fields found in quantum well structures grown in polar (0001) orientation. However, heteroepitaxially grown nonpolar GaN films contain a high density of extended defects such as basal-plane stacking faults (BSFs) and dislocations because of in-plane strain anisotropy [1]. We investigated the effect of BSFs on structural properties of *a*-plane (11-20) GaN films with different SiN_x interlayer by using x-ray diffraction (XRD) technique. (11-20) x-ray rocking curves (XRCs) measurements revealed significant reduction in in-plane anisotropy of XRC full width at half maximum (FWHM) in sample with single SiN_x layer. The XRC FWHMs for off-axis planes influenced by the I_1-type BSFs were correlated well with the BSF densities in transmission electron microscopy measurements. Williamson-Hall analysis of ω-scan peak width was also employed to investigate the origin of anisotropic ω-scan peak broadening. We found that the lateral coherence length (LCL) along the *c*-axis in the range of 371 to 479 nm could be obtained for an *a*-plane GaN film with high crystalline quality. This analysis shows that BSFs are a reliable source of XRC FWHM anisotropy in the nonpolar *a*-plane GaN films [2].

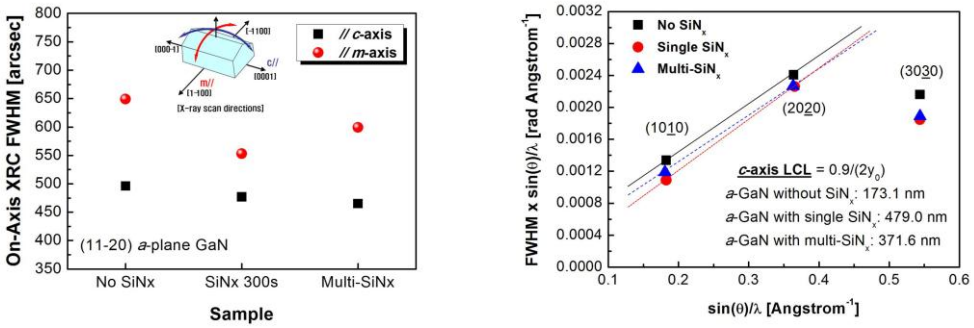


Fig 1. XRD measurements of *a*-plane GaN films with different SiN_x layers: (left) In-plane anisotropy of (11-20) XRC FWHMs. (right) Williamson-Hall plots of (*h*0*h*0) XRC FWHMs.

[1] T. Paskova, Phys. Status Solidi B 245, 1011 (2008).

[2] M. B. McLaurin, A. Hirai, E. Young, F. Wu, and J. S. Speck, Jpn. J. Appl. Phys. 47, 5429 (2008).

Ammonium polysulfide passivation for interface between GaN and atomic-layer-deposited $HfAlO_x$

Donghwan Lim, Woosuk Jung, and Changhwan Choi*
Division of Materials Science & Engineering, Hanyang University, 133-791, Seoul, Korea
E-mail*: cchoi@hanyang.ac.kr

Gallium nitride (GaN) is a wide bandgap semiconductor as an alternative to Si for high power and high temperature electronic devices [1]. However, it has a pontential issue such as interface degradation as a result of Ga and N out-diffusion during process. Therfore, for improving interface quality, ammonium polysulfide ($(NH_4)_2S_x$) passivation was proposed to remove native oxide and improve interface quality for GaN substrate [2]. In this study, we have investigated effects of $(NH_4)_2S_x$ exposure time on the interface properties of the GaN device with nano-laminated atomic-layer-deposited (ALD) HfAlOx dielectric. GaN substrates were treated with $(NH_4)_2S_x$ for 10, 20, and 30 minutes, respectively. Nano-laminated ALD $HfAlO_x$ oxide prepared by tri-methyl-aluminum source and H_2O oxidant and sputtered Ru gate were used for gate dielectric and gate electrode in MOS device, respectively. Atomic force microscope revealed out $(NH_4)_2S_x$ treatment did not degrade the roughness of the surface. From measuring X-ray photoelectron spectroscopy, it was clearly shown that sulfur ions were formed between GaN and $HfAlO_x$ surface. For $(NH_4)_2S_x$-passivated devices, C-V curves with clear accumulation and depletion behaviors were shown with low electrical leakage current density. Compared with the non-passivated (HCl treatment only), the $(NH_4)_2S_x$-passivated showed better C-V characteristics. Frequency dispersion and hysteresis were strongly related with exposure time. Longer time suppressed the frequency dispersion and hysteresis while an accumulation capacitance reduced. A sweet spot was observed with 20 minute. It is concluded that $(NH_4)_2S_x$ is an effective way for GaN passivation, but process such as exposure time and S concentration should be well controlled.

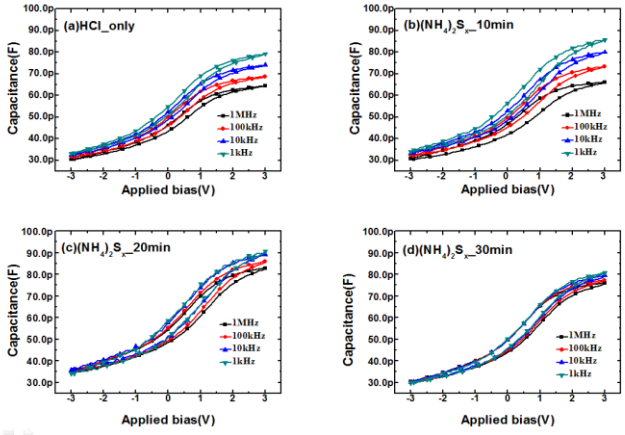


Fig 10. Measured capacitance-voltage curves of each sample

[1] D. Athanasios, G. Evgeni, C.M. Paul, and H. Marc, Springer: Berlin Germany p.230 (2007).

[2] Ching-Ting Lee, Yow-Jon Lin, and Day-Shan Liu, Applied physics letter volume 79, number16 (2001).

This research was supported by Basic Science Research Program through National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0024043)

A study on crystalline ZnTe channel characteristics for thin film transistor device

Yoonki Min, Jonggi Kim, Heedo Na, and Hyunchul Sohn
Department of Materials Science & Engineering, Yonsei University, Seoul 120-749, Korea
E-mail : hyunchul.sohn@yonsei.ac.kr

Recently, Chalcogenide TFTs based on $CuInSe_2$ and SnS_x have received much attention due to relatively high carrier mobilities (> 5 $cm^2/V \cdot s$) in comparison to a-Si and organic thin-film(< 1 $cm^2/V \cdot s$). Zinc telluride (ZnTe), a high mobility(μ_h ~ 340cm^2/vs) semiconductor at room temperature is a promising material for TFT device[1]. In this study, the effect of annealing condition on the crystallinity properties of ZnTe films with various annealing temperature was investigated. In addition, electrical properties of TFT device with ZnTe channel were investigated. ZnTe films were deposited on SiO_2/Si by RF magnetron sputter. Electrical properties of ZnTe film were confirmed by 4 point probe and Hall measurement. Weak diffraction peaks associated with hexalgonal c-Te were observed at annealing temperature 300℃. This results suggest that amorphous Te in ZnTe film was crystallized with increasing post annealing temperature and crystalline phase Te is expected to be affect the carrier concentration of ZnTe. The carrier concentration of ZnTe(n_h ~ $10^{13}/cm^3$) was confirmed by Hall measurement. ZnTe based TFT device shows the p-channel behavior and V_D-I_D curve observed low on current level(<20nA) due to low carrier concentration of ZnTe.

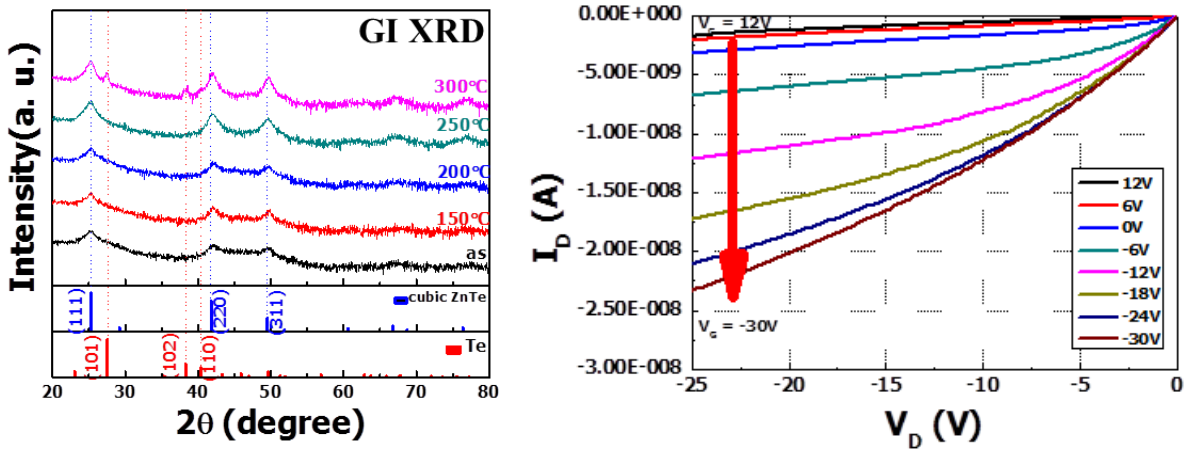


Fig 1. ZnTe physical property and TFT characteristic

[1] R. Ludeke, “A Survey of Optical and Electrical Properties of Thin Films of II–VI Semiconducting Compounds”, J. Vac. Sci. Technol., 8, 199 (1971).

Study of n-contact hole number of via hole vertical LEDs for electrical and optical properties

Chi Gyun Song[1], Hyung-Jo Park[2], Tak Jeong [2], Sang Hern Lee [2] and Joon Seop Kwak[1]
[1] Department of Printed Electronics Engineering, Sunchon National University, Jeonnam 540-742, Korea
[2]LED device team, Korea photonics Technology Institute, Gwangju 500-460, korea
E-mail : jskwak@sunchon.ac.kr

In recent years, Light-Emitting Diodes (LEDs) are widely used in various applications such as traffic signals, backlight module for displays and general lighting. However, insulating substrate used in conventional lateral LEDs have a droop effect, thermal reliability and current crowding problem. Nevertheless, vertical type GaN-LEDs have attracted interest due to their higher light emission efficiency, high-power and uniform current spreading.

In this paper, we report on the fabrication and characterization of GaN–based via hole vertical LEDs with various n-contact hole patterned using one via hole vertical LED and twenty-three via hole vertical LEDs, where n-GaN etching is done using Inductively Coupled Plasma(ICP). Experimental results show that the typical I-V and L-I characteristics of two kinds of via hole vertical LEDs, and the one hole via hole vertical LEDs decrease in the electrical and optical performance, also External Quantum Efficiency (EQE) was performed that one via hole vertical LEDs shows significant reduction in efficiency droop than twenty-three via hole vertical LEDs. Future investigations on the fabrication and characterization of five and eleven hole type vertical LEDs will be carried out to optimize the performance.

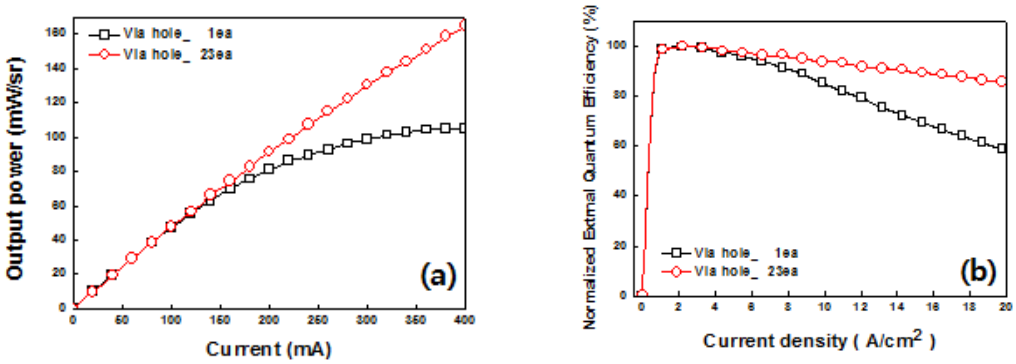


Fig 1. (a)L-I characteristics of the one via hole vertical LEDs and twenty-three via hole vertical LEDs, (b)EQE as a function of current for the two via hole vertical LEDs

Growth of semi-insulating C-doped/undoped GaN multiple-layer buffer

Chul-Ho Won, Sang-Min Jeon, Dong-Seok Kim, Soo-Jin Yu, Hee-Sung Kang, Young-Woo Jo, Do-Kywn Kim, Ryun-Hwi Kim, Dong-Hyeok Son, You-Mi Kwon, Vodapally Sindhuri, Jun-Hyeok Lee, Ji-Hyun Kim, Young-Jo Kim, and Jung-Hee Lee

School of Electronics Engineering, Kyungpook National University, Daegu 702-701, Korea

E-mail : jlee@ee.knu.ac.kr

GaN is very attractive material for power device applications due to its superior properties such as high electric field and wide energy bandgap. However, the semi-insulating (S.I.) (Al)GaN buffer layer must be required for the high breakdown voltage and low leakage current. Several methods, such as defect genaration and carbon (C) or iron (Fe) doping, were developed for growing the S.I. GaN buffer [1-3]. In this study, we have proposed a new S.I. GaN buffer consisting of C-doped/undoped GaN (C-GaN /u-GaN) multi-layers (MLs).

The C-GaN layer in the proposed ML buffer was grown at relatively low temperature of 900 ˚C while the u-GaN layer was grown at normal growth temperature of 1080 ˚C. It is believed that the electrons in the u-GaN layers sandwitched between C-GaN layers transfer to the C-doped layers to compensate deep acceptors in the C-doped layer, which makes the undoped layers fully depleted to increase the resistivity of the layer to extremely high value. As a result, the MLs becomes semi-insulating due to theis charge transfer between the u-GaN and the C-GaN layer. Several MLs were investigated by varying the thickness for the C-GaN from 6 to 25 nm but keeping the thickness of the u-GaN layer at 50 nm. For comparison, a thick single C-GaN layer was grown at 900 ˚C as a reference structure. The resistances of all proposed buffer layers extracted from I-V curve, were ~ 10^{10} Ω except for the buffer with 6 nm-thick C-GaN layer which has much lower resistance of 10^{7} Ω. This smaller resistance is due to the insufficient C doping concentration in C-GaN layer, confirmed by SIMS meausrement (Fig. 1), indicating that the u-GaN layer was not fully depleted. The AlGaN/GaN heterostructure was grown on ML buffers and the electrical properties of 2DEG were summaried in Table 1. The 2DEG properties with 12 nm-thick C-GaN layer was better than those of other structure because the crystalline quality of proposed buffer was degraded by increasing the thickness of C-GaN layer. Compared to the reference buffer layer with a single thick C-GaN layer, the proposed C-GaN/u-GaN MLs exhibited much more improved crystalline quality and 2DEG propoerties while maintaing the S.I. nature.

Table 1. The properties of experimented samples

C-GaN thickness of ML buffer (nm)	Resistance [Ω]	2DEG mobility [cm²/V·s]	2DEG density [/cm²]	FWHM of XRC (002)/(102) [arcsec]
6	~107	-	-	(386)/(667)
12	~10^{10}	1490	1.11 x 10^{13}	(421)/(670)
25	~10^{10}	1320	1.11 x 10^{13}	(441)/(692)
Reference (Thick C-GaN)	~10^{12}	855	8.69 x 10^{12}	(925)/(1550)

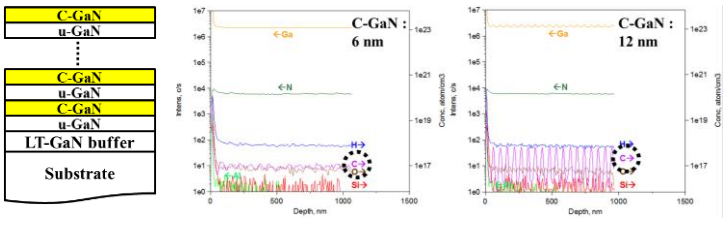


Fig 1. The structure (left) and SIMS results (right) of C-GaN/uGaN MLs buffer

[1] S. M. Hubbard, G. Zhao, D. Pavlidis, W. Sutton, and E. Cho, J. Cryst. Growth, 284, 297 (2010)

[2] S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, Appl. Phys. Lett., 81, 439 (2002)

[3] S. Katp, Y. Satoh, H. Sasaki, I. Masayuki, and S. Yoshida, J. Cryst. Growth, 298, 831 (2007)

Suppression of current collapse in AlGaN/GaN MISHFET with a novel buffer structure

Young-Jo Kim, Hee-Sung Kang, Dong-Seok Kim, Young-Woo Jo, Do-Kywn Kim, You-Mi Kwon, Dong-Hyeok Son, Ji-Hyun Kim, Jun-Hyeok Lee, Young Jun Yoon, Yong Soo Lee and Jung-Hee Lee
School of electronics engineering, Kyungpook National University, Daegu 702-701, Korea
E-mail : jlee@ee.knu.ac.kr

AlGaN/GaN HEMTs for high power and high frequency applications require a semi-insulating (S.I.) (Al)GaN buffer having a high resistance to minimize the buffer leakage current. However, at the high drain bias, channel electrons are injected into S.I. GaN buffer to be trapped, which would occasionally cause severe current collapse [1]. In this paper, we have proposed a novel GaN buffer structure which consists of carbon-doped (C-GaN)/undoped (u-GaN) multiple-layers (MLs) instead of conventional thick C-GaN buffer layer. The new buffer structure effectively suppresses the current collapse of the device. The AlGaN/GaN MISHEMTs with two different buffer structures were fabricated on sapphire substrate. The buffer layer structures were grown as follows; one for 1.3 um-thick C-GaN layer and the other for C-GaN (25 nm)/u-GaN (50 nm) MLs with total thickness of 2 um. The defined gate length and width of the devices are 3 and 50 μm, respectively.

Fig. 1(a) shows the I_{DS}-V_{DS} characteristics of AlGaN/GaN MISHEMTs with C-GaN buffer layer. As the drain bias increased to 100 V, severe degradation in on-resistance of the device was observed due to electron trapping into the C-GaN buffer layer. On the other hand, C-GaN/u-GaN MLs buffer shows negligible current collapse up to the drain voltage of 100 V as shown in Fig. 1(b). Fig. 2 describes a model which explains the suppressed current collapse in the proposed buffer structure. The electrons from u-GaN layers effectively compensate the deep acceptors in C-GaN layer before the channel electron current flows, preventing the channel electron from being trapped into the deep acceptor states. In conclusion, the proposed model and experimental results indicate that the C-GaN/u-GaN MLs buffer structure very effective in suppressing the current collapse.

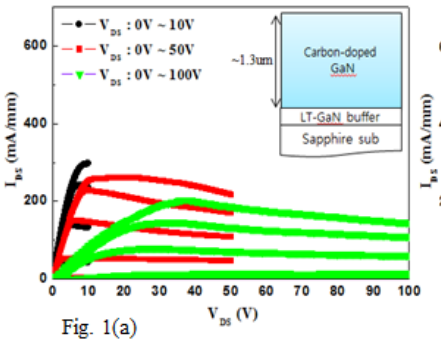


Fig. 1(a)

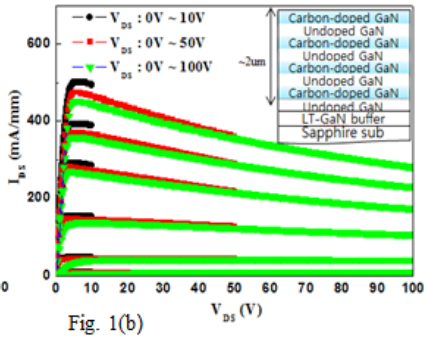


Fig. 1(b)

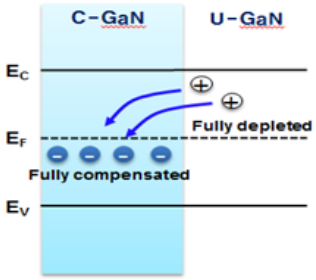


Fig. 2

Fig. 1 I_{DS}-V_{DS} characteristics of MISHEMTs with different buffet structure. (a) C-GaN buffer, (b) C-GaN/u-GaN MLs buffer.
Fig. 2 Proposed model of C-GaN/u-GaN MLs

[1] S.A. Chevtchenko, E. Cho, F. Bahat-Treidel, and J. Wurfl, Appl. Phys. Lett., 100, 223502 (2012)

Characteristics of AlGaN/GaN HEMTs on SiC with Pt-based Schottky Contacts

Hyung Sup Yoon, Byoung Gue Min, Ho Kyun Ahn, Jong Min Lee, Dong Min Kang, Sung Il Kim, Chul Won Ju, Hae Cheon Kim, and Jong Won Lim

RF Convergence Components Research Section, IT Components & Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea

E-mail : hsyoon@etri.re.kr

AlGaN/GaN HEMTs on SiC have attracted a lot of attention owing to their promising advantages in high power and high frequency applications. The widely used Ni-based Schottky contacts are subjective to degradation under extremely operating conditions[1-2]. In this work, we fabricated the AlGaN/GaN HEMTs on SiC with 0.17 µm T-shaped gate using Schottky contacts of multi-layered Pt/Ti/Pt/Au. The HEMT epitaxial layers consisted of a thick buffer, 2 µm GaN, a 25 nm undoped $Al_{0.25}Ga_{0.75}N$ Schottky layer on SiC grown using MOCVD. Ohmic contacts were achieved by Ti/Al/Ni/Au evaporation and RTA. The device isolation was formed by ion implantation. Pt/Ti/Pt/Au multi-layered Schottky metal contacts with T-shaped gate of 0.17 µm gate length were fabricated by electron-beam lithography. The devices had a gate width of 200 µm and a source-drain spacing of 5 µm. The devices showed the good pinch-off characteristics. The threshold voltage was - 2.52 V. The extrinsic transconductance was 250 mS/mm at a gate bias of -1.0 V and a drain bias of 10 V. The three-terminal breakdown voltage was 140 V at drain current of 1 mA/mm and gate bias of - 5 V. RF measurement shows that these devices have a f_T of 56 GHz and f_{MAX} of 200 GHz. These results will be usefully applied for high frequency and high power applications.

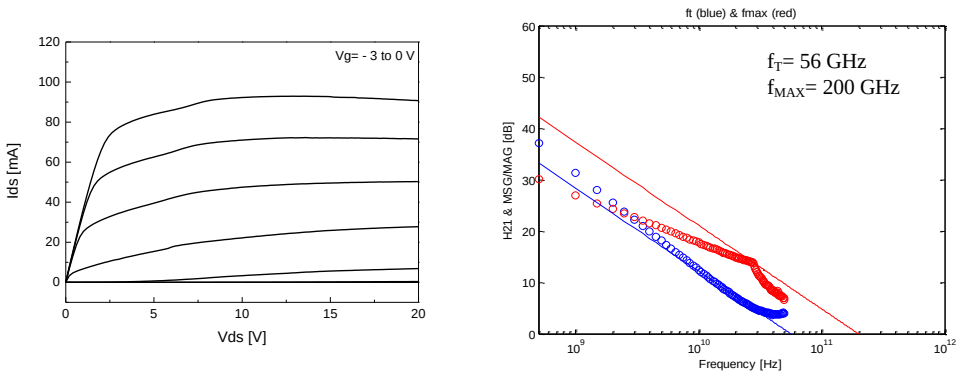


Fig 1. Measured DC and RF characteristics for 0.17 x 200 μm^2 GaN HEMT devices.

[1] U. K. Mishra, P. Parikh, and Y. –F. Wu, Pro. IEEE, vol. 90, no.6, pp.1022(2002).

[2] G. H. Jessen, *etal*, IEEE GaAs Digest, pp.277(2003).

Bias-dependent characteristics of AlGaN/GaN HEMTs on SiC with T-shaped gate of 0.25 um gate length

Jong-Min Lee, Byoung-Gue Min, Hyung Sup Yoon, Ho-Kyun Ahn, Dong Min Kang, Seong Il Kim, Sang-Heung Lee, Chul Won Ju, Hae Cheon Kim, and Jong-Won Lim

RF Convergence Components Research Section, IT Materials and Components Lab., Electronics and Telecommunications Research Institute, Daejeon, 305-700, Korea

E-mail : leejongmin@etri.re.kr

We have developed AlGaN/GaN high electron mobility transistor (HEMT) by using 4-inch compound semiconductor process [1]. This technology includes a T-shaped gate of 0.25 um gate length and ion-implantation isolation. To evaluate the possibility of drain voltage modulation to improve overall device performance, we characterize HEMTs operated over a range of drain bias conditions [2]. We measured DC and RF characteristics to provide a detailed understanding of the dependence of performance on drain bias conditions. In addition, large signal measurements were carried out at optimized source and load impedances. Measured devices demonstrated high power gain of 17 dB at 9.3 GHz throughout a wide voltage range from 25 to 40 V. These 600 um wide devices also generated 2.4 W output power with 5 dB gain compression at 40 V, which translates to 4.05 W/mm power density. Bias-dependent performance illustrates the compatibility of devices for high voltage and voltage variable applications.

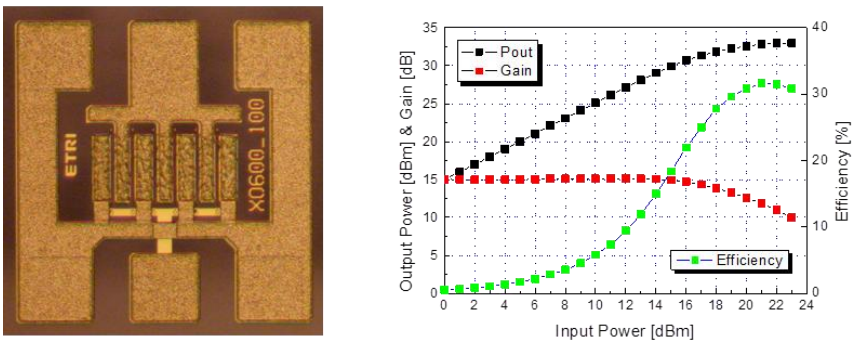


Fig 1. GaN HEMT device and its power characteristic

[1] J. W. Palmour, C. Hallin, A. Burk, F. Radulescu, D. namishia, H. Hagleitner, J. Duc, B. Pribble, S. T. Sheppard, J. B. Barner, and J. Milligan, IEEE MTT-S IMS Digest, 1226 (2010).

[2] J. D. Brown, S. Lee, D. Lieu, J. Martin, R. Ventury, M. J. Poulton, and J. B. Shealy, IEEE MTT-S IMS Digest, 303 (2007).

A study on the scalability of a threshold type cell select device using amorphous GeSe, and the experimental ways for reduction of threshold voltage

Hyung-Woo Ahn, Suyoun Lee, Doo Seok Jeong, Sang-Yeol Shin and Byung-ki Cheong
Electronic Materials Research Center, Korea Institute of Science and Technology, Seoul 136-791, Republic of Korea
E-mail : bkcheong@kist.re.kr

Recently, the threshold type cell selector using amorphous chalcogenides, referred to as Ovonic threshold switching (OTS) device, has received renewed attention due to high potential to be employed in novel switching devices [1]. We investigated switching characteristics of OTS devices composed of Pt/amorphous chalcogenides/Pt using GeSe. The driving current capacity of GeSe OTS device was verified to be superior to other selector devices based on crystalline Si. However, increase in V_{TH}, V_H, and J_H was observed with decreasing the device size rendering challenges to be resolved for non-destructive and low-power consuming devices. Decreasing the thickness of GeSe resulted in the reduction of V_{TH} above 40 nm, where the dependence agreed with the critical power dissipation model for threshold switching [2]. Furthermore, V_{TH} was associated with changes in electronic structure by addition of light element (nitrogen). In this presentation, we will suggest reasonable reasons for these reduction behaviors of V_{TH} [3].

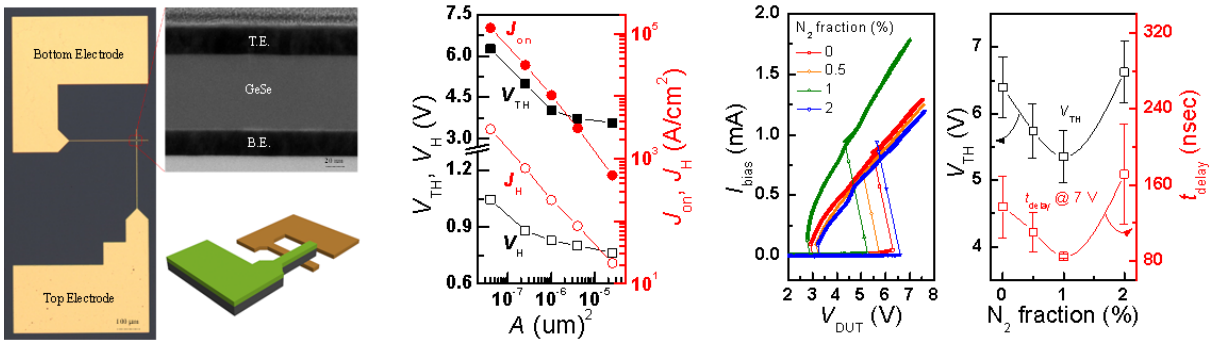


Fig 1. OTS device structure and threshold switching characteristics of GeSe OTS device

[1] Kau, DerChang et. al., Electron Devices Meeting (IEDM) (2009)
[2] Ahn, Hyung-Woo et. al., ECS Solid State Letters, 2(9) N31-N33 (2013)
[3] Ahn, Hyung-Woo et. al., Applied Physics Letters, 103, 042908 (2013)

Dependence of output power density on gate width of AlGaN/GaN HEMT on SiC substrate at 9.3GHz

Byoung-Gue Min, Hyung Sup Yoon, Ho-Kyun Ahn, Seong-Il Kim, Jong-Min Lee, Haecheon Kim, Dong-Min Kang, Chul-Won Ju, Sang-Heung Lee and Jong-Won Lim
RF Convergence Components Research Section, IT Components & Materials Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea
E-mail : minbg@etri.re.kr

We reported the fabrication process[1], DC and power characteristics of 0.25 μm AlGaN/GaN high electron mobility transistors on 4-inch SiC substrate. This summary focused on the results of power measurement at 9.3 GHz of the devices with the variations of the unit gate width and the total gate width. The unit gate widths of the multi-gate HEMT devices were varied from 50 μm to 200 μm. The total gate width of the largest device was 1.2 mm. The maximum output power density was acquired at the device of the unit gate width of 150 μm with 6-fingers. There was observed an increasing tendence of the output power density with the total gate width.

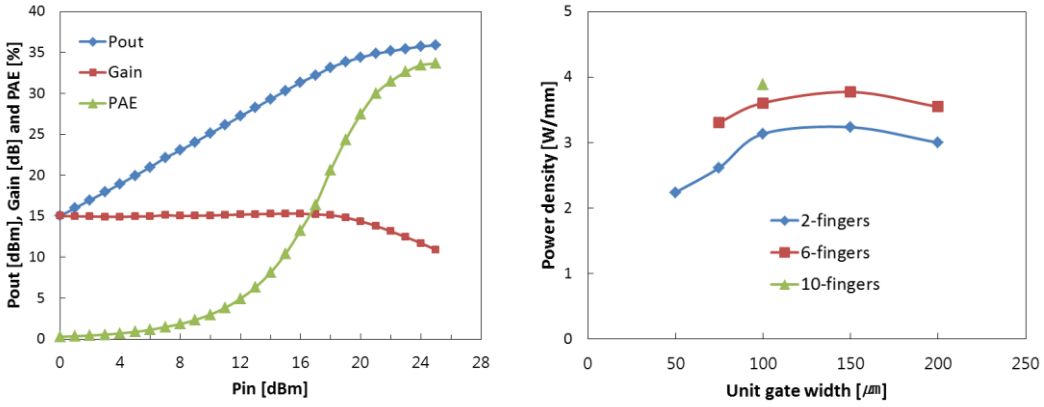


Fig 1. Power characteristics of AlGaN/GaN HEMT at 9.3GHz

[1] Jong-Won Lim, Ho-Kyun Ahn, Seong-il Kim, Dong-Min Kang, Jong-Min Lee, Byoung-Gue Min, Sang-Heung Lee, Hyung-Sup Yoon, Chul-Won Ju, Haecheon Kim, Jae-Kyoung Mun, Eun-Soo Nam and Hyung-Moo Park, Thin Solid Films 547, 106 (2013).

RF Performance of 13 nm-thick AlGaN/GaN HEMT with Thin Al_2O_3 Surface protection layer

Jun-Hyeok Lee[1)], Ryun-Hwi Kim[1)], Do-Kywn Kim[1)], Chul-Ho Won[1)], Ji-Hyun Kim[1)], Young-Jo Kim[1)]
Bok-Hyung Lee[2)], Byeong-Ok Lim[2)], Gil-Wong Choi[2)], In-Pyo Hong[3)] and Jung-Hee Lee[1)*]

[1)]School of Electronics Engineering, Kyungpook National University, Daegu, Korea
[2)]Samsung Thales Co., Ltd, Korea, [3)]Agency for Defense Development, Korea
*Corresponding author: Jung-Hee Lee, Tel : +82-53-940-8655, e-mail : jlee@ee.knu.ac.kr

AlGaN/GaN HEMT is an excellent candidate for high power and high radio frequency (RF) applications due to the superior properties such as wide bandgap, high breakdown field and high mobility/electron density of two-dimensional electron gas (2-DEG) [1]. For high RF performance, some parameters are required such as high transconductance (g_m), low series resistance (R_S) and narrow gate length (L_G) [2]. In this work, AlGaN/GaN heterostructure was epitaxially grown on semi-insulating SiC substrate. Si modulation-doped thin AlGaN barrier layer with thickness of 13nm was grown to increase the transconductance of the fabricated device. An in-situ 3 nm-thick GaN capping layer was also grown to prevent the AlGaN surface from being damaged during the fabrication. The 2-DEG density and mobility of AlGaN/GaN heterostructure were extracted by hall measurement as 8.5×10^{12} cm^2 and 2010 $cm^2 \cdot V^{-1} \cdot s^{-1}$, respectively. To maintain the original properties of the 2DEG channel from thermal damage during rapid thermal process (RTP), especially when the AlGaN layer is thin, 8 nm-thick Al_2O_3 layer was employed as a surface protection layer. For ohmic contact, two-step RTP was carried out initially at low temperature of 500 ℃ (20 sec) and then at higher temperature of 800 ℃ (30 sec) in nitrogen ambient. The Al_2O_3 layer in the gate region was then selectively removed to enhance the transconductance of the device. T-shaped gate with length of 0.2 μm was formed on the recessed AlGaN surface by depositing Ni/Au gate metal. The resistance parameters extracted from transmission-line measurement exhibited a low contact resistivity of 2.8×10^{-6} Ω-cm^2 (contact resistance of 0.3 Ω-mm) and the sheet resistance of 318 Ω/□ in the access region. It is noticed that the sheet resistance was not increased even after high temperature RTP, which indicates that the 8 nm thick-Al_2O_3 layer is very effective in protecting the AlGaN surface and the properties of 2-DEG channel. The transfer characteristics of the fabricated device exhibited excellent DC performances such as the maximum drain current of 895 mA/mm and the maximum transconductance of 330 mS/mm, and low gate leakage current (0.2 μA/mm at V_G = - 10 V) as shown in Fig. 1. The device also exhibited high cut-off frequency (f_T) of 60 GHz and the maximum oscillation frequency (f_{max}) of 103 GHz at a gate bias of -2 V and a drain bias of 10 V, respectively, as shown in Fig. 2. These excellent DC and RF performances are believed to be due to the enhanced transconductance with the use of thin AlGaN barrier layer and low series resistance of the device achieved by employing thin Al_2O_3 surface protection layer during RTP. The fabricated device exhibits high $f_T \cdot L_G$ product of 12 GHz·μm for L_G/t_{bar} ratio of 12.5 as shown in Fig. 3, which is comparable to the state-of-the-art results reported by others [3-5].

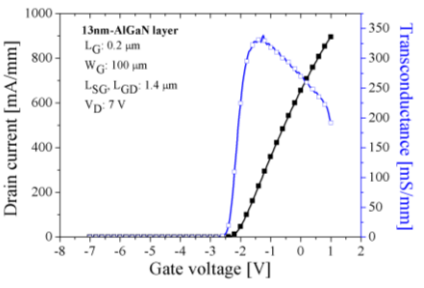


Fig. 1 The characteristics of I_D-V_G transfer curve

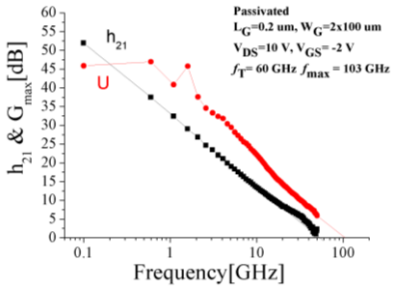


Fig. 2. The frequency performance of AlGaN/GaN HEMT

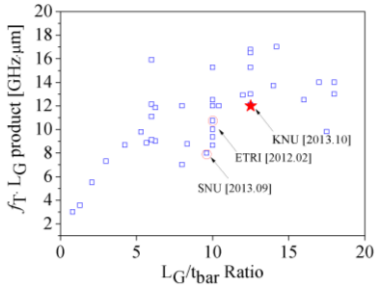


Fig. 3. Comparison of the $f_T \cdot L_G$ products – aspect ratio.

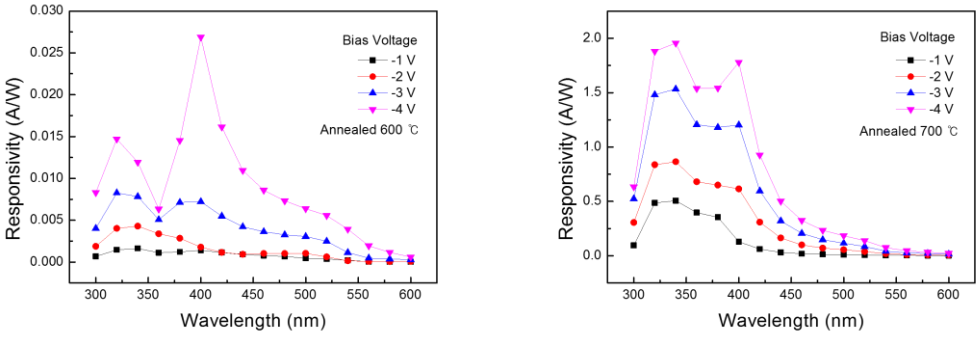
[1] P. Waltereit, et al., Phys. Status Solidi (a), V. 206, pp. 1215-1220, 2009.
[2] P. J. Tasker, et al., IEEE Electron Device Lett., V.10, N.7, pp.291-293.
[3] U.K Mishra, et al., ICNS-10 conference Proceeding, (2013)
[4] D. Kim, et al., SSDM 2013 conference Proceeding, (2013)
[5] S. Kim, et al., KCS 2012 conference Proceeding, (2012)

Acknowledgment
This work was supported by Agency for Defense Development (ADD) of Republic of Korea Contract UC110052GD.

Ultra-violet sensitivity of n-ZnO/p-GaN Hetero-junction Diode

Seong Gook Cho, Woong Tak Moon, and Eun Kyu Kim*
Department of Physics and Research Institute for Natural Sciences, Hanyang University, Seoul 133-791
*e-mail: ek-kim@hanyang.ac.kr

UV-detecting photodetector consisted of ZnO and GaN has taken a center stage due to similar properties such as lattice constant, wide band gap, and high optical transmittance. The ZnO is II-VI compound semiconductor with intrinsic n-type conductivity. The ZnO with p-type conductivity for making a ZnO homo-junction has been challenging problem because of its low reproducibility. Therefore, many studies for p-type III-V compound semiconductors have been attempted for p-n hetero-junction structure with n-type ZnO. Among these substrates, GaN is one of most promising candidates for ZnO-based p-n junction detector. However, ZnO-based photodetector was still limited by low responsivity in UV region and intrinsic defects in ZnO due to the limitation of chemical potential ($U_{Zn} + U_O < U_{ZnO}$) can decrease the responsivity. In recent paper, it is reported that this defects in ZnO can produces another photo-sensitive center [1]. In this study, we present an n-ZnO/p-GaN hetero-junction photodiode with UV and visible response.



(a) (b)

Figure 1. Photoresponse spectra of n-ZnO/p-GaN post-annealed at (a) 500 ^{o}C and (b) 600 ^{o}C.

[1] S. G. Cho, D. U. Lee, and E. K. Kim, Thin Solid Films, **545**, 517 (2013).

Photoluminescence anisotropy in InP quantum dot strings

Yongmin Kim[1], Yong Ho Shin[1], Jindong Song[2]
[1]*Department of Applied Physics and Institute of Nanoscience and Biotechnology, Dankook University, Yongin 448-701, Korea*
[2]*Korea Institute of Science and Technology, Seoul 136-791, Korea*
E-mail : yongmin@dankook.ac.kr

InP quantum dots were grown by using the molecular beam epitaxy technique. Quantum dots are connected and composed string-like one-dimensional structure. Two prominent photoluminescence transitions from normal quantum dots and string-like one-dimensional structure were observed which show strong optical anisotropy along [1-10] and [110] crystal directions. Both peaks also showed red-shift while rotating emission direction. Such optical behaviors are consequence of strain field induced by lattice mismatching. Such optical transition behaviors are the consequence of the valence band mixing caused by strain field along the [110] crystal direction.[1]

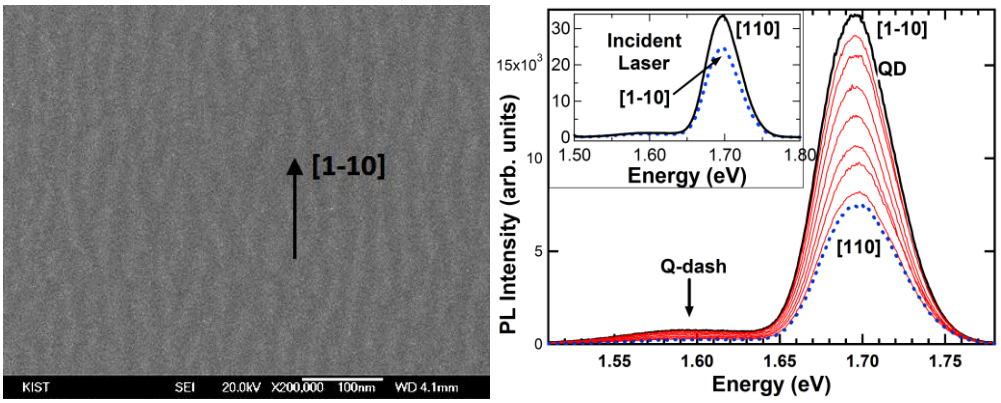


Fig 1. SEM image of InP quantum dot string structure (left) and its photoluminescence spectra.

[1] A. Mascarenhas, R. G. Alonso, G. S. Horner, S. Froyen, K. C. Hsieh and K. Y. Cheng, Phys. Rev. B **48**, 4907 (1993).

Optical study of non-polar *a*-axis ZnO single crystal for light emitting applications

Younghun Hwang and Youngho Um
Department of Physics, University of Ulsan, Ulsan 680-749, Korea
E-mail : yhum@ulsan.ac.kr

Due to the excellent optical properties, ZnO is a very promissing material for light emiiting devices in the blue or ultraviolet region. Compared with other wide bandgap semiconductors, ZnO has a larger exciton binding energy (60 meV) that provides more efficinet excitonic emissions at room temperature. Recent progress in single crystal growth has also opened up prospects for optoelectronic applications, as a substrate for grown of GaN or as a light emitting material. Single crystal ZnO is a hexagonal wurtzite crystal structure which belongs to a 6mm symmetry. It grows generally in polar (*c*-axis oriented) and non polar (*a*-axis oriented) planes, in which polar planes and especially (100) plane are stable [1]. Most of the studies dealt with *c*-plane oriented thin films. However, devices based on *c*-axis oriented wurtzite materials are known to present spontaneous and piezoelectric electrostatic fields which spatially separate electrons and holes in the active layers and, thus, limit the device quantum efficiency [2]. So this problem can be eliminated by growing non polar layer surfaces used in light emitting device structures. Unforfunately, very little is known optical properties about *a*-axis orietation ZnO single crystal. In this work, we describe a comprehensive study of optical properties of *a*-axis [especially (100) plane] ZnO single crystal grown by the hydrothermal method. This study will be useful to understand the optical properties of non polar *a*-axis oriented ZnO to improve quantum efficiency for ligh emitting devices.

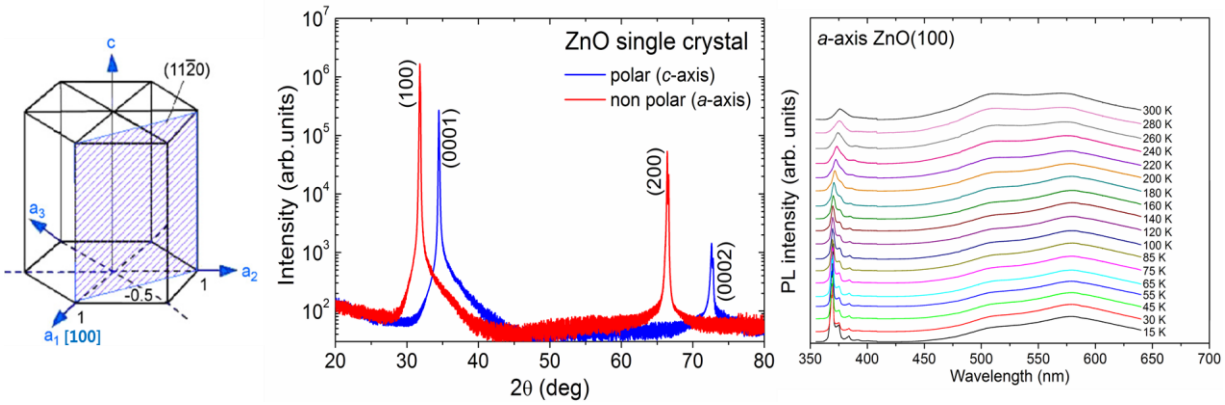


Fig 1. Non-polar *a*-axis ZnO (100) single crystal and its structural and PL properties.

[1] V. A. Coleman *et al*., Zinc Oxide Bulk, Thin films and Nanostructures [Elsevier], 1 (2006).
[2] T. Takeuchi et al., Appl. Phys. Lett. 73, 1691 (1998).

Unusual photoluminescence peak shift of InSb epitaxial layers grown by LP-MOCVD

Jinwook Jung[1], Sehun Park[1], Chulkyun Seok[1], Yongjo Park[2], Xiren Chen[3], Jun Shao[3] and Euijoon Yoon[1]

1. Department of Materials Science and Engineering, Seoul National University, Seoul 151-747, Korea
2. Energy Semiconductor Research Center, Advanced Institutes of Convergence Technology, Seoul National University, Suwon 443-270, Korea
3. Shanghai Institute of Technical Physics, Chinese Academy of Sciences, Shanghai 200083, China
E-mail : jjw5017@snu.ac.kr

Recently, InSb photodetectors for high temperature operation were developed by SemiConductor Devices (SCD) [1]. In order to fabricate these photodetectors, high quality of InSb epitaxial layers with low defect density have to be grown. In this work, homo-epitaxial InSb layers were grown by varying growth temperatures and its optical properties were analyzed with photoluminescence (PL) at 77 K. In Figure 1, strong band-to-band transition of InSb grown at 510 ^{o}C was observed. In case of lower growth temperatures, low PL intensity was observed and it is shifted to lower energy level. It implies that crystal quality of InSb can be degraded when it is prepared at low temperature. It may be caused by short mean free path of source materials on the growth surface and/or temperature dependence of source decomposition rate. At lower growth temperatures, rough surface morphology was observed by AFM measurement, indicating that source materials have low surface diffusion length with poor incorporation at step sites. It was reported that source materials are not fully decomposed at low growth temperature regions which may affect the formation of nonstoichiometric InSb epitaxial layers. Further PL investigation for the defect origin at low temperature regions will be reported.

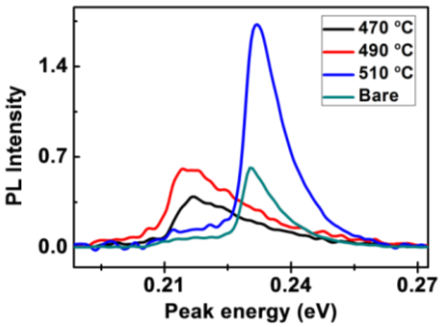


Fig 1. Photoluminescence spectrum of epitaxially grown InSb

[1] Itay Shtrichman *et al*. Proc. SPIE 8353, Infrared Technology and Applications XXXVIII, 83532Y (2012)

A Pipelined Digital Predistorter using CORDIC Processor

Jong Kang Park, Kyunghoon Kim, Youngoo Yang, and Jong Tae Kim
School of Electronic and Electrical Eng., Sungkyunkwan University., Gyeonggi-do 440-746, Korea
E-mail : jtkim@skku.edu

In a wireless communication, a predistorter is often employed to alleviate nonlinear distortions due to operating a power amplifier near saturation [1, 2]. In this paper, a new polynomial digital predistorter(DPD) using CORDIC processor is introduced. The CORDIC processor calculating trigonometric function converts I/Q-phase signal to AM/PM components and vice versa. We share the CORDIC processor to support both two modes of operation, vectoring and rotation modes. Each pipelined unit changes its mode of operation at every clock cycle. The DPD is entirely a fully pipelined design supporting for high rate pre-distortion. By adjusting only coefficients of polynomial, it conforms to the environmental change. The DPD was fabricated by standard CMOS 0.35 um technology as depicted in Fig. 1. Total cell area was estimated to 37,026 gates. Functional verification of the IC was done by comparing its output to the post-simulation results by chip testing equipment. Our DPD can operate with 40-50MHz clock speed from 2.7 V to 4.0 V supply as shown in Fig. 2.

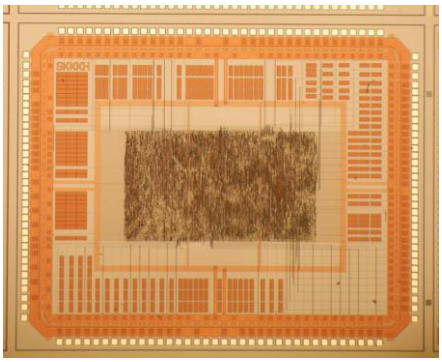


Fig. 1 Microphotograph for the fabricated DPD

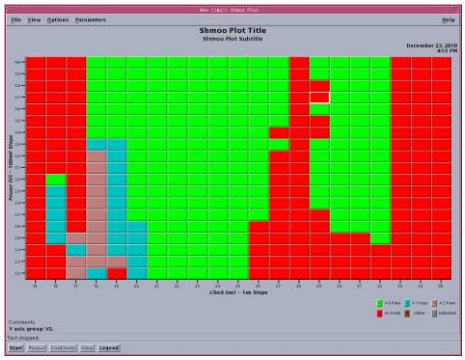


Fig. 2 Test result of chip

[1] I. Teikari, “Digital Predistortion Linearization Methods For RF Power Amplifiers,” Dissertation, Helsinki Univ. of Tech., 2008.
[2] J. K. Cavers, “Amplifier Linearization Using a Digital Predistorter with Fast Adaptation and Low Memory Requirements,” IEEE Trans. on Vehicular Tech., Vol. 39, No. 4, pp. 374-382, 1990.

Spectroscopic Ellipsometer 를 이용한 CVD Graphene 의 광학특성 평가

손우식 [1], 문정훈 [2], 현문섭 [1], 양준모 [1], 조병진 [2]

[1] 나노종합기술원 특성평가사업실, [2] 한국과학기술원 전기전자공학과

291 Daehak-ro,Yuseong-gu,Daejeon 305-701, Republic of Korea

E-mail : sounws@nnfc.re.kr

A CVD graphene film on a silicon wafer with 100 nm silicon dioxide on top was scanned with a spectroscopic ellipsometer with a focused spot (35 ㎛) at an angle of 71.6°. The spectroscopic ellipsometer data were analyzed with an optical model in which the optical constants were parameterized by harmonic oscillator. This parameterization is the key for the simultaneous accurate determination of the optical constants in the wavelength range 250~750 nm and the thickness of graphene, which was found to be 1.7~5.6 Å.

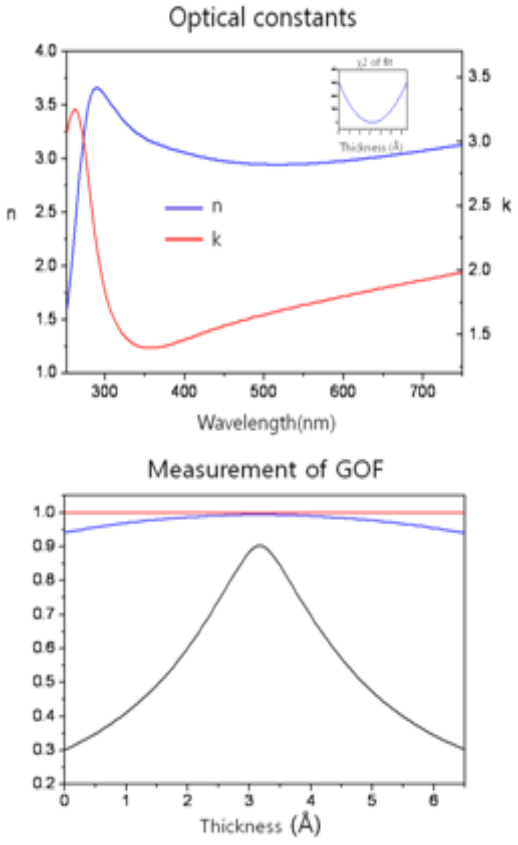


Fig 1. Thickness and optical coefficient of Graphene results

[1] J.W. Weber, V.E. Calado, and M.C.M van de Sanden, Appl Phys Lett, 97, 091904, 2010.

Monte Carlo simulation of scanning electron microscopic images of specimens for structural and compositional analysis

Myeong Chun Song and Jin Seung Kim
Department of Nano Science and Technology, Graduate School,
Chonbuk National University, Jeonju 561-756
E-mail : jin@jbnu.ac.kr

For quantitative analysis of SEM images in metrology and inspection in semiconductor device fabrication process, it is essential to have proper understanding of electron-specimen interaction and its consequence to the image formation. In this paper, we simulate the electron-specimen interaction by using Monte Carlo method. The three-dimensional trajectories of electrons in the probe beam after they entered the surface of a specimen, of the secondary electrons generated by the primary electrons are simulated.[1] Based on this trajectory simulation, we analyzed the spectral and directional properties of the secondary and backscattered electrons while changing the shape and composition of the specimen, and synthesized the SEM images. The image resembles realistic SEM images and shows the possibility of quantitative analysis based on the comparison of real and simulated SEM.

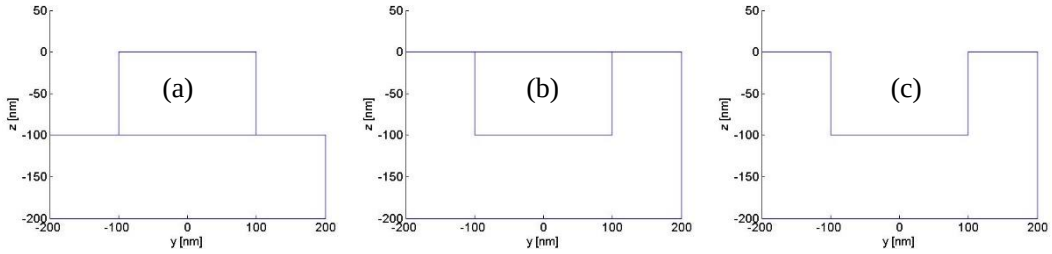


Figure 1. (a) An object of different material on a substrate. (b) An object of different material in the substrate. (c) A hole in the substrate.

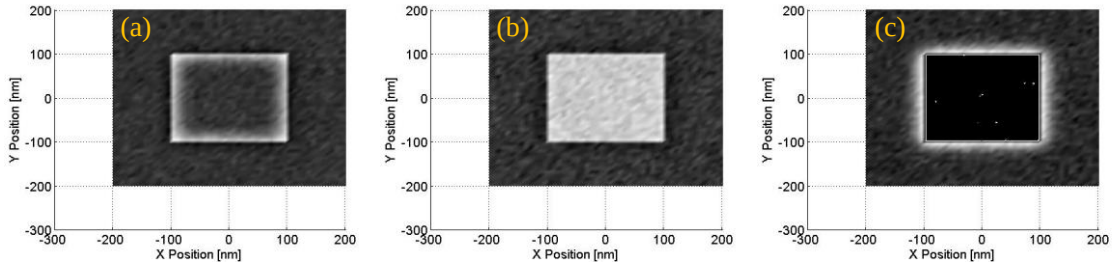


Figure 2. Images simulated for the specimens in Figure 1. (a), (b), and (c)

[1] D. C. Joy, Monte Carlo Modeling for Electron Microscopy and Microanalysis (Oxford, London, 1995).

Electronic structure of graphene: EELS and DFT calculation

Yun Chang Park and Jun-Mo Yang
National NanoFab Center (NNFC), Daejeon 305-701, Korea
E-mail : parkyc@nnfc.re.kr

Electronic structures of carbon and its related materials such as graphene, graphite, amorphous carbon, diamond, carbon nitride and silicon carbide are investigated by both electron energy loss spectroscopy (EELS) and density functional theory (DFT) calculation [1]. Atomic number 6 of carbon has 2 core electrons and 4 valence electrons. In the four-fold coordinated structure such as diamond and SiC, they show only σ* bonding structure (tetrahedrally directed sp^3 configuration). In the three-fold structure, strong sp^2 configuration and one weak bonding such as graphite and carbon-nitride, they show both π* and σ* boning structure. In this presentation, we demonstrate the defective single layer graphene by HRTEM, diffraction and EELS analysis. It shows 3 eV pre-peak prior to the π* bonding in the defective single layered grapheme structure which is consistent with the graphene edge structure obtained by early researcher [2].

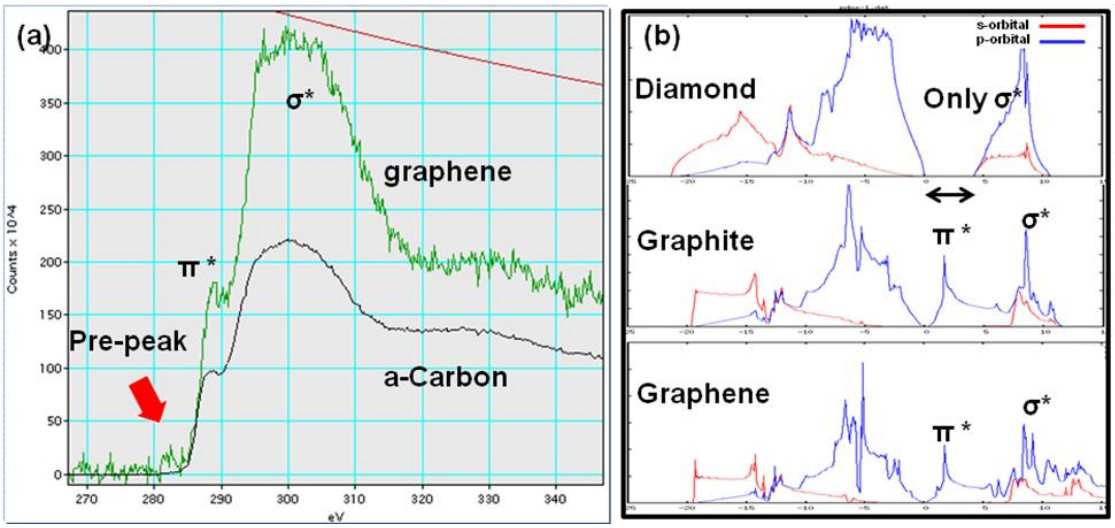


Fig. 1. (a) EELS spectrum shows pre-peak (red arrow) indicating defective single layered graphene structure. Spectrum of amorphous carbon was displayed for comparison. (b) Calculated density of state (DOS) shows π* and σ* bonding over the Fermi level in both graphite and graphene. Diamond with only σ* bonding was displayed for comparison.

[1] R.F. Egerton, Electron Energy Loss Spectroscopy in the Electron Microscope, Plenum, New York (1986).
[2] K. Suenaga and M. Koshino, Atom-by-atom spectroscopy at graphene edge, Nature, 468 (2010).

유성펜을 이용한 FIB 손상 방지용 보호층 증착 및 특성

박윤창 [1], 박병천 [2] Sergey Romankov[3] 박경진 [1], 유정호 [1], 이용복 [1], 양준모 [1]
[1] *나노종합기술원,* [2] *한국표준과학연구원,* [3] *전북대학교 신소재공학과*
E-mail : parkyc@nnfc.re.kr

FIB(Focus ion beam)는 특정영역에서의 TEM(Transmission electron microscopy) 시편제작이 가능하기 때문에 현미경분야에서 활발히 사용되고 있다. 그러나, 가속된 이온빔이 시편에 충돌하면서 TEM 시편의 표면에 인공적인 손상층이 생기고, 이로 인해 미세구조 해석에 어려움이 있다. 표면 손상을 막기 위한 방법으로 보호층 증착이 요구되고 있으나, 좁고 깊은 패턴의 경우, 물리증착방법은 채움 특성이 좋지 않고, Dual beam FIB 기반 화학증착방법은 미세한 전자빔 손상과 심각한 이온빔 손상이 있으며[1], 원자층 증착방법은 채움 특성은 좋으나, 고가의 장비가 필요하고, 느리다는 단점이 있다. 이에 쉽고, 빠르고, 저렴하면서 채움 특성이 우수한 보호층을 증착할 수 있는 새로운 방법이 요구되고 있다. 본 연구에서는 유성펜으로 시편 위에 직접 쓰는(direct writing) 방법으로 FIB 손상 방지용 보호층을 증착하였다. 우리는 이러한 방법을 유성펜 증착법(Permanent marker deposition, 이하 PMD)이라고 이름 지었고, PMD 의 미세구조, 성분, 채움과 손상(보호) 특성을 TEM 을 이용하여 평가하였다. PMD 방법은 FIB 손상방지용 보호층 증착방법의 대안이 될 수 있을 것으로 보이며, 이번 발표에서는 PMD 의 증착법과 응용에 대한 연구결과를 상세히 소개할 예정이다.

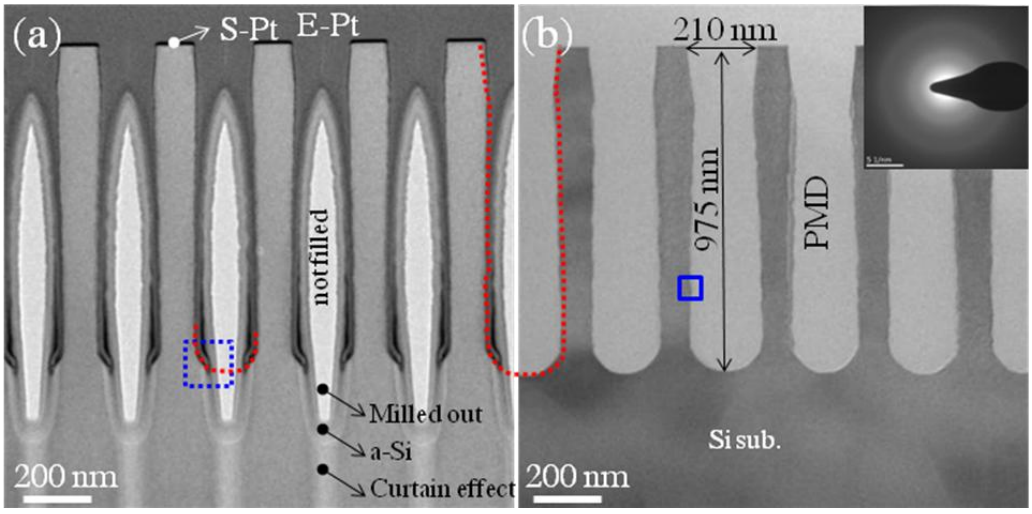


Fig. 1. 보호층 증착 방법에 따른 Si 트렌치 패턴의 단면구조. (a) sputtered-Pt 와 EBID-Pt 증착 시편의 구조, (b) PMD 증착 시편의 단면구조와 PMD 의 회절도형(inset).

[1] B.C. Park, Y.C. Park, H.J. Lee and Y.H. Kim, J. Vac. Sci. Technol. B 28(6), (2010).

집속이온빔(FIB)을 이용한 GaN 계 LED 의 3 차원 전위분석

박경진 [1], 곽상희 [1], 유정호 [1], 박윤창 [1] 양준모 [1]
[1] 나노종합기술원 특성평가실

직접 천이형 밴드갭을 가지는 Ⅲ-Ⅴ 질화물 반도체는 넓은 밴드 갭과 녹색에서 UV 까지 다양한 영역대의 파장을 가지며 고효율 광소자로 각광받고 있을 뿐만 아니라 고출력 고주파 소자로서 유용한 물성을 지니고 있다[1]. 그 중 GaN 반도체는 수 나노미터의 다중양자우물(multi quantum wells, MQWs)을 형성하여 LED 광 소자로 적용 되어지고 있다. Sapphire 기판을 이용하여 GaN 소자를 성장시키기 때문에 발광효율은 sapphire 기판과 GaN 박막간의 계면특성에 영향을 받으며 특히 GaN 박막에서의 관통전위(threading dislocation, TD) 밀도는 발광효율에 큰 영향을 주고 있어[2] 이러한 관통전위에 대한 연구가 활발하게 진행 되어지고 있다.

이러한 GaN 의 미세구조 및 특성은 집속이온빔(focused ion beam, FIB) 및 이온밀링법을 이용하여 100 nm 이하의 얇은 박편으로 제작하고 투과전자현미경(transmission electron microscope, TEM) 기법을 이용하여 분석이 수행되고 있다. 이러한 시편제작 방법의 다중양자우물 등의 미세구조 및 조성에 대한 정보는 취득할 수 있으나 관통전위 등과 같은 결함에 대한 분석에는 전체 소자의 특성을 대변하기 힘든 단점이 있다.

본 연구에서는 GaN 박막 내부의 전위구조 및 분포를 분석하기 위하여 특정영역에서 균일한 두께의 시편 제작이 가능한 FIB 를 이용하여 연속절편법으로 1 ㎛ ~ 50 nm 의 시편두께 범위에서의 내부 전위구조를 관찰하고 이를 이용하여 3 차원으로 재구성하여 전체 전위구조와 분포를 관찰하였다.

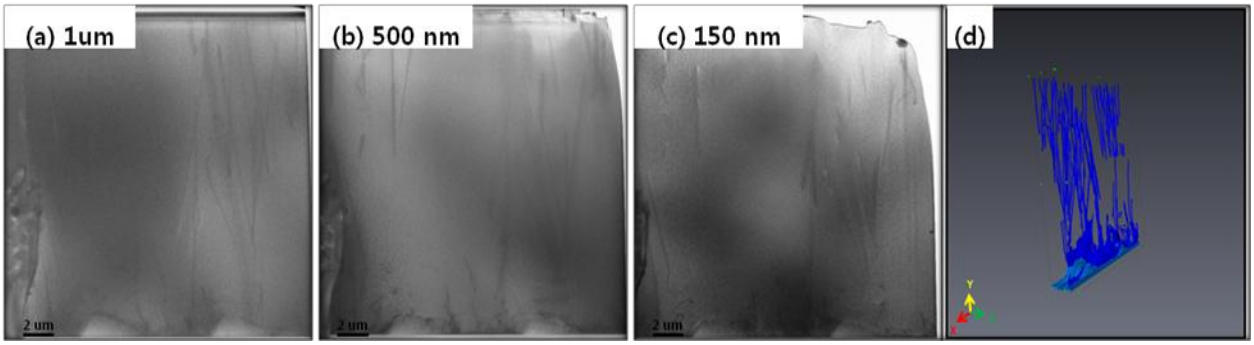


Fig. 1. GaN 계 LED 의 시편두께 변화에 따른 전위구조와 분포 (a) ~ (c) STEM 영상 및 (d) 3 차원 전위분포 영상.

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전계방출 전자빔의 전자광학계 정렬기술 연구

최성웅 [1], 이영복 [1], 김대욱 [1], 오태식 [1], 김영정 [2], 김호섭 [1]

[1] 선문대학교 나노과학과, [2] 선문대학교 신소재공학과

E-mail : hskim3@sunmoon.ac.kr

반도체공정에서 미세한 결함을 검사하는 전자빔장비의 전자빔은 전자렌즈의 광학축과 정교하게 정렬되어야 우수한 성능을 가질 수 있다. 고분해능을 가진 전계방출 방식의 전자빔은 고진공 또는 초고진공의 진공환경에서 작동되고 있는데, 전자빔원은 기계적 방식으로 extractor 전극과 정렬되고 있다. 이러한 방식은 고진공 상황에서 전자빔원을 광학 축에 정교하게 재정렬할 수 없어서 광학수차가 발생되어 전자빔장비의 성능이 저하되는 중요한 요인이 되고 있다 [1]. 이러한 문제점을 해결하기 위해서 고진공 환경에서 전자 빔원을 nm 정도로 이동시킬 수 있는 나노 포지셔너를 연구하였다 [2]. 나노 포지셔너는 나노미터에서 수 밀리미터까지 이동이 가능한 구조를 가지고 있으며, 대기압, 1.0 x 10^{-2} Torr, 1.0 x 10^{-6} Torr 진공 환경에서 정교하게 이동이 가능한 것을 확인하였다.

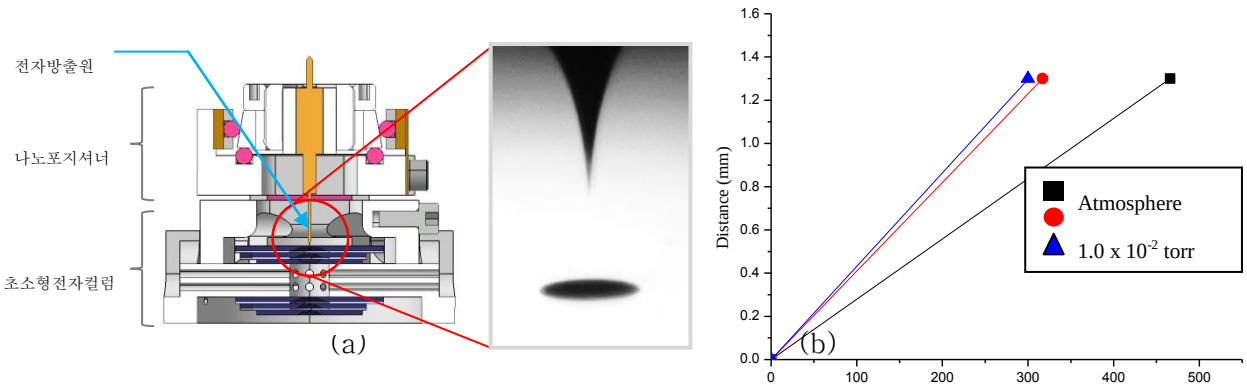

Fig 1. (a) 나노 포지셔너를 장착한 초소형 전자컬럼의 팁과 Extractor (b) 대기중과 진공에서 이동 그래프

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회절광 현미경을 이용한 극자외선 마스크의 이미징 성능측정

이재욱 [1], 홍성철 [1], 이승민 [1], 김종석 [2], 정시준 [3], 김정식 [4], 안진호 [1,2,3,4]
신소재공학과 [1], 정보디스플레이공학과 [2], 나노융합과학과 [3], 나노반도체공학과 [4],
한양대학교
E-mail : jhahn@hanyang.ac.kr

EUV lithography 에서 마스크의 CD 계측과 결함검사 기술이 중요한 문제로 여겨 진다. 기존의 검사 방법은 노광광원(13.5nm)과 다른 파장의 광원을 쓰거나 전자빔을 사용해 측정을 하기 때문에 실제 극자외선 노광에 미치는 영향을 예측하기 어렵다. 마스크 CD 계측과 결함검사를 위한 방법으로 노광광원과 같은 광원을 사용하여 검사를 하는 Actinic inspection 기술이 개발되고 있다.[1,2] 이 논문에서는 Actinic inspection 기술인 회절광 현미경 기술을 이용하여 EUV 마스크의 Critical Dimension (CD)측정과 결함 검출, 이미징 성능 측정 실험을 진행하였다.

회절광현미경(CSM)은 EUV 마스크를 반사하고 나온 회절광을 CCD 로 찍은 사진을 위상복원 알고리즘으로 원래의 EUV 마스크의 이미지를 재구성하는 기술이다. 위상복원 알고리즘을 이용해 Contact hole, Line and space 와 같은 다양한 패턴을 원래의 이미지로 재구성할 수 있는 것을 확인하였다. 이러한 마스크의 이미지 재구성 기술을 이용하여 마스크 내의 결함이나 패턴 제작 오차 등을 검출 및 측정을 할 수 있다. 또한 마스크의 이미지를 재구성하는 것 뿐만 아니라 측정한 패턴영역이 웨이퍼에 4 배 축소 노광을 했을 때 어떻게 영향을 미치는지 시뮬레이션이 가능하다. 위상복원기술을 이용하여 L/S 패턴을 NA, σ 와 같은 조명조건을 달리하였을 때 웨이퍼에 맺히는 Aerial image 가 어떻게 변화하는지 실험을 해보았고, PSM 을 제작하여 CD 측정뿐만아니라 Mask 에서의 Phase shift 현상도 관찰할 수 있었다. 또한 마스크의 회절패턴을 얻은 결과 88nm, 100nm, 128nm mask CD 각각에 대하여 0 차광과 ±1 차광의 비율이 PSM 의 경우 binary mask 에 비해 ±1 차광의 비율이 높고 이를 통해 image contrast 와 NILS 가 향상되는 점을 확인할 수 있었다.

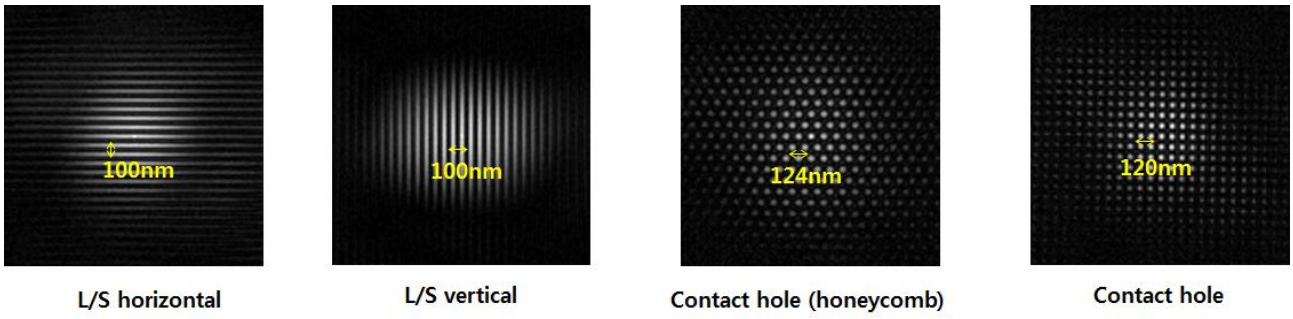

Fig 1. Reconstructed images of various patterns of EUV massk

[1] K. A. Goldberg and I. Mochi, J. Vac. Sci. Technol. B 29, 06F502 (2011)
[2] J.G. Doh, S.S. Lee, J.U. Lee, S.C. Hong, C.Y. Jeong, D. G. Lee, S.S. Kim and J. Ahn, Jpn. J. Appl. Phys. 51, 06FB04 (2012).

GPA 를 이용한 Strained Silicone 의 응력분포 해석에 대한 시편제작 방법의 영향

이용복, 박윤창, 유정호, 박경진, 이완규, 양준모

나노종합기술원 특성평가실

E-mail : yong9795@nnfc.re.kr

트렌지스터의 크기가 작아지면서 발생한 누설전류와 발열의 문제를 해결하기 위해서 스트레인드(strained) 실리콘이 개발되었다. 이러한 스트레인드 실리콘은 웨이퍼 상단 에피층(epilayer)의 결정에 변형을 가하여 전자 이동을 빠르게 한 것으로 반도체 소자의 작동 속도를 높이고 소비전력을 줄일 수 있게 되었다. 이렇게 개발된 strained Si 에 대해서 고분해능 투과전자현미경(HRTEM) 이미지로부터 응력을 해석하는 방법을 채택하였다. 그것은 GPA(geometrical phase analysis) 방법이며, 격자변형이 있는 영역과 격자변형이 없는 영역을 투과한 전자의 위상(phase) 사이에 그 차이를 해석하여 응력분포를 측정하는 방법이다. 응력분포는 이러한 위상변화의 차이로부터 격자변형의 변형율(strain)을 측정하여 분석할 수 있다 [1,2].

본 연구에서는 스트레인드 실리콘을 모사한 $Si_{1-x}Ge_x$/Si wafer 의 계면에서 응력분포를 측정하는 방법에 대해서 설명하고 시편 제작법에 따라서 고분해능 영상의 품질은 각각 다르기 때문에 응력분포의 해석에 끼치는 영향을 알아보고자 한다. 실온에서 이온밀링 방법으로 제작된 시편의 경우, $Si_{1-x}Ge_x$/Si wafer 의 계면에서 응력분포는 이온빔에 의한 시편손상으로 저온에서 제작한 시편보다 뚜렷하게 나타나지 않았다. 위상차를 이용하여 응력분포를 해석하는 경우에 TEM 시편의 상태는 매우 중요한 변수로 작용하였다. 추후에는 TEM 시편 제작방법을 다르게 하여 GPA 분석법에 적합한 조건을 찾고자 한다.

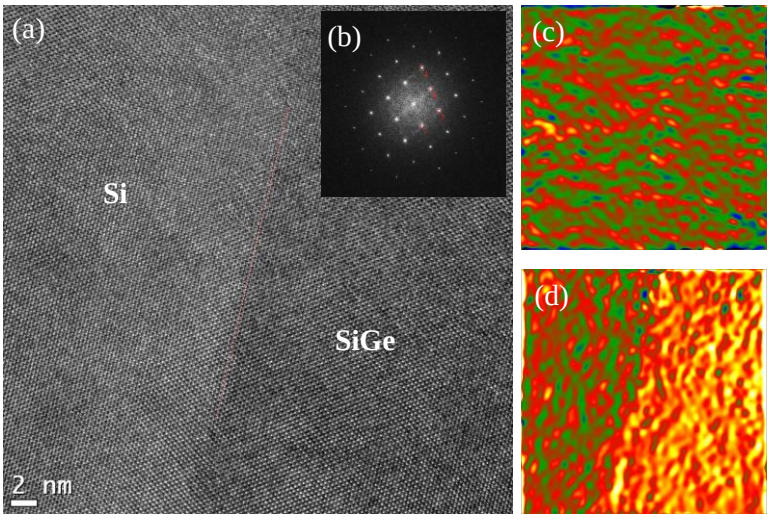

Fig. 1. (a) HRTEM image at x500k and (b) SADP of the strained Si; (c) strain ε_{xx} , (d) strain ε_{yy} ; prepared at low temperature

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고속 검사를 위한 멀티전자빔 검사장비 연구

이승범 [1], 정원영 [1], 조현우 [1], 이준호 [1], 이영복 [2], 최성웅 [2], 김대욱 [2], 오태식 [2], 김호섭 [2]

[1] 경기도 성남시 중원구 상대원동 333-5 LIG 에이디피

[2] 선문대학교 나노과학과

E-mail : hskim3@sunmoon.ac.kr

반도체공정에서 미세한 결함을 검사하는 전자빔장비는 검사속도의 한계가 있는 단일빔 방식을 극복하기 위하여 멀티빔 기술에 대한 관심이 많아지고 있다. 반도체 공정의 FEOL(Front End of Line)의 경우, 300 mm 웨이퍼의 결함을 EBI (Electron Beam Inspection)으로 검사하는데 수십시간 이상이 소요되고 있는 실정이다. 이러한 문제점은 측정에 사용되는 전자빔의 숫자를 증가시키는 방식으로 증가되는 전자빔숫자에 따라 검사속도가 증가하게 된다. 초소형 전자칼럼은 구조가 기존의 전자컬럼에 비하여 1/100 이하로 축소할 수 있으므로 다수의 전자칼럼을 배열할 수 있는 특징을 가지고 있다. 따라서 동시에 구동되는 전자컬럼의 숫자가 증가하면 검사시간이 획기적으로 단축될 수 있다. 그림 1 은 멀티전자빔 검사장비로서 4 개의 멀티전자칼럼이 포함된 컬럼챔버, 진공에서 구동하는 300 mm 웨이퍼 스테이지를 포함한 메인챔버, 복수의 컬럼을 제어하는 제어시스템 등으로 구성되어 있다. 멀티전자빔 장비는 전자광학계, 멀티빔 배열 및 제어, 이미지 획득 및 처리, 멀티빔과 연동되는 스테이지 구동기술 등이 필요하다. 이러한 요소기술에 대한 개발현황 및 연구에 대하여 논의한다.

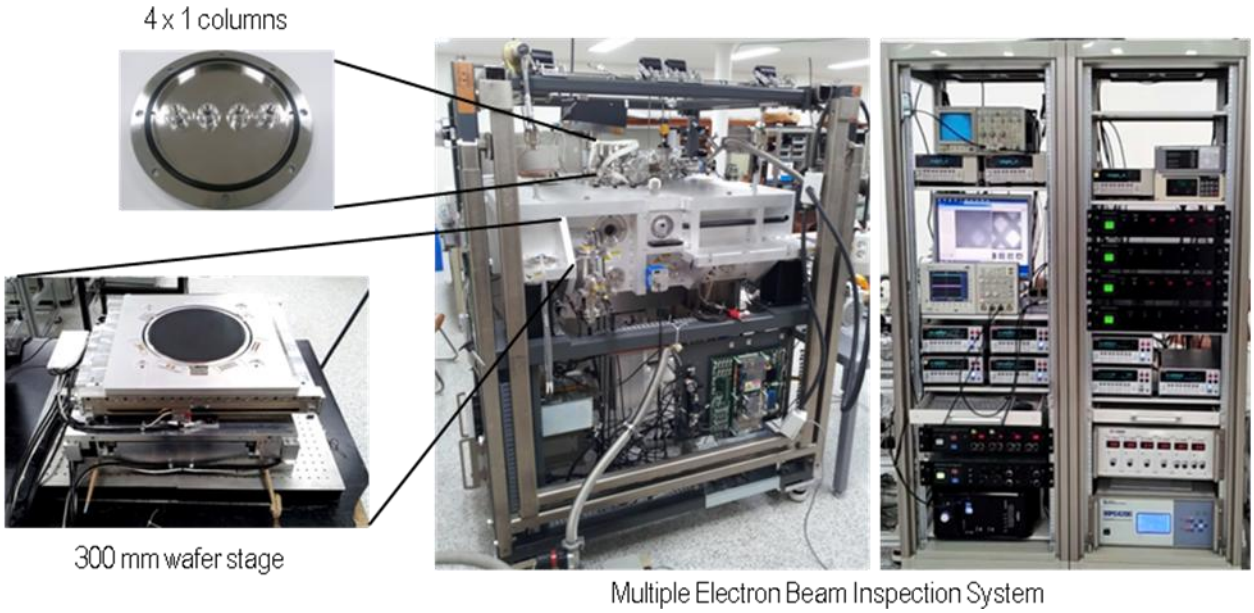


Fig 1. 멀티전자빔 검사장비 시스템

[1] H.S. Kim, M.L. Yu, U. Staufer, L. P. Muray, D. P. Kern, and T. H. P. Chang, J. Vac. Sci. Technol. B 11(6) 2327 (1993).

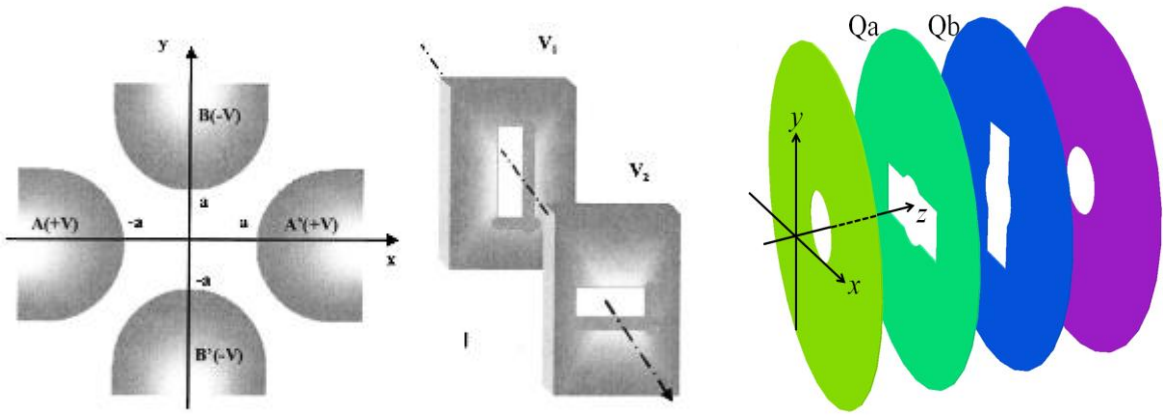
대면적 스캔을 위한 quadrupole einzel lens 구조 연구

이영복, 김대욱, 오태식, 김호섭

선문대학교 나노과학과

E-mail: hskim3@sunmoon.ac.kr

멀티전자빔을 위한 초소형 전자칼럼은 원형 아퍼처 구조의 포커스렌즈를 사용하고 있으나, 넓은 영역을 스캔 할 때에 이미지 왜곡 형상이 발생한다. 이러한 문제를 해결하기 위하여 사각구조 아퍼처를 포함한 quadrupole lens 로 구성된 einzel lens 설계 및 구동에 대한 연구가 진행되고 있다 [1]. 본 연구는 시뮬레이션으로 설계된 quadrupole lens 구조를 기초로 하여 einzel 렌즈 및 칼럼을 제작 및 특성 평가에 관한 것이다. Quadrupole lens 구조는 4 개의 전극층으로 구성되었다. 첫 번째 전극과 네 번째 전극은 원형 aperture 로 되어 있으며, 중앙에 있는 두 번째와 세 번째 전극은 사각구조의 렌즈로 구성되어 있다. Quadrupole lens 의 사각 전극층은 기존 원형 아퍼처 구조를 FIB 로 식각하는 방식과 반도체 MEMS 공정으로 제작되었다. Quadrupole lens 구조는 전극간의 간격에 따라 등간격 구조, 비등간격으로 구분한다. 그림 1 은 이상적인 quadrupole lens, 직사각형 quadruple lens, 디자인된 quadrupole lens 를 보여주고 있다. 등간격구조는 4 개의 전극 간격이 각각 500 um 로 구성되어 있으며, 비등간격 구조는 중앙 전극 간격이 850 um 이고 외부 전극간격은 500 um 간격으로 되어 있다. 이러한 구조의 quadrupole 렌즈로 구성된 전자컬럼으로 100 mm x 100 mm 크기의 대면적에서 스캔 테스트와 렌즈의 특성을 평가하였다.



(a) (b) (c)

Fig 1. (a) 이상적인 quadrupole lens, (b) 직사각형 quadrupole lens,

(c) 설계된 quadrupole lens 구조

[1] T. S. Oh, D. W. Kim. S. Ahn, Y. C. Kim, S. J. Ahn and H. S. Kim, *J. Vac. Sci. Technol. A* 26, 1443 (2008).

멀티 전자칼럼 제어방식에 대한 연구

이순용 [12], 임선종 [1], 김호섭 [2]
[1] 한국기계연구원 광응용기계연구실, [2] 선문대학교 나노과학과
E-mail: hskim3@sunmoon.ac.kr

단일 칼럼을 가진 전자빔 검사 장비의 검사 속도를 향상시키기 위한 방법으로는 복수의 전자빔을 사용하는 방법과 복수의 전자 칼럼을 사용하는 방법이 있다. 복수의 전자 칼럼을 사용하는 방법에는 마그네틱 전자 칼럼의 크기를 줄이는 방식과 초소형 정전기 렌즈를 이용하는 방법 등이 있다.[1] 마크네틱 전자칼럼으로 구성하는 멀티 칼럼 구조는 크기의 소형화에 제한적인 단점을 가지고 있으나 초소형 정전기렌즈방식은 크기가 매우 작아서 복수개의 멀티 칼럼 구조가 용이한 장점을 가지고 있다. 본 연구는 초소형 정전기 렌즈를 이용한 멀티 전자 칼럼 시스템을 구성하고 전자 칼럼의 숫자가 증가해도 확장성을 용이하게 했다. 멀티 전자 칼럼 제어는 전자 칼럼의 숫자가 증가에 따라 칼럼 제어모듈(EGPS, DS)의 숫자도 함께 증가하게 되고, 칼럼 제어모듈의 제어는 칼럼 제어 PC 에서 이루어진다. 칼럼 제어 PC 에서 모든 칼럼 제어모듈을 제어 할 수 있지만 제어 시스템의 확장성과 편의성을 위해 칼럼 제어 PC 에 2 칼럼 제어모듈을 연결하였다. 추가되는 전자 칼럼은 2 칼럼 제어 모듈을 메인 PC 에 연결하여 멀티 칼럼의 수를 확장 할 수 있다. 메인 PC 는 칼럼 제어 PC 에 입력되는 전자 칼럼의 데이터 분석을 할 수 있다. 메인 PC 와 칼럼 PC 는 이더넷 통신으로 연결하고 칼럼 PC 에서 각 칼럼을 제어하는 제어모듈은 CAN 통신을 사용하였다.[2] 그림 1 은 1 기의 메인 PC 에서 칼럼 제어 PC 가 2 개의 칼럼을 제어하는 방식을 보여주고 있다.

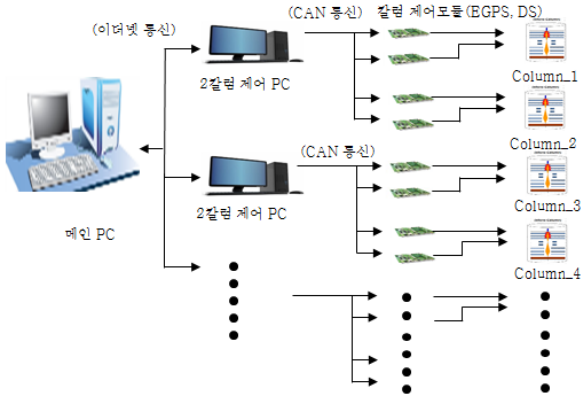


Fig 1. 멀티 칼럼 시스템 구상도

[1] 임선종,이순용,김호섭, 한국정밀공학회 2013 추계학술대회 논문집,727, (2013).
[2] 임선종,이순용, International Vacuum Nanoelectronins Conference,410,(2012).