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G. Device & Process Modeling, Simulation and Reliability 분과

Room H 난실 (본관, 5층)

2013년 2월 6일(수) 09:40-10:55

[WH1-G] Device Simulation

좌장: 박찬형(광운대학교), 조인욱(SK 하이닉스)

WH1-G-1	09:40-09:55	Si:P Nanowire as Next-Generation Interconnect for Ultra-Scale Devices: Investigation of Metallic Properties with a Tight-Binding Approach Hoon Ryu ¹ , Sunhee Lee ² , and Gerhard Klimeck ³ ¹ Supercomputing Center, Korea Institute of Science and Technology Information, ² Samsung Advanced Institute of Technology, ³ Network for Computational Nanoelectronics, Purdue University
WH1-G-2	09:55-10:10	Quantum Simulation of P-Type Nanowire Schottky Barrier MOSFETs: Silicon Versus Germanium Channel Jaehyun Lee, Wonchul Choi, and Mincheol Shin Department of Electrical Engineering, KAIST
WH1-G-3	10:10-10:25	Surface Roughness Effects in Schottky Barrier Tunneling Transistors : Comparative Study against Ohmic Contact Devices Hyo-Eun Jung and Mincheol Shin Department of Electrical Engineering, KAIST
WH1-G-4	10:25-10:40	Computational Study of P-Type Germanium Nanowire Field Effect Transistors Ju-Young Jung ¹ , Hoon Ryu ² , and Mincheol Shin ¹ ¹ Department of Electrical Engineering, KAIST, ² Supercomputing Center, Korea Institute Science and Technology Information
WH1-G-5	10:40-10:55	Enhanced Photoresponse of Plasmonic Terahertz Wave Detector based on Silicon Field Effect Transistors with Asymmetric Source and Drain Structures Min Woo Ryu, Sung-Ho Kim, and Kyung Rok Kim School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology